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Rapid QSTS Simulations for High-Resolution Comprehensive Assessment of Distributed PV

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Motivation

In future hi-pen PV scenarios with 1000s of PV systems on most circuits, conservative, worst-case snap shot impact analysis will unnecessarily limit PV integration and thus we need to improve the PV impact study methods and tools.

QSTS: Quasi-static time series analysis captures time-dependent aspects of power flow, including the interaction between the daily changes in load and PV output and control actions by feeder devices and advanced inverters.

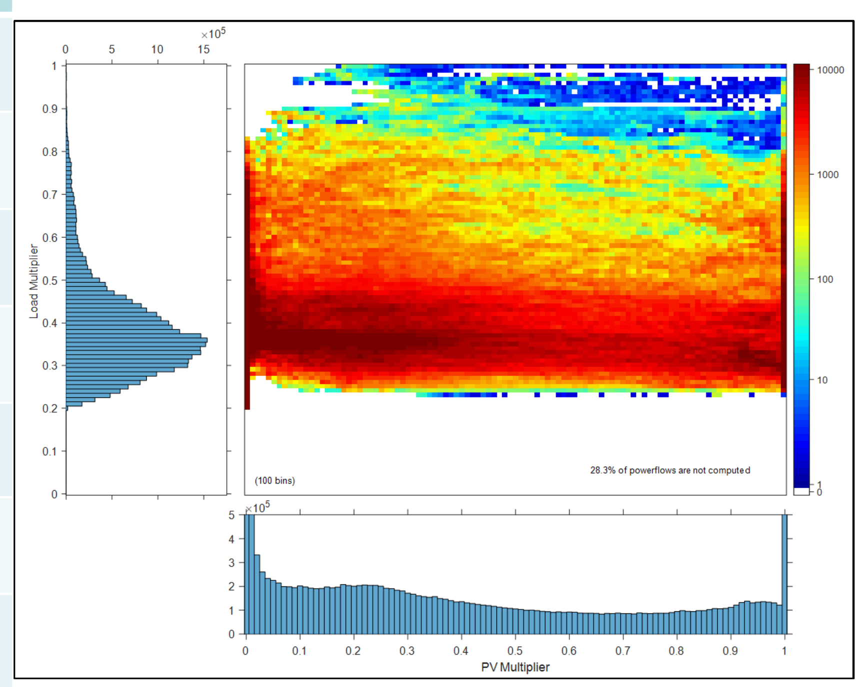
Challenge: A yearlong QSTS simulation with 1-second resolution has the computational burden of solving 31.5 million power flows taking 10-120 hours with existing methods.

Goal: The goal of this project is to develop new and innovative methods for rapid QSTS simulations to assess Distributed PV impacts accurately: Reduce the computational time and complexity of QSTS analysis to achieve year-long time series solutions that can be run in less than 5 minutes

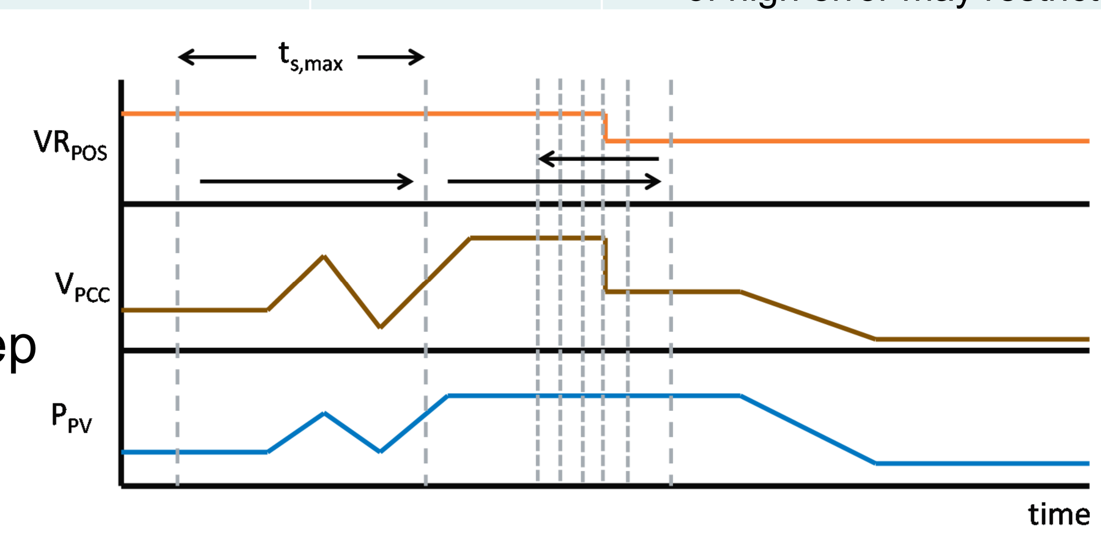
Fast Time-Series Approximations

Algorithm	Reduction in Solution Time	Notes
Causal Variable Time-Step	92.7%	Good performance
Non-Causal Variable Time-Step	95.5%	Good performance
Quantization	96.8%	Good performance
Linearized Voltage Drop	<50%	Little speed improvement and large error
Machine Learning	TBD	Still investigating several different algorithms to improve accuracy
Event-Based Simulation	TBD	Testing the linear sensitivities and formulating equations to deliver all required output metrics
Intelligent Sample Selection	89%	Currently pursuing 2 algorithms. The low probability of high error may restrict continued research

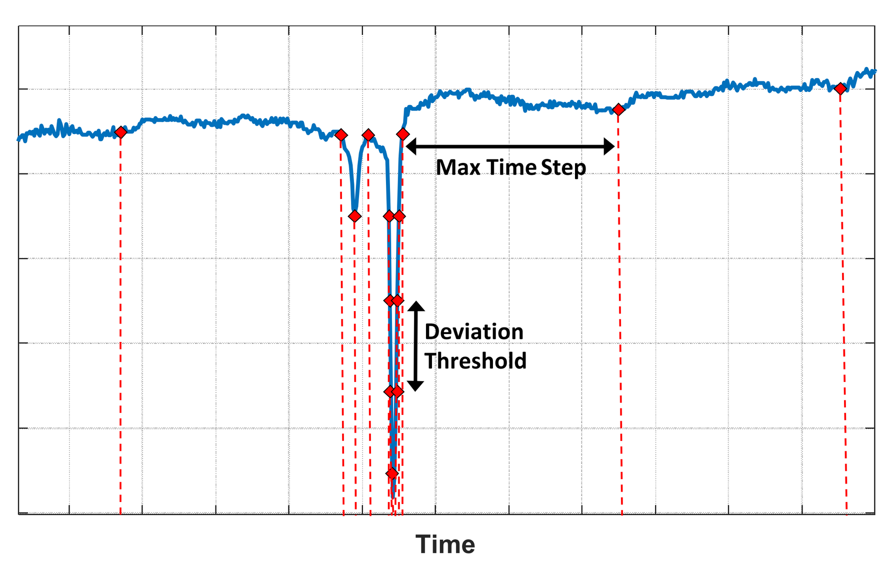
Quantization Example



Causal Variable Time Step

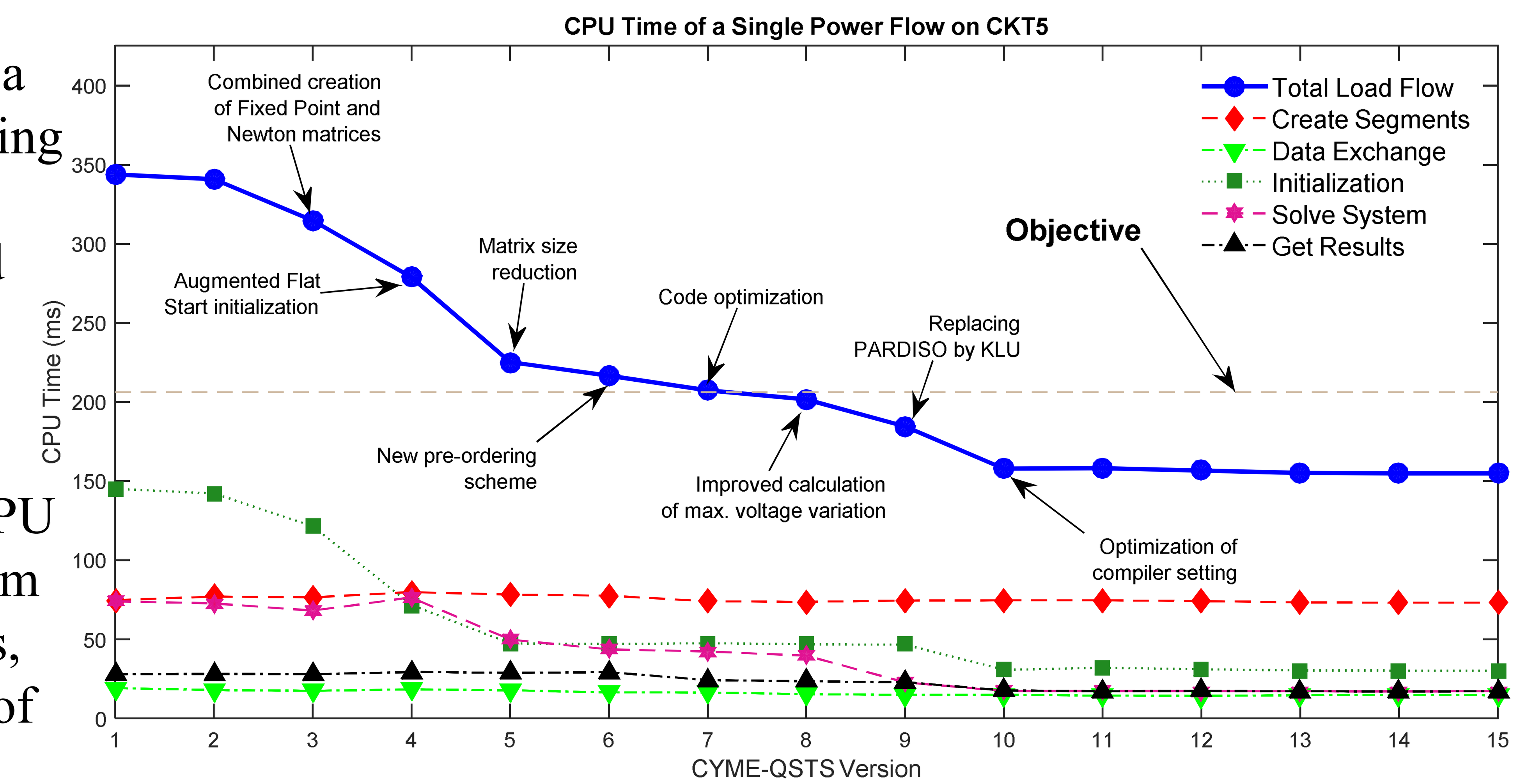


Non-Causal Variable Time Step



Improved Power Flow Solution Algorithms

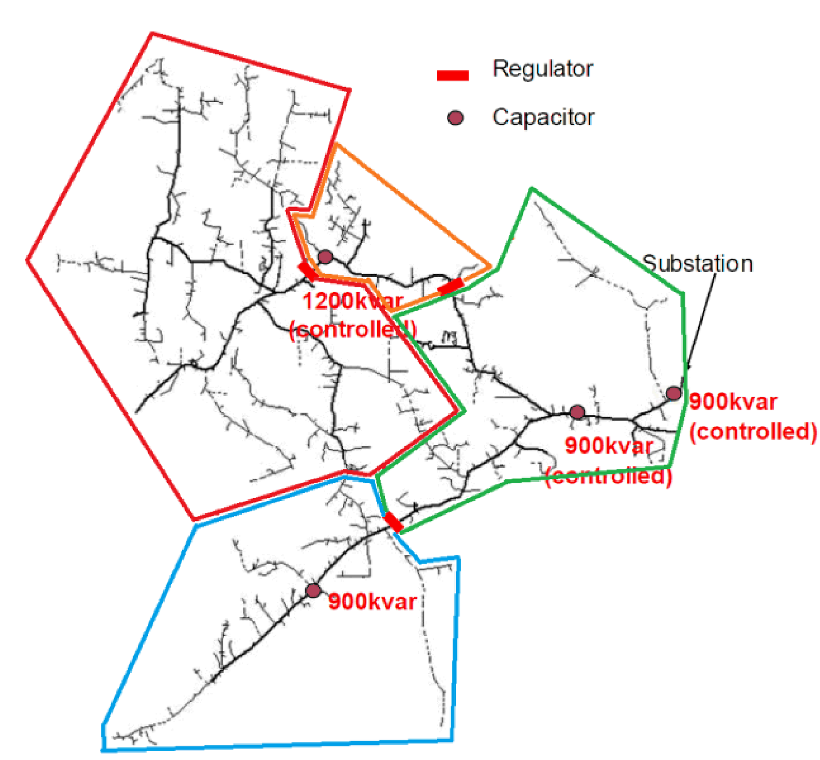
- **Objective:** Reduce by 40% the CPU time necessary to execute a single power flow using CYME's Newton-Raphson Unbalanced (NRU) engine.
- For CKT5 (the base-case network), the CPU time was reduced from 343.8 ms to 154.8 ms, yielding a reduction of 55%. For IEEE 8500 Node Test Feeder a reduction of 61%.



Parallelization of QSTS to Increase Speed

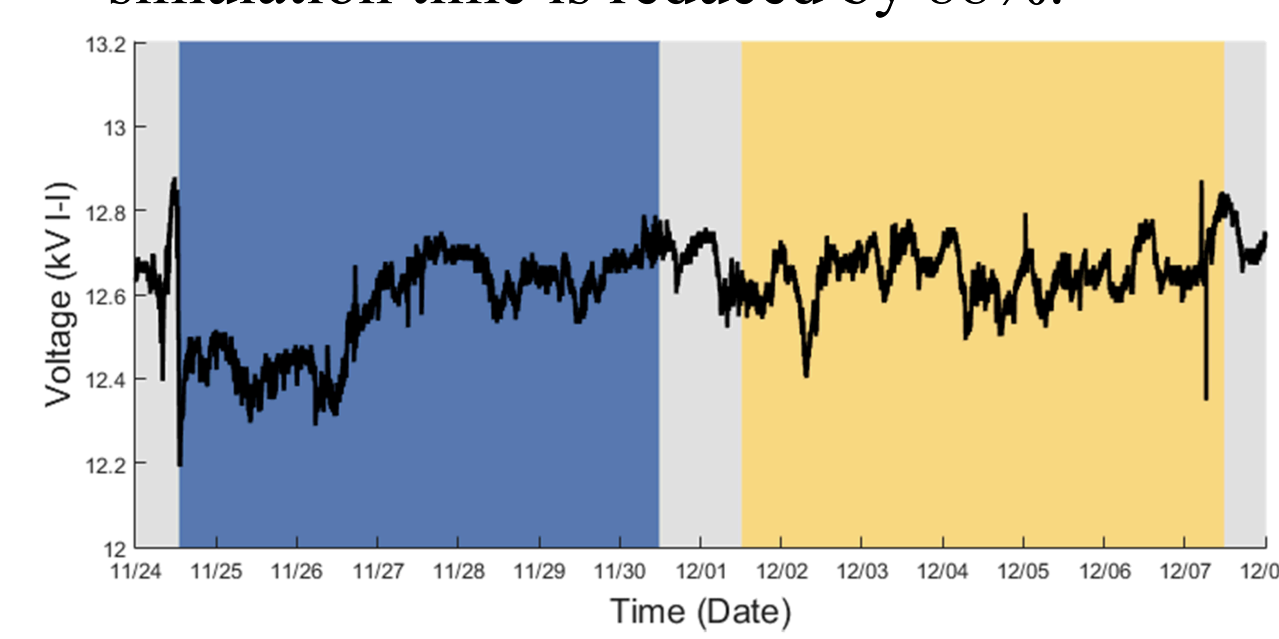
Diakoptics:

- Circuit is intelligently divided and power flows for division calculated (multi-core)
- Diakoptic methods showing 53% to 94% reduction in solution times.



Temporal Decomposition:

- Yearlong QSTS is split into individual solutions and computed via multiple cores
- Solutions are "stitched" together after processing.
- Utilizing 10 parallel processes the required simulation time is reduced by 88%.



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