A Novel Charge Sensitive Pre-Amplifier Structure for Biological Temperature Readout Applications

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***Abstract*— Charge sensitive pre-amplifier architectures have been studied for decades for various applications, most of which adopt a gain stage with capacitor feedback to integrate the signal and a reset path to provide DC bias. For the biological temperature readout front-end, we propose a novel structure without the gain stage, which implies a strong potential for fully integrated high frequency applications. The proposed design provides 0.94 mV/pC with high conversion linearity while consuming only 1.4 micro watts of power with buffer under a 1.2-V supply rail. The prototype occupying a chip area of 0.038 square millimeter is fabricated in 130 nm standard CMOS process.**

Keywords— Charge amplifier, PVDF, charge integration

I. INTRODUCTION

Continuous biomedical monitoring is always desired both in hospital environment and at home, which requires low power and low supply voltage sensor front-end readout electronics. Sensor readout technique has always been one of the strongest driving forces behind the innovation of CMOS integrated circuits (IC). Current-mode transducer is one of the most common types of biosensors. Polyvinylidence fluoride (PVDF), a ferroelectric polymer which exhibits promising degree of compatibility with most of the polymeric substrates used for disposable device fabrication. A change in temperature of the polymer results in the generation of electric charge due to the change in the molecular orientation of the electrical dipoles inside the material. A charge sensitive pre-amplifier is required to perform charge-to-voltage conversion so that the signal can be further processed by the subsequent stages of the sensor readout system.

Charge-sensitive amplifiers are used in a variety of application ranging from medical imaging [1] and particle physics [2][3] to data storage [4]. The configuration is always composed of a gain stage which forms a virtual ground and a current summing node at the inverting input with a feedback capacitor that integrates the input charge and a reset path that in parallel of the capacitor to bias the output at DC. We propose a design that eliminates the gain stage such that the integration process and the DC bias process are achieved by independent circuitry. Due to the elimination of the gain stage, the integration process is no longer limited by the bandwidth of the gain stage. Although our application involves a low frequency operation, we believe it has a strong potential for higher frequency operations due to its wideband nature.

The paper is organized as follow: section II will review the traditional charge sensitive pre-amplifiers. The proposed structure and detailed analysis are presented in section III. Section IV presents the measurement results of the proposed design and is followed by a conclusion as Section V.

II. TRADITIONAL CHARGE SENSITIVE PRE-AMPLIFIERS

A. State-Of-The-Art

The work published in [5] is usually considered the state-of-the-art charge sensitive amplifier structure, although the application was for bio-signal voltage amplification. The configuration is shown in Fig. 1.

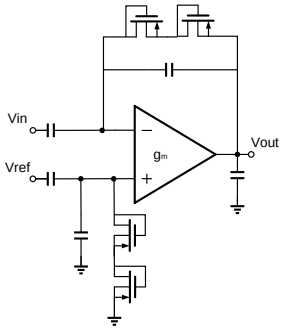

Fig. 1. Schematic of state–of-the-art charge sensitive amplifier.

The voltage signal is differentiated by an input capacitor and is integrated through the feedback capacitor across the operational transconductance amplifier. Very large MOS-bipolar pseudo-resistors are used to reset the circuit so that amplification of low frequency signals is possible.

B. Traditional Configuration for This Application

The target PVDF sensor has a strong response to temperature variation rate which means that the current coming out of sensor is proportional to the rate of the change of the ambient temperature [6]:

$$I_p(t) = p_Q A \frac{dT}{dt} \quad (1)$$

where p_Q is the pyroelectric coefficient, A is the area of the

PVDF transducer, and I_p is the current produced by the transducer due to the temperature change. It can be shown that,

$$\Delta Q_P = p_Q A \Delta T \tag{2}$$

which implies that the temperature is proportional to the accumulated charge.

The traditional charge sensitive pre-amplifier is configured as shown in Fig. 2.

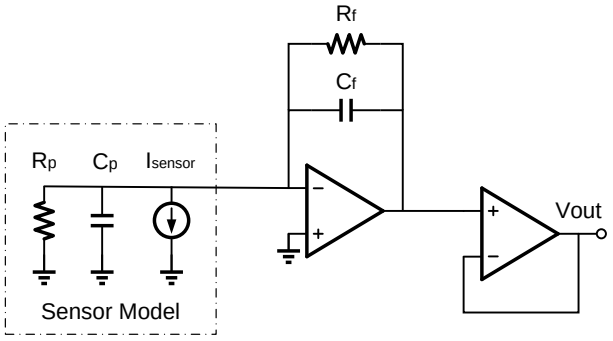

Fig. 2. Schematic of the traditional charge amplifier configuration.

The input charge is integrated by capacitor, C_f creating a voltage at the output, whose amplitude is approximately $-Q_p/C_f$. The feedback resistor, R_f provides a DC path to reset the signal. The output can be expressed as,

$$V_{out}(t) = -\frac{Q_P}{C_f} e^{-t/\tau} \tag{3}$$

where $\tau = R_f C_f$ = 100 MΩ × 1 nF, is the time constant of the circuit chosen to uphold the time constant of the PVDF transducer. Commercial operational amplifiers and discrete components are used in this implementation.

III. Current Mirror Based Charge Sensitive Pre-amplifier

A. The Motivation and Basic Operation

The initial motivation of this design was to integrate the charge processing components on-chip while still being able to interface with the same PVDF sensor. The on-chip integration capacitor is set to 100 pF which does not consume prohibitively large silicon area. To achieve the same time constant, a giga-ohm resistance is needed. Biasing the transistor in deep-ohmic region can realize giga-ohm incremental resistance on-chip [1], but it is difficult to develop a model accurate enough to achieve a predictable time constant complying the transducer. Switched capacitor circuitry could be an option but it requires a clock.

We therefore propose a design that adopts drain-to-source incremental resistance enhanced by a cascode stage to realize the reset function, while the DC level is achieved by an additional loop.

Since the integration capacitor is reduced from 1 nF to 100 pF, to maintain the similar gain or the output voltage swing, a current attenuator is needed. The current mirror based charge sensitive pre-amplifier schematic presented in the Fig. 3 can accomplish this task.

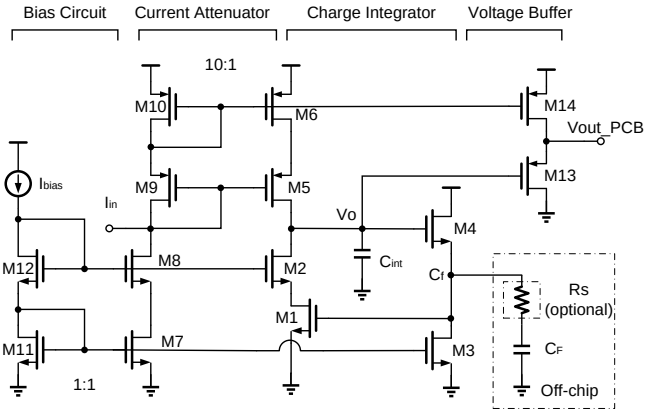

Fig. 3. Schematic of the proposed design.

Since both the equivalent parallel impedance of the transducer and the output impedance of a cascode stage are very high, most of the charge signal will go into the drains of the diode connected PMOS current reference M9 and M10, which render a small signal resistance of roughly $2/g_m$. The signal is then attenuated by the step-down current mirror by a factor of 10 at the PMOS mirror transistors, M5 and M6. Either of the cascode stages M5 and M6 or M1 and M2 are biased to provide GΩ incremental resistance over a voltage swing over 0.6 V. The simulated parallel small signal resistance of the cascode combination is about 0.9 GΩ. The feedback network constructed by M1, M2, M3 and M4 is designed such that at frequencies much lower than the signal frequency, the high loop gain provides the correct DC bias point for the cascode string. At frequencies around or higher than the signal frequency, the loop gain is reduced by the impedance of the off-chip capacitor so that the high output impedance of the cascode stage is maintained.

B. Detailed Circuit Analysis

The sensor current signal is in the tens of nano-amperes thus necessitating that the circuit be biased at low current level to obtain high output impedance of the mirror transistors and to reduce the power dissipation. Since the voltage signal will appear at the junction of the cascode stages, the voltage headroom requirement will limit both the current attenuating accuracy and the noise performance in a way that the mirror transistors cannot be biased at strong inversion. This can be alleviated by carefully biasing the cascode devices. The incremental output resistance of a cascode stage can be expressed as,

$$r_o = A_{int,2} r_{o1} + r_{o1} + r_{o2} \tag{4}$$

where $A_{int,2}$ represents the intrinsic gain of M2, r_{01} and r_{02} represent the small signal drain-to-source resistances of M1 and M2, respectively. The same argument applies to M5 and M6. Thick gate-oxide transistors are used as cascode devices to obtain higher intrinsic gain. The transistors are sized such that either looking up or down at V_O, it sees an over 2-GΩ small-signal resistance. To maintain a predictable DC operating point for the high impedance cascode stage, a high-DC-gain negative feedback loop is constructed by M1, M2, M3 and M4. M4 operates as a source follower while M3 is simply the current source for M4. M1, M2, M5 and M6 construct a cascode gain stage.

There are three major functional goals regarding this feedback loop. First, the loop gain should be high at frequencies much lower than the operating frequencies so that the DC bias point is predictable, which guarantees that the cascode stage can provide a large incremental resistance. Second, the loop gain should be less than one at the operating frequencies so that the large incremental resistance provided by the cascode stage is not attenuated by the loop, which guarantees that the on-chip capacitor integrates at operating frequencies. Third, the phase margin should be large enough so that the loop is stable and the output exhibits smooth settling with a current pulse input.

The loop gain can be approximated as,

$$T_{loop} = \frac{g_{m4}}{g_{ds3} + g_{ds4} + g_{m4} + sC_F} \cdot \frac{g_{m1}}{g_{ds1} \,.\, {g_{ds2}}/{g_{m2}} + g_{ds6} \,.\, {g_{ds5}}/{g_{m5}} + sC_{int}} \tag{5}$$

Rearranging the equation,

$$T_{loop} = \frac{A_{sf}}{1+s\frac{C_F}{g_{ds3}+g_{ds4}+g_{m4}}} \cdot \frac{A_{cc}}{1+s\frac{C_{int}}{g_{cc}}} \tag{6}$$

where

$$A_{sf} = \frac{g_{m4}}{g_{ds3}+g_{ds4}+g_{m4}} \tag{7}$$

$$A_{cc} = \frac{g_{m1}}{g_{cc}} \tag{8}$$

$$g_{cc} = g_{ds1} \,.\, {g_{ds2}}/{g_{m2}} + g_{ds6} \,.\, {g_{ds5}}/{g_{m5}} \tag{9}$$

where A_{sf} represents the gain of the source follower, A_{cc} represents the gain of the cascode stage and g_{cc} represents the parallel small signal conductance of the cascode stage. Equation (6) represents a two-pole system whose second pole is arbitrarily defined by the PVDF sensor. Transistors need to be carefully sized so that the loop transmission expressed in equation (5) achieves the three aforementioned goals. The first goal is easy to achieve due to the high gain nature of the cascode stage. The DC bias point is then determined by (10),

$$V_O = V_{gs1} + V_{gs4} \tag{10}$$

The second goal is to make the loop gain roll down to below 0 dB at frequencies about 10 times higher than the second-pole frequency, which is the operating frequency. This can only be achieved when the first pole is low enough.

To make the loop stable, which is the third goal, the second pole frequency is needed to be somewhat less than 0 dB so that the loop has a phase margin of somewhat higher than 45 degrees. This calls for an even lower first pole. But hopefully, this can be alleviated by compensation: if a series resistor R_S is added to C_F, the transfer function is modified to,

$$T_{loop} = \frac{A_{sf}(1+sR_SC_F)}{1+s\frac{C_F}{g_{ds3}+g_{ds4}+g_{m4}}} \cdot \frac{A_{cc}}{1+s\frac{C_{int}}{g_{cc}}} \tag{11}$$

It can be observed that if $R_SC_F = {C_{int}}/{g_{cc}}$, compensation is achieved.

As explained above, either the second or the third goal requires a low gain at the second pole. This can be accommodated by either reducing the DC gain or employing a very low frequency first pole. However, since the high output impedance of the cascode stage is desired (low g_{cc}), and the transconductance (g_{m1}) efficiency therefore aspect ratio of M1 is constrained by the DC bias point, the gain of the cascode stage cannot be reduced much. Therefore, A_{sf} should be reduced by making g_{m4} a small portion of the denominator of the equation (7).

Since the off-chip capacitor value is arbitrarily set to 220 μF to create a low frequency pole, the summation of g_{ds3}, g_{ds4} and g_{m4} needs to be small. It is easy to achieve small values for the first two terms especially at low bias current levels. To achieve a small value of g_{m4} (tens of nS), an extremely long channel device is needed. Again, the DC bias point and the bias current of M3 also poses a limit on the minimum value of g_{m4}. This trade-off is alleviated by adopting low-threshold-voltage devices offered by the process. The extremely long channel transistor is constructed by putting shorter transistors in series to maintain the accuracy of the transistor model.

PMOS source-follower structure is used to buffer the charge signal with a gain close to unity. The DC bias point can be trimmed off-chip by adding current source or sink at the node C_f.

IV. Experimental Results

The proposed design's prototype is fabricated in 130 nm standard CMOS process. The on-chip integration capacitor consumes 174 μm × 163 μm of the die area while the circuit only takes 36 μm × 49 μm of the die area.

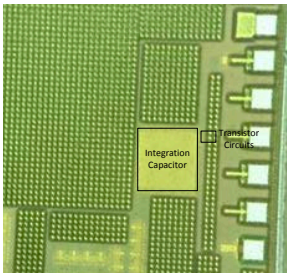

Fig. 4. Die photo of the integration capacitor and the transistor circuits (partialy hidden by metal fill).

Fig. 5 shows a transient response of the charge sensitive pre-amplifier to a current pulse with width of 20 ms and height of approximately 20 nA. The current signal gets attenuated by a factor of 10 and integrated by the on-chip 100 pF capacitor, which should give an approximately 400 mV-height voltage ramp. The measurement shows a 331 mV-height voltage ramp followed by a smooth settling behavior.

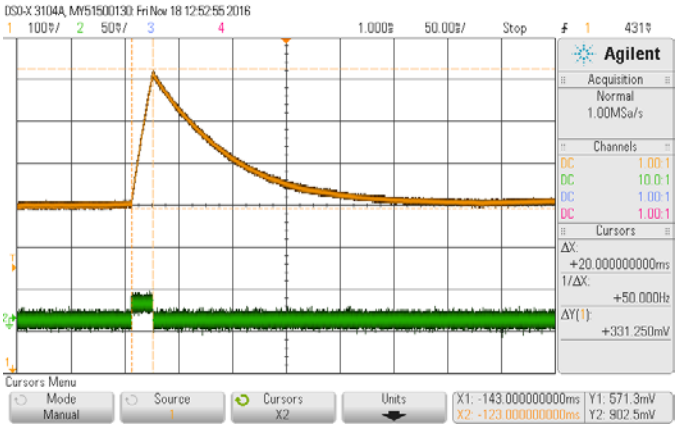

Fig. 5. Transient output voltage response (orange) to a current pulse with peak value of 20 nA and pulse width of 20 ms represented as a scaled voltage pulse (green).

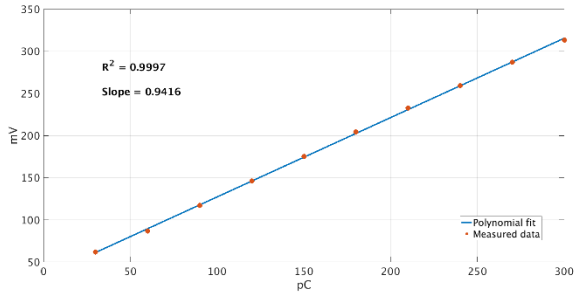

Fig. 6: Charge-to-voltage conversion regression analysis (10 points are taken).

Fig. 6 plots the different input charge amounts versus the height of the output ramp voltage. The different input charge amounts are generated by a fixed pulse width of 500 µs but different peak-value current pulses. This plot also suggest a conversion gain of 0.94 mV/pC for the cascade of the current attenuator and the charge amplifier. Fig. 7 shows the output of the charge sensitive pre-amplifier when a 20 Hz, 40 nA-amplitude sinusoidal current source is issued at the input. The current signal is converted by a voltage signal through a 1 MΩ resistor and its transconductance configuration on board. The measurement suggests correct function of integration.

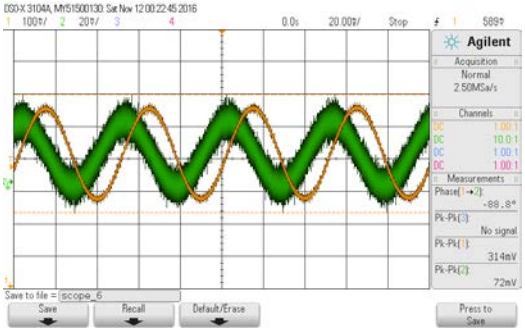

Fig. 7. Transient output voltage (orange) response to a 20 Hz 60 mV sinusoidal current input shown as a scaled voltage signal (green).

V. Conclusion

A novel current mirror based charge sensitive pre-amplifier is designed and fabricated in 130 nm standard CMOS process. The proposed circuit is designated to interface with PVDF temperature sensor for low frequency operations. The pseudo-resistor of the charge amplifier is realized by the small signal resistance of a cascode stage in a predictable range. The idea is verified by measurement results.

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