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Evaluation of a "Field Cage" for Electric Field Control in GaN-based HEMTs that Extends the Scalability of Breakdown into the kV Regime

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***Abstract*— A distributed impedance "field cage" structure is proposed and evaluated for electric field control in GaN-based, lateral high electron mobility transistors (HEMTs) operating as kilovolt-range power devices. In this structure, a resistive voltage divider is used to control the electric field throughout the active region. The structure complements earlier proposals utilizing floating field plates that did not employ resistively connected elements. Transient results, not previously reported for field plate schemes using either floating or resistively connected field plates, are presented for ramps of dV_{ds}/dt = 100 V/ns. For both DC and transient results, the voltage between the gate and drain is laterally distributed, ensuring the electric field profile between the gate and drain remains below the critical breakdown field as the source-to-drain voltage is increased. Our scheme indicates promise for achieving breakdown voltage scalability to a few kV.**

Keywords – High Electron Mobility Transistor; Field Plate; AlGaN/GaN; Quantum Well.

I. INTRODUCTION

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are very promising devices for the next generation of kilovolt (kV) power electronics [1,2,3,4], operating with internal electric fields higher than those of silicon devices. They have the ability to achieve a low on-state resistance for two primary reasons. First, a high electron mobility exists in the 2DEG conduction channel, due to the formation of a polarization-enhanced GaN quantum well created at the AlGaN/GaN interface. Second, they have high breakdown electric fields on the order of 4 MV/cm [5], due to the wide bandgap of GaN (E_g = 3.4 eV). This makes them promising devices to operate in the kilovolt (kV) regime. Additionally, AlGaN/GaN HEMTs are majority-carrier devices which allow enhanced switching speeds at high voltages.

One performance metric for power switching HEMTs is the ratio $V_B^2/R_{on,sp}$, where V_B is the breakdown voltage and $R_{on,sp}$ is the "specific", area-normalized on-state resistance. It is desirable to maximize this ratio; however, in present devices this ratio continues to be well below the ideal values predicted by the Lateral Figure of Merit (LFOM) equation: $V_B^2/R_{on,sp} = q\mu_{ch} n_s E_c^2$ [6,7,8,9]. Here q is the electron charge, μ_{ch} is the electron mobility in the 2DEG channel, n_s is the electronic sheet density in the channel, and E_c is the critical electric field. Note that in HEMTs the critical breakdown field is likely to be an "effective" value that is likely less than the bulk critical field due to avalanche breakdown. Nevertheless, the bulk value is utilized in this paper and represents an idealized, best-case scenario. Deviations in the value of the effective breakdown field do not affect the conclusions regarding the advantages conferred to device scaling by the proposed "field cage" structure presented in this paper.

Although the wide bandgaps of GaN and AlGaN are expected to enable the high-frequency switching capability of such unipolar field effect transistors to be extended to the kilovolt regime, at higher internal electric fields than silicon devices, this goal has yet to be reliably attained. In fact, the difficulty of scaling the breakdown voltage of AlGaN/GaN HEMTs into the kV regime is strongly related to the non-uniform off-state electric field distribution in such devices. One must sufficiently minimize large electric field spikes in the active region that can cause premature breakdown. In the off-state, these electric field spikes typically occur near the drain-side edge of the gate electrode and result in excessive gate leakage current or surface breakdown. This represents a major impediment to scaling the breakdown voltage with geometrical dimensions derived from assuming a more uniform electric field profile extending from the gate edge to the drain.

Electric field control in both widely used Si-based power devices and GaN-based HEMTs is typically managed with field plates designed to smooth the field profiles. Indeed, several field plate implementation schemes for both silicon devices [10,11,12] and GaN devices [13,14,15,16,17,18,19,20,21,22,23,24,25,26,27] using a combination of gate and source-connected field plates are often used, but they still exhibit difficulty in achieving voltage scalability into the kilovolt regime for reasons that will be described in Section II.

Furthermore, appropriate device passivation and encapsulation improves breakdown voltage by eliminating surface flashover, but the fundamental problem of voltage scalability due to the non-

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uniform field distribution remains even when combining such measures with conventional field plate schemes.

In this work, we conduct AlGaN/GaN HEMT simulations that compare the effectiveness of various field plate implementations in mitigating electric field spikes in the GaN channel to provide a more uniform electric field distribution. In doing so, the value of utilizing a distributed impedance "field cage" structure to control electric field spikes in the active region is made apparent. We consider this idea to be an extension of previously reported schemes that utilize floating field plates, *i.e.*, not resistively connected to each other as in this work, such as the work of Nakajima *et al.* [28], or as reported for silicon LDMOS devices [29,30].

For all simulations we use the Synopsys Sentaurus Device tool suite. The Sentaurus software solves the drift-diffusion equations, within the Boltzmann formalism, self-consistently with the Poisson equation. However, the ionization integrals for avalanche breakdown were not evaluated in order to avoid excessive computation time; thus breakdown is not directly calculated, but can be estimated based on the generated electric field distributions.

In the field cage scheme, multiple electrodes, biased proportionately to their lateral gate-drain position, are used to control the electric field throughout the active region of the device. The electrodes may be biased with a resistive voltage divider connected to the drain at one end. Hence, the electric field in the active region is shown to remain relatively uniform as the source-to-drain voltage is increased. This indicates that the field cage concept is a promising one for achieving breakdown voltage scalability. Additionally, the simulated field cage structures are shown to achieve excellent electric field control from DC bias to ramps of dV_{ds}/dt = 100 V/ns, where V_{ds} is the source-to-drain voltage.

This paper is organized as follows: In Sec. II we present our proposed field cage device and compare its performance to other commonly used field-plate structures. In Sec. III the off-state electric field characteristics of several field cage devices are compared and discussed, and a transient analysis is presented in Sec. IV. Implementation considerations are discussed in Sec. V, and the paper is concluded in Sec. VI.

II. LATERAL HEMT "FIELD CAGE" DEVICE

One implementation for a lateral GaN-based HEMT with a field cage is shown in the bottom schematic of Fig. 1, along with standard field plate schemes for comparison purposes (top and middle schematics of Fig. 1). As observed in Fig. 1, the field cage is similar to standard field plate implementations for electric field management in HEMTs in the sense that we utilize a gate field plate (GFP) in conjunction with a source connected field plate (SCFP). However, our proposed structure differs from a typical GFP + SCFP implementation in that we also add voltage divider field plates (VDFPs) to our device between the SCFP and the drain in conjunction with an impedance network to allow for a more linear potential drop between the gate and the drain. Consequently, a more uniform electric field in the 2DEG channel is achieved. Hence, we coin the term "field cage" for this design since the VDFPs and connecting impedance network control the electric field within the channel. In such an approach, the field cage resistance values are chosen in accordance with transient response constraints, as discussed in Sec. IV. The field cage capacitances, also depicted in Fig. 1, correspond to intrinsic parasitic capacitances between adjacent field plates and between the field plates and the channel. These capacitances are not

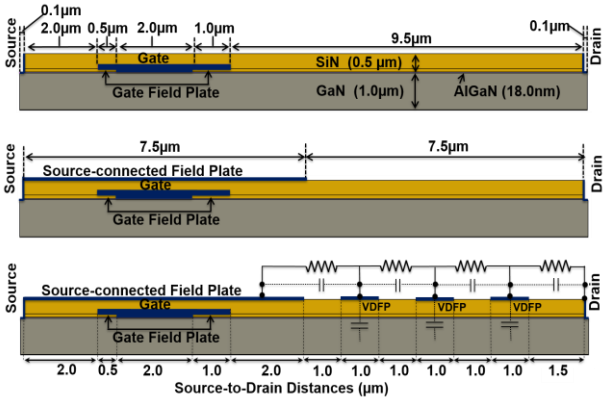

Fig. 1. Top: Standard gate field plate (GFP) scheme; Middle: Standard gate- and source-connected field plate (SCFP) scheme; Bottom: Our proposed HEMT field cage device using an impedance network and voltage divider field plates (VDFPs).

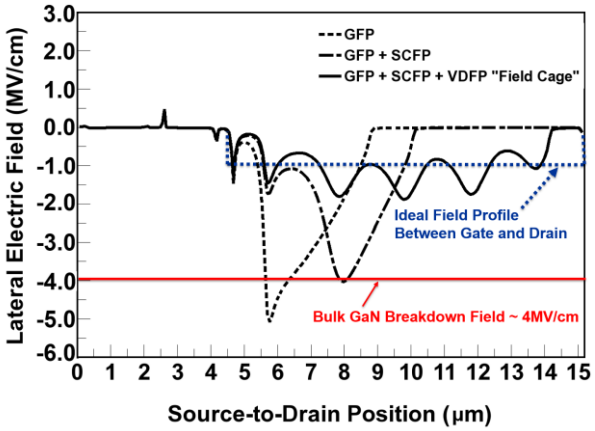

Fig. 2. Lateral component of the off-state electric field profile along the AlGaN/GaN interface for each of the devices depicted in Fig. 1. Devices are biased at pinch-off, V_{gs} = -8.0 V, V_{ds} = 1.0 kV. The ideal flat field profile is also shown.

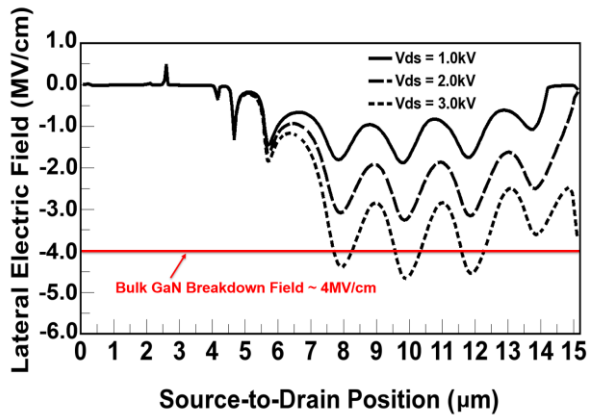

Fig. 3. Lateral component of the off-state electric field along the AlGaN/GaN interface of the field cage device shown in Fig. 1 for three drain voltages. Devices are biased in pinch-off, V_{gs} = -8.0 V.

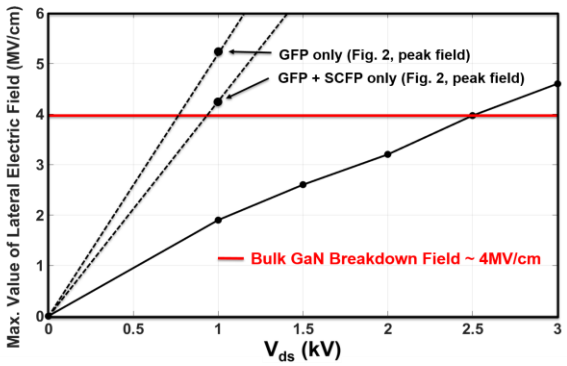

Fig.4. Plot of the maximum value of the electric field for each of the three cases shown in Fig. 3, as well as for two additional biases, indicating linear scalability to biases of about 2.5 kV, after which the maximum electric field exceeds the bulk GaN critical electric field.

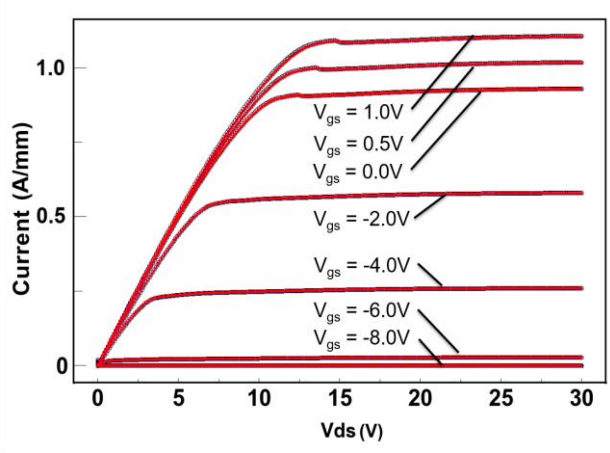

Fig. 5. Steady-state forward *I-V* characteristics of each of the three devices shown in Fig. 1. The curves for each device are identical at steady-state for a given bias, as expected, and are difficult to distinguish on a linear scale.

explicitly chosen as simulation inputs, but are instead parasitic capacitances, and must be minimized through appropriate device design.

As shown in Fig. 1, the simulated HEMT heterostructure consists of an 18.0 nm thick $Al_{0.28}Ga_{0.72}N$ barrier grown on a 1.0 µm thick GaN channel/buffer. A 0.5 µm thick SiN_x passivation layer is employed with a resistivity of 3×10^{12} Ω-cm. At the SiN_x /AlGaN interface the surface donor trap density is 1.0×10^{13} cm^{-2}. Both the AlGaN barrier and GaN buffer have a donor doping concentration of 1.0×10^{16} cm^{-3}. The resultant off-state 2DEG sheet density of the devices depicted in Fig. 1 is approximately 8×10^{12} cm^{-2}. The dimensions are illustrated in Fig 1.

The field plates in the structure are simulated with a finite thickness of 1.0 nm and form a Schottky barrier with the underlying SiN_x. Furthermore, for the field cage simulations presented in this paper, the field cage resistive network is treated as a circuit external to the HEMT, although the field plates are still simulated as metal contacts fabricated on the SiN_x surface. Possibilities regarding the actual fabrication of the resistors will be discussed in Sec. V.

The efficacy of the field cage approach, as opposed to using only GFP and/or SCFP standard schemes, is evident when inspecting the off-state lateral component of the electric field at the AlGaN/GaN interface (the lateral component is shown, since impact ionization in the vertical direction will be suppressed by the AlGaN/GaN heterointerface; this is discussed further below). Shown in Fig. 2 are lateral electric field profiles for the three devices depicted in Fig. 1. In these cases, V_{gs} = -8.0 V (pinch-off condition) and V_{ds} = 1.0 kV. When using only a GFP without the SCFP or field cage, there is a large spike in the lateral electric field located just under the drain-side edge of the gate, which exceeds the bulk GaN breakdown field, which is taken to be 4 MV/cm. Although adding the SCFP mitigates the problem by reducing the magnitude of the field spike as seen in the dashed curve of Fig. 2, the spike is still prominent and exceeds 4 MV/cm. The primary effect of adding the SCFP is a just a lateral shift of the peak to the edge of the SCFP. Fortunately, as observed in the solid curve of Fig. 2, the field cage scheme makes kV regime operation more promising as the field cage "flattens" the electric field between the gate and drain. This is further evidenced by the results of an initial scalability study shown in Fig. 3, where it is observed that even for a 2.0 kV source-to-drain bias, the lateral component of the off-state electric field is still well below the critical field for breakdown. Additional insight is gained by plotting the maximum magnitude of the lateral electric field for each field profile of Fig. 3 as a function of bias voltage. As shown in Fig. 4, linear voltage scalability is observed to about 2.5 kV bias, at which point the electric field exceeds the bulk GaN critical field value.

Prior to generating the results of Figs. 2-4, the I_{ds} - V_{ds} and I_{ds} - V_{gs} characteristics of the GFP structure depicted in Fig. 1 (top) were first calibrated to experimental data by varying the gate Schottky work function and GaN bulk trap density. A Schottky work function of 5.0 eV and a defect trap density of $N_{A,trap} = 2.5 \times 10^{17}$ cm^{-3}, assumed to exist in the GaN layer at approximately 1.0 eV below the conduction band, provided a very good fit to the experimental data for a low-voltage calibration bias condition (V_g = -6.0 V, V_{ds} = 10.0 V). After doing the calibration, the off-state electric field profiles of the devices depicted in Fig. 1 were then determined at bias voltages of V_{gs} = -8.0 V and V_{ds} = 1.0 kV. A value of V_{gs} = -8.0 V was used, as opposed to -6.0 V for the calibration, because the use of a 1.0 kV drain bias resulted in a shift of the pinch-off voltage on the order of 1V. It is important to note that the negative gate voltages used to achieve the blocking state pinch-off voltage imply a depletion mode (normally-on) device. However, power electronic systems usually require enhancement-mode (normally-off) devices. Enhancement-mode devices will be addressed in future work. Excluding them in this analysis does not affect the conclusions regarding electric field management.

As an additional check that the devices of Fig. 1 exhibit proper HEMT behavior, one expects that forward *I-V* characteristics of each device type be identical in steady-state. This is indeed found to be the case, as is shown in Fig. 5, where the curves for each device are virtually indistinguishable from each other at identical bias conditions.

III. OFF-STATE FIELD CHARACTERISTICS

The results presented in Figs. 2-4 indicate that the proposed field cage is a promising design for GaN-based HEMTs operating

in the kV regime. However, the electric field profiles shown in Figs. 2 and 3 are still far from optimal in the sense that they are not "flat" between the gate and the drain. Hence, the middle and bottom schematics of Fig. 6 are considered, in which the same field cage structure of Fig. 1 is retained (as shown again in the top of Fig. 6), except that they use seven-segment field cages instead of a three-segment structure. These seven-segment structures are identical to each other except for the width and spacing of the field plates. As observed in Fig. 7, the off-state (V_{gs}= -8.0 V, V_{ds} = 1.0 kV) lateral electric field profiles are considerably smoother between the gate and the drain for the seven-segment structures as compared to those of the three-segment structure. However, as is also observed in Fig. 7, there is only a minor difference between the two seven segment structures in the off-state lateral electric field profiles at the AlGaN/GaN interface. This indicates that while increasing the number of segments in the structure has a considerable impact on the electric field profile, the details of the geometry of the field plates connecting the resistive network to the surface of the HEMT is not critical.

The corresponding electric field profiles along the heterostructure growth direction (*i.e.*, perpendicular to the direction of the source-to-drain current) are also evaluated at the AlGaN/GaN interface for each of the three structures depicted in Fig. 6 and are shown in Fig. 8. Although the magnitudes of all three curves in Fig. 8 exceed the targeted critical value of 4 MV/cm in GaN, this is not as concerning as it would be for the lateral field profiles, since an avalanche conduction path is more difficult to form in the vertical direction due to the quantum confinement in the channel, which impedes the acceleration of carriers to the critical velocity in the vertical direction necessary for impact ionization to occur.

Refinement of the seven-segment structure may further flatten the off-state electric field profiles. However, as discussed, the insensitivity of the field profiles to the VDFP geometry suggests that the field plate parasitic capacitances are insignificant (as can also be predicted with some simplified parallel-plate capacitance models of the VDFP plates abutting the SiN_x dielectric), and the use of even more field plates is therefore feasible. For example, if a 15-plate structure is used as shown in Fig. 9 (middle), even smoother off-state field electric profiles are obtained and the results approach those of the limiting case of a continuous resistive field plate (RFP) connecting the SCFP and the drain, as shown in the bottom portion of Fig. 9; the resulting field profiles for the three structures depicted in Fig. 9 are shown in Fig. 10.

Ultimately, the optimal number of field cage segments and their spatial configuration reaches a point of diminishing returns. For the purposes of the transient analysis that must be performed in order to choose appropriate resistance values for the field cage resistors, the analysis is focused to studying the middle schematic of Fig. 6, which is the 7-plate structure with 0.5 µm wide VDFPs and 0.5 µm spacing between the VDFPs.

IV. TRANSIENT ANALYSIS

While the use of additional field cage segments, and hence additional resistors, has been shown to result in smoother electric field profiles in the active region of the device during the off-state, a drawback of this approach is an obvious increase in the *RC* time constant that is characteristic of the transient response of the device during switching. When attempting to control the *RC* time constant within design constraints, the field cage resistances must be maximized so as to minimize the persistent off-state leakage current through the field cage resistive network. However, the

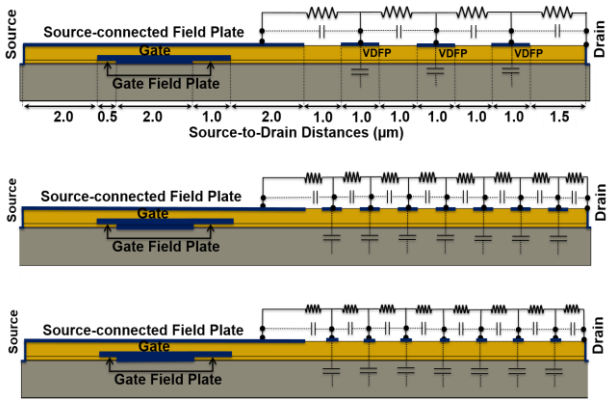

Fig. 6. Variation of the field cage structure of Fig. 1; Top: Fig. 1 3-plate device, VDFP widths = 1.0 µm, plate spacing = 1.0 µm; Middle: 7-plate device, VDFP widths = 0.5 µm, spacing = 0.5 µm; Bottom: 7-plate device, VDFP widths = 0.25 µm, spacing = 1.0 µm.

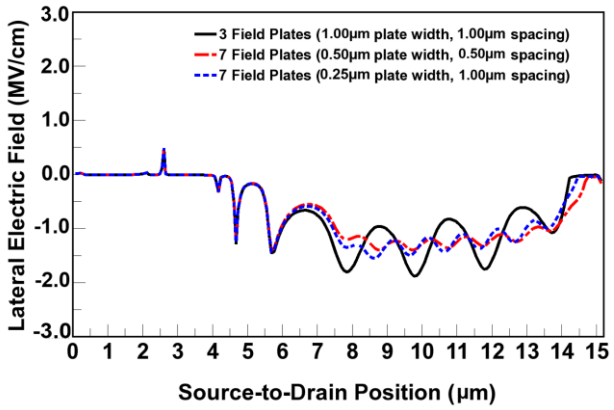

Fig. 7. Lateral component of the electric field along the AlGaN/GaN interface for each of the three structures depicted in Fig. 6. Devices are biased in pinch-off, V_{gs} = -8.0 V, V_{ds} = 1.0 kV.

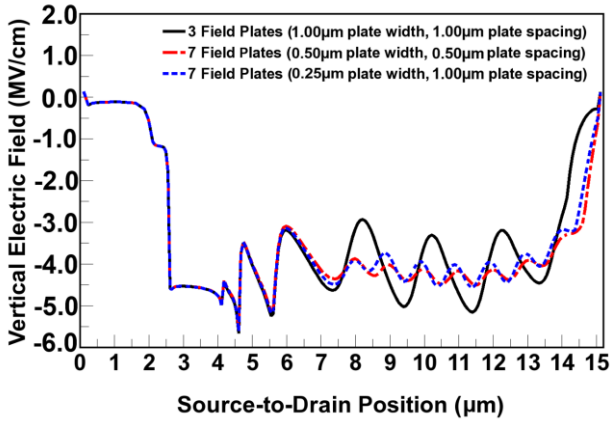

Fig. 8. Vertical component of the electric field along the AlGaN/GaN interface for each of the three structures depicted in Fig. 6. Devices are biased in pinch-off, V_{gs} = -8.0 V, V_{ds} = 1.0 kV.

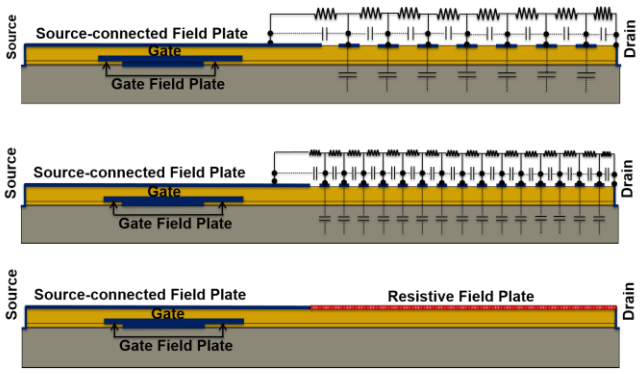

Fig. 9. Further field cage structure variations. Top: 7-plate device, VDFP widths = 0.5 µm, spacing = 0.5 µm (same as middle Fig. 6); Middle: 15-plate device, VDFP widths = 0.25 µm, spacing = 0.25 µm; Bottom: Continuous Resistive Field Plate (RFP) device.

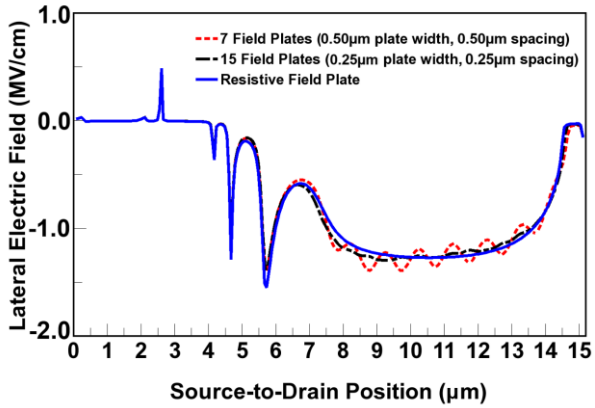

Fig.10. Plot of lateral electric field profiles for 7-plate, 15-plate, and resistive field plate (RFP) devices of Fig. 9, showing the limiting behavior of the RFP at pinch-off, V_{gs} = -8.0 V, V_{ds} = 1.0 kV.

resistances must be chosen carefully so as to not increase the *RC* switching delay beyond acceptable limits.

Such design constraints depend, of course, on the application. For example, during steady-state, continuous mode operation of a DC-to-DC step-down power converter, also known as a buck converter, a HEMT is utilized as a "switch" that is cycled off/on at a particular frequency. When the transistor resistive network (field cage) is in a low voltage state in such a circuit, the current through the field cage resistors is inconsequential, as V_{ds} is nearly zero and the HEMT channel resistance is extremely small compared to that of the total field cage resistance. However, in the transistor blocking state, with V_{gs} set to pinch-off, the voltage across the field cage network for the intended operating conditions could be well in the kV regime. Consequently, some of the current that is intended to pass through the HEMT channel and circuit load will leak through the field cage impedance network and cause undesired power loss.

In order to minimize total losses, which serve as an upper bound on power loss through the HEMT resistive field cage network, the circuit efficiency η is considered as the relevant metric. The calculated ratio of high voltage, blocking state power loss through the field cage, as compared to the ideal power intended to be delivered to the load, must be minimized. Assuming that a worst-case situation exists where $V_{ds} = V_{br}$, the power loss through the field cage is characterized as

$$1-\eta = \frac{V_{br}^2 / R_{tot}}{V_{br} I_{load}} \tag{1}$$

where R_{tot} indicates the total field cage resistance and I_{load} is the intended load current. Rearranging eqn. (1) yields

$$R_{tot} = \frac{V_{br}}{(1-\eta) I_{load}} \ . \tag{2}$$

For example, at V_{ds} = 1000 V if it is required that total power losses be less than two percent ($\eta = 0.98$) and the load current density be constrained to have a maximum value of $I_{max} = 50\ \mu A/\mu m$, then using Eqn. (2) one obtains $R_{tot} = 10^9\ \Omega \bullet \mu m$, which is equivalent to $R = 125\ M\Omega$ per resistor for a 7-plate field cage transistor of $1.0 \mu m$ width, as shown in Fig. 6.

As indicated in the simulation results of Fig. 11, the switching time of the device, using $R = 125\ M\Omega$ for each of the seven resistors shown in Fig. 6 (middle), is approximately 57 ns. One also observes in Fig. 11 that the characteristic *RC* delay of the turn-on results in an approximately 125 V transient voltage overshoot on each field plate as the parasitic capacitances associated with each field plate discharge. To obtain the results of Fig. 11, the drain voltage is ramped between 1.0 kV (off-state) and 20 V (on-state) at dV_{ds}/dt = 100 V/ns, and the gate voltage varies from V_{gs} = -8.0 V for the off-state to an on-state value of V_{gs} = 2.0 V during this same ramp time interval. The *RC* delay time of turn on, denoted as τ in Fig. 11, is calculated as the average time for all field plates to reach steady state, for each resistor having a resistance of either 100, 125, or 150 MΩ. The switching time varies linearly, as expected if the field cage resistances are varied about the 125 MΩ value, as indicated in the Fig. 11 inset data.

While the steady-state, high-voltage electric field profiles provide insight regarding the promise of the field cage concept to achieve kV regime scalability, one must also consider how well the electric field profiles behave during the transient regime. To easily visualize the extent of the variation of the transient electric field profiles, the maximum value of the lateral electric field for three of the field cage structures discussed previously was tabulated at 1.0 ns intervals and the results are plotted in Fig. 12. As observed in Fig. 12, the maximum value of the electric field is less than 4 MV/cm over the entire transient regime. Furthermore, the similarity of the results for each device indicates the relative insensitivity to the field plate capacitances, as was discussed in Sec. III.

V. IMPLEMENTATION CONSIDERATIONS

Three approaches are considered here to implement the field cage scheme in an actual power HEMT. First, discrete, off-chip resistors can be used with contact wires connecting to metal vias attached to each of the VDFPs fabricated on the SiN_x surface. This is perhaps the easiest but crudest approach, although it may

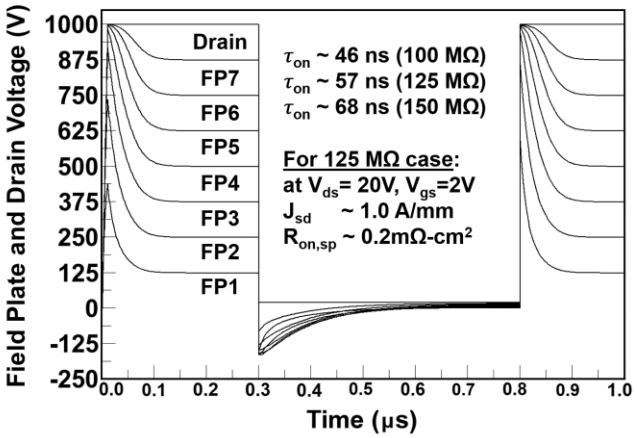

Fig. 11. Transient response of the middle schematic depicted in Fig. 6 (VDFP width = 0.5 µm, spacing = 0.5 µm) for 125 MΩ field cage resistors. VDFP labels FP1 through FP7 are such that FP1 is closest to the gate. Results are qualitatively similar for cases with field cage resistors of 100 MΩ and 150 MΩ.

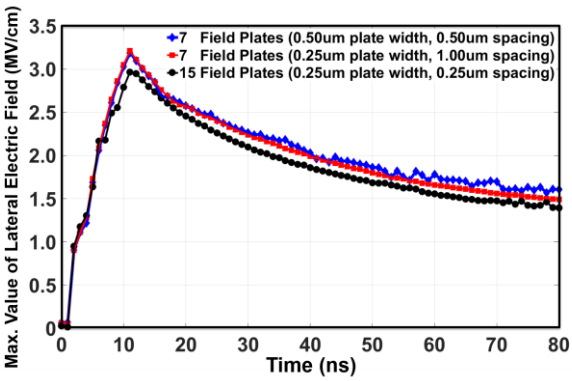

Fig. 12. Transient evolution of the maximum value of the lateral component of the electric field along the AlGaN/GaN interface, corresponding to the two 7-plate devices shown in Fig. 6 (and corresponding results shown in Fig. 7) and the 15-plate device shown in Fig. 9 (and corresponding results shown in Fig. 10).

suffice in some applications. A second approach is to fabricate the resistors on the same die as the HEMT, but otherwise external to the device. Finally, the third and most elegant approach is to fully integrate resistive elements directly on the SiN_x surface connecting each VDFP; considerations regarding this approach are discussed below.

In order to successfully fabricate the field cage resistances directly on the SiN_x surface connecting the VDFPs, a few considerations must be addressed, in addition to achieving the intended resistance values. First, the resistors must remain in the ohmic conductive regime for the voltage range considered. Second, the compatibility of the resistive material with the given material system must be considered (the SiN_x surface in our prototypical device), and third, in such a fully integrated approach it is also important that the resistors be insensitive to thermal fluctuations and be decoupled from electric fields within the device.

A potential material for fully-integrated resistors connecting the VDFPs is *p*-type $Al_xGa_{1-x}N$ with a high Al mole fraction *x*. The low hole mobility [31,32] allows for a high resistance even when the doping is significantly higher than that of silicon. Other advantages of using Al-rich AlGaN for the resistor elements are a high breakdown field (exceeding 10 MV/cm) [33], and the fact that it eliminates the need to etch the epitaxial GaN to define the resistors. The disadvantage of using AlGaN is a relatively less-mature Ohmic contact technology and the fact that dopants tend to have high activation energies, which introduces the risk of thermal instability.

Another possibility for resistor implementation is a procedure where the epitaxial GaN is selectively etched away in a region along the edge of the die, in order to expose an underlying silicon substrate (power GaN HEMTs are often grown on Si substrates). Then, a resistor could be fabricated in the exposed Si using implant doping. The resistor contacts may then be routed to the individual VDFPs on the SiN_x surface using vias in a two-level metal scheme.

Non-stoichiometric titanium nitride (TiN_x) is also a material that can be deposited to achieve a large resistivity range, depending on the nitrogen content. However, to date few studies exist of high-field conduction in highly resistive TiN_x, which is an important consideration for the field cage implementation.

Of course, in integrating resistive elements directly on the SiN_x surface, one must also carefully consider how bond wires would be connected to the field plates and pads. For the 0.5 µm separation between field plates discussed in this proposal, fabrication could be made more complicated if the bond wires were susceptible to arcing. *E.g.*, for the 7-field plate structures of Figs. 6 and 9, a 125 V potential difference between bond wires of 0.5 µm separation results in an electric field of 2.5 MV/cm, which is close to the breakdown voltage of air (~ 3 MV/cm). A discussion of fabrication methods to alleviate this concern is beyond the scope of this paper.

Finally, it is noted that in implementing an RFP device, no voltage divider field plates are necessary.

VI. CONCLUSION

By means of a TCAD investigation, it has been demonstrated that a distributed impedance field cage structure shows excellent prospects for improving the voltage scalability of lateral AlGaN/GaN HEMTs to the kilovolt regime. This is in contrast to only using standard gate- and source-connected field plate schemes. Through careful design optimization of the field cage segments, the structure is shown to achieve excellent electric field control in the AlGaN/GaN channel for both DC conditions (off-state pinch-off) and during transient ramps of dV_{ds}/dt = 100 V/ns. The transient response of prototypical field cage devices is on the order of tens of nanoseconds, consistent with use in a typical application, such as a switching device in a buck converter circuit. Although fabrication of these devices may be challenging, several implementation schemes are possible, and a practical path forward for directly fabricating the field cage resistors on the device surface may be at hand by making use of readily available resistive materials, such as p-doped AlGaN.

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