Design of a Low Parasitic Inductance SiC Power Module with Double-sided Cooling

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***Abstract*—In this paper, a low parasitic inductance SiC power module with double-sided cooling is designed and compared with a baseline double-sided cooled module. With the unique 3D layout utilizing vertical interconnection, the power loop inductance is effectively reduced without sacrificing the thermal performance. Both simulations and experiments are carried out to validate the design. Q3D simulation results show a power loop inductance of 1.63 nH, verified by the experiment, indicating more than 60% reduction of power loop inductance compared with the baseline module. With 0Ω external gate resistance turn-off at 600V, the voltage overshoot is less than 9% of the bus voltage at a load of 44.6A.**

Keywords—low parasitic inductance; double-sided cooling; SiC power module

I. INTRODUCTION

The power loop parasitic inductance induced by the interconnections in packaging can lead to large voltage spikes during turn-off transients of active switches. The undesired voltage spikes can potentially exceed the device's voltage ratings and have significant impact on the safe operation of fast switching devices such as SiC and GaN [1, 2]. Therefore, it is meaningful to reduce the parasitic inductance in the module design stage to mitigate the voltage spikes without sacrificing the switching speed.

Previously, several different low parasitic power modules have been designed. In reference [3], a low parasitic single switch SiC power module is realized with power overlay. A phase leg configuration can be implemented with the aid of a specially designed blade connectors. The power loop inductance is 5 nH, and laminated busbar can be connected to the module. In reference [4, 5], low parasitic phase leg modules are built utilizing the P-cell and N-cell concepts. The loop inductances of these modules are 6.5 nH and 4.8 nH respectively. Utilizing gold stud bump and placing PCB on top of the devices, reference [6] further reduced the parasitic inductance to 0.86 nH by confining the commutation loop area within the thickness of device. Similarly, reference [7] also minimized the commutation loop area by implementing a specialized triple-conductor double-ceramic multi-layer substrate. Laminated busbar is utilized, and the loop inductance is 4.5 nH.

However, as summarized in Table I, all these previous designs are only capable of single-sided cooling and it is desirable to design a module with both low parasitic inductance and good thermal performance.

TABLE I. SUMMARY OF LOW PARASITIC INDUCTANCE POWER MODULES WITH SINGLE-SIDED COOLING.

Organization	L_{ds}	Comment
GE [3]	5.00 nH	Blade connector is needed, laminated busbar design
UTK [4]	6.50 nH	Applies P-cell, N-cell concepts to module design
CPES [5]	4.80 nH	Embeds decoupling caps, laminated busbar connection
Fraunhofer ETH [6]	0.86 nH	Embeds decoupling capacitor
Nissan Fuji [7]	4.50 nH	Multi-layer substrate adds cost, laminated busbar connection

Double-sided cooled module can effectively improve the thermal performance of the power module. However, the parasitic inductances are not optimized in some of the existing double-sided cooled module summarized in Table Ⅱ. In a Si IGBT double-sided cooled module [8], single switch is cooled from both sides. However, long copper bars are used in order to realize a phase leg configuration resulting in a large value of parasitic inductance. In another SiC double-sided cooled module [9], the commutation loop area is still large as it is not confined to the thickness level of the device. Based on the resin mold module design in [8], a recent commercial low parasitic (7.5 nH) SiC module is developed by confining the commutation loop in the thickness level of the device[10]. However, thermal grease is required as heat spreader is used in the resin mold module thus limiting its thermal performance. In reference [11], a low parasitic Si IGBT module is designed with double-sided cooling.

Utilizing double-etching and three-layer copper substrate, the loop area is minimized. However, the design is complicated and not cost-effective as double-etching and multi-layer substrates are required.

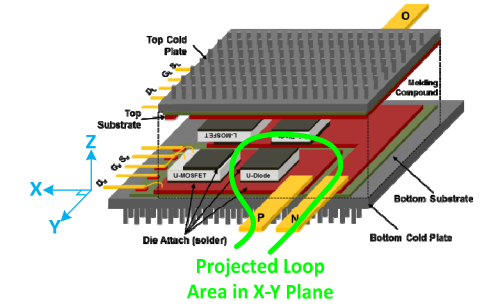
In this paper, a low parasitic inductance SiC power module with double-sided cooling is designed by utilizing two conventional cost-effective substrates. By designing the layout and pattern of the two substrates, low parasitic inductance is achieved and each device can be cooled from both sides. In the following sections, the new design will be discussed and compared with a baseline un-optimized double-sided cooled power module. Both simulation and experiment are done to validate the new design.

TABLE Ⅱ. SUMMARY OF THE PARASITIC INDUCTANCE VALUE OF EXISTING DOUBLE-SIDED COOLED POWER MODULE.

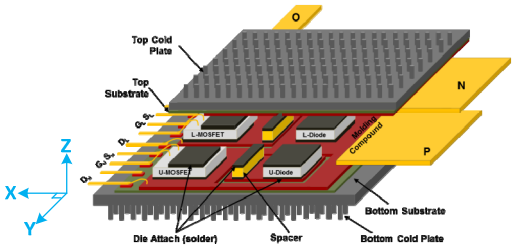
Organization	L_{ds}	Comment
Denso [8]	Not given	Inductance is large due to the long copper bar connection
ORNL [9]	6.03 nH	Parasitic inductance is not optimized
Denso [10]	7.50 nH	Parasitic inductance is reduced, but thermal grease is needed to connect the module to heatsink
University of Nottingham [11]	Not given	Parasitic Inductance is small, Double etching and multi-layer substrate is expensive

II. DESIGN OF THE LOW PARASITIC INDUCTANCE SIC POWER MODULE WITH DOUBLE-SIDED COOLING

The goal of the design is to achieve a low parasitic power module with double-sided cooling. To ensure double-sided cooling, each device needs to be in direct contact with both top and bottom substrates. In terms of reducing turn-off voltage spikes, minimizing the commutation loop area and placing decoupling capacitors in the module are of vital importance [2].



(a) Baseline power module and its commutation loop



(b) Low parasitic power module

Fig. 1. Layout comparison of two double-sided cooled power modules.

To reduce the commutation loop area, a special island substrate layout is designed. Fig. 1 shows the structure layout comparison of a previously designed double-sided cooled module and the new design. The X-Y-Z coordinates are defined such that the devices are distributed in the X-Y plane for both designs. The Z-axis is utilized to realize vertical interconnections and achieve double-sided cooling.

In the baseline module, the commutation loop is formed in the X-Y plane as shown in Fig. 1 (a). Since the device's width and length are usually large (in the range of several mm) compared with its thickness (in the range of several hundreds of μm), the resulting commutation loop covers a large area in the projection of X-Y plane. To reduce the loop area in the new design, the commutation loop is shifted to X-Z plane with the aid of an island substrate layout. To be specific, the upper switch MOSFET and lower switch diode are initially placed close to each other following the P-N cells design concept. Then a dedicated island is patterned in the substrate, and a copper-molly composite shim is used as an interconnection between the top substrate and bottom substrate. With this island design pattern and vertical interconnection, the commutation loop is projected on to the X-Z plane. As a result, the commutation loop area is reduced as it is restricted within the thickness level of devices.

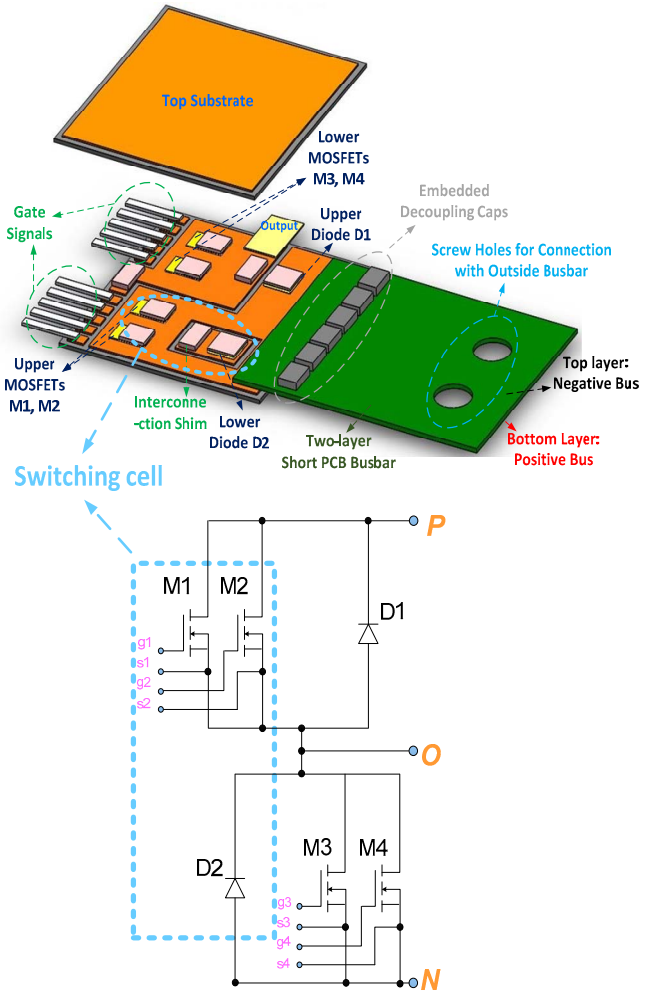


Fig. 2. Exploded side view of the low parasitic inductance power module and its circuit diagram.

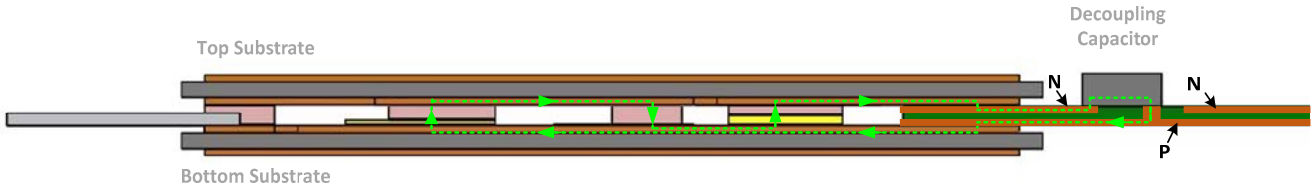


Fig. 3. Current commutation loop illustration for low parasitic inductance power module.

However, as pointed out in references [2, 6, 12], the parasitic inductance of terminal connections and external bus bar will also contribute to the total power loop inductance. Although the parasitic inductance of the power module itself is small, the voltage overshoot can be large if the parasitic inductance outside the modules are not decoupled. Adding decoupling capacitors on the module's DC bus terminal side can effectively offset the parasitic inductances caused by external circuit layout. Therefore, in the module design stage, it is important to integrate decoupling capacitors in the module as well.

In this design, a 7oz two-layer PCB with controlled thickness is used to solve this issue. Fig. 2 illustrates the whole structure of the low parasitic double-sided cooled power module together with its circuit diagram. The decoupling capacitors are easily soldered on a short laminated PCB bus bar and the PCB is closely soldered to the bus terminals of the power module.

Another function of the PCB bus bar is to realize easy connection of the power module with outside bus bars. As can be seen from Fig. 2, the connection with external bus bars can be implemented through screw-hole connections at the other end of the short PCB.

As discussed above, two conventional cost-effective AlN substrates are patterned to obtain low parasitic inductance. Phase leg configuration is realized where two 1200V SiC MOSFETS and one anti-paralleled 1200V SiC Schottky diode together forms one switch. The MOSFETs and diodes are specially designed: both sides of the device are metallized and solderable. Gate connections are implemented with 5 mil bond wires. The whole commutation loop is shown in Fig. 3 assuming current is going from positive bus to negative bus. As can be seen, the loop area is greatly reduced as it is shifted to X-Z plane.

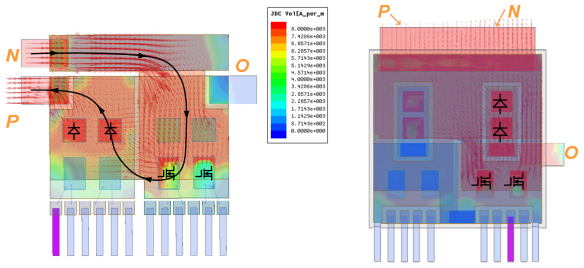
III. Simulation Results

The mechanical layouts of the baseline module and new double-sided cooled module are imported into Ansys Q3D. Then the materials are added, and the power loop inductance values are simulated as summarized in Table 3.

TABLE Ⅲ. Q3D Simulation Result of Parasitic Inductance for Different Modules.

Module	Lower Device Turn-off L_{ds}
Baseline Module	6.03 nH
Newly Designed Module	1.63 nH

As can be seen, the power loop inductance is reduced from 6.03 nH to 1.63 nH. More than 70% reduction is achieved in the new design. Fig. 4 illustrates the current density distributions for both modules. The loop area of the baseline module is also illustrated as indicated by the black solid line. It can be observed that the commutation loop in the previous design is in the X-Y plane and contours a large area. On the contrary, as has been discussed in detail in the previous section, the loop area in newly designed module is confined in the Z-axis where the device's thickness is marginal.

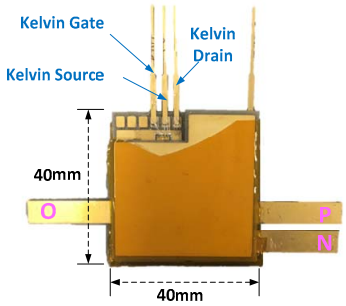


(a) Baseline power module (b) Low parasitic power module

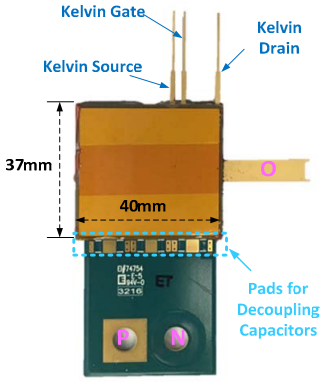
Fig. 4. High frequency current density distributions of different modules.

IV. Experiment Results

Both the baseline module and low parasitic module are fabricated for experimental comparisons. At this initial design stage, only one SiC schottky diode is used as upper switch and one SiC MOSFET is soldered as the lower switch. Double pulse tests are performed to characterize the lower MOSFET's switching performance and extract the module's parasitic inductance.



(a) Baseling power module

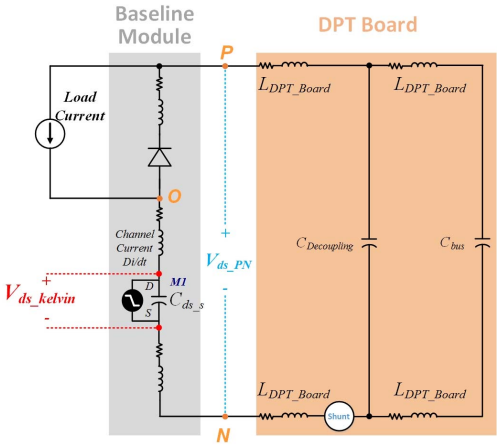


(b) Low parasitic power module

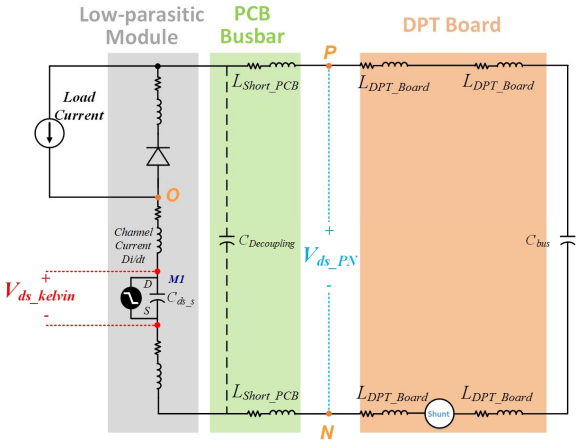
Fig. 5. Fabricated modules without pin-fin heatsink.

Fig. 5 shows the fabricated power modules without pin-fin heatsinks. For the low parasitic power module, the PCB bus bar is soldered in the same process the devices are soldered. The exposed pads on the PCB are used for soldering decoupling capacitors. Notice that each module is fabricated with access to the device's drain-source voltage $V_{ds,Kelvin}$ directly through a kelvin connection. The kelvin drain-source voltage is only connected to passive voltage probe for sensing. Therefore, little current will be introduced in the sensing loop and $V_{ds,Kelvin}$ can represent the real voltages across the device during switching transients. Meanwhile, as shown in Fig. 5, the voltage across the P, N terminals V_{ds_PN} will also be recorded in experiment.

Fig.6 shows the circuit diagrams of each power module together with these two voltage sensing points indicated. For the baseline module shown in Fig. 6 (a), the decoupling capacitors are located on the testing board and the drain-source current of the MOSFET can be obtained from the shunt. Only parasitic inductance and resistance of the package exist in between those two voltage sensing points. Therefore, with a knowledge of the rate of change of current during turn-off, the parasitic inductance of the power can be extracted directly by comparing the Kelvin sensed drain-source voltage V_{ds_Kelvin} with the terminal voltage V_{ds_PN}.



(a) Baseline power module



(b) Low parasitic module

Fig. 6. Circuit diagrams of the extraction circuit for each module.

Fig. 7 illustrates the dedicated experiment set-up used to extract the parasitic inductance of the baseline module. Aside from the film decoupling capacitors, surface mounted ceramic capacitors are soldered on the back side of the printed circuit board to form a two-stage decoupling network.

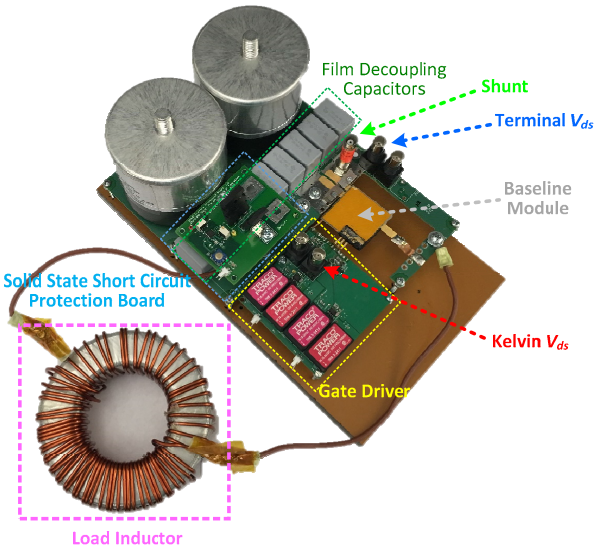


Fig. 7. Test bench for parasitic inductance extaction of baseline module.

Double pulse test is done at 600V DC bus, and Fig. 8 shows the turn-off waveforms at 46A with a turn-off gate resistor of 10Ω. The di/dt rate is calculated to be -4.08 A/ns and corresponding voltage difference is 26.90V. Therefore, the parasitic inductance of the baseline module $L_{loop\ base}$ is calculated to be:

$$L_{loop\ base} = L_{ext} = 26.9\text{V}/(4.08\text{A/ns}) = 6.59\ \text{nH} \quad (1)$$

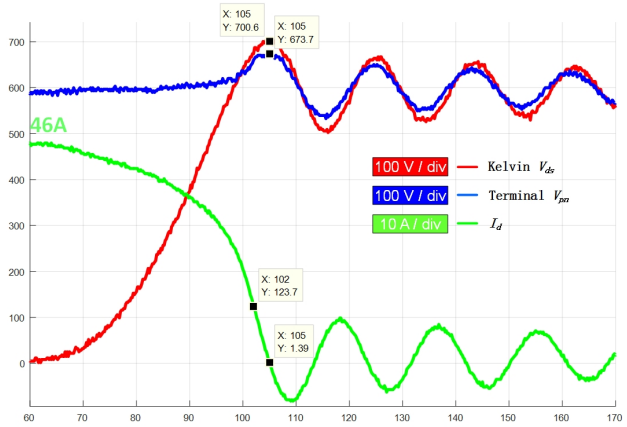


Fig. 8. Experimental turn-off waveforms of lower MOSFET in baseline module.

Compared with the simulation result in Table Ⅲ, less than 10% difference is obtained. Similar parasitic extraction approach can be applied to the low parasitic power module if the decoupling capacitors are not added as indicated by the dashed line in Fig. 6 (b). However, even without soldering the decoupling capacitors, the extracted parasitic inductance L_{ext}

will differ from the module's power loop inductance. In fact for the low parasitic module circuit, L_{ext} consists of two parts: the power loop inductance of the power module $L_{loop\ low}$ and the parasitic inductance of the short PCB busbar $L_{PCB\ Busbar}$. Simply applying the same method will not provide an accurate inductance value of the power module. Therefore, a frequency domain analysis approach is used instead to extract the parasitic inductance of the power module solely.

To implement frequency domain analysis, six 1 kV 0.15 uF ceramic decoupling capacitors are soldered as shown in Fig. 9. The capacitance of is selected such that the voltage across the decoupling capacitor is unchanged during the turn-off switching transients making this decoupling path effectively short at high frequency. In this way, the ringing frequency of the Kelvin drain-source voltage V_{ds_Kelvin} will be mainly determined by the power loop inductance of the newly designed module $L_{loop\ low}$ and the junction capacitance C_{ds} of the device at bus voltage.

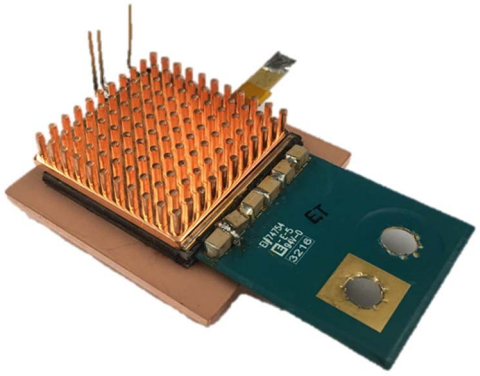


Fig. 9. Fabricated low parasitic inductance power module with decoupling capacitors and fin-pin heatsinks.

Similar to Fig. 7, the double pulse test bench for evaluating the parasitic inductance of the new module is shown in Fig. 10. The same gate drive circuits are used but the gate resistors are varied. Fig. 11 illustrates the experiment turn-off waveforms of the lower switch at 600 V with an external gate resistance of 5Ω. The load current is set to 44.6 A. The blue curve indicates the terminal voltage V_{ds_PN}, and as expected its value is unchanged during the turn-off switching transients. The red curve (V_{ds_Kelvin}) denotes the real voltage across the devices which peaks to 638V under this above mentioned conditions. The ringing frequency f_0 of V_{ds_Kelvin} is calculated to be 210.5 MHz based on the experiment waveform. At 600V, the device's junction capacitance is read to 220 pF according to the datasheet (CPM2-1200-0025B), and its value is almost unchanged when drain-source voltage is above 500V. Correspondingly, the parasitic inductance of the module is calculated to be:

$$L_{loop\ low} = \frac{1}{4\cdot\pi^2\cdot f_0^2\cdot C_{ds}} = 2.60\ \text{nH} \qquad (2)$$

As can be observed, the extracted parasitic inductance in experiment is larger than the simulation result. One of the explanations is due to the discrepancy that two MOSFETs in parallel are simulated in Q3D while the real fabricated module only has one MOSFET.

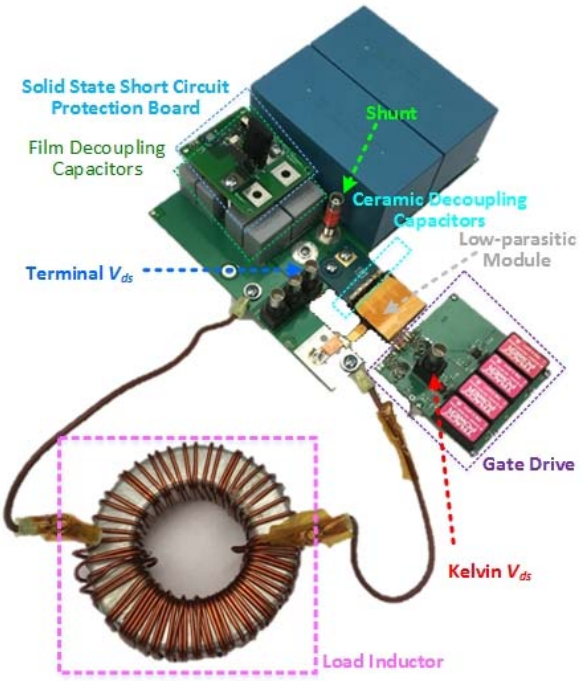


Fig. 10. Test bench for parasitic inductance extaction of the new module.

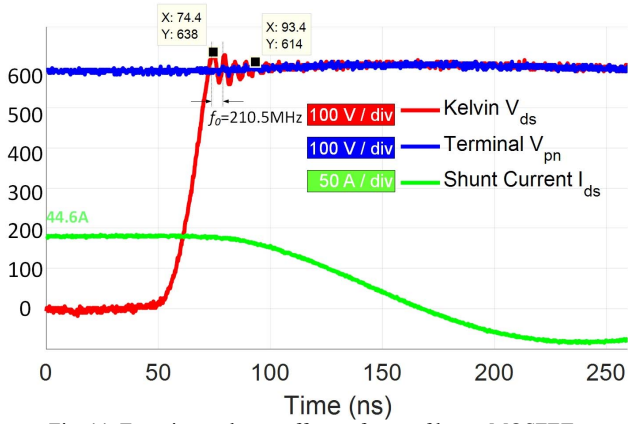


Fig. 11. Experimental turn-off waveforms of lower MOSFET in low parasitic module with 5Ω external gate resistance.

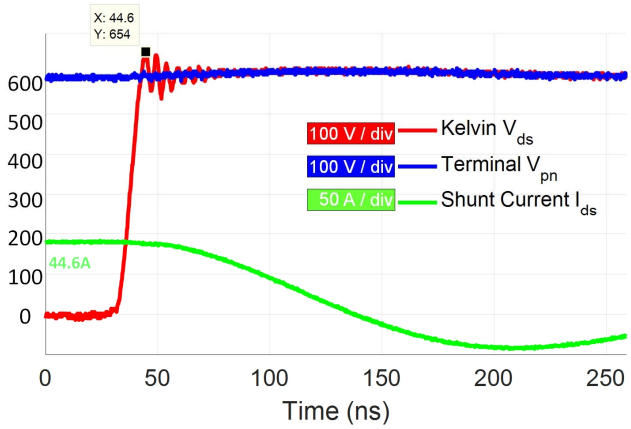


Fig. 12. Experimental turn-off waveforms of lower MOSFET in low parasitic module with 0Ω external gate resistance.

Another experiment is carried out for the same module where the external gate resistance is further reduced to 0Ω at the same DC bus voltage and load condition. Fig. 12 shows the waveforms. Compared with Fig. 11, the voltage overshoot is increased from 638 V to 654 V. Still, the overshoot voltage is less than 9% of the DC bus voltage at a load current of 44.6 A.

V. Conclusion and Future Work

In this paper, the design of a low parasitic inductance SiC power module with double-sided cooling is explained in detail. By introducing the island substrate layout design with vertical interconnection and implementing decoupling capacitors with PCB busbar, the power loop inductance of the power module is effectively reduced.

Simulation result shows a 70% reduction in parasitic inductance compared with a previously designed baseline double-sided power module.

Dedicated double pulse test boards are designed to extract the parasitic inductance of each module experimentally. The experiment result shows a good agreement with the simulation result for baseline module (6.03 nH in simulation and 6.59 nH from experiment). For the low parasitic module, the extracted parasitic inductance is 2.6 nH compared with 1.63 nH in simulation. From the experiment result, more than 60% parasitic inductance reduction is achieved with the new design.

In terms of future work, a phase leg module with two MOSFETs in parallel is to be fabricated for testing. The parasitic inductance of two devices in parallel is to be extracted experimentally and compared with simulation results. Meanwhile, the characterization of the thermal performance and evaluation of thermal-mechanical stress for the new design needs to be studied as well.

Acknowledgment

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References

[1] C. Zheng, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in Power Electronics Conference (IPEC), 2010 International, 2010, pp. 164-169.

[2] C. Zheng, D. Boroyevich, P. Mattavelli, and K. Ngo, "A frequency-domain study on the effect of DC-link decoupling capacitors," in Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, 2013, pp. 1886-1893.

[3] L. D. Stevanovic, R. A. Beaupre, E. C. Delgado, and A. V. Gowda, "Low inductance power module with blade connector," in Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE, 2010, pp. 1603-1609.

[4] C. Zheng, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications," IEEE Transactions on Power Electronics, vol. 29, pp. 2307-2320, 2014.

[5] S. Li, L. M. Tolbert, F, and F. Z. Peng, "Stray Inductance Reduction of Commutation Loop in the P-cell and N-cell-Based IGBT Phase Leg Module," IEEE Transactions on Power Electronics, vol. 29, pp. 3616-3624, 2014.

[6] E. Hoene, A. Ostmann, B. T. Lai, C. Marczok, A. Musing, and J. W. Kolar, "Ultra-Low-Inductance Power Module for Fast Switching Semiconductors," PCIM 2013, 2013.

[7] S. Tanimoto and K. Matsui, "High Junction Temperature and Low Parasitic Inductance Power Module Technology for Compact Power Conversion Systems," IEEE Transactions on Electron Devices, vol. 62, pp. 258-269, 2015.

[8] N. Hirano and e. al, "DENSO Technical Rev," Vol16, pp. 30-37, 2011.

[9] Z. Liang, "Integrated double sided cooling packaging of planar SiC power modules," in 2015 IEEE Energy Conversion Congress and Exposition (ECCE), 2015, pp. 4907-4912.

[10] H. Ishino, T. Watanabe, K. Sugiura, and K. Tsuruta, "6-in-1 Silicon carbide power module for high performance of power electronics systems," in 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), 2014, pp. 446-449.

[11] A. K. Solomon, A. Castellazzi, N. Delmonte, and P. Cova, "Highly integrated low-inductive power switches using double-etched substrates with through-hole viases," in 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), 2015, pp. 329-332.

[12] F. Yang, Z. Liang, Z. Wang, and F. Wang, "Parasitic inductance extraction and verification for 3D Planar Bond All Module," in 2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM), 2016, pp. 1-11.