

Exceptional service in the national interest



Wafer Level Fabrication of Planarized Josephson Junctions with TaN_x Barriers

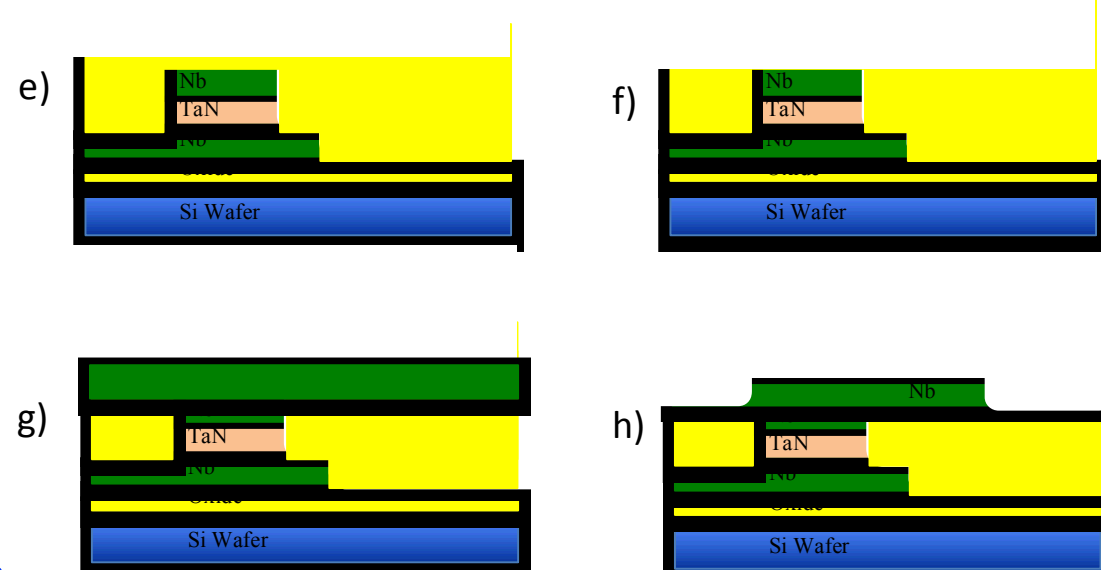
M.D. Henry, S. Wolfley, J. Miner, E.A. Douglas, T.R. Young, R. Lewis, L. Brunke, C.J. Pearce, T. Monson, N. Missert

Abstract

Niobium and aluminum-based Josephson junctions are now produced at the wafer level with CMOS fabrication techniques for uses such as quantum computation and superconducting computing electronics [1]. However, the cornerstone Nb/Al-AIO_x/Nb junction relies on a thin aluminum oxide layer whose electronic properties must be carefully grown and stabilized. Further, Nb/Al-AIO_x/Nb junctions with moderate critical current densities require the addition of a shunt resistor, which adds complexity to the design and fabrication [2]. In this work, a TaN_x barrier, planarized wafer level process is demonstrated using niobium superconducting layers and tantalum nitride for the barrier layer. Control over the sputtering parameters during deposition permits variation of the TaN_x electronic properties from superconducting to insulating at cryogenic temperatures. Nb/TaN_x/Nb junctions may offer increased robustness in fabrication sensitivity and fabrication process variations relative to those of Nb/Al-AIO_x/Nb [3].

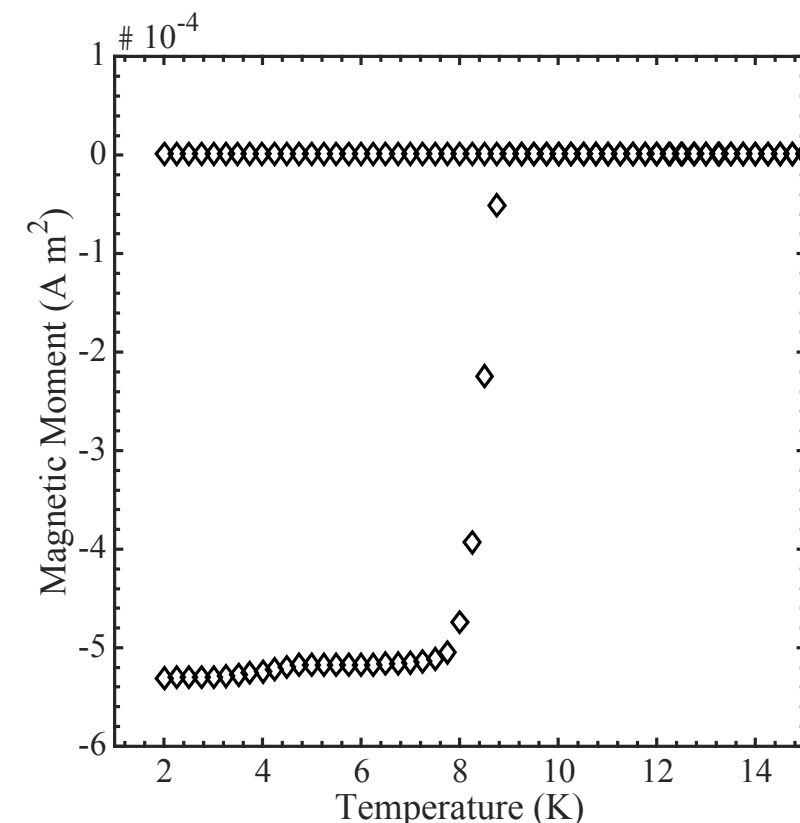
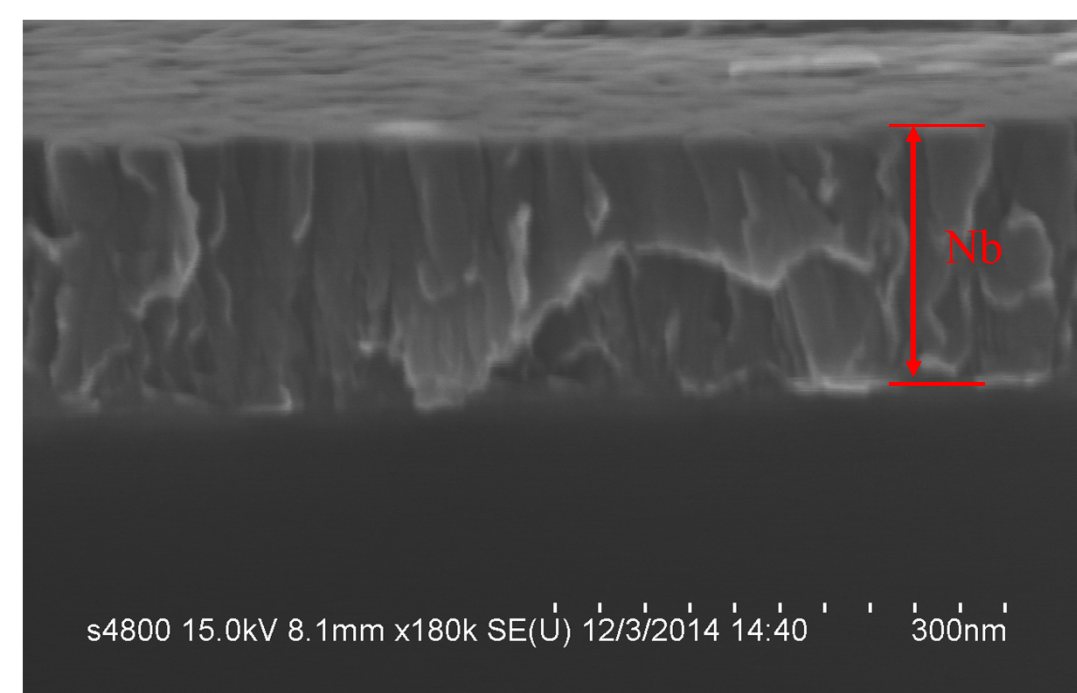
Fabrication Sequence

- Trilayer of Nb (200 nm) / TaN_x ~ (10/20/40nm) / Nb (200 nm) is deposited
- Mesa etch is patterned and etched into the bottom layer of Nb.
- Metal 1 etches the remaining stack down to the bottom oxide.
- CVD Silicon dioxide is deposited over the metal stack.
- CMP flattens the oxide.
- A first oxide etch slowly etches back the oxide everywhere until the top Nb is exposed.
- Metal 2 (Nb 200 nm) is deposited.
- Metal 2 is patterned.



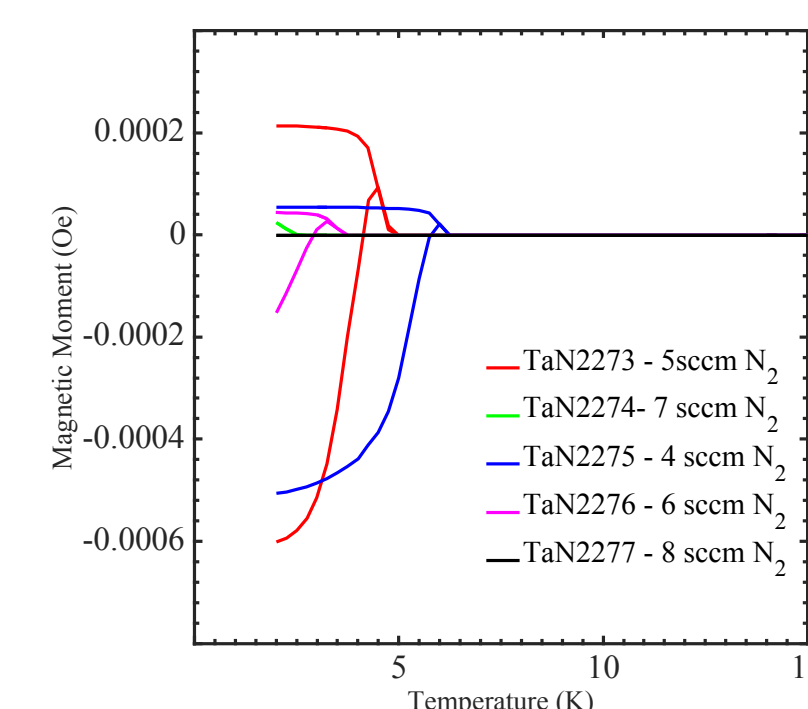
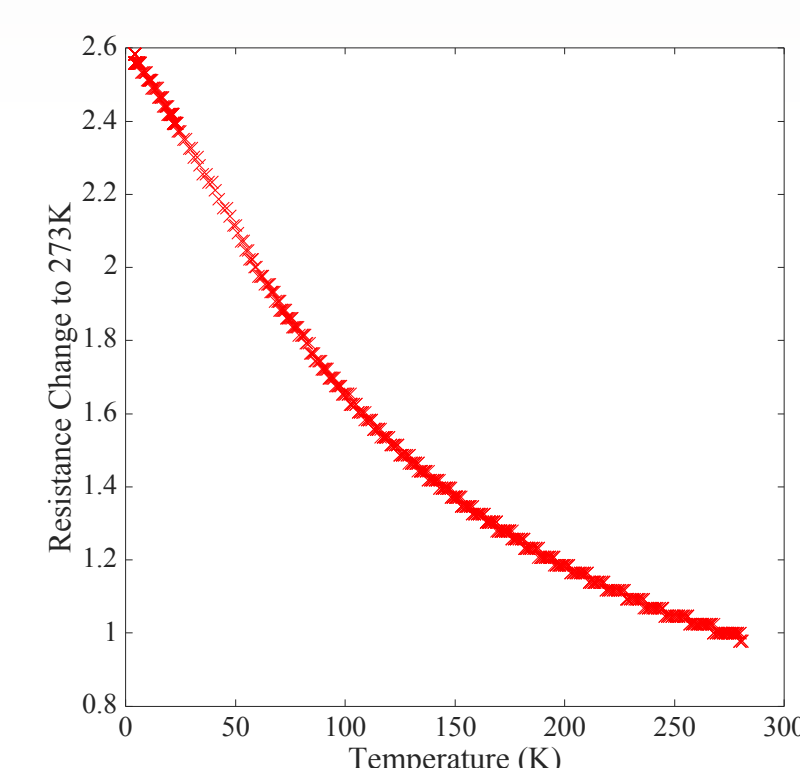
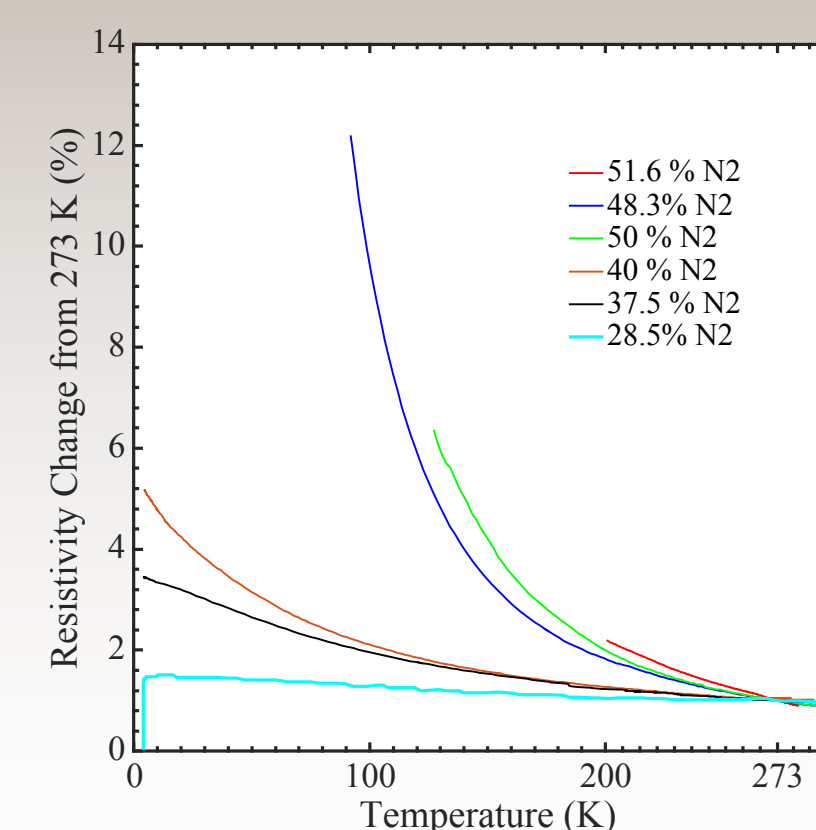
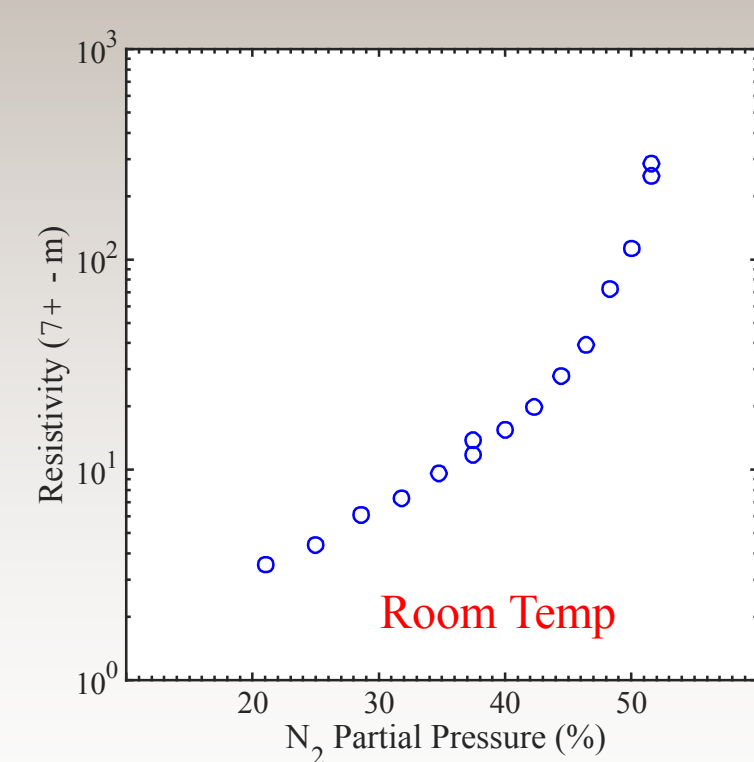
Niobium Characterization

The RT sputter deposited Nb film has been characterized to be resistant to oxidation for periods longer than 17 mo with transition temperatures at ~8.5 K (dirty limit) as measured using Quantum Designs magnetic properties measurement system (MPMS). Film stress was set to 700 MPa for 200 nm thick depositions, using a Denton Discovery 550 sputter system: DC power 225W, Ar flow 22.5 sccm, chamber pressure 4.8 mTorr.



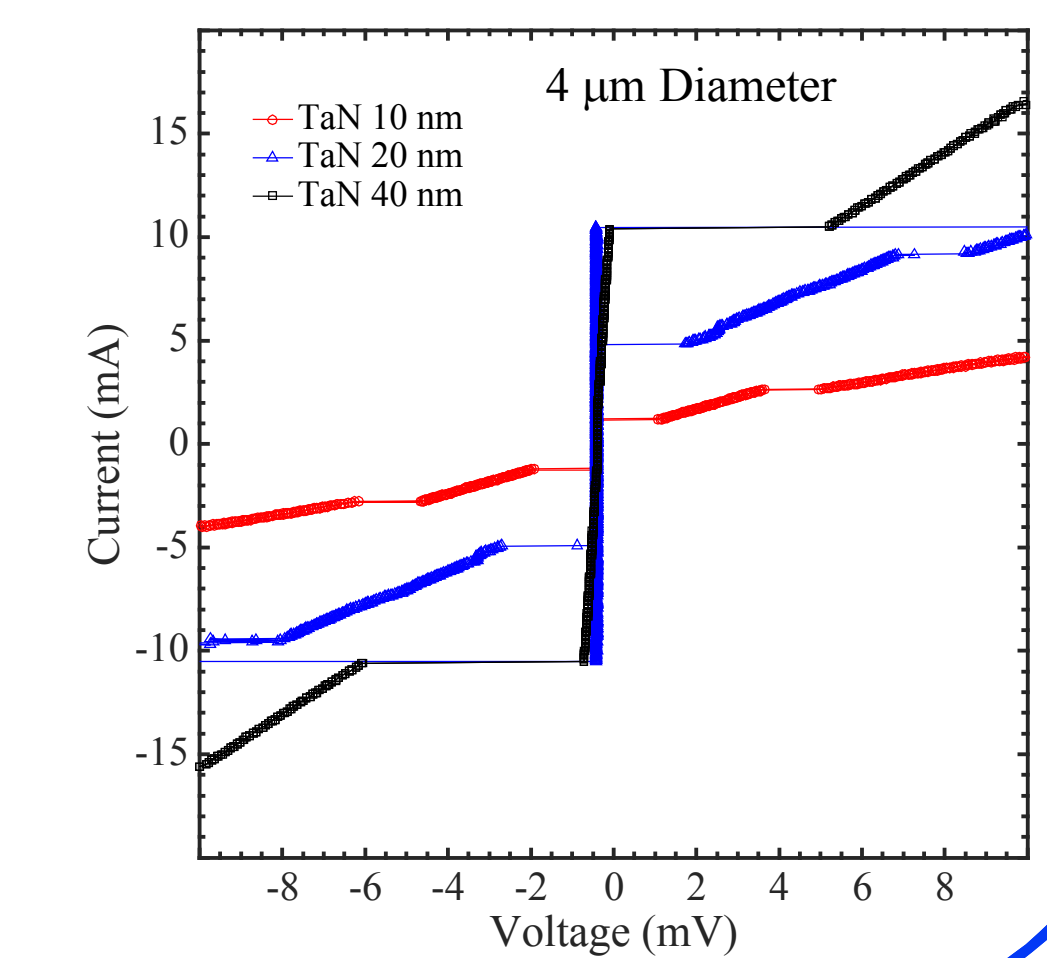
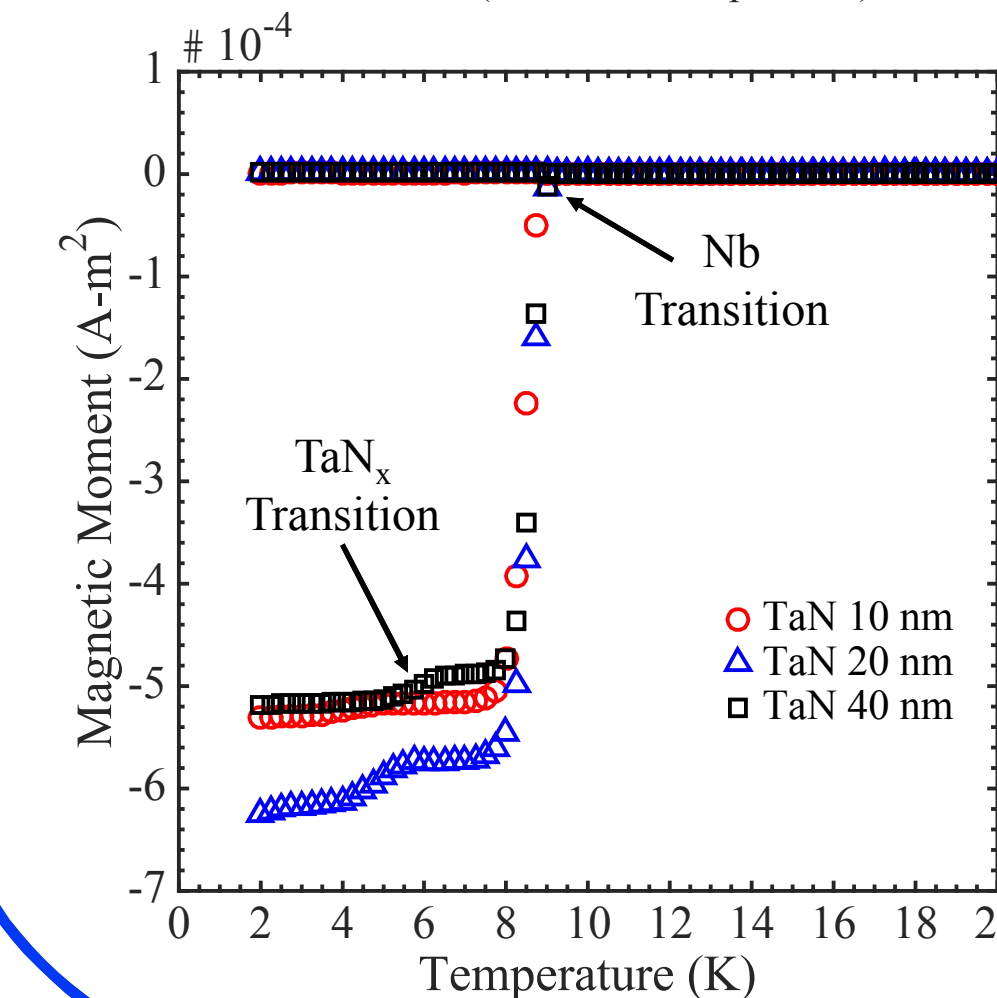
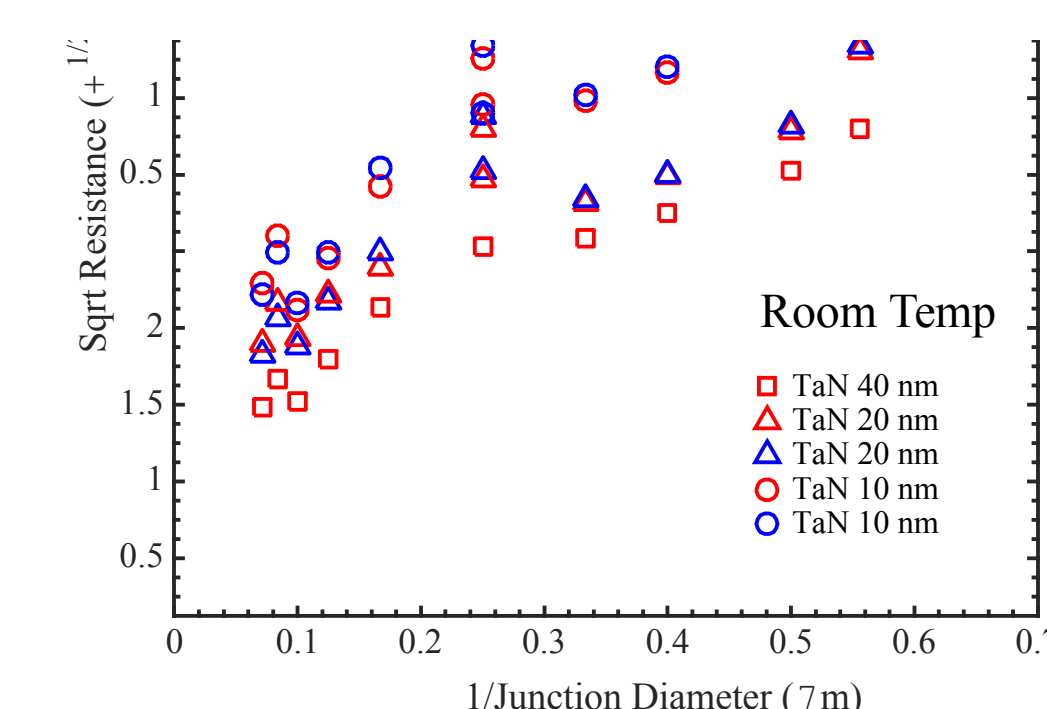
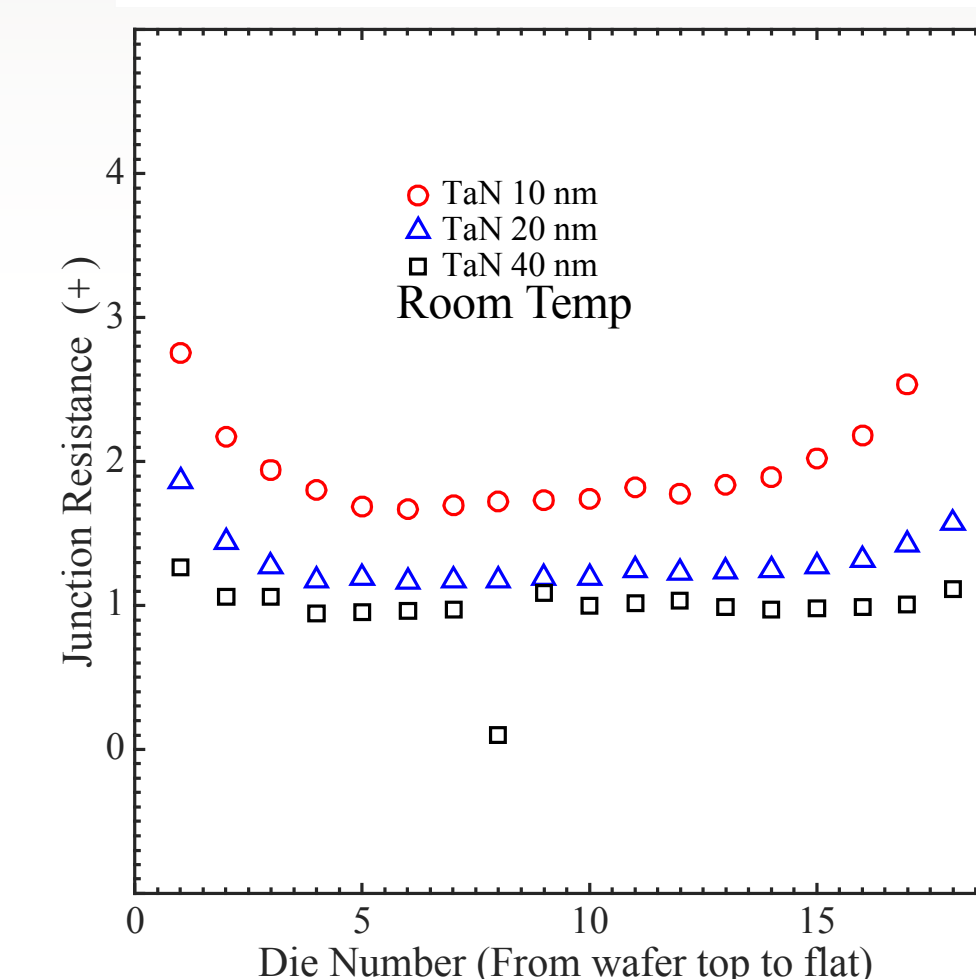
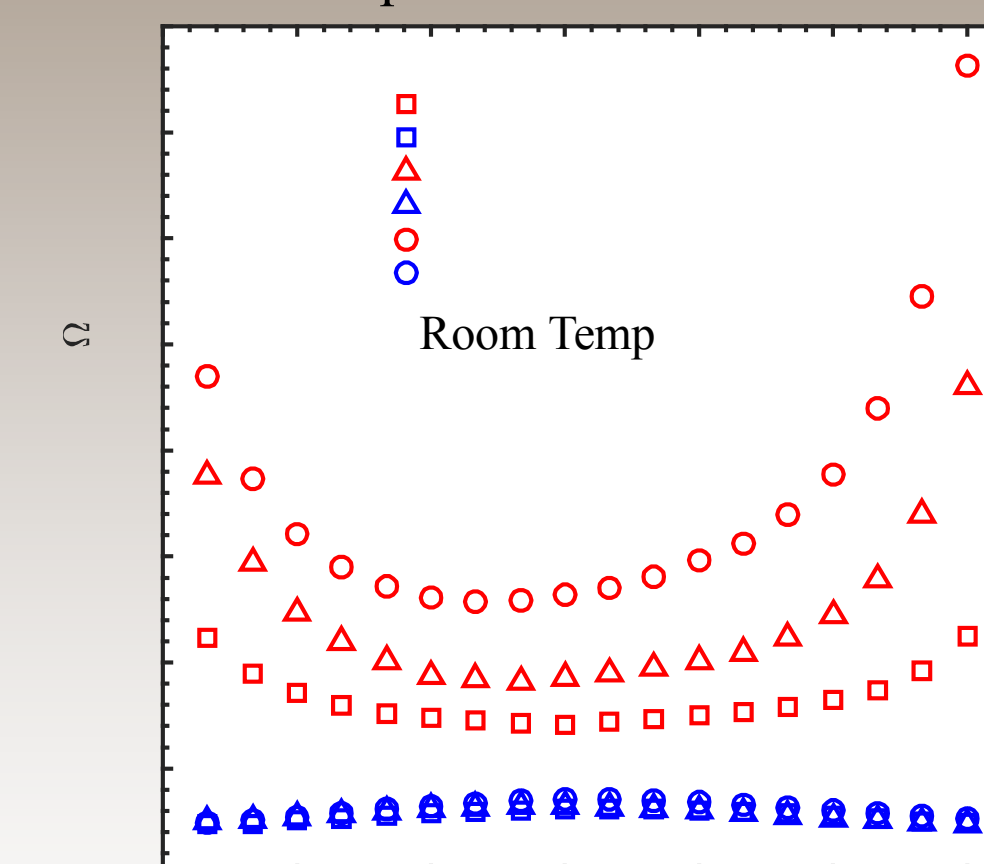
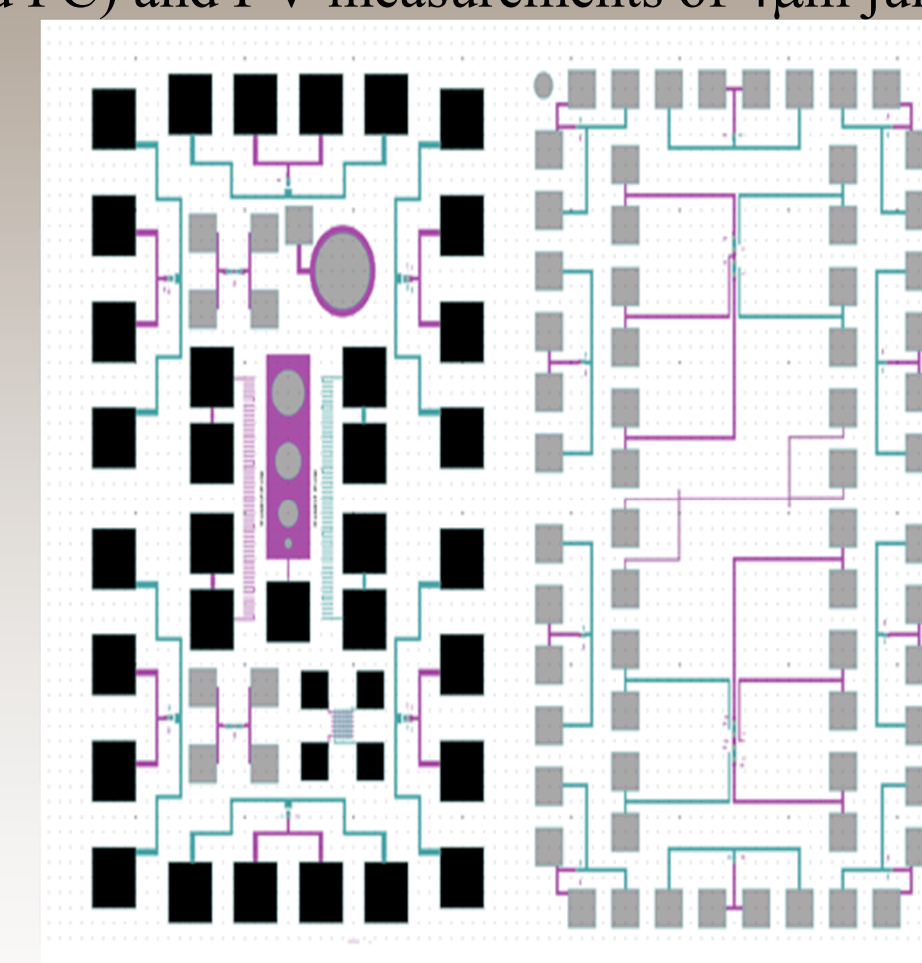
TaN_x Characterization

The TaN_x was reactively sputtered in the same system as the Nb. Calibration of the film was performed by adjustment of the N₂ and Ar partial pressure and deposition power. By sweeping the N₂, TaN_x can undergo RT resistivity change as well as RRR variations altering the film from superconducting to more insulating. The deposition parameters utilized for JJ devices was : Ar 15 sccm, N₂ 8 sccm, 250 W power at 3.9 mTorr.



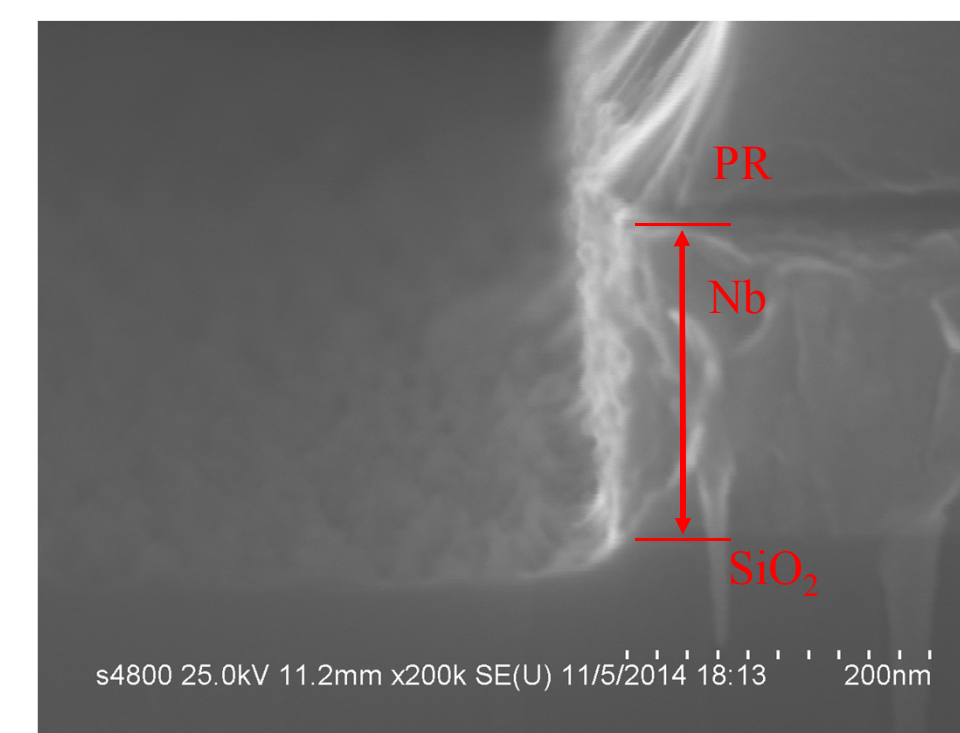
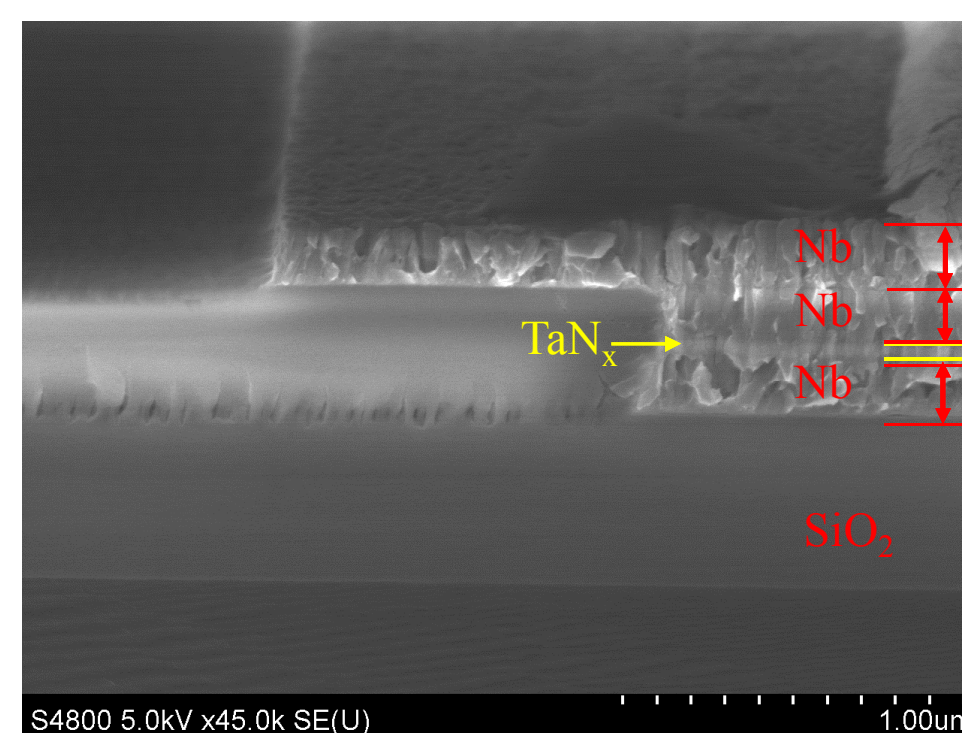
Wafer Layout and Performance

Junctions were fabricated from 0.5 μm to 14 μm diameters along with test structures such as serpentine resistors (1344 squares) and capacitive devices. All resistive measurements were made using a 4-probe Keithley sourcemeter. Dies were measured along the wafer center from wafer top to flat at room temperature. MPMS measurements on patterned die (ZFC and FC) and I-V measurements of 4 μm junctions in LHe were performed.



Plasma Etch and CMP

A fluorine based ICP RIE is used to etch the Nb and TaN_x films for metal 1, mesa and metal 2 patterned with Az 4110 photoresist. Etches were performed using a PlasmaTherm Versaline ICP RIE with the following conditions: SF₆/C₄F₈/Ar 50/90/5 sccm, pressure of 15 mTorr, and ICP/bias powers of 900/15 W.



References

- [1] S. K. Tolpygo, V. Bolkhovsky, T. J. Weir, C. J. Galbraith, L. M. Johnson, M. A. Gouker, *et al.*, "Inductance of Circuit Structures for MIT LL Superconductor Electronics Fabrication Process With 8 Niobium Layers," *Applied Superconductivity, IEEE Transactions on*, vol. 25, pp. 1-5, 2015.
- [2] S. K. Tolpygo, V. Bolkhovsky, T. J. Weir, L. M. Johnson, M. Gouker, and W. D. Oliver, "Fabrication Process and Properties of Fully-Planarized Deep-Submicron Nb/Al-Josephson Junctions for VLSI Circuits," *Applied Superconductivity, IEEE Transactions on*, vol. 25, pp. 1-12, 2015.
- [3] A. B. Kaul, S. R. Whiteley, T. Van Duzer, L. Yu, N. Newman, and J. M. Rowell, "Internally shunted sputtered NbN Josephson junctions with a TaN_x barrier for nonlatching logic applications," *Applied Physics Letters*, vol. 78, pp. 99-101, 2001.
- [4] M.D. Henry, S. Wolfley, T. Monson, B.G. Clark, E. Shaner, R. Jarecki, "Stress dependent oxidation of sputtered niobium and effects on superconductivity," *Journal of Applied Physics*, vol. 115, 2014.