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Wafer Level Fabrication of Planarized Josephson Junctions with TaN_x Barriers

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***Abstract*—A planarized Nb/TaN/Nb junction technology is presented for creating wafer scale planarized SNS shunted Josephson junctions. This work characterizes reactive magnetron sputtered layers with planarized PECVD deposited silicon dioxide. Junctions and films were electrically tested at room temperature and then again 4 K. Superconductors were tested using Meissner measurements.**

***Index Terms*— Josephson junction, superconducting, Wafer scale integration, niobium, tantalum nitride**

I. Introduction

Niobium and aluminum-based Josephson junctions are currently fabricated at the wafer level using CMOS fabrication techniques and statistical process control for uses such as quantum computation and superconducting computing electronics; MIT-LL and HYPRES [1-3]. However, the cornerstone Nb/Al-AlOx/Nb SIS Josephson junction technology relies on a thin aluminum oxide layer with electronic properties that are not only sensitive to the oxidation parameters, but all subsequent fabrication steps. This places firm limits on where the junctions can be placed in a fabrication process, restricts choices of wiring dielectrics, and prohibits having junctions in multiple layers. Further, Nb/Al-AlO_x/Nb junctions with moderate critical current densities, J_c < 20 kA/cm^2, require the addition of a shunt resistor, which adds complexity to both design and fabrication

Alternative junction technologies are being explored with barrier materials such as TaN_x [4, 5], HfN [6], and AlN [7] with the expectation that nitrides can provide a higher level of robustness and greater thermal stability than AlOx. Other promising technologies include siliciding with Nb to create a self-shunted junction [8]. But, niobium-silicide requires a dual target sputtering technology or precision target composition matched with chamber pressures.

In this work, we advance the research into TaN_x barriers [4] towards a 6 inch process. We demonstrate an early wafer level technology using niobium superconducting layers with a tantalum nitride barrier layer utilizing techniques inspired by Tolpygo et al. [1, 8, 9]. We incorporate a planarized SiO_2 wiring insulator and a second Nb wiring layer and demonstrate excellent planarity which allows this process to scale to multiple layers. Devices are characterized using room temperature resistance measurements on process control structures, metal serpentines, and on junctions. Cryogenic testing measured Meissner effect on films, film resistivity, and junction current—voltage (IV) characteristics.

II. Film Characterization

All films were sputter deposited at room temperature using a Denton Discovery 550 sputter tool on 150 mm, 2 – 20 Ω-cm resisitivity, (100) silicon wafers with ½ micron thick thermal silicon dioxide. Previous work demonstrated a niobium film deposited under stress can prevent bulk film oxidation and limit surface oxidation approximately 5-7 nm, as predicted by Halbritter, for a demonstrated period of 17 months at atmosphere [10-13]. The conditions for this deposition were 225 W, 22.5 sccm Ar with a chamber pressure of 4.8 mTorr. The film was measured using a Quantum Designs magnetic properties measurement system (MPMS) to have a bulk film Tc of 8.5 K.

To characterize the TaN_x barrier material, TaN_x was sputtered using a Ta target and a combination of Ar and N_2 gas. Deposition parameters were set to 250 W pulsed DC, chamber pressure ranged from 3.5 to 4.6 mTorr, Ar flow set to 15 sccm and N_2 flow varied from 4 to 16 sccm. Blanket test films were deposited approximately 100 nm thick and measured at room temperature using a VersaProbe VP10 4 probe resistivity measurement system. The films exhibit an exponential resistivity dependence with the partial pressure of N_2 as shown in Figure 1.

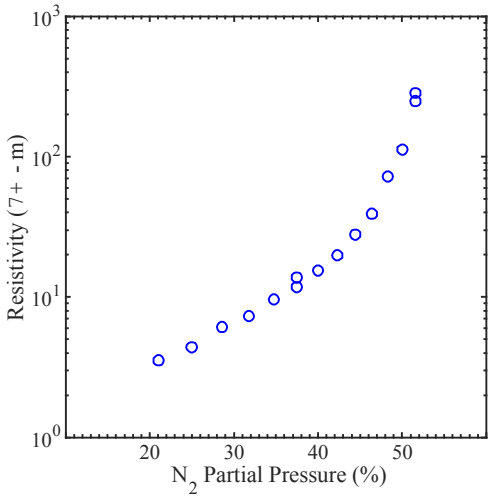

Figure 1. Four probe measurement of reactively sputtered TaN films as N_2 partial pressured was varied.

The same wafers were then cleaved and resistance versus temperature measurements made using a Keithley 2400 four probe measurement. Variation of the TaN_x stoichiometry

tunes the film properties from superconducting to insulating [16,17]. We find similar results on our films as shown in Figures 2 and 3. For N_2 flows of 4, 5, and 6 sccm, a MPMS Meissner measurement shows superconducting films with transition temperature, Tc of 6, 5, and 3.5 K respectively. For 8 sccm of N_2 and higher, we observe metallic behavior, and no superconducting transition above 2 K. For still higher N2 content the films were insulating.

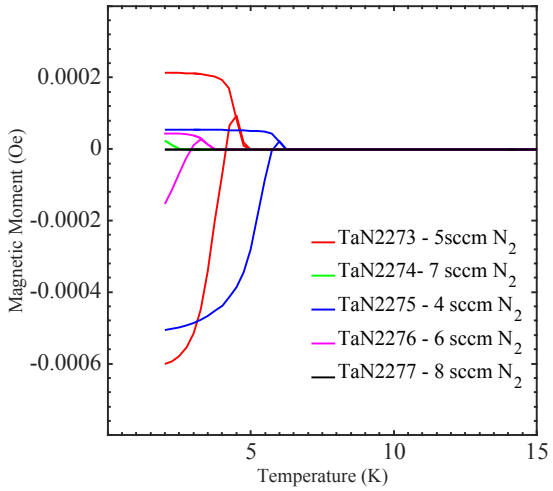

Figure 2. MPMS measurements of TaN_x films sputtered with different partial pressures of N_2. For Ar flows of 15 sccm and N_2 flow of 4-6 sccm a superconductive transition was observed above 2 K.

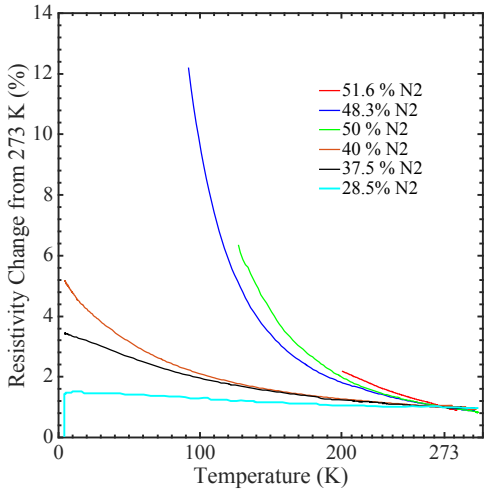

Figure 3. Four probe resistivity measurements showing the RRR of TaN_x films with different N_2 partial pressures ranging from 28.5% to 51.6%

III. Device Fabrication

Wafer level fabrication began with trilayer deposition on thermal grown silicon dioxide wafers on silicon. The full fabrication sequence is displayed in Figure 4. Niobium, tantalum nitride, niobium trilayers were deposited. The Nb films were all 200 nm thick and three different 10, 20 and 40 nm thick TaN_x films were sputtered with N_2 flow set to 8 sccm. The wafers were then patterened with Az 4110 resist and etched in a PlasmaTherm ICP RIE using fluorine etch chemistry. A micrograph of an etched Nb line is shown in figure 5. Etch parameters were set to 900 W ICP power, 15 W bias power, 15 mTorr of pressure, SF_6 50 sccm, C_4F_8 90 sccm, and Ar at 5 sccm. Previous work [14, 15] has shown this mixed mode Bosch etch to etch niobium and silicon while leaving a thin CF_x polymer on the sidewalls of the niobium. The first etch, defined the bottom layer Nb film, 'metal 1', and the etch landed on the silicon dioxide layer. The second etch, here termed 'mesa etch', defined the junction and stopped in the bottom Nb film of the trilayer.

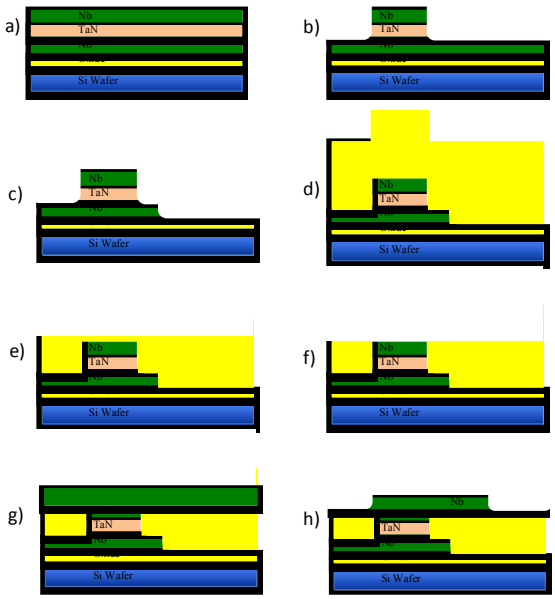

Figure 4. Wafer level fabrication sequence of the Josephson junctions. Step a) sputter deposition of the trilayer stack, b)etch course features and wiring layer 1, c) mesa etch to define junctions, d) PECVD oxide (SiO_2) deposition, e) CMP planarization of the wafer, f) Ar sputter etch to reveal tops of the junctions, g) Nb metal 2 deposition, h) Nb metal 2 pattern and etch.

After etch, 600 nm of SiO_2 was deposited using a Plasma-Therm Versaline plasma enhanced chemical vapor deposition at a platen temperature of 250 °C with N_2O and SiH_4 flow of 550 sccm and 300 sccm, respectively. A refractive index of 1.46 was measured at 633nm with a Woollam M2000 variable angle spectroscopic ellipsometer. This provided enough SiO_2 for chemical mechanical polishing (CMP) to flatten the oxide film out across the wafer. We note that to reduce dishing, the CMP did not expose any of the top junction electrode. To expose the top Nb, a third etch was performed with closely match etch rates for Nb and SiO_2 which exposed the top electrode of the junction while maintaining wafer planarity. This etch was performed in a PlasmaTherm capacitively coupled plasma reactive ion etcher (CCP - RIE) using 25 sccm Ar, 400 W of platen power, and 10 mTorr of pressure on a 25 C platen. clearing of the junction top electrodes was confirmed by resistivity measurements on test structures across the wafer.

Top layer wiring was created by sputtering 200 nm thick top niobium. This Nb was patterned and etched, as described earlier to create the metal 2 layer. Finally, Ti/Au contact pads were evaporated and patterned by lift-off. Figure 6 shows a cross section SEM of the final device.

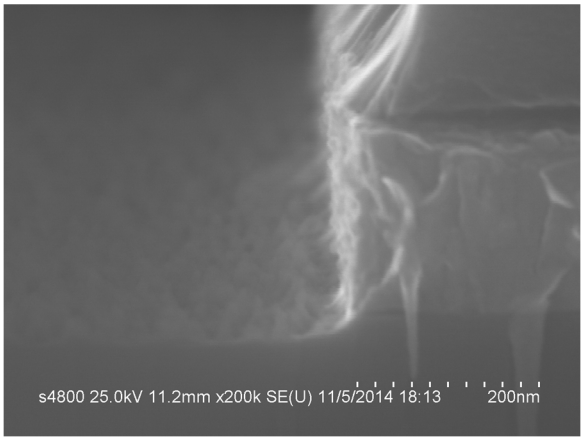

Figure 5. SEM micrograph cross section of etched Nb on SiO_2. Az 4110 photoresist and a 90 seconds SF_6, C_4F_8, Ar etch used.

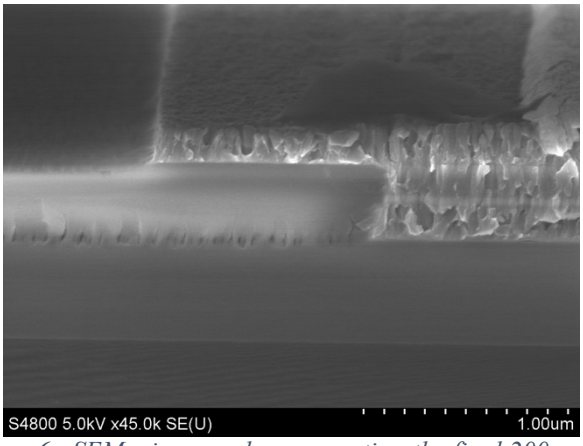

Figure 6. SEM micrograph cross section the final 200 nm Nb on a planarized Nb/TaN_x/Nb junction stack. A thin TaN_x layer is seen between the Nb layers.

IV. Electrical Measurements

The junction wiring was designed for four probe measurements which allow device resistances to be directly probed. The resistance of the 6 μm diameter junctions and serpentines test structures in metal 1 and metal 2 were probed using a Keithley 2400 sourcemeter, at room temperature. The serpentines resistances, measured across all three wafers, are shown in figure 9. Good uniformity in metal 2 is observed equating to an average resistivity of 246 nΩ-m. A larger variation between wafers is evident in the metal 1 ; this is attributed to a timed etch with a 5% plasma etch distribution yielding different metal 1 thicknesses and is expected. A thin fluorine etch resistant layer such as Al would greatly improve uniformity.

The resistance of the 6 μm Josephson junction measured at room temperature from top of the wafer to the flat is shown in figure 10. The 10 nm TaN_x barrier are the most resistive, followed by 20 nm, with the 40 nm TaN_x barriers offering the lowest resistance. Junctions at the wafers' edges slightly higher resistance than at the center. However, TaN_x films blanket deposited without Nb and measured using a profilometer confirm uniformity from center to edge is approximately 0.1% for 40 nm films and 1% for 20 nm films. This suggests the TaN_x stoichiometry varies with thickness and location on the wafer.

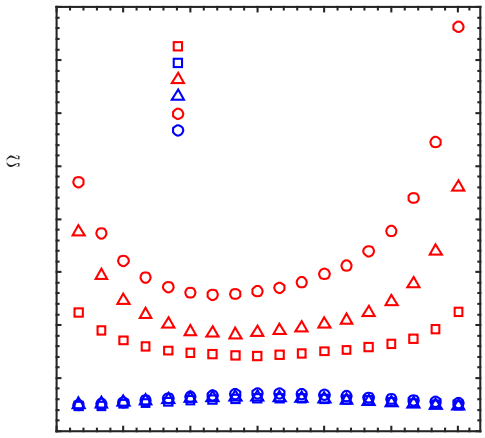

Figure 7 Room temperature resistance of serpentines in metal 1 and metal 2 using four probe on the 10, 20, and 40 nm TaN_x thicknesses.

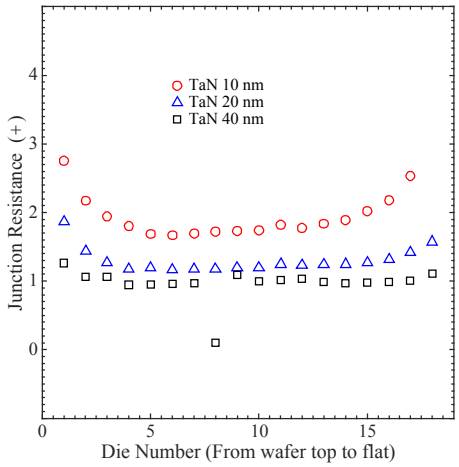

Figure 8 Room temperature resistance of the 6 μm junction using four probe measurements for the 10, 20 and 40 nm TaN_x barrier thicknesses.

Dies from each wafer were chosen the resistance of and all junctions measured, seen in figure 9 in the format of square root of resistance vs. inverse junction diameter. Although good repeatability between die is observed, some deviation from a straight line suggests electrical contribution from the perimeter of the junction.

Die from each wafer were measured in the MPMS down to T = 2 K. This measurement interrogates the superconductive properties of both Nb and the TaN_x films using the Meissner effect, shown in figure 10. In all samples Nb shows a robust superconducting $T_c \approx 8.4$ K. A TaN_x transition is also observed at 6 K for the 40 nm film, 4.5 K for

the 20 nm film, and a 3.5 K transition for the 10 nm film. This effect suggests that TaN_x in trilayer films deviates from that shown in bare films in Fig. 3; a result likely due to the oxidation of the bare TaN_x films. This Meissner measurement also suggests that the TaN_x films have varying stoichiometry with deposition thickness.

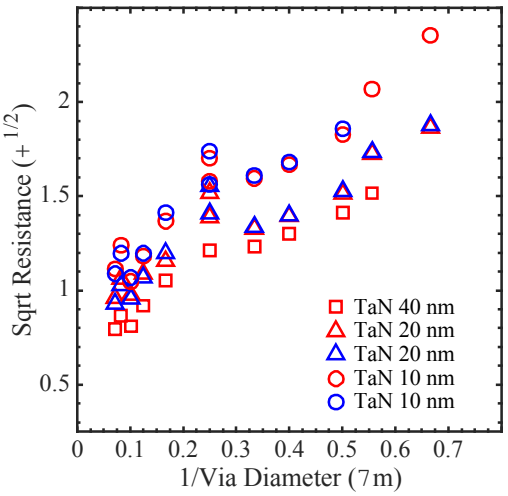

Figure 9. Room temperature resistance of all junctions taken from two adjacent die for the 10, 20 and 40 nm TaNx thickness.

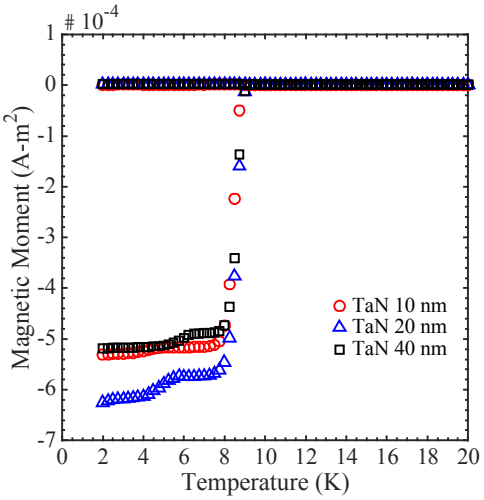

Figure 10. MPMS susceptibility (Meissner) measurements of pattened die for the three TaN wafers indicating a Nb transition and subsequent thickness dependent transition in TaNx.

Junctions were then wire bonded and submerged in liquid helium for 4 K I-V testing. Figure 11 shows four wire measurements of a 4 μm diameter junction performed by sweeping current while measuring voltage. Two peculiarities are evident. First, the critical current increases with the barrier thickness. Second, multiple switching events occur in the IV curves. The explanation of both phenomena is found by looking at the room temperature resistance data in Figs. 7, 8, and 9 which also show the lower resistivity of the thicker barrier[16, 17]. The Meissner effect data from figure 10 shows all three TaN_x barriers becoming superconducting close to 4 K. Put together, these data suggest that the TaN_x weak links in these devices are switching from superconducting to normal conduction and that the hysteresis we observe in some of these devices, which is not shown in figure 11, is related to resistive heating of the TaN_x barriers. It is interesting to observe that the thinnest TaN_x barrier behaves most like an SNS junction although while the thicker barriers display more hysteresis and are certainly superconducting. The solution to these difficulties will require more resistive TaNx and a better understanding of the Nb/TaN_x interface.

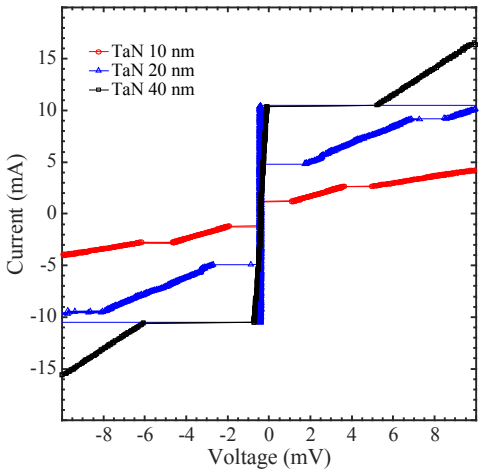

Figure 11. Conductivity of the 4 μm JJ at 4 K for the 10, 20 and 40 nm TaN barrier thicknesses.

V. Conclusions

This work has presented a sputtered TaN_x Josephson junction barrier technology in two metal depositions using Nb electrodes and wiring for wafer scale fabrication. TaN_x films can be tuned during deposition to exhibit superconducting or insulating properties at 4 K. A key development of this work is a planarization technique based on CMP of the SiO_2 layers which will enable stacking multiple junction layers.

Electrical and Meissner measurements were made on the films and junctions at room and cryogenic temperatures to quantify uniformity and device performance. These devices show increasing I_c with barrier thickness and Meissner results on trilayers suggest that part or all of the TaN_x barrier becomes superconducting near 4 K with the critical temperature dependent on barrier thickness.

Acknowledgment

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References

[1] S. K. Tolpygo, V. Bolkhovsky, T. J. Weir, L. M. Johnson, M. Gouker, and W. D. Oliver, "Fabrication Process and Properties of Fully-Planarized Deep-Submicron Nb/Al–Josephson Junctions for

VLSI Circuits," *Applied Superconductivity, IEEE Transactions on,* vol. 25, no. 3, pp. 1-12, 2015.

[2] P. Febvre, N. De Leo, M. Fretto, A. Sosso, M. Belogolovskii, R. Collot, and V. Lacquaniti, "Overdamped Josephson junctions for digital applications," *Physica C: Superconductivity,* vol. 484, pp. 175-178, 1/15/, 2013.

[3] D. S. Holmes, A. L. Ripple, and M. A. Manheimer, "Energy-efficient superconducting computing—power budgets and requirements," *IEEE Transactions on Applied Superconductivity,* vol. 23, no. 3, pp. 1701610-1701610, 2013.

[4] A. B. Kaul, S. R. Whiteley, T. Van Duzer, L. Yu, N. Newman, and J. M. Rowell, "Internally shunted sputtered NbN Josephson junctions with a TaNx barrier for nonlatching logic applications," *Applied Physics Letters,* vol. 78, no. 1, pp. 99-101, 2001.

[5] S. Chaudhuri, and I. J. Maasilta, "Superconducting tantalum nitride-based normal metal-insulator-superconductor tunnel junctions," *Applied Physics Letters,* vol. 104, no. 12, pp. 122601, 2014.

[6] S. i. Morohashi, T. Imamura, and S. Hasuo, "Nb Josephson junction with a Hf/HfN double overlayer," *Journal of Applied Physics,* vol. 72, no. 7, pp. 2969-2972, 1992.

[7] H. Akaik, T. Funai, N. Naito, and A. Fujimaki, "Characterization of NbN tunnel juctions with radical nitrided aln barriers," *Ieee Transactions on Applied Superconductivity,* vol. 23, no. 3, 2013.

[8] S. K. Tolpygo, V. Bolkhovsky, T. Weir, L. M. Johnson, W. D. Oliver, and M. A. Gouker, "Deep sub-micron stud-via technology of superconductor VLSI circuits," *Superconductor Science and Technology,* vol. 27, no. 2, pp. 025016, 2014.

[9] S. K. Tolpygo, and D. Amparo, "Fabrication process development for superconducting VLSI circuits: minimizing plasma charging damage," *Journal of Physics: Conference Series,* vol. 97, pp. 012227, 2008.

[10] M. D. Henry, S. Wolfley, T. Monson, B. G. Clark, E. Shaner, and R. Jarecki, "Stress dependent oxidation of sputtered niobium and effects on superconductivity," *Journal of Applied Physics,* vol. 115, no. 8, pp. 083903, 2014.

[11] J. Halbritter, "On the oxidation and on the superconductivity of niobium," *Applied Physics A*, no. 43, pp. 48, 1987.

[12] J. Halbritter, "Transport in superconducting niobium films for radio frequency applications," *Journal of Applied Physics,* vol. 97, no. 8, pp. 083904, 2005.

[13] R. Ghez, "On the Mott-Cabrera oxidation rate equation and the inverse-logarithmic law," *The Journal of Chemical Physics,* vol. 58, no. 5, pp. 1838, 1973.

[14] M. D. Henry, and R. L. Jarecki, *Superconductive silicon nanowires using gallium beam lithography*, Sandia National Laboratories (SNL-NM), Albuquerque, NM (United States), 2014.

[15] M. D. Henry, "ICP etching of silicon for micro and nanoscale devices," California Institute of Technology, 2010.

[16] T. Van Duzer, and C. W. Turner, *Principles of superconductive devices and circuits*, 2nd ed., Upper Saddle River, NJ Prentice Hall, Inc, 1999.

[17] L. Yu, R. Gandikota, R. K. Singh, L. Gu, D. J. Smith, X. Meng, X. Zeng, T. Van Duzer, J. M. Rowell, and N. Newman, "Internally shunted Josephson junctions with barriers tuned near the metal–insulator transition for RSFQ logic applications," *Superconductor Science and Technology,* vol. 19, no. 8, pp. 719, 2006.