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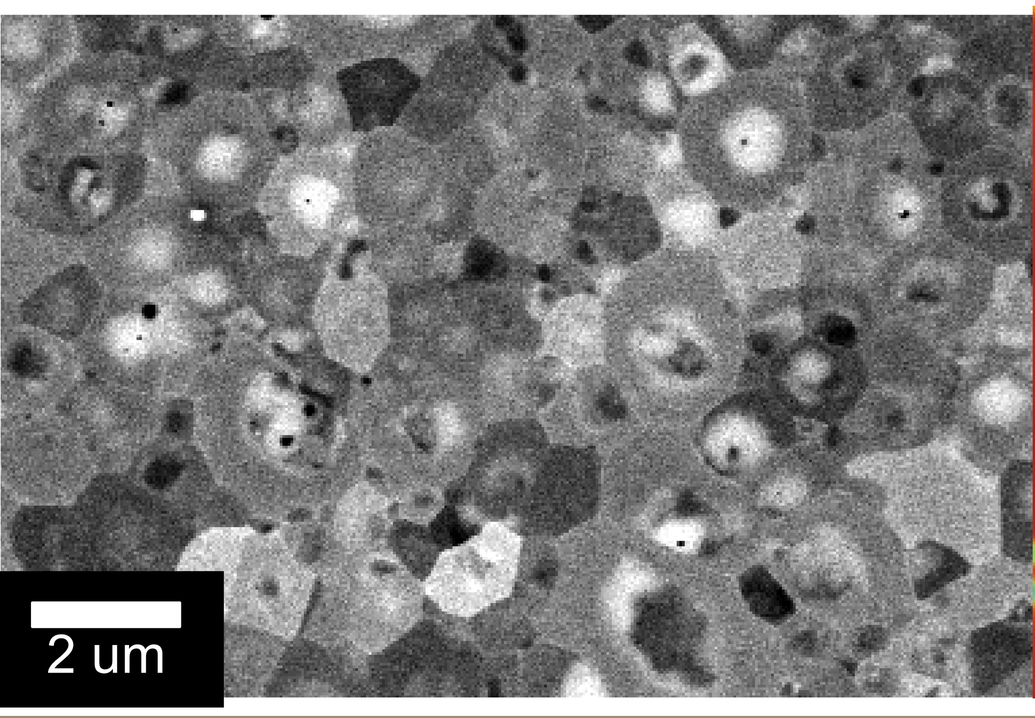
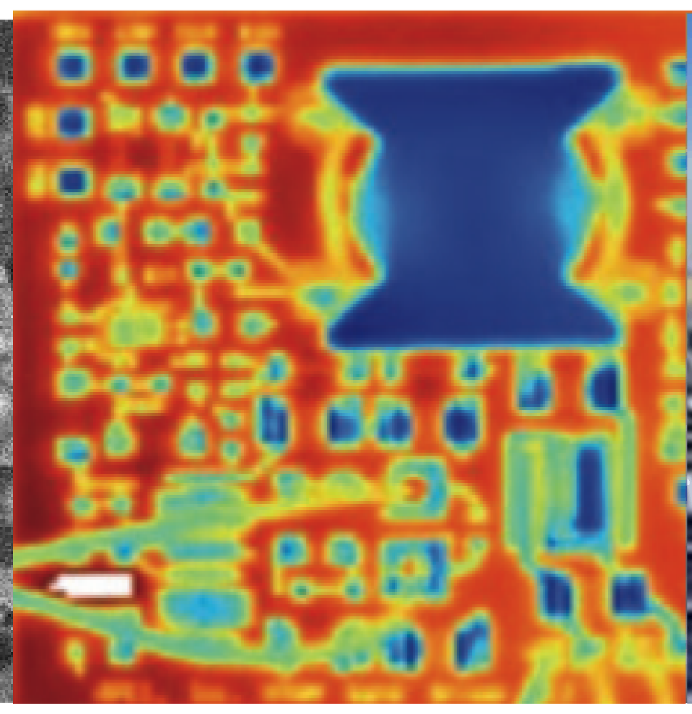
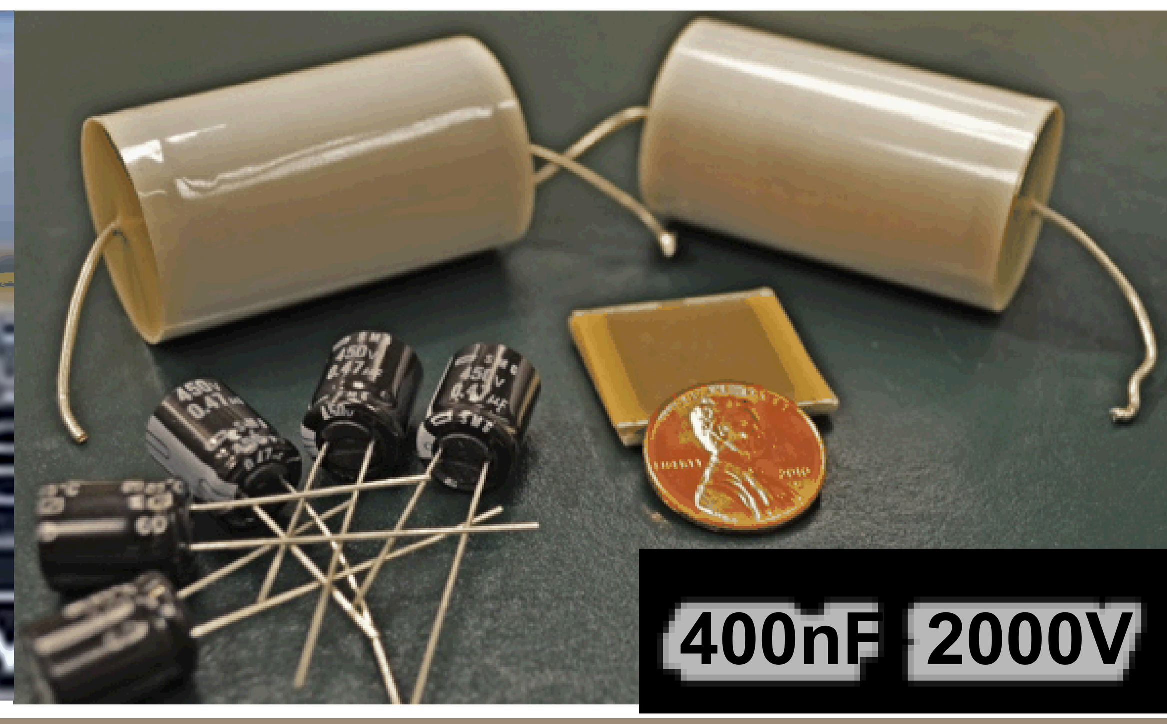






Novel High Energy Density Dielectrics for Scalable Capacitors

Harlan Brown-Shaklee (SNL)

Sandia National Laboratories, Albuquerque, NM

Motivation

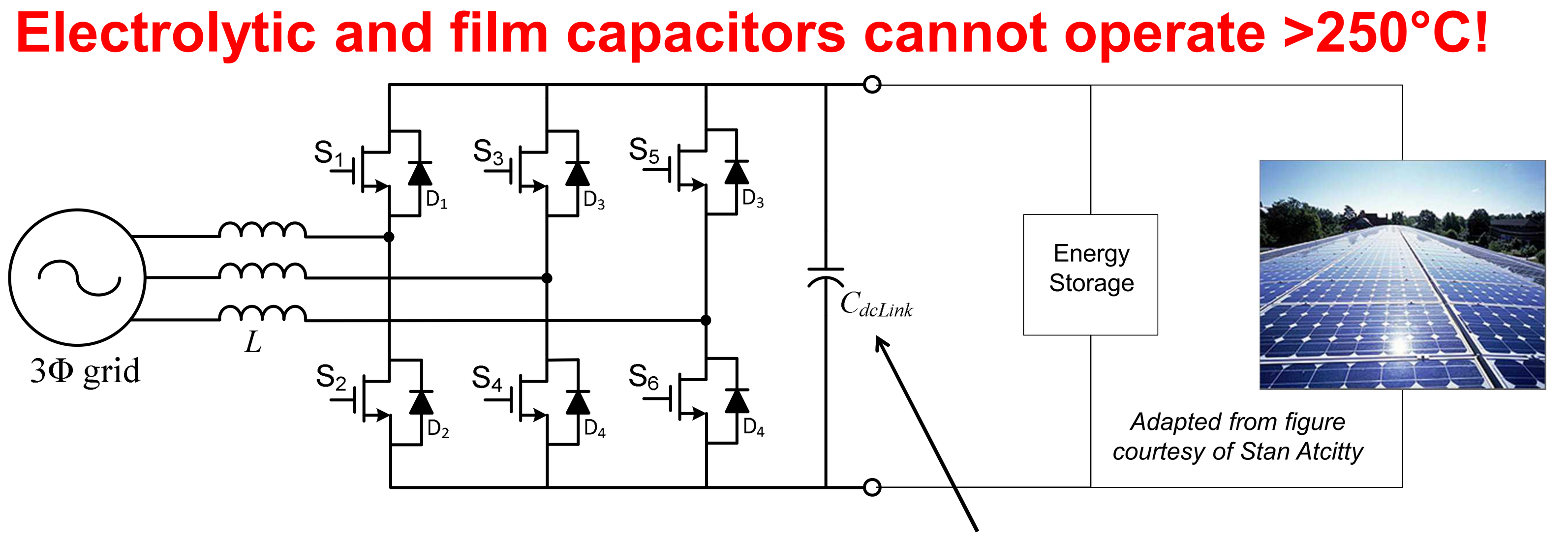
Developments in high temperature wide bandgap (WBG) switching technology has placed higher demands on passive electronic components like capacitors, resistors, and packaging

-Silicon switches operate at 6-12kHz with a maximum operating temperature of ~200°C

-WBG (SiC and GaN) switches operate >100kHz and >250°C

-Higher operating temperatures and voltages reduce the lifetime of capacitors.

Electrolytic and film capacitors cannot operate >250°C!



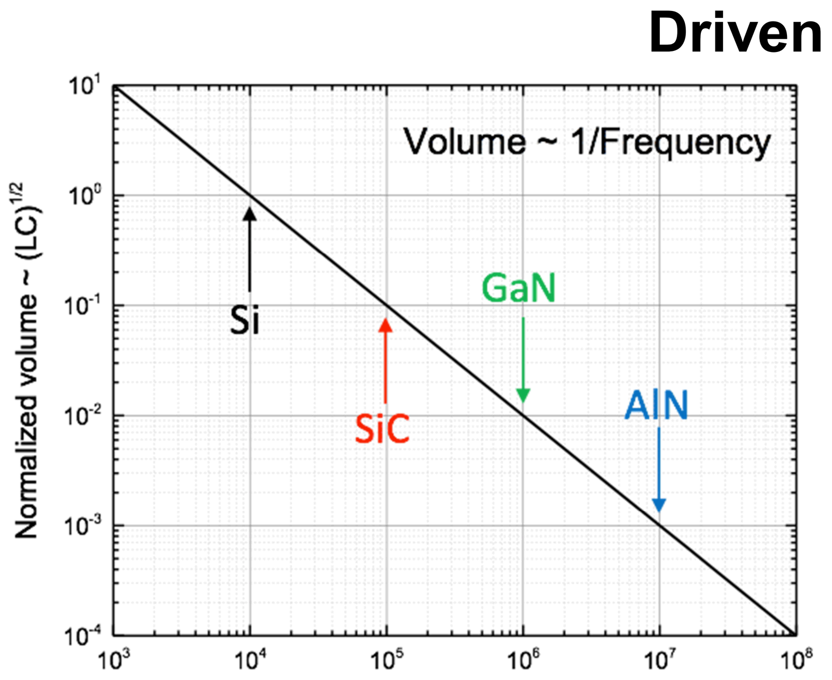
DC Link

High frequency switching reduces the required bus capacitance but requires high temperature stable devices

$$f_{Switch} \propto \frac{1}{2\pi\sqrt{LC}}$$

Notional Design	Si Switched Module	SIC Switched Module	WBG Switched Module
Frequency (MHz)	**0.012**	0.100	**10**
Bus Voltage (Volts)	1000	1000	1000+
Power (kW)	>100	>100	>100
Bus Capacitance (μF)	**1000-4000**	40-50	**<10**
Inductance (nH)	40-180	20-40	<5
Bus Capacitor Volume	**High**	Moderate	**Low**
Operating Temperature	**<150°C**	<150°C	**>200°C**
Capacitor Family	Electrolytic	Polymer Film	**Ceramic**

Cost Driven → **Performance Driven**



Passive component and packaging stability at high temperatures will limit the full potential of fast switching WBG topologies

Capacitor Families

1) Electrolytic-Low \$/Farad, Low Voltage **T_{max}<150°C**

2) Polymer-Medium \$/Farad, High Voltage, **T_{max}<150°C**

3) Ceramic-High \$/Farad, **T_{max}>200°C**

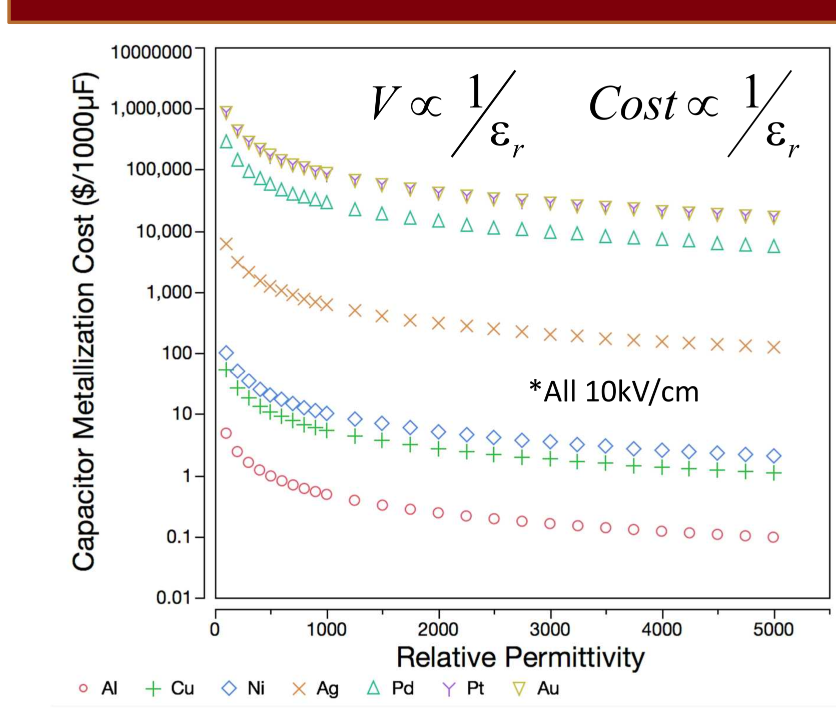
Performance and Cost

High temperature capacitor reliability is a function of chemistry, temperature, processing and electric field

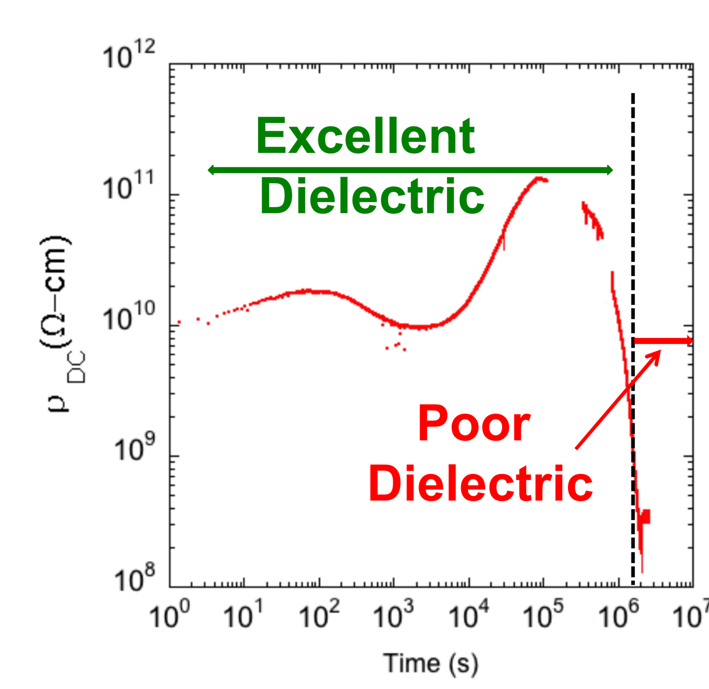
-Capacitor de-rating must account for lifetime at a predicted stress level

Dielectric *Chemistry* Governs Lifetime and Cost

Cost of DC link is dominated by metallization spot price and dielectric permittivity



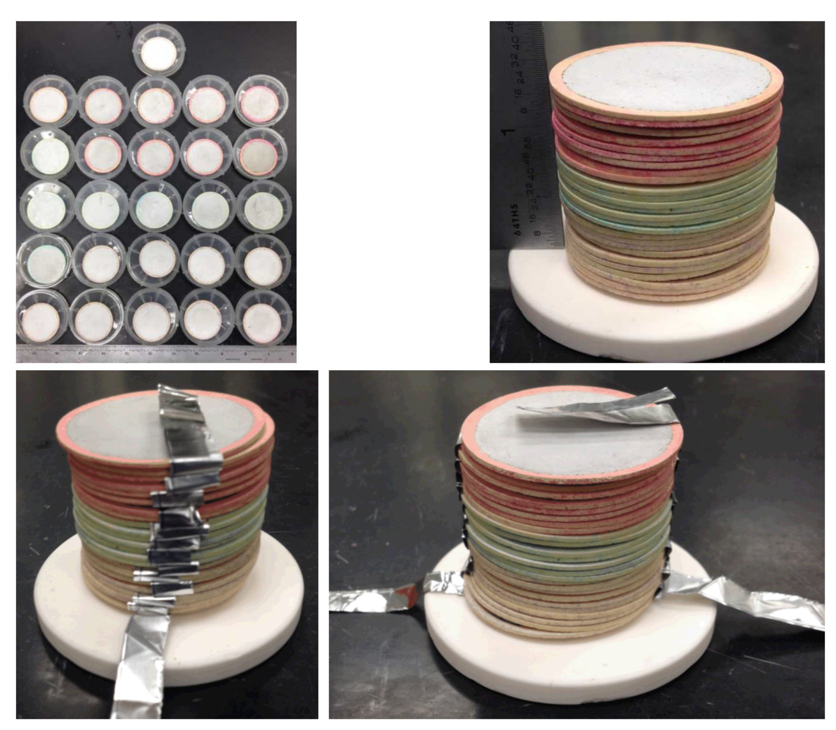
Dielectric stress in disc capacitor held at constant 1000V at 250°C



High frequency, high temperature, and high voltage inverters favors thick dielectric layers that do not require precious metal cofire

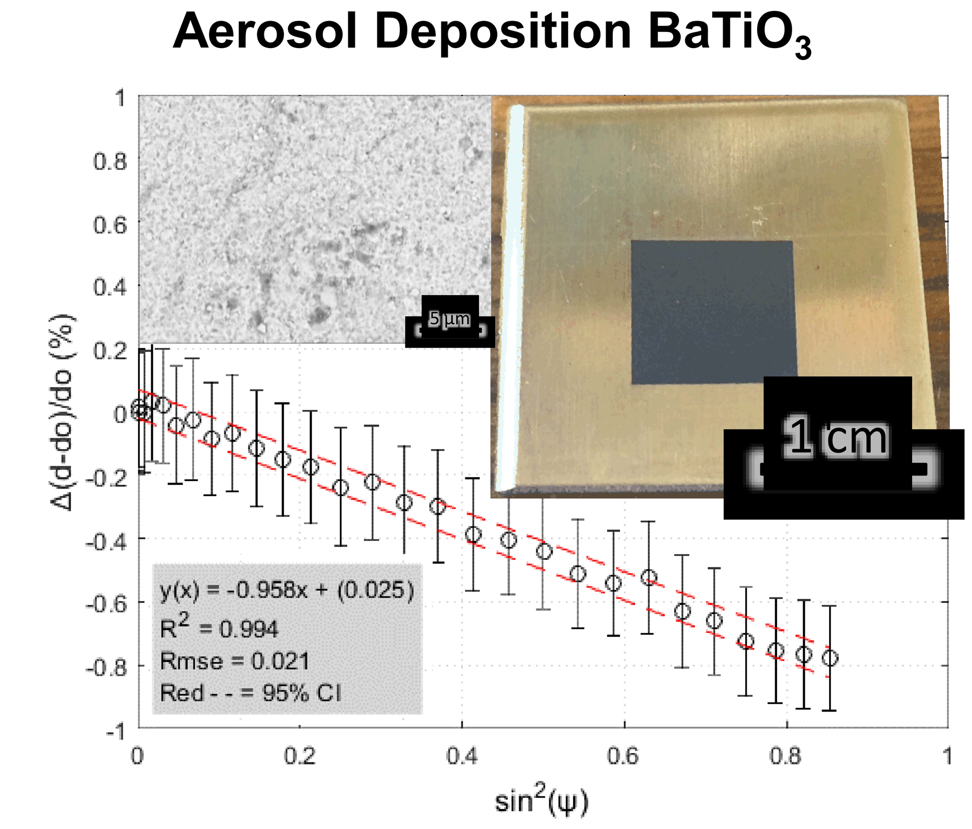
Scalable Capacitor Fabrication Techniques

DC Link Capacitor Prototype



~400nF Capacitor built *without* precious metal cofire

Aerosol Deposition $BaTiO_3$



Room temperature deposition of stressed $BaTiO_3$ dielectric

Future Work

- *Demonstrate ceramic capacitor prototypes in DC link test bed*
- *Evaluate long term performance of these high temperature dielectrics*

U.S. DEPARTMENT OF ENERGY NNSA National Nuclear Security Administration

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