Phasor-Domain Steady-State Modeling and Design of the DC-DC Modular Multilevel Converter

Heng Yang, *Student Member, IEEE*, Jiangchao Qin, *Member, IEEE*,
Suman Debnath, *Member, IEEE*, and Maryam Saeedifard, *Senior Member, IEEE*

***Abstract*—The DC-DC Modular Multilevel Converter (MMC), which originated from the AC-DC MMC, is an attractive converter topology for interconnection of medium-/high-voltage DC grids. This paper presents design considerations for the DC-DC MMC to achieve high efficiency and reduced component sizes. A steady-state mathematical model of the DC-DC MMC in the phasor-domain is developed. Based on the developed model, a design approach is proposed to size the components and to select the operating frequency of the converter to satisfy a set of design constraints while achieving high efficiency. The design approach includes sizing of the arm inductor, Sub-Module (SM) capacitor, and phase filtering inductor along with the selection of AC operating frequency of the converter. The accuracy of the developed model and the effectiveness of the design approach are validated based on the simulation studies in the PSCAD/EMTDC software environment. The analysis and developments of this paper can be used as a guideline for design of the DC-DC MMC.**

I. Introduction

THE DC-AC Modular Multilevel Converter (MMC) has become the most attractive converter topology for high voltage applications because of its salient features, i.e., high efficiency, scalability/modularity, and superior harmonic performance [1]. Over the past few years, extensive research effort has been made to address the technical challenges associated with the operation and control of the MMC and to improve its performance for various applications [2,1,3]. Those applications mainly include High-Voltage DC (HVDC) transmission systems [4,5,6], variable speed drives [7,8,9,10], and flexible AC transmission systems [11].

The salient features of the DC-AC MMC have enabled the emergence of the single-stage DC-DC MMC, which can potentially replace the conventional back-to-back DC-AC-DC converter configurations [12,13] for medium/high power DC-DC conversion systems, e.g., interconnection of medium-/high-voltage DC grids [14,15,16,17]. Similar to the DC-AC MMC, the circuit topology of the DC-DC MMC, which hereafter is referred to as the DC MMC, is derived based upon stacking up a number of identical Sub-Modules (SMs). However, operation and control of the DC MMC are significantly different from the DC-AC MMC [18]. In the DC MMC, the DC power flow is determined by external parameters, i.e., the DC-link voltages and output power. To keep the energy balanced among all SM capacitors, the amount and direction of the AC active power flow is controlled by injecting an AC circulating current component within each phase-leg of the converter to compensate for the DC power. Thus the AC circulating current is a necessity to guarantee proper operation of the converter. However, from the efficiency and device current rating perspectives, circulating current must be minimized. Since both frequency and amplitude of the circulating current in the DC MMC can be chosen arbitrarily, their values affect the converter efficiency and the size of passive components. Although a higher AC circulating current frequency, which is referred to as the operating frequency, reduces the size of passive components, it increases the power losses of the converter. Furthermore, the DC MMC topology inherently requires a large phase filtering inductor to remove the AC component presented in the phase current [19]. However, an over-sized inductor will add to the system cost and size/volume. Although the basics of operation and control of the DC MMC have been investigated in [20,19,21,22], its optimal design has not been explored. Since the basics of operation of the DC MMC are significantly different from the DC-AC MMC, the developed passive component sizing methods for the DC-AC MMC in [23,24,25] are not applicable to the DC MMC.

This paper presents the design considerations for the DC-DC MMC to achieve high efficiency while satisfying the design constraints. A phasor-domain steady-state model of the DC MMC is developed and used to determine the AC and DC components of the arm current, and phase current. In addition, the dynamics of SM capacitor voltage ripple is derived. Subsequently, a systematic approach is developed such that based on certain given design constraints, the size of passive components as well as the operating frequency of the converter can be determined. Accuracy of the developed model and the design approach is validated based on simulation studies in the PSCAD/EMTDC software environment.

II. The DC MMC

The circuit diagram of an M-phase-leg DC MMC is shown in Fig. 1 in which the DC-link 2 voltage v_{dc2} is greater than the DC-link 1 voltage v_{dc1}. The DC MMC consists of M nominally identical phase-legs and two arms per phase-leg, i.e., an upper arm (represented by superscript "p") and a lower arm (represented by superscript "n"). Each arm consists of series connection of N nominally identical half-bridge SMs and an

H. Yang, J. Qin and M. Saeedifard are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA (e-mails: hyang302@gatech.edu; qinj@ieee.org; maryam@ece.gatech.edu).

S. Debnath is with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907-2035 USA (email: sdebnat@purdue.edu)

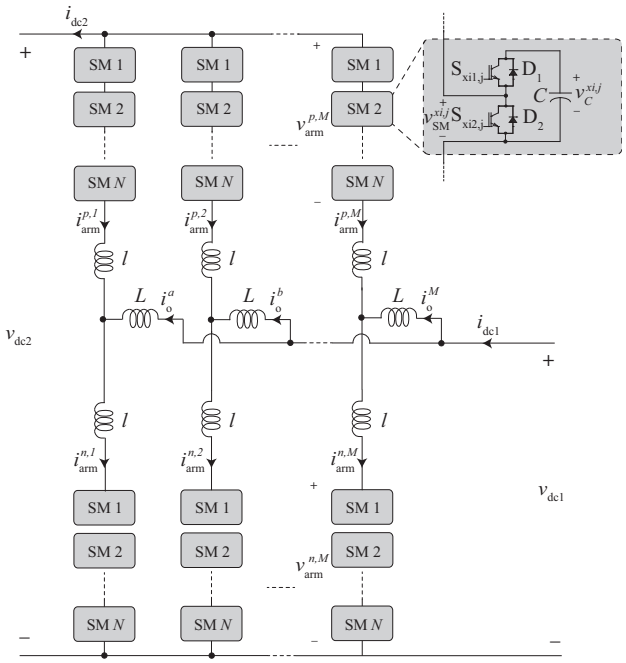

Fig. 1. Circuit diagram of an M-phase-leg DC MMC.

arm inductor l. The output terminal/mid-point of each phase-leg is connected to the converter DC-link 1 terminal via the phase filtering inductor L. By symmetrical connection of two unipolar DC MMCs, the unipolar configuration of Fig. 1 can be expanded to a bipolar one [19]. The analysis and developments in this paper are based upon the unipolar configuration and are equally valid for the bipolar case as well.

For high-power applications, multiple phase-legs are required to increase the power rating of the converter. For the case of $M = 1$, a series LC filter is inserted to establish a path for the AC circulating current [20]. For the case of $M > 1$, the phase-legs operate in an interleaved manner, i.e., the gating signals among phase-legs are identical with a phase shift of $2\pi/M$.

Each SM of the DC MMC of Fig. 1 can provide two voltage levels at its terminal, i.e., zero or $v_C^{xi,j}$, $x \in \{p, n\}$; $i \in \{1, 2, ..., N\}$; $j \in \{1, 2, ..., M\}$, depending on the state of its complementary switches $S_{xi1,j}$ and $S_{xi2,j}$. Ideally, the average value of each SM capacitor voltage is maintained at v_{dc2}/N. The two switching states of SM-i in arm-x of phase-j are:

- $S_{xi1,j} = 1$ and $S_{xi2,j} = 0$: ON-state or inserted,
- $S_{xi1,j} = 0$ and $S_{xi2,j} = 1$: OFF-state or bypassed.

The voltage of each arm of the DC MMC, i.e., $v^{x,j}_{arm}$, $x \in \{p, n\}$; $j \in \{1, 2, ..., M\}$, is controlled by the number of inserted SMs. During normal operation, the voltage of each arm consists of a DC as well as an AC component. The lower arm DC voltage component is determined by v_{dc1}, while the upper arm DC voltage component is determined by the ratio of v_{dc1}/v_{dc2}. The AC voltage component, on the other hand, is controlled to drive an AC circulating current component within each phase-leg, exchanging active AC power between the upper and lower arms of the corresponding phase-leg. Ideally, the amplitudes of the AC component of the arm voltages/currents and phase currents among phase-legs are identical. The phase angles of the AC component of arm voltages/currents and phase currents among M phase-legs are displaced by $2\pi/M$. The nominal DC power can flow bidirectionally between the input and output terminals. To guarantee the power balance between the upper and lower arms of each phase-leg such that the divergence of the SM capacitor voltages between upper and lower arms are minimized, an AC active power must be exchanged between the upper and lower arms of each phase-leg.

A. Steady-State Model

To develop a mathematical model of the DC MMC, the following assumptions are made:

1) The number of SMs per arm is assumed to be considerably large. Based on this assumption, the arm voltages can be represented by ideal voltages sources;
2) The converter components are ideal and lossless, i.e., input power equals the output power;
3) A proper capacitor voltage balancing strategy based on the sorting algorithm is adopted to maintain the SM capacitor voltages balanced within each arm.

In deriving the steady-state model of the converter, for the sake of simplicity, only one phase-leg is considered. Nevertheless, the mathematical model of one phase-leg can be extended to the case of an M-phase-leg DC MMC. Fig. 2 shows the corresponding equivalent circuit of a single phase-leg of the DC MMC, where $v^x_{arm,dc}$ and $\tilde{v}^x_{arm,ac}$ represent the DC and AC components of the arm voltage, respectively, $i^x_{arm,dc}$ and $\tilde{i}^x_{arm,ac}$ represent the DC and AC components of the arm current, respectively, $i_{o,dc}$ represents the DC component of the phase current, and $\tilde{i}_{o,ac}$ represents the AC component of the phase current, which should be ideally equal to zero. The cascaded SMs within each arm are represented by ideal controllable voltage sources. Since the converter consists of M identical phase-legs, the rated DC power is equally shared among the phase-legs.

Based on the superposition principle, the converter phase-leg equivalent circuit can be decomposed into DC and AC sub-circuits. To derive the DC equations, a DC equivalent circuit of a single phase-leg is obtained and shown in Fig. 3. The DC equivalent circuit is obtained by disabling AC voltage sources shown in Fig. 2 such that inductors are represented as short circuit. Based on the assumption of a lossless conversion, the upper and lower arm voltage and current DC components can be represented by:

$$v^p_{arm,dc} = v_{dc2} - v_{dc1}, \tag{1}$$

$$v^n_{arm,dc} = v_{dc1}, \tag{2}$$

$$i^p_{arm,dc} = -\frac{i_{dc2}}{M}, \tag{3}$$

$$i^n_{arm,dc} = \frac{i_{dc2}}{M}\left(\frac{v_{dc2}}{v_{dc1}} - 1\right). \tag{4}$$

The upper and lower arm DC power can be represented by:

$$P^p_{arm,dc} = \left(\frac{v_{dc1}}{v_{dc2}} - 1\right)\frac{P}{M}, \tag{5}$$

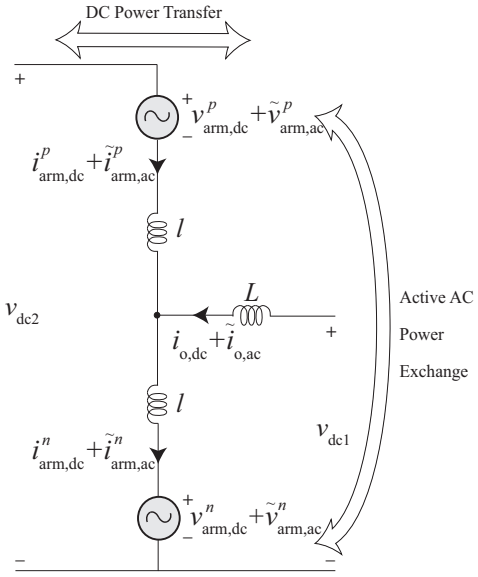

Fig. 2. Equivalent circuit of one phase-leg of the DC MMC.

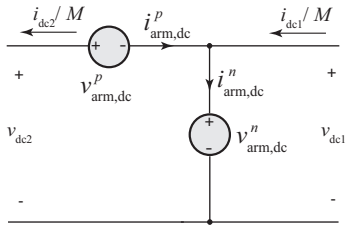

Fig. 3. DC equivalent circuit of one phase-leg of the DC MMC.

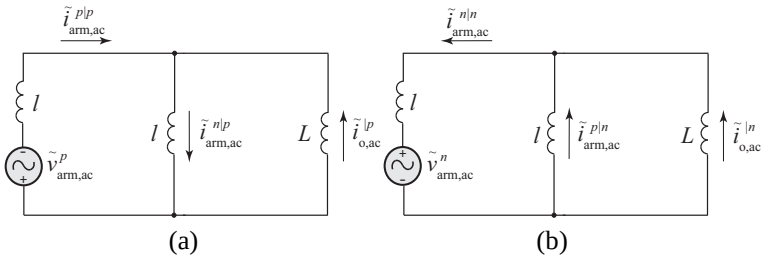

Fig. 4. AC equivalent circuit of: (a) the upper arm and (b) the lower arm.

$$P^{n}_{\text{arm,dc}} = (1 - \frac{v_{\text{dc1}}}{v_{\text{dc2}}})\frac{P}{M}, \tag{6}$$

where P is the converter output power, which is considered positive when power flows from the DC-link 1 to DC-link 2.

Based on the superposition principle, two AC equivalent circuits are derived by disabling the DC voltage sources shown in Fig. 2. Since neither of the DC-link 1 and DC-link 2 terminals of the converter carries any AC component under normal operation, for the AC analysis, they can be represented as short circuits.The AC equivalent circuit of the upper arm shown in Fig. 4(a) is obtained by enabling only the upper arm AC voltage source and the AC equivalent circuit of the lower arm shown in Fig. 4(b) is obtained by enabling only the lower arm AC voltage source. In this way, the AC component of the arm currents and the phase current produced by the AC voltages of the upper and lower arms are analyzed separately. In Fig. 4, $\tilde{i}^{p|p}_{\text{arm,ac}}$ and $\tilde{i}^{p|n}_{\text{arm,ac}}$ represent the AC component of the upper arm current produced by the AC voltages of the upper and lower arms, respectively, $\tilde{i}^{n|p}_{\text{arm,ac}}$ and $\tilde{i}^{n|n}_{\text{arm,ac}}$ represent the AC component of the lower arm current produced by the AC voltages of the upper and lower arms, respectively, and $\tilde{i}^{|p}_{\text{o,ac}}$ and $\tilde{i}^{|n}_{\text{p,ac}}$ represent the AC component of the phase current produced by the AC voltages of the upper and lower arms, respectively. Based on the equivalent circuits of Figs. 4(a) and (b), the following equations are derived for the arm current and phase current AC components by combining the results from the analysis of Fig. 4(a) and (b):

$$\tilde{i}^{p}_{\text{arm,ac}} = -\frac{\tilde{v}^{p}_{\text{arm,ac}} + \frac{X_L}{X_l+X_L}\tilde{v}^{n}_{\text{arm,ac}}}{j(X_l + \frac{X_l X_L}{X_l+X_L})}, \tag{7}$$

$$\tilde{i}^{n}_{\text{arm,ac}} = -\frac{\tilde{v}^{n}_{\text{arm,ac}} + \frac{X_L}{X_l+X_L}\tilde{v}^{p}_{\text{arm,ac}}}{j(X_l + \frac{X_l X_L}{X_l+X_L})}, \tag{8}$$

$$\tilde{i}_{o,\text{ac}} = (\frac{X_l}{X_L + X_l})\frac{\tilde{v}^{p}_{\text{arm,ac}} - \tilde{v}^{n}_{\text{arm,ac}}}{j(X_l + \frac{X_l X_L}{X_l+X_L})}, \tag{9}$$

where X_l is the arm inductive reactance, X_L is the phase inductive reactance.

The arm AC active power can be calculated by:

$$P^{x}_{\text{arm,ac}} = \text{Re}(\tilde{v}^{x}_{\text{arm,ac}}\tilde{i}^{*x}_{\text{arm,ac}}), \tag{10}$$

where $\tilde{i}^{*x}_{\text{arm,ac}}$ represents the complex conjugate of the upper and lower arm current AC components. By substituting $\tilde{i}^{p}_{\text{arm,ac}}$ from (7) and $\tilde{i}^{n}_{\text{arm,ac}}$ from (8) into (10), the arm AC active power are represented by the following equations:

$$P^{p}_{\text{arm,ac}} = \frac{X_L}{(X_l^2 + 2X_l X_L)}|\tilde{v}^{p}_{\text{arm,ac}}||\tilde{v}^{n}_{\text{arm,ac}}|sin(\phi), \tag{11}$$

$$P^{n}_{\text{arm,ac}} = -\frac{X_L}{(X_l^2 + 2X_l X_L)}|\tilde{v}^{p}_{\text{arm,ac}}||\tilde{v}^{n}_{\text{arm,ac}}|sin(\phi), \tag{12}$$

where ϕ represents the upper arm voltage AC component phase angle with respect to lower arm voltage AC component. In the AC analysis presented in this paper, all phase angle of voltages/currents are represented with respect to the AC component of the lower arm voltage.

The AC component of the arm current in the DC MMC serves as a mean for exchanging power between the upper and lower arm of each phase-leg. To maintain the steady-state power balance of each SM capacitor, the summation of the active AC power and DC power flowing through each arm must be equal to zero. By equating AC and DC powers for each arm, the power balance constraint for each phase-leg is represented by the following equation:

$$(\frac{v_{\text{dc1}}}{v_{\text{dc2}}} - 1)\frac{P}{M} = -\frac{X_L}{(X_l^2 + 2X_l X_L)}|\tilde{v}^{p}_{\text{arm,ac}}||\tilde{v}^{n}_{\text{arm,ac}}|sin(\phi). \tag{13}$$

Fig. 5 presents the effects of the conversion ratio on the arm power at various number of phase-legs to transfer one per unit power. As the conversion ratio increasing, the DC

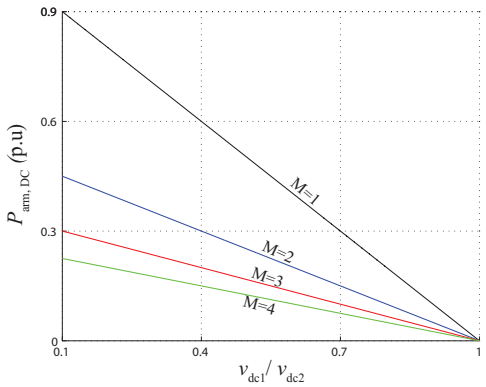

Fig. 5. Arm DC power versus conversion ratio to transfer one per unit power.

power transferred by each arm decreases which implies that the AC power required to maintain the power balance of each SM capacitor voltage reduces. In addition, since the phase-legs share the converter power equally, as the number of phase-legs increasing, the power stress on each arm decreases.

III. Converter Design and Component Sizing

As shown in (13), there are an infinite number of possible combinations of circuit parameters and control variables that satisfy the power balance equation. Since all parameters in (13) are correlated, changing one parameter will affect the other parameters and the converter performance.

The objective of the component sizing is to minimize the total power losses while satisfying a set of given design constraints. The design constraints include the magnitude of the SM capacitor voltages ripple, total semiconductor power losses, and the amplitude of the AC component of the phase current. The semiconductor power losses, i.e., conduction and switching, mainly depend on the magnitude of the arm current [23]. Since the DC component of the arm current is determined by the operating conditions, the main design goal is to minimize the magnitude of the AC component of the arm current. For this purpose, sizing of the arm and phase filtering inductors as well as the SM capacitor are discussed in this section. In addition to the component sizing, selection of the operating frequency of the converter is also explained.

A. Arm Inductive Reactance

In this subsection, a simplified model of the DC MMC is employed to size X_l. The simplified model is derived by assuming that $X_L >> X_l$. Consequently, (7), (8), and (13) are simplified to:

$$\tilde{i}^{p}_{\text{arm,ac}} = \tilde{i}^{n}_{\text{arm,ac}} = -\frac{1}{2jX_l}(\tilde{v}^{p}_{\text{arm,ac}} + \tilde{v}^{n}_{\text{arm,ac}}), \tag{14}$$

$$(\frac{v_{\text{dc1}}}{v_{\text{dc2}}} - 1)\frac{P}{M} = -\frac{1}{2X_l}|\tilde{v}^{p}_{\text{arm,ac}}||\tilde{v}^{n}_{\text{arm,ac}}|sin(\phi). \tag{15}$$

In the DC-AC MMC used in HVDC applications, the arm reactance serves two main functions: (i) attenuating the high-frequency components of the circulating current and (ii) limiting the DC-side short-circuit fault current. In contrast, in the DC MMC, the AC circulating current is required to exchange active power between the upper and lower arm of each phase-leg, whereby power balance can be maintained within each phase-leg. As a result, the magnitude of the circulating current is controlled to maintain the SM power balance and it does not need to be suppressed by passive components. In the DC MMC, the arm inductor acts as a line impedance such that the voltage across the inductor generates an AC component for the arm current. Since the AC active power needed to be exchanged between each upper and lower arm pair is a fixed value determined by (5) and (6), the amplitude of the AC component of the arm voltage should be maximized in order to minimize the arm current which leads to minimized device current rating and power losses.

For proper operation of the converter, the following constraints must be satisfied: (i) the half-bridge SM can only insert a positive voltage in the ON-state, thus the instantaneous arm voltage must be greater than zero, and (ii) the maximum instantaneous arm voltage must be smaller than the DC-link 2 voltage. Since the arm voltage contains a DC component and an AC component, to satisfy the constraint (i), the amplitude of the AC component of each arm should be smaller than the DC component. To satisfy the constraint (ii), the amplitude of the AC component of each arm should be smaller than the difference between the DC-link 2 voltage and the DC component of each arm. The constraints on the amplitude of the AC component of the upper and lower arms are expressed by:

$$|\tilde{v}^{p}_{\text{arm,ac}}| \leqslant \text{Min}[v^{p}_{\text{arm,dc}}, (v_{\text{dc2}} - v^{p}_{\text{arm,dc}})], \tag{16}$$

$$|\tilde{v}^{n}_{\text{arm,ac}}| \leqslant \text{Min}[v^{n}_{\text{arm,dc}}, (v_{\text{dc2}} - v^{n}_{\text{arm,dc}})]. \tag{17}$$

Therefore, once the DC-link 1 voltage, DC-link 2 voltage, and rated power are given, the amplitude of the arm current AC component can be solved for various phase shifting angle by (14) and (15). The amplitude of the arm AC current versus phase shifting angle, ϕ, for different arm inductive reactance is plotted in Fig. 6 in which $v_{\text{dc1}} = 0.5v_{\text{dc2}}$ is assumed. Once the arm inductance is selected, the amplitude of arm current AC component moves along one unique curve shown in Fig. 6 as the phase shifting angle increases. As ϕ approaches π, the amplitude of the arm AC current component reaches a minimum. To minimize the converter losses, the arm AC current amplitude should be minimized by controlling the phase shifting angle and corresponding arm AC voltage amplitude. Based on Fig. 6, as the arm inductance decreases, the rate of change of the amplitude of the AC circulating current arm current with respect to the ϕ increases at the vicinity of the achievable minimum circulating current. As a result, a sufficiently large X_l should be selected to ensure that the controller is able to converge to the achievable minimum AC circulating current. Selection of the arm inductance value depends on the controller type/design.

On the other hand, the size of X_l affects the maximum attainable converter output power, P_{max}. Fig. 7 presents the effects of X_l on P_{max} at various conversion ratio. As show in Fig. 7, P_{max} reduces as X_l increasing. In addition, as the conversion

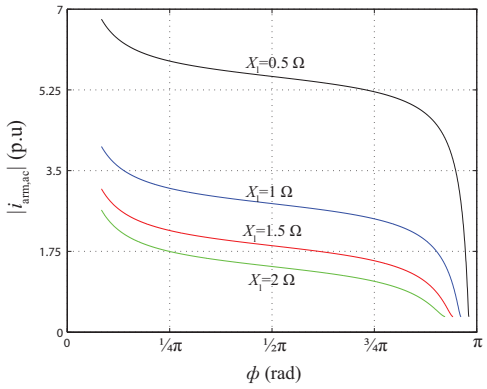

Fig. 6. Arm AC current amplitude verses arm voltage phase shifting angle.

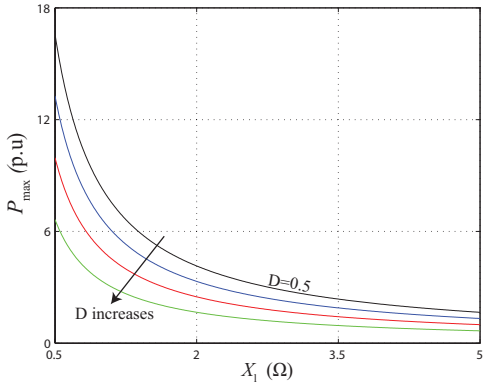

Fig. 7. The maximum attainable converter output power verses arm inductive reactance.

ratio deviates from 0.5, $P_{\max}$ deceases at fixed X_l. Consequently, the maximum value of X_l must be sized to ensure the rated converter power is smaller than $P_{\max}$.

B. Phase Filtering Inductive Reactance

For proper operation and minimized power losses of the DC MMC, the AC component of the output phase current should be negligible. This necessitates a large X_{L}, which for high power/voltage applications, adds to the system cost and complexity. Therefore, it is of interest to determine the minimum X_{L} that satisfies the constraint on the amplitude of AC current component of the phase current. The amplitude of the phase AC current can be determined by solving (9) for various X_{L}. Fig. 8 presents the amplitude of the AC component of the phase current verses X_{L} at various conversion ratio. As X_{L} increasing, the current amplitude decreases. However, the rate of change of the phase current AC component is reduced as X_{L} increases, which implies the marginal cost of reducing the phase current AC component is increased. In addition, as the conversion ratio deaviate from 0.5, the phase current ripple decreases at the same X_{L}. The minimum X_{L} that ensures the phase current amplitude below the design constraint is selected as the best value of X_{L}.

C. SM Capacitive Reactance

The dynamic of the sum of the SM capacitor voltages in the upper or lower arms were derived in the work done in [3] and

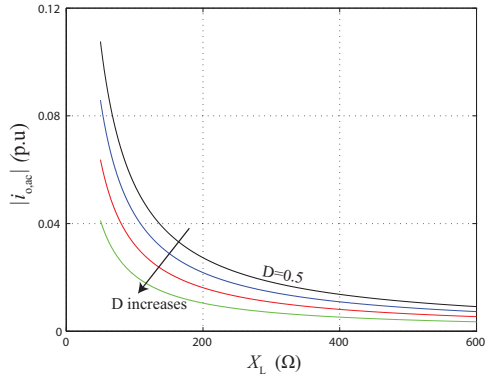

Fig. 8. Phase AC current amplitude versus phase filtering inductive reactance.

is expressed by:

$$\frac{\mathrm{d}v^{\Sigma p,n}}{\mathrm{d}t} = \frac{N}{C} m^{p,n} i^{p,n}_{\mathrm{arm}}, \tag{18}$$

where C is the SM capacitance, $v^{\Sigma p,n}$ is the sum of SM capacitor voltages of the upper or lower arm, and $m^{p,n}$ represents the insertion index of the upper or lower arm.

The sum of the SM capacitor voltages is given by:

$$v^{\Sigma p,n} = N v_{C,\mathrm{nominal}} + N\Delta v_C^{p,n}, \tag{19}$$

where $v_{C,\mathrm{nominal}}$ represents the nominal value of the SM capacitor voltage and $\Delta v_C^{p,n}$ represents the ripple component of the SM capacitor voltage of the upper or lower arm. The submodule capacitance C is normally sized large enough such that it is safe to assume $|\Delta v_C^{p,n}| \ll v_{\mathrm{dc2}}$.

The insertion indices of the upper and lower arms are expressed as:

$$m^p = \frac{(v_{\mathrm{dc2}} - v_{\mathrm{dc1}}) + V^p_{\mathrm{arm,ref}} \cos(\omega t + \phi_{\mathrm{ref}})}{v_{\mathrm{dc2}}}, \tag{20}$$

$$m^n = \frac{v_{\mathrm{dc1}} + V^n_{\mathrm{arm,ref}} \cos(\omega t)}{v_{\mathrm{dc2}}}, \tag{21}$$

where $V^p_{\mathrm{arm,ref}}$ and $V^n_{\mathrm{arm,ref}}$ represent the reference for the amplitude of the AC component of the upper and lower arms, respectively, ϕ_{ref} represents the reference for the phase angle of the AC component of the upper arm voltage, and ω represents the converter operating frequency.

The arm currents can be expressed by:

$$i^p_{\mathrm{arm}} = -\frac{i_{\mathrm{dc2}}}{M} + I_p \cos(\omega t + \phi_p), \tag{22}$$

$$i^n_{\mathrm{arm}} = \frac{i_{\mathrm{dc2}}}{M}\left(\frac{v_{\mathrm{dc2}}}{v_{\mathrm{dc1}}} - 1\right) + I_n \cos(\omega t + \phi_n), \tag{23}$$

where ϕ_p and ϕ_n represent the phase angle of the AC component of the upper and lower arm currents, respectively, and I_p and I_n represent the amplitude of the upper and lower arm current AC component, respectively.

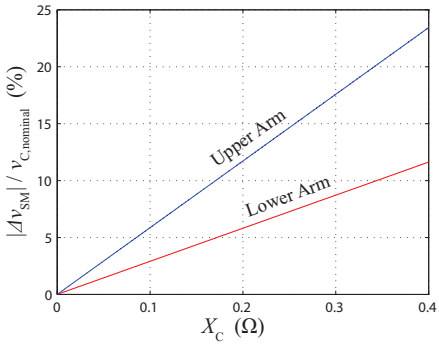

Fig. 9. The ratio of magnitude of the SM capacitor voltage ripple and SM nominal voltage verses SM capacitive reactance at D=0.7.

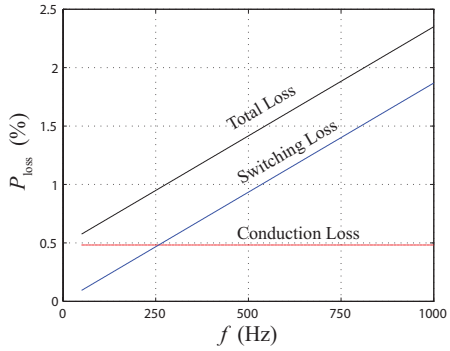

Fig. 10. Converter semiconductor device losses verses the operating frequency.

Substituting for $m^{p,n}$ from (20) and $i^{p,n}_{arm}$ from (22) into (18) then integrating both sides of the results, the SM capacitor voltage ripple component can be expressed by:

$$\Delta v_C^p = X_C[(1-\frac{v_{dc1}}{v_{dc2}})I_p \sin(\omega t+\phi_p)- \frac{V^p_{arm,ref} i_{dc2}}{M v_{dc2}} \sin(\omega t+\phi_{ref}) + \frac{I_p V^p_{arm,ref}}{4 v_{dc2}} \sin(2\omega t+\phi_{ref}+\phi_p)], \quad (24)$$

$$\Delta v_C^n = X_C[\frac{v_{dc1} I_n}{v_{dc2}} \sin(\omega t+\phi_n)+ (\frac{v_{d2}}{v_{d1}}-1)\frac{V^n_{arm,ref} i_{dc2}}{M v_{dc2}} \sin(\omega t) + \frac{I_n V^n_{arm,ref}}{4 v_{dc2}} \sin(2\omega t+\phi_n)], \quad (25)$$

where X_C represents the SM capacitive reactance which is defined as $X_C = 1/\omega C$.

As shown in (24) and (25), the ripple component of the SM capacitor voltage of the upper and lower arms carry two fundamental component terms as well as a second-order harmonic term. The amplitude of the fundamental terms depends upon the ratio of the input and output DC-link voltages. The SM capacitor voltages in the upper and lower arms are functions of the conversion ratio. As the conversion ratio deviating from 0.5, the difference of the SM capacitor voltage ripple between the upper and lower arms varies. Therefore, it is important to size X_C to ensure the magnitude of the SM capacitor voltage ripple of both arms below the design constraint.

Solving (24) and (25), the normalized SM capacitor voltage ripple versus the SM capacitive reactance is shown in Fig. 9 for $v_{dc1}/v_{dc2} = 0.7$. As shown in Fig. 9 the amplitude of the SM capacitor voltage in the lower arm is greater than that in the upper arm. As the X_C decreasing, the magnitude of the SM capacitor voltage ripple of both arms decreases. Based on Fig. 9, the best value of X_C is selected as its maximum value that ensures the magnitude of SM capacitor voltage ripple of both arms satisfy the given design constraint.

D. Operating Frequency

Unlike the DC-AC MMC used in the HVDC applications in which the operating frequency is imposed by the converter AC-side frequency, the operating frequency of the DC MMC is a free design parameter. The operating frequency can be chosen based on a trade-off between the component size/cost and the converter efficiency. To choose a proper AC operating frequency, the power losses of the converter are evaluated at various operating frequencies. Since a higher operating frequency leads to smaller passive components size/cost, the maximum AC operating frequency that satisfies the power loss constraint is identified as the best operating frequency. Since the semiconductor devices make the major contribution to the converter total power losses [26], the power loss constraint is set for semiconductor devices losses. To calculate the power losses, a power loss estimation method based on semiconductor behavior model is adopted from [27,28]. By applying this method, the total conduction and switching losses of the DC MMC at the given operating condition are evaluated for various operating frequencies. The converter semiconductor device losses versus the converter operating frequency are shown in Fig. 10. As shown in the figure, the switching losses increases as the operating frequency increasing whereas the conduction loss is independent of the operating frequency. Once the operating frequency is chosen, the arm and phase filtering inductances as well as the SM capacitance can be determined based on the operating frequency and their corresponding reactances that determined in the previous steps.

The overall procedure to size the components of the DC MMC is illustrated in the flowchart of Fig. 11. Given the nominal operating conditions and the design constraints, first, X_l is selected based on the converter power and the controller convergence test. X_l should be sized to guarantee that the controller converges to the achievable minimum arm AC current. As shown in Fig. 11, several iterations might be required to find the best set of components, which satisfy the design constraints. Once X_l is selected, the amplitude of the AC component of the phase current is calculated for various X_L. A minimum X_L that satisfies the phase current AC component amplitude constraint can be identified as the best value of X_L in this step. The magnitude of the SM capacitor voltage ripple will then be calculated for different X_C. A maximum X_C that satisfy the constraint on the SM voltage ripple magnitude is identified as the best value of X_C. In the next step, semiconductor power losses are estimated at various operating frequencies and the maximum frequency that satisfies the power loss constraint

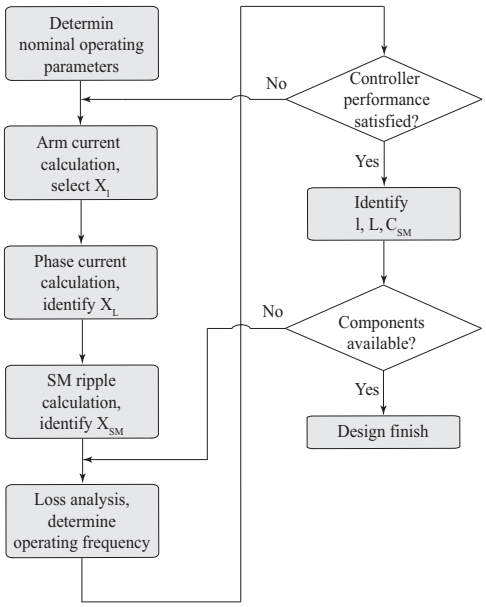

Fig. 11. Flowchart of the component sizing procedure of the DC MMC.

can then be identified as the best value. After this step, the controller performance will be evaluated by simulation studies. If the controller fails to converge to the minimum achievable amplitude of AC circulating current, X_l will be resized. Then, the arm and output inductors as well as the SM capacitor can be sized.

IV. Simulation Results

Two case studies are reported in this section on a three-phase-leg DC MMC of Fig. 1, using parameters and corresponding constraints listed in Tables I and II. The studies are conducted to validate the developed stady-state model and demonstrate the accuracy of the converter design process. The sizes of passive components are determined based on the design procedure in Fig. 11. Two modes of operations are simulated to mimic the bidirectional power flow: the buck mode of operation which is defined as DC power flowing from DC-link 2 to DC-link 1 and the boost mode of operation which is defined as DC power flowing from DC-link 1 to DC-link 2. The designed converters are simulated in PSCAD/EMTDC software environment. The SPWM modulation scheme and the open loop control strategy in [19] are used in the simulation studies.

A. Simulation Results for $v_{dc1}/v_{dc2} = 0.5$

The steady-state converter waveforms for buck and boost modes of operation of the DC MMC are provided in Figs. 12 and 13, respectively, where $v_{dc1}/v_{dc2} = 0.5$. In both figures, the SM capacitor voltages and arm currents of only the phase-*a* are shown. The nominal conditions, design constraints, converter parameters, and analytical results are shown in Table I. By following the described design procedure, an X_l of 2 Ω is selected to ensure the convergence of the controller. An X_L of 450 Ω is chosen, which results in 9.8 A phase AC current amplitude. X_{SM} is selected as 0.2 Ω, which results in 3.8% SM capacitor voltage ripple. An AC operating frequency of 360 Hz is chosen, leading to 0.5% semiconductor power losses.

Since $v_{dc1}/v_{dc2} = 0.5$, the DC components of i^p_{arm} and i^n_{arm} have the same magnitude as shown in Figs. 12(c) and 13(c). The magnitudes of the SM capacitor voltages ripple in the upper and lower arms are the same, i.e., 74 V for buck mode of operation and 78 V for boost mode of operation. The peak to peak magnitude of the AC component of the phase current is equal to 18 A for both modes of operation. As confirmed by the waveforms of Figs. 12 and 13, the magnitude of the SM capacitor voltages ripple and AC component of the phase current are below the design constraints for both modes of operation.

TABLE I
Nominal conditions and design constraints for case A

Nominal Conditions	**Value**
Output power, P	7 MW
DC-link 1 voltage, v_{dc1}	4.4 kV
DC-link 2 voltage, v_{dc2}	8.8 kV
Design Constraints	**Value**
Phase current ripple, $\lvert i_{o,ac,p\text{-}p}\rvert/i_{o,dc}$	5%
SM voltage ripple, $\lvert\Delta v_{SM}\rvert/v_{C,nominal}$	4%
Converter power losses	1%
Converter Parameters	**Value**
Number of SMs per arm, N	4
SM capacitor, C_{SM}	2 mF
Arm inductor, l	0.89 mH
Phase filtering inductor, L	132 mH
Operating frequency, f	360 Hz
Performance Parameters	**Analytical Results**
Phase current ripple, $\lvert i_{o,ac,p\text{-}p}\rvert$	19.6 A
SM capacitor voltage ripple $\lvert\Delta v_{SM}\rvert$	81.6 V
Converter power losses	0.5%

B. Simulation Results for $v_{dc1}/v_{dc2} = 0.7$

The corresponding simulation results for $v_{dc1}/v_{dc2} = 0.7$ for buck and boost modes of operation are provided in Figs. 14 and 15, respectively. The nominal conditions, design constraints, converter parameters, and analytical results are shown in Table II. An X_L of 120 Ω is chosen, which results in a phase AC current with a magnitude of 9.5 A. X_{SM} is selected as 0.11 Ω, which leads to 3.9% SM capacitor voltage ripple. An AC operating frequency of 360 Hz is used, resulting in 0.5% semiconductor power losses. Since the current sharing between the upper and lower arm pairs changes with the DC-link 1 and DC-link 2 ratio, when $v_{dc1}/v_{dc2} = 0.7$ the upper and lower arms unequally contribute to the DC current as shown in Figs. 14(c) and 15(c). This, consequently, leads to unequal amplitude of the SM capacitor voltages in the upper and lower arms, as shown in Figs. 14(e) and 15(e). In this case, X_{SM} is sized based on the amplitude of the lower arm SM capacitor voltage ripple, which is larger than the upper arm. For both modes of operation, the converter transfers 7 MW power.

The amplitude of the SM capacitor voltage ripple of the lower arm is 80 V in the buck mode operation and 83 V in the boost mode operation. As shown in Figs. 14(d) and 15(d), the peak to peak magnitude of the AC component of the phase current

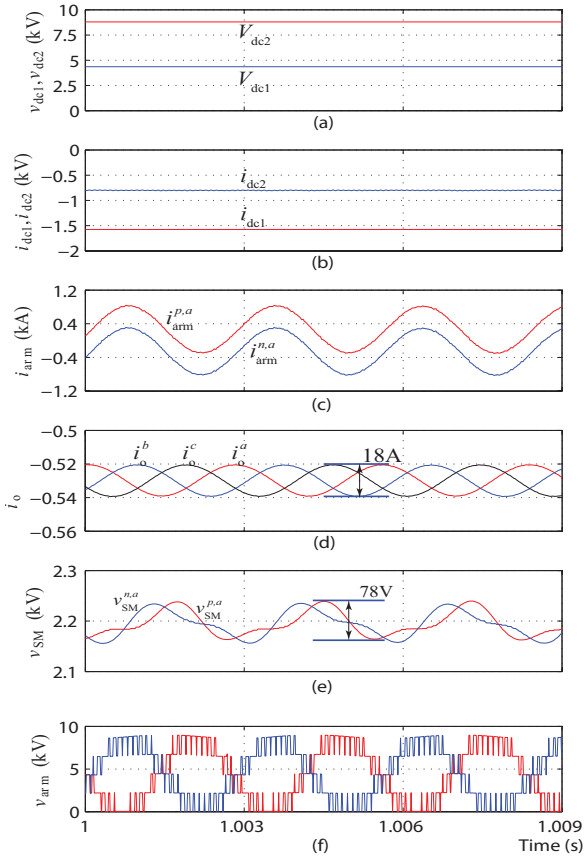

Fig. 12. Steady-state converter waveforms for buck mode of operation for $v_{dc1}/v_{dc2} = 0.5$: (a) input and output dc voltages, (b) input and output currents, (c) upper and lower arm currents of phase-*a*, (d) phase currents, (e) SM capacitor voltages of the upper and lower arm of phase-*a* and (f) upper and lower arm voltages of phase-*a*.

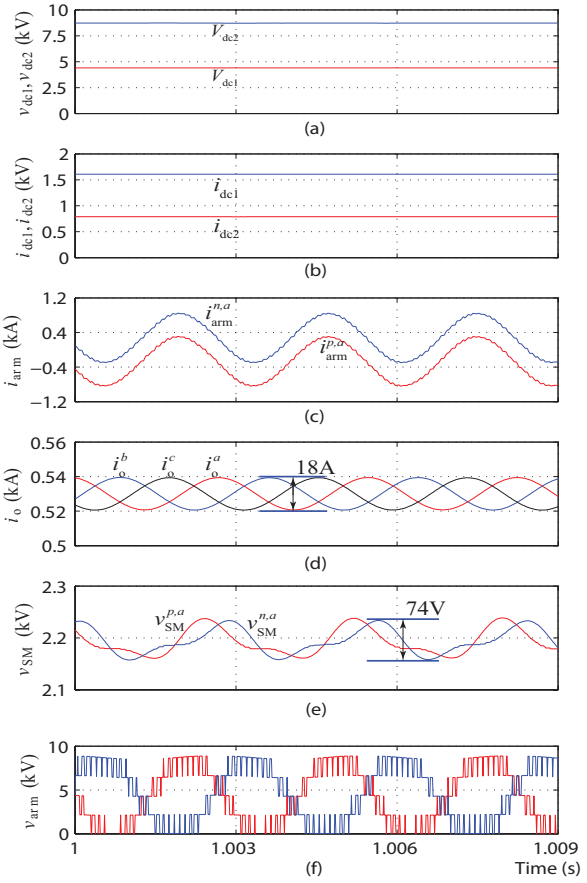

Fig. 13. Steady-state converter waveforms for boost mode of operation for $v_{dc1}/v_{dc2} = 0.5$: (a) input and output dc voltages, (b) input and output currents, (c) upper and lower arm currents of phase-*a*, (d) phase currents, (e) SM capacitor voltages of the upper and lower arm of phase-*a* and (f) upper and lower arm voltages of phase-*a*.

is equal to 18 A for both modes of operation. As confirmed by the waveforms of Figs. 14 and 15, in both modes of operation, the amplitudes of the SM capacitor voltage ripple and AC component of the phase current are below their per-specified constraints.

V. Conclusion

In this paper, a phasor-domain steady-state mathematical model for the DC MMC is developed. Based on the developed model, a systematic procedure of sizing the converter components is developed. Proper sizing of the components ensures the converter achieve high efficiency while satisfying a set of given design requirements. Simulation results are presented to demonstrate the accuracy of the proposed method.

References

[1] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electro.*, vol. 30, pp. 37–53, Jan 2015.

[2] A. Nami, J. Liang, F. Dijkhuizen, and G. Demetriades, "Modular multilevel converters for hvdc applications: Review on converter cells and functionalities," *IEEE Trans. Power Electro.*, vol. 30, pp. 18–36, Jan 2015.

[3] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist, and H.-P. Nee, "Dynamic analysis of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 60, pp. 2526–2537, July 2013.

[4] D. H. J. E. F. B. W. W. R. Li, G. P. Adam, "Hybrid cascaded modular multilevel converter with dc fault ride-through capability for the HVDC transmission system," *IEEE Trans. Power Del.*, vol. 30, pp. 1853–1862, Aug 2015.

[5] S. M. A. A. L. H. S. N. N. Ahmed, L. Angquist and S. H. P. Nee, "Efficient modeling of an mmc-based multiterminal dc system employing hybrid hvdc breakers," *IEEE Trans. Power Del.*, vol. 30, pp. 1792–1801, Aug 2015.

[6] J. Qin and M. Saeedifard, "A zero-sequence voltage injection-based control strategy for a parallel hybrid modular multilevel hvdc converter system," *IEEE Trans. Power Del.*, vol. 30, pp. 728–736, April 2015.

[7] S. Debnath, J. Qin, and M. Saeedifard, "Control and stability analysis of modular multilevel converter under low-frequency operation," *IEEE. Trans. Ind. Electron.*, vol. PP, no. 99, pp. 1–1, 2015.

[8] A. Antonopoulos, L. Angquist, S. Norrga, K. Ilves, L. Harnefors, and H.-P. Nee, "Modular multilevel converter ac motor drives with constant torque from zero to nominal speed," *IEEE Trans. Ind. Applicat.*, vol. 50, pp. 1982–1993, May 2014.

[9] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Trans. Power Electron.*, vol. 30, pp. 349–357, Jan 2015.

[10] A. Antonopoulos, L. Angquist, L. Harnefors, and H.-P. Nee, "Optimal selection of the average capacitor voltage for variable-speed drives with modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30,

TABLE II
NOMINAL CONDITIONS AND DESIGN CONSTRAINTS FOR CASE B

Nominal Conditions	**Value**
Output power, P	7 MW
DC-link1 voltage, v_{dc1}	6.16 kV
DC-link2 voltage, v_{dc2}	8.8 kV
Design Constraints	**Value**
Phase current ripple, $\lvert i_{o,ac,p\text{-}p}\rvert/i_{o,dc}$	5%
SM voltage ripple, $\lvert\Delta v_{SM}\rvert/v_{C,nominal}$	4%
Converter power losses	1%
Converter Parameters	**Value**
Number of SMs per arm, N	4
SM capacitor, C_{SM}	4.1 mF
Arm inductor, l	0.89 mH
Phase filtering inductor, L	97.3 mH
Operating frequency, f	360 Hz
Performance Parameters	**Analytical Results**
Phase current ripple, $\lvert i_{o,ac,p\text{-}p}\rvert$	19 A
SM capacitor voltage ripple $\lvert\Delta v_{SM}\rvert$	86 V
Converter power losses	0.5%

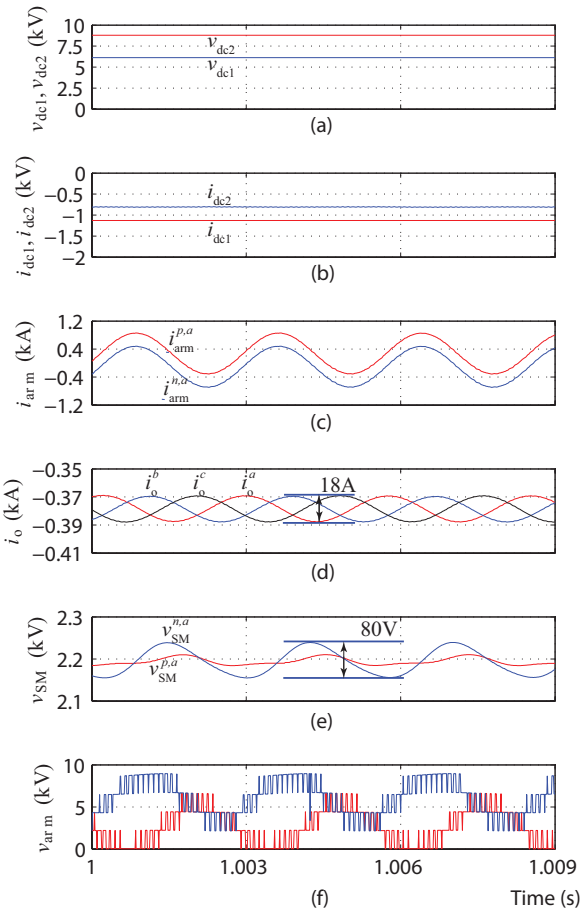

Fig. 14. Steady-state converter waveforms for buck mode of operation for $v_{dc1}/v_{dc2} = 0.7$: (a) input and output dc voltages, (b) input and output currents, (c) upper and lower arm currents of phase-*a*, (d) phase currents, (e) SM capacitor voltages of the upper and lower arm of phase-*a*, and (f) upper and lower arm voltages of phase-*a*.

pp. 227–234, Jan 2015.

[11] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel vsc technologies for power transmission," in *IEEE Transmission and Distribution Conference and Exposition*, pp. 1–16, April 2008.

[12] T. C. G. F. H. T. Luth, T. M. M. C. Merlin and C. D. Barker, "High-frequency operation of a dc/ac/dc system for hvdc applications," *IEEE Trans. Power Electon.*, vol. 29, pp. 4107–4115, Aug 2014.

[13] J. Qin and M. Saeedifard, "Predictive control of a modular multilevel converter for a back-to-back hvdc system," *IEEE Trans. Power Del.*, vol. 27, pp. 1538–1547, July 2012.

[14] D. R. T. C. D. Barker, C. C. Davidson and R. S. Whitehouse, "Requirements of dc-dc converters to facilitate large dc grids," in *CIGRE Symp.*, pp. 1–10, Aug 2012.

[15] M. M. C. C. E. Sheridan and T. C. Green, "Assessment of dc/dc converters for use in dc nodes for offshore grids," in *10th IET int. Conf. AC DC Power Transmiss.*, pp. 1–6, Dec 2012.

[16] A. Parastar, Y. C. Kang, and J.-K. Seok, "Multilevel modular dc/dc power converter for high-voltage dc-connected offshore wind energy applications," *IEEE Trans. Ind. Appl.*, vol. 62, pp. 2879–2890, May 2015.

[17] P. Bresesti, W. Kling, R. Hendriks, and R. Vailati, "Hvdc connection of offshore wind farms to the transmission system," *IEEE Trans. Energy Conversion*, vol. 22, pp. 37–43, March 2007.

[18] G. Kish and P. Lehn, "A comparison of modular multilevel energy conversion processes: Dc/ac versus dc/dc," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 951–958, May 2014.

[19] G. Kish, M. Ranjram, and P. Lehn, "A modular multilevel dc/dc converter with fault blocking capability for hvdc interconnects," *IEEE Trans. Power Electro.*, vol. 30, pp. 148–162, Jan 2015.

[20] J. Ferreira, "The multilevel modular dc converter," *IEEE Trans. Power Electro.*, vol. 28, pp. 4460–4465, Oct 2013.

[21] G. Kish, C. Holmes, and P. Lehn, "Dynamic modeling of modular multilevel dc/dc converters for hvdc systems," in *IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–7, June 2014.

[22] S. Norrga, L. Angquist, and A. Antonopoulos, "The polyphase cascaded-cell dc/dc converter," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4082–4088, Sept 2013.

[23] C. Oates, "Modular multilevel converter design for vsc hvdc applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, pp. 505–515, June 2015.

[24] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," in *European Conference on Power Electronics and Applications (EPE)*, pp. 1–10, Sept 2013.

[25] Q. Tu, Z. Xu, H. Huang, and J. Zhang, "Parameter design principle of the arm inductor in modular multilevel converter based hvdc," in *International Conference on Power System Technology (POWERCON)*, pp. 1–6, Oct 2010.

[26] L. Wu, J. Qin, M. Saeedifard, O. Wasynczuk, and K. Shenai, "Efficiency evaluation of the modular multilevel converter based on si and sic switching devices for medium/high-voltage applications," *IEEE Trans. Electron Devices*, vol. 62, pp. 286–293, Feb 2015.

[27] U. Drofenik and J. W. Kolar, "A general scheme for calculating switching- and conduction-losses of power semiconductors in numerical circuit simulations of power electronic systems," in *Proc. International Power Electronics Conference (IPEC), Niigata, Japan, April*, pp. 4–8, 2005.

[28] Q. Tu and Z. Xu, "Power losses evaluation for modular multilevel converter with junction temperature feedback," in *IEEE Power Eng. Soc. General Meeting*, pp. 1–7, 2011.

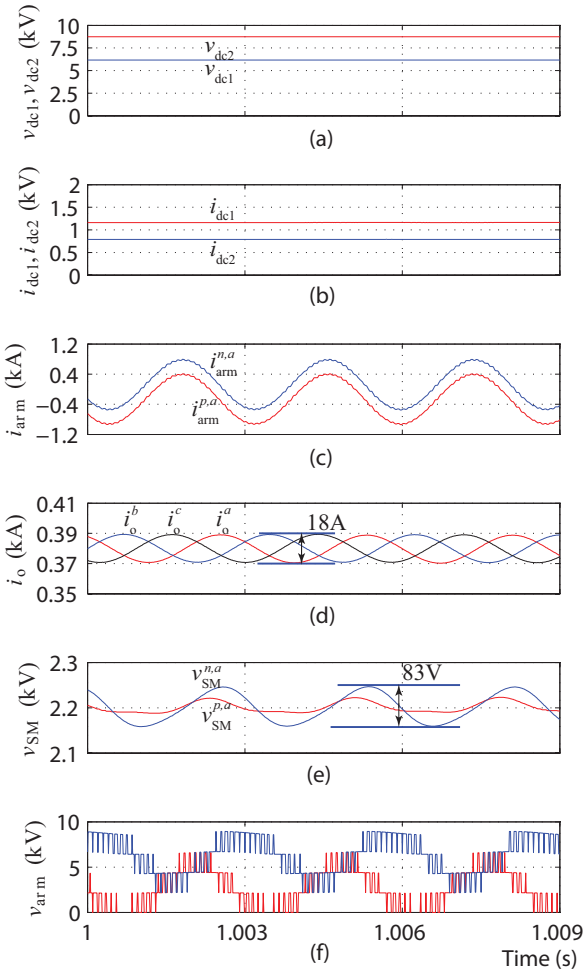

Fig. 15. Steady-state converter waveforms for boost mode of operation for $v_{dc1}/v_{dc2} = 0.7$: (a) input and output dc voltages, (b) input and output currents, (c) upper and lower arm currents of phase-*a*, (d) phase currents, (e) SM capacitor voltages of the upper and lower arm of phase-*a*, and (f) upper and lower arm voltages of phase-*a*.