Report Tracking Number: RPT-0000000621

Award number: DE-SC0007830

Award recipient: Prof. Ping Gui, Department of Electrical Engineering, Southern Methodist University

Project title: Design and Implementation of Low-Power 10Gb/s/channel Laser/Silicon Photonics Modulator Drivers with SEU Tolerance for HL-LHC

Street Address/City/State/Zip: 6251 Airline Rd., Junkins Bldg, Suite 319, Dallas, TX 75205

Postal Address: 6251 Airline Rd., Junkins Bldg, SMU P.O. Box 750338, Dallas, TX 75275, Phone Number: 214-768-1733; Email: pgui@smu.edu

Report Date: Feb 22, 2015

Period Covered By the Report: May 1, 2015 – Feb 22, 2016

Final Technical Report

Executive Summary of Accomplishments (May 1, 2015-March 30, 2017)

During the funding period of this award from May 1, 2014 through March 30, 2016, we have accomplished the design, implementation and measurement results of two laser driver chips: LpGBLD10+[1-5] which is a low-power single-channel 10Gb/s laser driver IC, and LDQ10P [6-8], which is a 4x10Gb/s driver array chip for High Energy Physics (HEP) applications. With new circuit techniques, the driver consumes a record-low power consumption, 31 mW @10Gb/s/channel and occupies a small area of 400 µm × 1750 µm for the single-channel driver IC and 1900umx1700um for the LDQ10P chip. These characteristics allow for both the LpGBLD10+ ICs and LDQ10P suitable candidate for the Versatile Link PLUS (VL^+) project, offering flexibility in configuring multiple Transmitters and receivers.

Detailed report

I. General description

The low power GBT chip set includes a laser driver, named GBLD10+, targeted at driving Vertical- cavity surface-emitting lasers (VCSELs). The block diagram of the laser driver is represented in Figure 1. The ASIC is composed of a laser modulation circuit and of a current sink for laser bias. Both the laser modulation and bias currents are programmable. To optimize the system response the driver circuit has programmable pre-emphasis, which can be enabled on either edge. All functions of the ASIC are programmable via I2C interface. The ASIC features also power-on reset feature, which ensures that after power on the chip is in well-defined, ready-to-use state.

II. LASER DRIVER specifications

LDQ10+ is a compact low-power radiation-hard 4x 10 Gb/s VCSEL driver array developed in 65 nm CMOS technology. Each channel in LDQ10 can provide a modulation current up to 8 mA and bias current up to 12 mA. Edge pre-emphasis is employed to compensate for the bandwidth limitations due to parasitic and the turn-on delay of VCSEL devices. LDQ10 occupies a chip area of 1900 µm × 1700 µm and consumes a total power consumption of 130 mW (32mW/channel) for 6.0mA bias current and 4.0mA modulation current as typical driving current settings. The modulation amplitude degrades less than 5% after 300 Mrad total ionizing dose. Directly wire-bonded to the VCSEL array, LDQ10+ servers as laser drivers for 2-way, 2-line communication between different modules in high-luminosity LHC experiments.

2.1 Driver array architecture and driving current

The block diagram of LDQ10 is shown in Fig. 1. It consists of four driver channels each working up to 10 Gb/s. Each channel provides bias and modulation current ranging from 0 to 12 mA and 0 to 8 mA, respectively, as is shown in Fig. 2. Here the bias current refers to the maximum current (the eye height) flowing into the VCSEL and the modulation refers to the AC amplitude (eye depth) of the current.

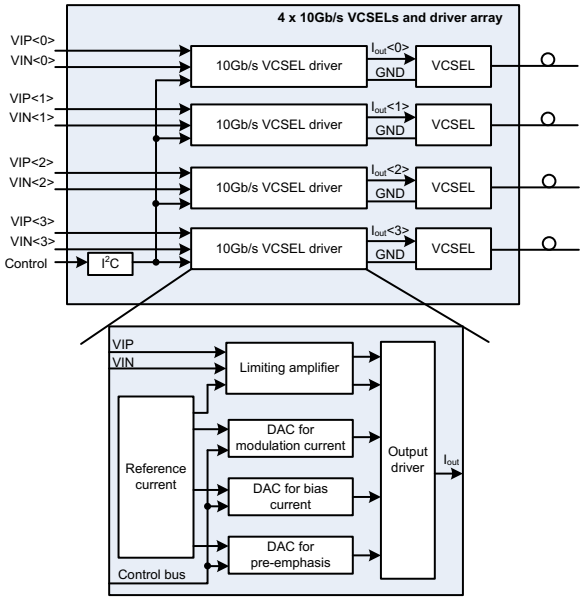


Fig. 1: Block diagram of LDQ10P array

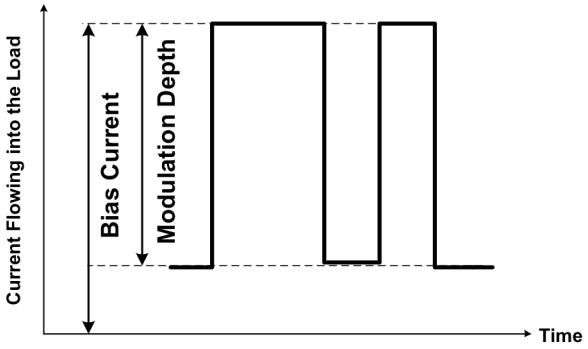
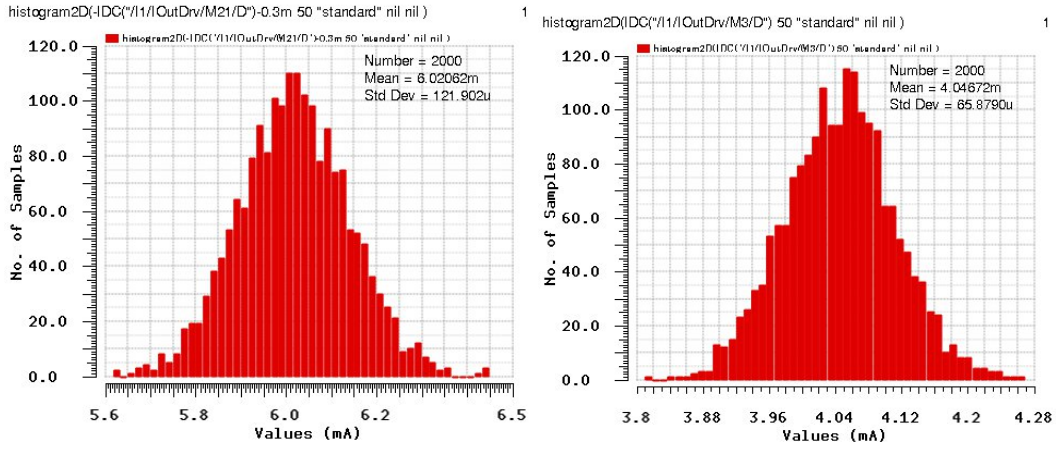


Fig 2: Bias current and modulation current definition

Bias and modulation current variation is simulated in Monte-Carlo simulations of 2000 runs as shown in Fig. 3. The 3σ value of bias and modulation current is 0.36 mA and 0.2 mA, respectively, which is small compared to the nominal value (6 mA for the bias

current and 4 mA for the modulation current). The design is thus robust against process variations and device mismatch.



(a)

(b)

Fig. 3: Monte-Carlo simulation (a) Bias Current (b) Modulation current.

2.2 Power-up protection

All circuits are powered by 1.2 V for low-power operation except for the OD stage which is powered by 2.5 V to accommodate the high turn-on voltage of VCSEL (typically 1.7 V). The transistors are biased carefully to guarantee no transistor works with more than 1.2 V. Each channel can be individually powered on/off to further save power consumption when needed. Commonly, the power on sequence of the chip should firstly power the 1.2V pads, after that power the 2.5V pads to protect the 1.2 V transistors. In the latest version of LDQ10+, a power-up protection circuit is design to safeguard the circuit at whatever power on sequences. In other words, if the 1.2 V power supply is not ready, 2.5 V will not be powered on to the chip.

2.3 Performance specification and measurement results

1) Performance specification

At 10 Gb/s, each of the 4 channels in the LDQ10 consumes 32 mW under typical settings (4 mA modulation current and 6 mA bias current) and the total power consumption is 130 mW including the digital control circuitry. This work achieved a power efficiency of 3.25 pJ/b. The overall performance parameters are summarized in Table I.

TABLE I: performance summary of LDQ10+

Parameters	Min.	Typ.	Max.	Unit
Technology		65		nm
Supply Voltage		2.5/1.2		V
Channel Number		4		-
Data Rate		10		Gbps
Power Consumption		130		mW
Power Efficiency		3.25		pJ/b
Bias Current	0	6	12	mA
Modulation Current	0	4	8	mA

2) Electrical measurement results

For electrical characterization, an Agilent JBERT N4903B was used for high-speed PRBS7 data generation and an Agilent DSA91204A oscilloscope was used for output waveform measurements. The jitter performance of the LDQ10P was measured with PRBS7 input data and at a BER of 10E-12. The test pattern length of PRBS7 is 127.

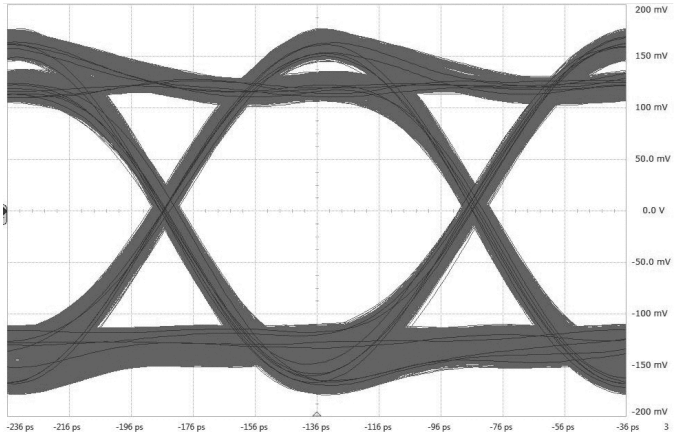


Fig. 4: 10 Gb/s electrical eye diagram with PRBS7 input data and

Fig.4 shows the electrical eye diagram at 10 Gb/s with 4 mA modulation current and 6 mA bias current. The total jitter TJ(BER) is defined as the amount of eye closure at a

given BER, which is the width of the eye minus the eye opening; RJ, DDJ and PJ are defined as random jitter, data dependent jitter and periodic jitter. The total jitter TJ(BER=10E-12) in electrical eye diagram is 15.47 ps with an RMS random jitter component of 0.68 ps.

3) Optical measurement results

The optical test board of the LDQ10 is assembled with a Philips Photonics ULM850-25-TT-N01xxU VCSEL array. The eye diagram at 10 Gb/s is shown in Fig. 5, where the total jitter TJ(BER=10E-12) is 17.97 ps and RMS random jitter is 0.84 ps, demonstrating the good performance of the LDQ10.

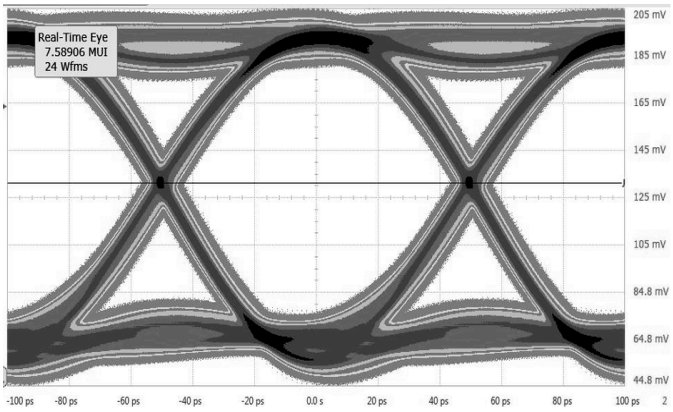


Fig. 5: 10 Gb/s optical eye diagram with PRBS7 input data.

4) Crosstalk measurement results

Crosstalk among channels may increase the jitter and corrupt the eye diagram. The worst-case scenario for the channel under test happens when the other three channels are transmitting the same data but a different data sequence from the one being transmitted by the channel under test. In our design, a power/ground mesh with a large amount of on-chip decoupling capacitors was used to minimize the crosstalk effects. Table II shows the comparison of performance between the scenario of only one channel being turned on (no crosstalk) and the worst-case scenario when all 4 channels are turned on (with crosstalk). As evident from the results, the increase in the total jitter is less than 2 ps at the worst-case scenario compared to when only a single-channel is running. This demonstrates that the crosstalk has negligible effects on the driver performance.

TABLE II: Crosstalk Measurement Results

	Single-channel on	All 4 channels on
TJ (ps)	17.52	18.03
DDJpp (ps)	8.04	8.11
RJrms (fs)	690	700

5) Pre-emphasis measurement results

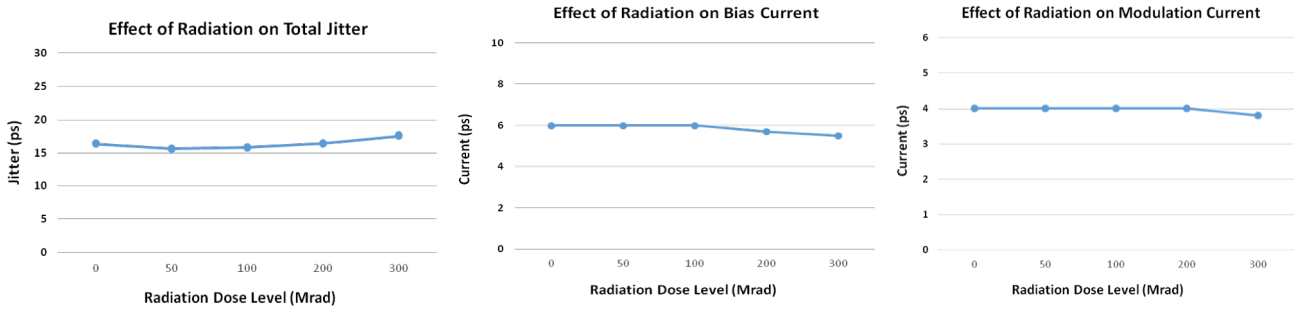
Frequency-domain edge pre-emphasis is employed in LDQ to accommodate different parasitics and compensate for the VCSEL turn-on delays. Table III shows the comparison of the measured performance at 10 Gb/s with/without pre-emphasis. With pre-emphasis, more frequency peaking is introduced to sharpen the rising and/or falling edge. The total jitter is improved by 2.4 ps with pre-emphasis compared to the case without pre-emphasis.

TABLE III: Pre-emphasis Measurement Results

	No pre-emphasis	Rising-edge pre-emphasis
TJ (ps)	22.24	19.83
DDJpp (ps)	6.68	6.38
RJrms (fs)	1.02	1.01

6) Irradiation measurement results

During the irradiation tests the chips X-ray were irradiated, while being powered on, for 3 days up to 300 Mrad dose with a dose rate of 9 Mrad/hour. Plots of the total jitter and modulation depth vs. TID are displayed in Fig. 6. The change in these parameters under ionizing dose up to 300 Mrad is minimum. The measurement results demonstrate the good tolerance of the LDQ10 to ionizing radiation.



(a) (b) (c)

Fig. 6: (a) Plot of total jitter vs. ionizing dose. (b) plot of modulation current vs. ionizing dose. (c)

II. LASER DIODE-DRIVER INTERCONNECTION AND LAYOUT

The connection between the 4-channel drivers and laser diodes (VCSELs) are depicted in Fig. 1. As shown in Fig. 7, the cathodes of the VCSELs should be wire bonded to chip ground pads on the right hand side. The anodes of the 4 VCSELs should be wire bonded to corresponding output pads (OUT1- OUT4). The cathodes of the VCSELs are not recommended to be connected to the ground on PCB other than on chip for the sake of having less noise and better jitter performance. The bond wire lengths are around 0.7 mm. In schematic simulation, each bond wire has an equivalent inductance at 0.5

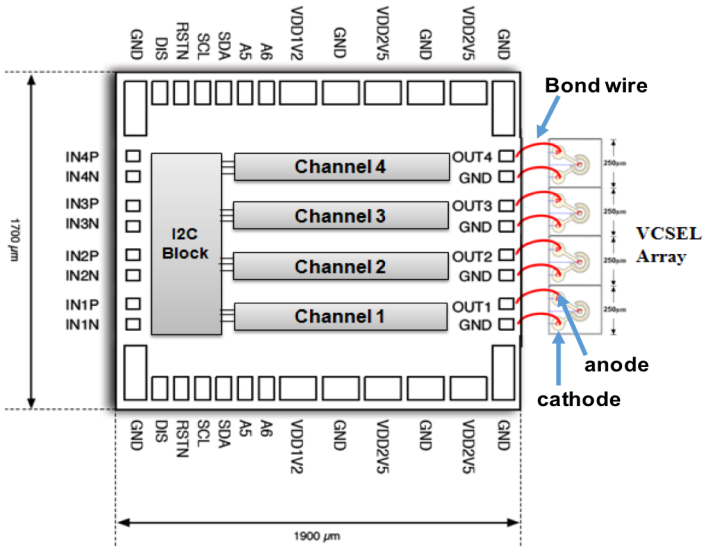


Fig. 7: Connection between the 4-channel drivers and the laser

nH~0.9 nH. The layout of the LDQ10 chip is shown in Fig. 8.

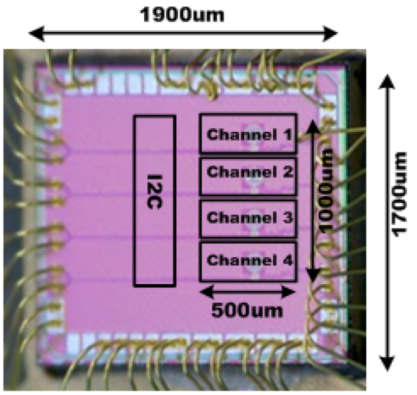


Fig. 8. Die photo of LDQ10P

III. PRE-EMPHASIS AND DE-EMPHASIS

VCSELs display asymmetric fall/rise times with the rise time being faster than the fall time which might lead to inter-symbol interference (ISI). A reconfigurable edge pre-emphasis technique is introduced to address this problem by enabling the pre-emphasis on the falling edge, rising edge or both edges. The LDQ10 has 20×7-bit I2C registers to control the different functions of each of the four channels, including the channel turn-on/off switches, the bias current, the modulation current, and the pre-(de-) emphasis configuration. The control bits are high voltage effective at around 1V. The definition and mapping of all control bits are shown in Table IV and V. The control bit [0] represents the LSB. There are three emphasis strength control bits to change the pre-emphasis amplitude. For bias current and modulation current control, there are 7 bits in total to control the current values and each 1 LSB corresponds to 0.16 mA current changes.

Table IV: Register Mapping of LDQ10+

Bits / Reg.	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	-	-	Global	Global	Global	Global	**Global**

			Emphasis Function Enable	Modulation Current Enable	Bias Current Enable	Limiting Amplifier Enable	**Chip Enable**
1	-	-	-	-	-	-	SDA Strength
2	-	-	-	-	-	-	-
3	-	-	-	-	-	-	-
4	-	Falling Edge Emphasis Enable	Rising Edge Emphasis Enable	Modulation Current Enable	Bias Current Enable	Limiting Amplifier Enable	**Channel 0 Enable**
5	Bias Current[6]	Bias Current[5]	Bias Current[4]	Bias Current[3]	Bias Current[2]	Bias Current[1]	Bias Current[0]
6	Modulation Current[6]	Modulation Current[5]	Modulation Current[4]	Modulation Current[3]	Modulation Current[2]	Modulation Current[1]	Modulation Current[0]
7	-	-	-	-	Emphasis Strength[2]	Emphasis Strength[1]	Emphasis Strength[0]
8	-	Falling Edge Emphasis Enable	Rising Edge Emphasis Enable	Modulation Current Enable	Bias Current Enable	Limiting Amplifier Enable	**Channel 1 Enable**
9	Bias Current[6]	Bias Current[5]	Bias Current[4]	Bias Current[3]	Bias Current[2]	Bias Current[1]	Bias Current[0]
A	Modulation Current[6]	Modulation Current[5]	Modulation Current[4]	Modulation Current[3]	Modulation Current[2]	Modulation Current[1]	Modulation Current[0]
B	-	-	-	-	Emphasis Strength[2]	Emphasis Strength[1]	Emphasis Strength[0]
C	-	Falling Edge	Rising Edge	Modulation Current	Bias Current	Limiting Amplifier	**Channel 2 Enable**

		Emphasis Enable	Emphasis Enable	Enable	Enable	Enable	
D	Bias Current[6]	Bias Current[5]	Bias Current[4]	Bias Current[3]	Bias Current[2]	Bias Current[1]	Bias Current[0]
E	Modulation Current[6]	Modulation Current[5]	Modulation Current[4]	Modulation Current[3]	Modulation Current[2]	Modulation Current[1]	Modulation Current[0]
F	-	-	-	-	Emphasis Strength[2]	Emphasis Strength[1]	Emphasis Strength[0]
10	-	Falling Edge Emphasis Enable	Rising Edge Emphasis Enable	Modulation Current Enable	Bias Current Enable	Limiting Amplifier Enable	**Channel 3 Enable**
11	Bias Current[6]	Bias Current[5]	Bias Current[4]	Bias Current[3]	Bias Current[2]	Bias Current[1]	Bias Current[0]
12	Modulation Current[6]	Modulation Current[5]	Modulation Current[4]	Modulation Current[3]	Modulation Current[2]	Modulation Current[1]	Modulation Current[0]
13	-	-	-	-	Emphasis Strength[2]	Emphasis Strength[1]	Emphasis Strength[0]

Notes:

1. Different colours represent the control registers for different channels (yellow: channel 0; green: channel 1; orange: channel 2; grey: channel3).
2. Register 0~1 controls the global circuits, where all four channels function can be turned on and off together.
3. Register 4~7 controls the channel 0, Register 8~B controls channel1, Register C~F B controls channel2, Register 10~13 B controls channel3.

Table V: Definition of Register Mapping in LDQ10+

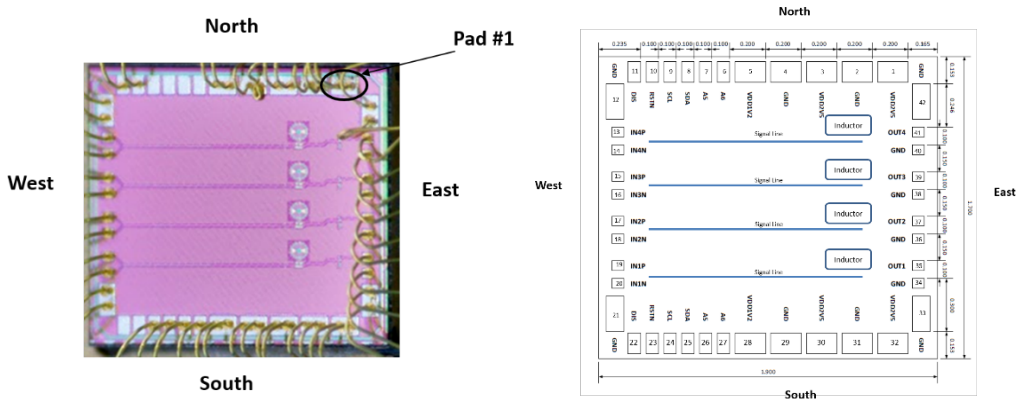
Symbol	Default Value	Function Description
Global Chip Enable	1	Global chip ready
Global **X** enable	All the values are 1, except pre-emphasis function	**X**(limiting amplifier, modulation current, bias current…) part function in all channels ready
X enable	All the default values are 1, except pre-emphasis function	**X**(limiting amplifier, modulation current, bias current…) part function in this channel enabled
MOD[6:0]	2F	Laser modulation current setting by $I_{BIAS} = 0.16 \cdot BiasSet < 6:0 >$ mA
BIAS[6:0]	26	Laser bias current setting by $I_{Mod} = 0.16 \cdot ModSet < 6:0 >$ I□pre□=0.95*PRE<3:0> mA
Emphasis Strength [2:0]	0	Laser pre-emphasis amplitude strength setting

Notes:

1. In default value of LDQ10, all the pre-emphasis switches are set to “off”, including global and single-channel switch. The default pre-emphasis strength is the minimum.
2. When enabling pre-emphasis function, global switch should be turned on (Reg0=1F) first of all. Only after that, each channel can be controlled independently.

IV. PACKAGE AND PIN OUT

1. LDQ10 has three kinds of pads in total: Power pads, digital pads, and high-speed data pads. The total number of pads is 42. The over view of all these pads is shown in Fig.9 The pin types are shown in Table VI.



a. The Chip Diagram of LDQ10 b. The Block Diagram of LDQ10P

Fig. 9: The Block Diagram of LDQ10P (unit: mm)

Table VI: Pin Location for LDQ10

Name	Pin Location	Type	Typical Voltage Range
GND	2, 4, 12, 21, 29, 31, 33, 34, 36, 38, 40, 42	Power	0
VDD1V2	5, 28	Power	1.2 V
VDD2V5	1, 3, 30, 32	Power	2.5 V
INN INP	13~20	High Speed	INP/INN: 0.5¬1.1 V
OUT	35, 37, 39, 41	High Speed	1.5¬2.3 V

SCL	9, 24	Digital	1.2 V
SDA	8, 25	Digital	1.2 V
RSTN	10, 23	Digital	1.2 V
DIS	11, 22	Digital	0
A5	7, 26	Digital (address Pad)	0 or 1.2 V
A6	6, 27	Digital address Pad)	0 or 1.2 V

5.1 Power Pads

2. Power pads include ground pads (GND), 1.2 V power pads (VDD1V2), and 2.5 V power pads (VDD2V5). ESD block is added under each power pad for protection as is shown in Fig.10

Fig. 10: ESD under PAD metal

a) Ground Pads (12 in total)

3. There are three kinds of ground pads in total. Four pads are located at the corners of the chip, four pads are placed on the north and south sides of chips, and another four pads are placed next to driver output pads, providing cathode connection for VCSEL array. The sizes of each kind of ground pad are shown in Fig. 11.

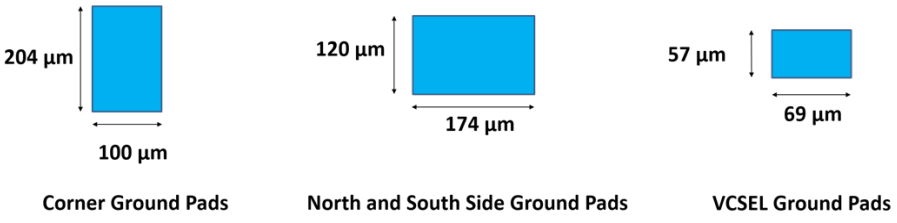


Fig. 11: Three different types of ground pads

b) 1.2/2.5V Power Pads (6 in total)

4. Power pads include 1.2 V and 2.5 V power pads. All these pads are located at north and south side of chip. The size of these pads are the same as ground pads at south edge, as is shown in Fig 12.

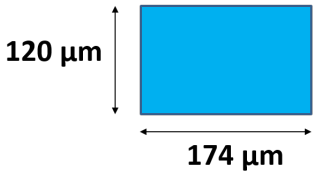


Fig. 12: 1.2/2.5V Power pads size

5.2 High-Speed Data Pads (12 in total)

5. High-speed data input and output pads are using smaller size metal than power pads. Smaller size could reduce parasitic capacitance on the signal path and help ease the limit of speed of laser driver.

6. The input signal are differential, therefore each channel has 2 signal pads at input node. The output of each channel is single-ended, and only one output signal pad is used for each channel (with a VCSEL cathode gnd pad next to it). The input pads are terminated with 50 ohm on-chip resistors. Output pads are directly boned to VCSEL, and impedance, matching are not needed due to short bonding distance.

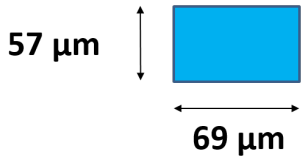


Fig. 1. Fig. 13: High-speed Data Pads

7. The ESD lock of the output signal pad is located under the pad metal, while the input signal path ESD is located near the input of limiting amplifier. The size of high-speed signal data pads is shown in Fig. 13. The ESD protection of high-speed input/output pads are shown in Fig. 14.

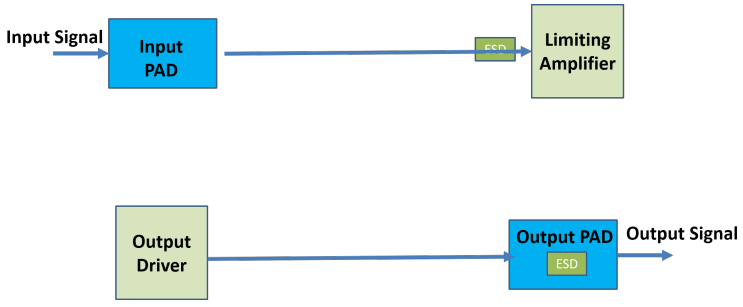


Fig. 2. Fig. 14: ESD protection of high-speed signal pads

5.3 Digital Pads (12 in total)

8. Digital pads include DIS, RSTN, SCL, SCA, A5 and A6.
9. DIS means disable-pad. When the logic value is 1, all the four channels will turn off and the current flow will be reduced to the minimum. RSTN means reset-n. When the logic value is 0, I2C setup are set back to default value. SCL is the clock input and SCA provides the data for I2C block. A5 A6 are I2C address inputs.
10. The digital pads are summarized in the following Table VII. Dimension of the digital pads are shown in Fig. 15.

Table VII: PADs Definition for LDQ10

Name	**IO Type**	**Function Description**
A6	IO	I^2C address, internal pull-down (0)
A5	IO	I^2C address, internal pull-down (0)
SDA	IO	I^2C data, external pull-up to VDD required
SCL	I	I^2C clock, external pull-up to VDD required
DIS	I	Global disable, internal pull-down (0)
RSTN	I	Global reset, internal pull-up (1)

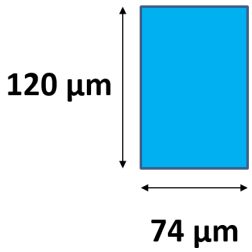


Fig. 3. Fig. 15: Digital pads size

V. Initial Power-Ups

On power-up, the transition detection logic is reset. The power-up default states of all the registers are set according to the Table 7.2.8.The on-chip Power-on Reset (POR) circuit holds

the device in reset until VDD has reached a high enough voltage to deactivate the POR circuit (i.e., release the device from reset). The reset is being kept active by the POR circuit at least for 400 µs. The power on reset time depends on rise time of the power supply line. If the power supply ramps slowly, the reset time may be longer to ensure the proper reset. When the device exits the POR condi- tion (releases reset), digital part of the device should be operational, but this is not necessarly true for the analog part. System designer should ensure that the device operating parameters (i.e., voltage, tempera- ture, etc.) are met. The *RST* (RSTN) input has the same impact on the circuit as internally generated POR signal. An active RSTN signal (low level) voids any I^2C transaction and brings all the registers to default values.

VI. Acronyms

ASIC – Application Specific Integrated Circuit

DJ – Deterministic Jitter

FPGA – Field Programmable Gate Array

Gbps – Gigabits per second

LA – Limiting Amplifier

LD – Laser Diode

LDD – Laser Diode Driver

MMF – Multimode fibre

OMA – Optical Modulation Amplitude

PCB – Printed Circuit Board

Rx – Receiver

SerDes – Serializer/Deserializer

TIA – TransImpedance Amplifier

TJ – Total Jitter

TP – Test Point

TRx - Transceiver

Tx – Transmitter

VII. REFERENCES

[1] T. Zhang, **P. Gui**, S. Chakraborty, T. Liu, G. Wu, P. Moreira, F. Tavernier, "A 10 Gb/s Distributed-Amplifier-based VCSEL Driver IC in 130-nm CMOS," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, Vol. 24, Iss. 7, 2016.

[2] T. Zhang, S. Kulis, P. Gui, F. Tavernier, and P. Moreira, "A Compact Low-power 10 Gb/s VCSEL Driver IC," *Journal of Instruments*, JINST_11_C01015, 2016.

[3] T. Zhang, F. Tavernier, P. Moreira, and **P. Gui**, "A 10 Gb/s Laser Driver in 130 nm CMOS Technology for High-energy Physics Applications," *Journal of Instruments*, JINST_10_C02036, 2015.

[4] T. Zhang, S. Kulis, **P. Gui**, F. Tavernier, P. Moreira, "A Compact Low-power 10 Gb/s VCSEL Driver IC," presented in Proceedings of *Topical Workshop on Electronics for Particle Physics (TWEPP)* 2015.

[5] T. Zhang, F. Tavernier, P. Moreira, and **P. Gui**, "A 10 Gb/s Laser Driver in 130 nm CMOS Technology for High-energy Physics Applications," presented at *Topical Workshop on Electronics for Particle Physics (TWEPP)* 2014.

[6] Z. Zeng, G. Wang, K. Sun, S. Kulis, P. Moreira, and P. Gui, "Compact Low-Power Driver Array for VCSELs in 65-nm CMOS Technology", **IEEE Transactions on Nuclear Science, Vol. 64, Iss. 4, 2017**.

[7] Z. Zeng, T. Zhang, G. Wang, P. Gui, S. Kulis and P. Moreira, "LDQ10: A Compact Ultra Low-Power Radiation-Hard 4X10 Gb/s Driver array," accepted to **Journal of Instrumentation 12 P02020, January 2017, doi: 10.1088/1748-0221/12/02/P02020**.

[8] Z. Zeng, T. Zhang, G. Wang, P. Gui, S. Kulis and P. Moreira, "LDQ10: A Compact Ultra Low-Power Radiation-Hard 4X10 Gb/s Driver array," presented in Proceedings of *Topical Workshop on Electronics for Particle Physics (TWEPP)* 2016.