Final Technical Report (FTR)

Project Title:	Road to Grid Parity through Deployment of Low-Cost 21.5% N-Type Si Solar Cells
Project Period:	09/30/2013 – 09/30/2016
Submission Date:	04/19/17
Address:	5775 Peachtree Industrial Blvd. Norcross, GA 30092
Website (if available)	www.suniva.com
Award Number:	DE-EE0006354
Project Team:	Suniva, Inc. Georgia Institute of Technology
Principal Investigator:	Dr. Vijay Yelundur Senior Manager of Cell Technology Phone: 770-709-5342 Email: vyelundur@suniva.com
Business Contact:	Rachel Delovsky Phone: 770-609-2027 Email: rdelovsky@suniva.com
Technology Manager:	Manav Sheoran
Project Officer:	Thomas Rueckert
Grant Specialist:	Edward Campbell
Contracting Officer:	Diana Bobo

Executive Summary: This project seeks to develop and deploy differentiated 21.5% efficient n-type Si solar cells while reaching the SunShot module cost goal of ≤ $0.50/W. This objective hinges on development of enabling low cost technologies that simplify the manufacturing process and reduce overall processing costs. These comprise of

1. Boron emitter formation and passivation
2. Simplified processing process for emitter and BSF layers and
3. Advanced metallization for the front and back contacts.

In Task 1, process and device modeling was leveraged to refine process windows and expedite rapid process development for emitter formation as well as giving insight into back contact layouts for maximizing device performance. Along with our subcontractor, Suniva successfully fabricated, tested and characterized many cells with efficiencies over 20% made using our baseline process using screen printed contacts on the front and PVD metallization on the rear. Then we modified Task 2 to pursue PECVD AlOx/SiNx as the emitter passivation and ARC film stack. The work plan was modified to procure an automated PECVD tool, develop an optimal passivation and ARC film stack, and prove the cost-effectiveness of the process step. The optimum cell requires significant improvements in recombination in the base and back surface of the cells. This was accomplished in Task 3 through the optimization of the dopant profiles in the back surface field (BSF) complemented with improved passivation of the back surface. Then in Task 4 we optimized the bifacial metallization by optimizing cost and cell performance. In Task 5, we enabled finer line printing through implementation of an improved texturing process that reduced the printed linewidths in conjunction with new screens and pastes optimized for contacting B emitters. Suniva used some of these optimizations and improvements to demonstrate efficiencies greater than 20.0% on 5 cells combining PECVD passivation with bifacial prints. Unfortunately in April 2017 Suniva found itself in a very challenging financial situation and made the decision to terminate this award.

Table of Contents

Background:

This project attempts to develop and deploy a differentiated technology that can achieve the SunShot target of < $0.50/W module. The program goal is to produce 21.5% efficient screen-printed solar cells based on n-type Si wafers. Currently, no company in the world is producing such cells. Two companies, Sunpower and Panasonic, that are mass producing >21% n-type cells utilize the IBC and HIT cell structures which are very expensive to make because of the process complexity and number of steps. These modules are being sold at a price of > $1.20/W, far above the SunShot goal. The technology in this award can exploit the high efficiency and LID free potential of n-type cells without introducing cost. Besides raising cell efficiency, significant effort has been devoted to the challenge of reducing cost by simplifying the process so that the SunShot goal of ≤ $0.50/W can be achieved.

Project Objectives: This project seeks to develop and deploy differentiated 21.5% efficient n-type Si solar cells while reaching the SunShot module cost goal of ≤ $0.50/W.

This objective hinges on development of three enabling low cost technologies that simplify the manufacturing process and reduce overall processing costs. These comprise of

1. Boron emitter formation (via ion implantation or APCVD)and passivation using deposited Al2O3 layers,

2. Simplified processing (co-anneal) process for emitter and BSF layers and

3. Advanced metallization for the front and back contacts using advanced screen printing and alternative metallization for back contacts.

Project Results and Discussion:

Progress against Go/No-Go deliverables

Go/No-Go #1 – Demonstrated NREL verified efficiency >19.0% (95% x 20%) on 5 cells with boron emitters using HVM -APCVD equipment – ***Complete***

A key objective in budget period 1 was to establish and validate a starting baseline for cell performance. Along with our subcontractor (UCEP/GTRC), Suniva successfully fabricated, tested and characterized many cells [[with efficiencies over 20%]] made using the APCVD boron emitter processes from two APCVD equipment vendors and our baseline process. The IV results on 12 such cells tested at Suniva are presented in Table 1 below.

Table 1: Cell IV results measured at Suniva.

Measured at Suniva

Sample ID	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eff (%)
WA4-31	39.0	645.2	79.73	20.08
WA4-33	39.0	648.2	79.97	20.22
WA4-38	39.0	648.5	79.54	20.11
WA1-57	39.3	648.9	79.16	20.17
WA4-84	39.2	647.0	79.05	20.05
WA1-88	39.3	649.4	78.55	20.05
WA4-86	39.1	647.9	79.33	20.08
WA4-32	38.9	645.5	79.8	20.04
WA4-35	38.9	648.3	79.52	20.08
WA4-82	39.1	647.6	79.17	20.03
WA1-85	38.9	649.4	79.38	20.07
WA1-58	39.0	649.3	78.96	20.00
Average Suniva	39.1	648	79.36	**20.08**

These same cells were sent to NREL for verification. Five samples were chosen randomly out of the lot and measured by NREL. The results are tabulated in Table 2. While there is a negative differential between the measurements at NREL and Suniva, the results are consistent with the previously reported differences in such measurements. These results are partly offset by the differences in measurement protocols at NREL and F-ISE since the NREL measurement does not discount the

additional shading losses (reduction in Jsc values) due to the probe bars present during the setup. The Jsc measurements performed at F-ISE are based on Kelvin probe measurements that eliminate any added shading from the probe bars. The extrapolated efficiency shown in Table 2 represents the cell efficiency if the shading loss from the probe bars is neglecting. The extrapolated efficiency [[for each of the five cells tested at NREL is comfortably over 19%, which]] satisfies Go-No Go #1.

Table 2 IV results of 5 randomly chosen samples measured at NREL.

Sample ID	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eff (%)	Extrapolated Eff (%)
NREL WA4-31	37.3	644.7	79.00	19.02	19.24
NREL WA4-33	37.2	646.4	79.16	19.04	19.17
NREL WA4-34	37.2	647.1	78.99	19.03	19.23
NREL WA4-38	37.2	646.4	78.69	18.93	19.18
NREL WA1-57	37.5	647.9	78.36	19.02	19.11

Original PMP Go/No-Go #2 - Demonstrated NREL verified efficiency >19.5% (95% x 20.5%) on 5 cells combining APCVD and PVD for metallization - ***Complete***

Solar cells with a boron emitter formed by ion implantation and anneal, and rear contacts formed by PVD were fabricated and sent to NREL for efficiency verification. Emitter formation by APCVD was not included in these cells since we decided not to pursue the APCVD tool and ceased demo activities with our vendor Ion implantation was chosen as a suitable replacement since we have access to the equipment and supplies on our site. The efficiency of five cells, all of which are greater than 19.5%, is shown in Table 1. We present this data as evidence that we have met Go/No-Go #2 as defined in the original PMP and seek DOE approval.

Table 3: Efficiency of solar cells with an implanted boron emitter and PVD rear metallization as tested by NREL.

ID	area (cm2)	Voc(V)	Jsc (mA/cm2)	FF(%)	Efficiency (%)
A45-77	239.176	0.6585	38.54	80.83	20.53
A34-90	239.124	0.6557	38.44	79.97	20.16
A45-80	239.139	0.6567	38.42	78.98	19.93
A45-86	239.120	0.6540	38.55	81.20	20.47
A45-67	239.178	0.6540	38.44	79.60	20.02

Modified PMP Go/No-Go #2 – Demonstrated NREL verified efficiency >19.0% (95% x 20.0%) on 5 cells combining PECVD Passivation on Implanted Emitters with Bifacial prints– ***In Progress and expected to be completed in time for Continuation Review Meeting***

Samples have been prepared and delivered to NREL for measurement and verification of efficiency. Cells with bifacial prints (using screen print and firing approach) and PECVD passivation of the emitter were prepared at Suniva and sent to NREL for measurement. The cells have a five bus configuration that enables lower Rseries and better performance in accordance with the project goals. This does present a challenge in the measurement as it requires an updated tester setup to probe the five buses concurrently for accurate measurements. Suniva is working with NREL to establish and verify the improved protocols for these measurements. As of Aug. 31, 2015, NREL efficiency verification has not been completed.

Project status

This project seeks to develop and deploy a differentiated technology based on n-type Si that can achieve the SunShot target of < $0.50/W module. The program goal is to produce 21.5% efficient low-cost ion-implanted and screen-printed solar cells. The original work plan included the use of APCVD for diffusion and passivation in conjunction with PVD metallization to meet the technical challenges cost effectively without compromising efficiency. We believe our proposed technology can exploit the high efficiency and LID free potential of n-type cells without introducing cost. The original Statement of Project Objectives was been modified to reflect pathways that overcome two significant obstacles that were encountered in BP2. The first obstacle that was identified was the poor uniformity of the APCVD AlOx/TiO2 front side emitter passivation and ARC. The tool vendor also recognizes this shortcoming but has no short term solution. Thus we choose to abandon APCVD and pursue PECVD AlOx/SiNx as the emitter passivation and ARC film stack instead. The second obstacle in the original plan is the lack of compatibility between PVD and standard module integration. Instead of PVD, we opted for screen printing on both sides with a bifacial print pattern since it is cost effective at current silver prices, and offers a reliable module integration solution.

This project was terminated during BP3 not because of a lack of progress in the project, but due to overwhelming commercial challenges facing Suniva. The subtasks completed in the project are listed below followed by a summary of the accomplishments in each task.

Task 1 – Cell optimization via modeling

Subtask 1.1 - Develop and update calibrated PC1D model using baseline cell parameters
Milestone: Model matches the measured device results (QE, Jsc, Voc, Efficiency) within 1% relative.

Status : **Complete**

Subtask 1.2 *- Model impact of new profiles on FSRV and cell characteristics*
Milestone: Model-derived dopant profile optimized
Status: Complete

Subtask 1.3 –Cross-Validate model with different implant and anneal conditions for both boron and phosphorus
Status: Complete
Subtask 1.4 –Develop 2D device model and quantify the gains in performance
Milestone: Calibrated 2D device model matches device performance with varying back contact geometry
Status**: Complete**

Subtask 1.5 - Combine the measured SRV, dopant profiles and updated parameters (Joe_Metal etc.) and optimize model
Milestone: Doping profile and SRV targets optimized.
Status**: Complete**

Subtask 1.6- Develop and quantify the gains for selectively doped emitter and BSF layers and optimize cell design for best performance
Milestone:
Status: Not complete

Task 1 Summary: In this task, process and device modeling was leveraged to refine process windows and expedite rapid process development for emitter formation as well as giving insight into back contact layouts for maximizing device performance. Process models helped narrow the experimental windows to be tested and 1D and 2D device models aided in setting the right metrics for process improvements and optimization of device/contact layouts. These tools were critical in diagnosing performance limiting issues and enabled the development team to focus on the key challenges.

Suniva through its subcontractor GTRC developed and calibrated a 2D device model for bifacial cells. The model includes the capability to generate the dopant profiles for phos and boron doped layers as a function of process conditions as well as the capability to predict the device performance resulting from a combination of these dopant profiles through a device simulation package. This enables us to simulate multiple process conditions and rapidly determine the optimal process space to focus our experimental development plans. Figure 1 shows the schematic of the bifacial cell configuration used in 2D simulations. Table 4 shows the excellent match between model predictions and experiment results for the same device.

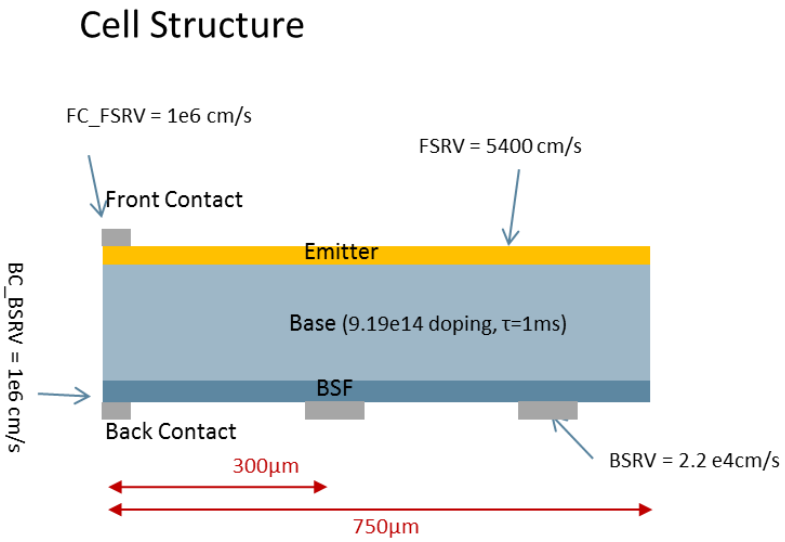


Figure 1: Latest cell structure configuration modeled in Sentaurus.

Table 4: IV parameters predicted by model

ID	Thickness	Voc	Jsc	FF	Eff
Exp.	180	658.8	39.2	81.2	21.0
Model	180	659.5	39.2	81.2	21.0

With this simulation platform in place, GTRC simulated several process conditions to determine how to improve the Joe and Job' through dopant profile optimizations as well as the entitlement of such modifications. Based on different Boron implant and anneal combinations, several Boron emitter profiles were simulated and used in the model to calculate the surface recombination velocity and J0e. The simulated J0e values were in good agreement with measured J0e values for implant and anneal conditions on test structures. As expected, higher Rsheet emitters showed lower Joe values and lower SRV values. It is also known that Boron emitters can be contacted at lower surface concentrations compared to Phosphorus profiles, but it's unclear what the limits are.

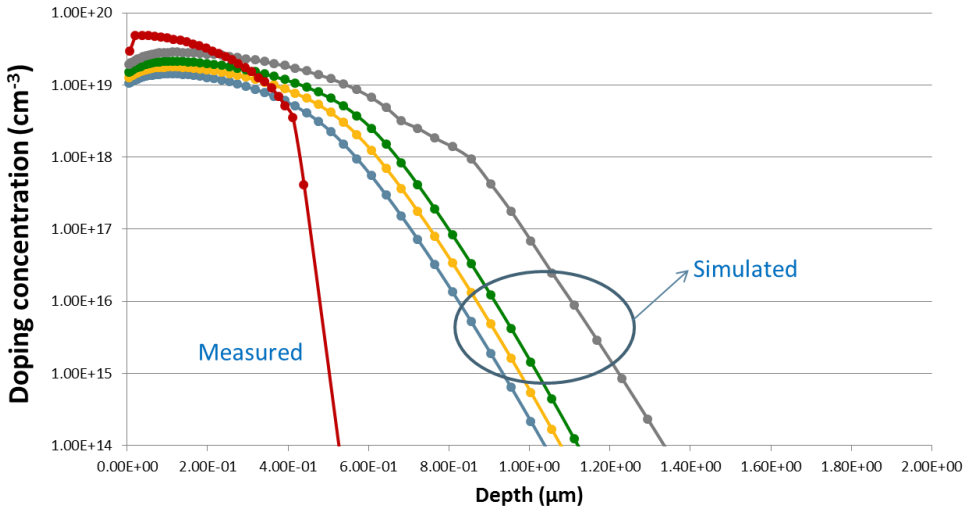


Figure 2: Boron emitter profiles – simulated and measured – with J0e values consistent with measurements on test structures

Table 5: Simulated and measured J0e and SRV values for Boron emitters

Rsheet (ohm/sq)	Measured J_{0e} (A/cm^2)	Surface Recombination Velocity (cm/s)
90	80	5400
157	22	1183
124	28	1487
100	32	1534
71	50~100(expected)	2438

If series resistance dominated by contact resistance becomes an issue for higher sheet resistance emitters, then selective emitters would be required to achieve the desired combination of low J0e and low series resistance.

Similarly series resistance is important for the phosphorus side of the cell as well, especially for the bifacial design that was adopted in this project for manufacturability and cost reasons. It is also desirable to have a co-anneal process instead of a two-anneal process for the same reasons. With these constraints, different phosphorus profiles were simulated using the Sentaurus model and used in conjunction with the measured profile for a two-anneal process that has resulted in a 21% cell. Same as the case was for boron emitters, lighter phosphorus BSF helps in achieving low J0b. But, if contact resistance becomes an issue with lighter doping, selective doping would be required for phosphorus BSF also.

With different combinations of boron and phosphorus layer sheet resistances, selective and homogenous doping and two-step or co-anneal process steps, Sentaurus modeling shows multiple paths towards >21.7% cell efficiency as summarized in Table 6.

Table 6: Simulated data showing multiple paths to >21.7% cell efficiency

Emitter/BSF	Parameters	Two Step Annealing			Co-Annealing	Co-Annealing	Co-Annealing
		Homo B/P (ohm/sq)	Homo B/P (ohm/sq)	Selective B/ Homo P	Selective B / Homo P	Selective B / Homo P	Selective B / Selective P
Emitter (Joe)	B Sheet-rho (ohm/sq)	100~160	70	150/70 (field/contact)	150/70	150/70	150/70
	Joe,field (fA/cm2)	22~32	50	22/50 (field/contact)	22/50	22/50	22/50
	SRV,field (cm/s)	1000~1500	<2500	1000/2500 (field/contact)	1000/2500	1000/2500	1000/2500
BSF (Job')	Sheet-rho	~75	~75	~75	75	130	130/75 (field/contact)
	Job',field (fA/cm2)	<70	<70	<70	<65	<45	45/65
	SRV,filed (cm/s)	<22000	<22000	<22000	<15000	<10000	<10000/<15000 (field/contact)
Required total Rs (ohm-cm2)		<0.4	<0.3	<0.5	<0.45	<0.55	<0.50
Expected Efficiency (%)		>21.7%	>21.7%	>21.7%	>21.7%	>21.7%	>21.7%

Task 2 - Front surface doping, passivation, and anti-reflection coating

Subtask 2.1 – *Integrate APCVD into baseline cell process*
Milestone: 10 cells were fabricated using APCVD and have a Suniva-verified efficiency of >20.0%. 5 of those cells were also independently verified by NREL to be within 5% (i.e. over 19%) of the Suniva measured values.
Status : **COMPLETE**

Subtask 2.2 – Define specifications and procure PECVD tool
Milestone: Suniva will finalize the purchase specifications of the PECVD tool of choice, review with DOE and place PO for the machine.

Subtask 2.3- Transfer Emitter Anneal and Chemical treatment process from UCEP to Suniva Lab
Milestone: Demonstrate Emitter and Passivation quality with Lab process
Status: Complete

Subtask 2.4 - *Process Development: Emitter formation and Passivation process to improve FSRV*
Milestone: Demonstrate Emitter and Passivation quality with Lab process and Joe with metal ≤45fA/cm2
Status: Complete

Subtask 2.5 – Prepare Facilities, construction, environment and safety approvals, install and qualify tool (tool acceptance)
Milestone: Demonstrate film thickness uniformity ≤10% for standard AlOx and SiNx recipes qualified onsite as verification of purchase specifications being met satisfactorily. Present results of tool qualification to DOE.
Status: Complete

Subtask 2.6 - Optimize process parameters for deposition of PECVD AlOx/SiNx
Milestone: AlOx/SiNx Stack optimized for implanted B emitter (Rsheet between 60-120ohm/sq) with weighted average front reflectance <5%. NREL verified average efficiency ≥19.3% (95% x 20.3%) from 5 cells; Suniva-verified average efficiency of 20.5% from at least 50 cells.
Status: Not Complete

Subtask 2.7 - Demonstrate Production compatible process for emitter passivation with PECVD tool
Milestone: Tool throughput > 2400wph, front side ARC uniformity<7% (within wafer, wafer to wafer within batch, batch to batch between cleaning cycle)
Status: Not Complete

Task 2 Summary:
The original work plan for this task involved leveraging APCVD to innovate three important aspects of the cell architecture: emitter doping, front surface passivation, and anti-reflection coating. However, the work plan was modified to reflect pathways that overcome two significant obstacles that were encountered in BP2. The first obstacle that was identified was the poor uniformity of the APCVD AlOx/TiO2 front side emitter passivation and ARC. The tool vendor also recognizes this shortcoming but has no short term solution. The task was modified to pursue PECVD AlOx/SiNx as the emitter passivation and ARC film stack instead and the work plan below has been modified (Subtasks 2.2 to 2.7) to procure an automated PECVD tool, develop an optimal passivation and ARC film stack, and prove the cost-effectiveness of the process step. As part of our initiative to find alternative passivation solutions to APCVD tool, we sent out samples to a PECVD vendor for AlOx/SiNx passivation and demonstrated that the alternative approach helps us achieve the goal of Joe <45fA/cm2 for industrial emitters. The results of this evaluation on symmetric test structures is shown in Figure 3 and 4

and confirm that PECVD indeed can deliver the uniformity and passivation quality needed for our application.

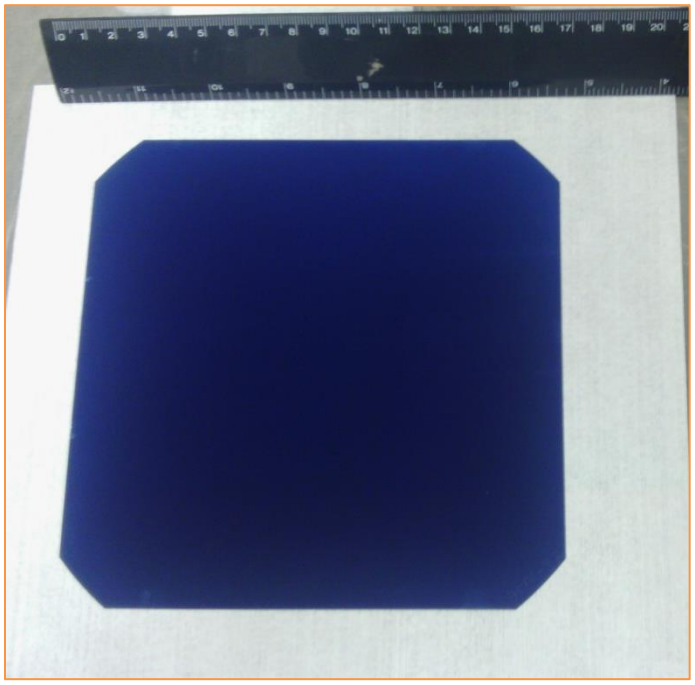


Figure 3: PECVD AlOx/SiNx stack layer deposited in HVM PECVD equipment demonstrating the good cosmetic uniformity required for front side application.

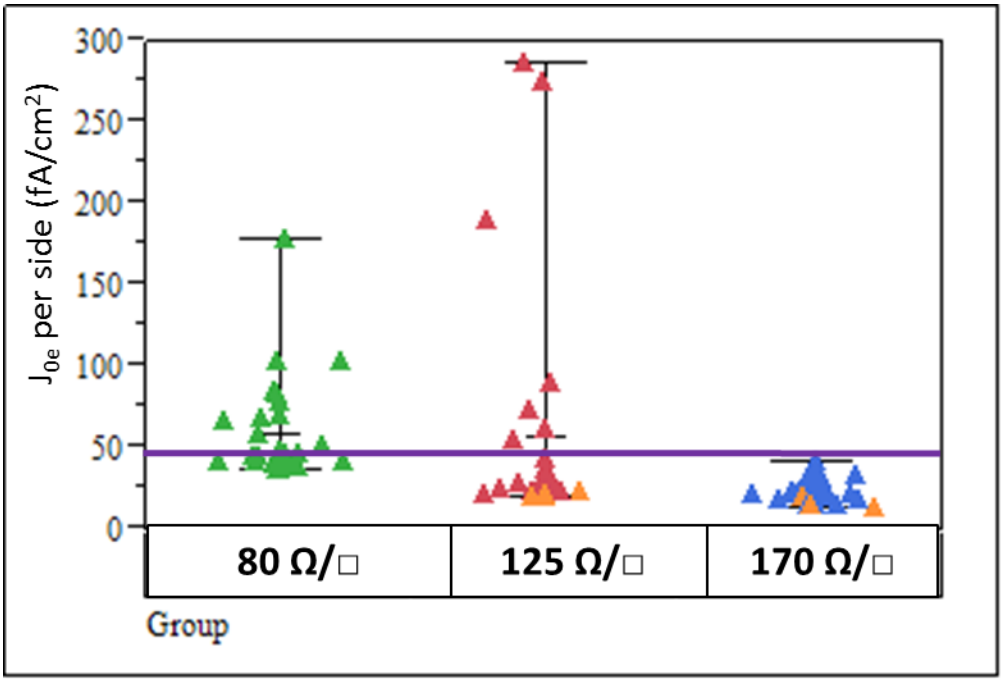
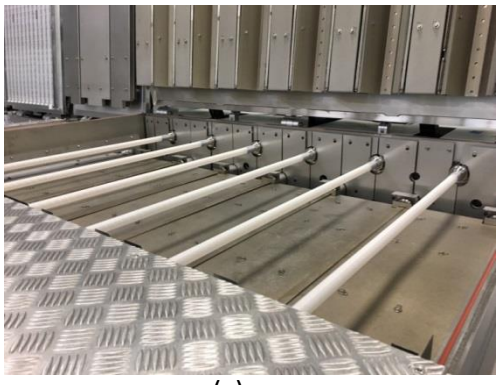


Figure 4: Joe $\leq$ 45fA/cm2 with PECVD AlOx/SiNx stack demonstrated on symmetric structures with different emitter dopant profiles.

The PECVD tool has been placed and the vendors have completed installation, startup, and signoff. Pictures of the tool can be seen in Fig.5 showing the integrated tool with all modules opened (a), the inside of the AlOx process module (b), the inside of the SiNx process module (c), and a wafer transport tray in the tray loading station (d).

(a)

(b)



(c)

(d)

Fig. 5: PECVD tool for deposition of AlOx and SiNx layers.

Task 3 – Back Passivation, P BSF Profile, and Base Optimization

Subtask Task 3.1 - Analyze Baseline cells to determine Job (with Metal) components for BSF
Milestone: Established methodology to determine Jo components
Status: Complete

Subtask Task 3.2 - *Optimize Dose and Anneal combination to improve Job*
Milestone: Minimized Job for PERT with Job <= 200fA/cm2
Status: Complete

Subtask 3.3 - Establish/Qualify wafer resistivity/lifetime requirements compatible with selectively doped layer and order material
Milestone: Validate material specs with vendor by demonstrating 20% bifacial cell efficiency and order material.
Status: Complete

Subtask 3.4– Determine the optimum metal coverage for lowest Rseries and Job_Metal
Milestone: Finalized BSF (Selective or Homogenous) and metal contact pattern for a screen printed -bifacial cell that results in Job≤120 fA/cm2.
Status: Complete

Task 3 Summary:
The optimum cell requires significant improvements (reductions) in recombination in the base and back surface of the cells. This was accomplished through the improvements and optimization of the dopant profiles in the back surface field (BSF) complemented with improved passivation of the back surface. This task hinges on accurate measurement of the recombination induced by the metal (J_{0metal} or J_{0b_metal}). In order to determine this value we varied the metal fraction contacting the silicon and extract the recombination parameter (J_{0cell}) from the illuminated I-V results. We extracted these values both using mini-cells and the Suns-Voc method and also using full area cells. The advantage of the Suns-Voc method is that it is easier to span a large space in terms of process variables because each wafer spans a large range of metal contact fractions (F_{metal}) typically from about 5% up to about 40%. It has the disadvantage that it does not encompass the entire wafer and could be skewed by some local defects which pull down the entire cell V_{oc}, but not on individual sections of the wafer. To remedy this problem, we used entire cells with different numbers of gridlines on the rear (180, 270, or 360), which correspond to approximately 9%, 12% and 15% metal coverage on the rear (phos-implanted) side of this device. The full area cells were fabricated and I-V results measured under 1 Sun. Then we calculated J_{0cell} from the measure J_{sc}, V_{oc}, and temperature using this relationship:

$J_{0cell} = J_{sc} * \exp(-qV_{oc}/kT)$ where q = the charge on the electron, k = the Boltzmann constant, and T = the temperature in Kelvins. The results are plotted in Figure 3 below.

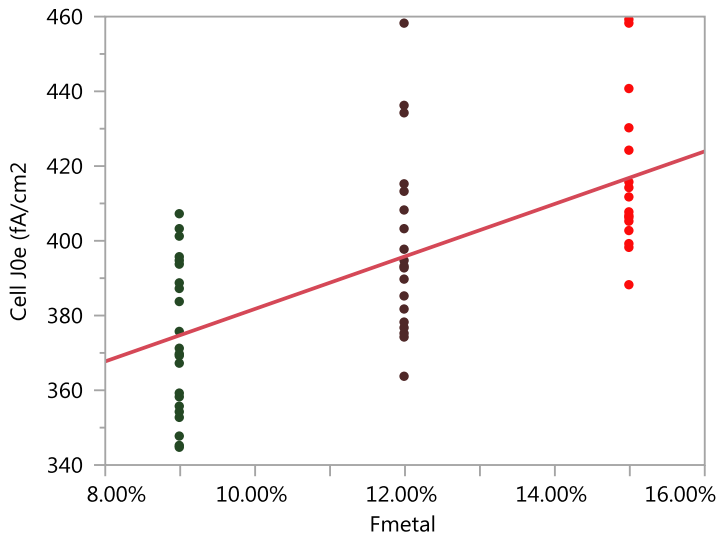


Figure 6: Results from the full area devices with different metal coverages.

Each dot represents a different cell. The red line is the linear least squares fit to all of the data. It has a slope of 700 fA/cm^2 per % F_{metal}.

The data shown in Figure 6 allow us to determine J_{0b_Metal} on the phosphorus-implanted side of our devices. From previous discussions we know that we can write the J_{0cell} parameter as an area-weighted average of the various recombination components of the cell:

$$J_{0cell} = J_{0e}*(1 - F_{metal}) + J_{0metal}*F_{metal} + J_{0,other}$$

$$J_{0cell} = F_{metal}(J_{0metal} - J_{0e}) + J'_{0,other} \qquad \text{re-group terms of } F_{metal}$$

$$\text{Slope} = J_{0metal} - J_{0e} \approx 700 \text{ fA/cm}^2 \qquad \text{From Figure 3 above}$$

We have already determined J_{0e} from measuring lifetime on symmetrically implanted samples. We have measured this value at a variety of doses, but in this case we use only the value at $3.4 \cdot 10^{15}$ cm^{-2} of 110 fA/cm^2.

J_{0metal} = 700 + 110 ≈ 810 fA/cm^2 for this a phosphorus dose of $3.4 \cdot 10^{15}$ cm^{-2}.

We now need to know the functional dependence of J_{0metal} on implant dose in order to model the results and determine whether we can achieve $J_{0b} \leq 120$ fA/cm^2. We already have this data for J_{0e}. Here we assume that the functional dependence is the same as was determined for the Suns-Voc results.

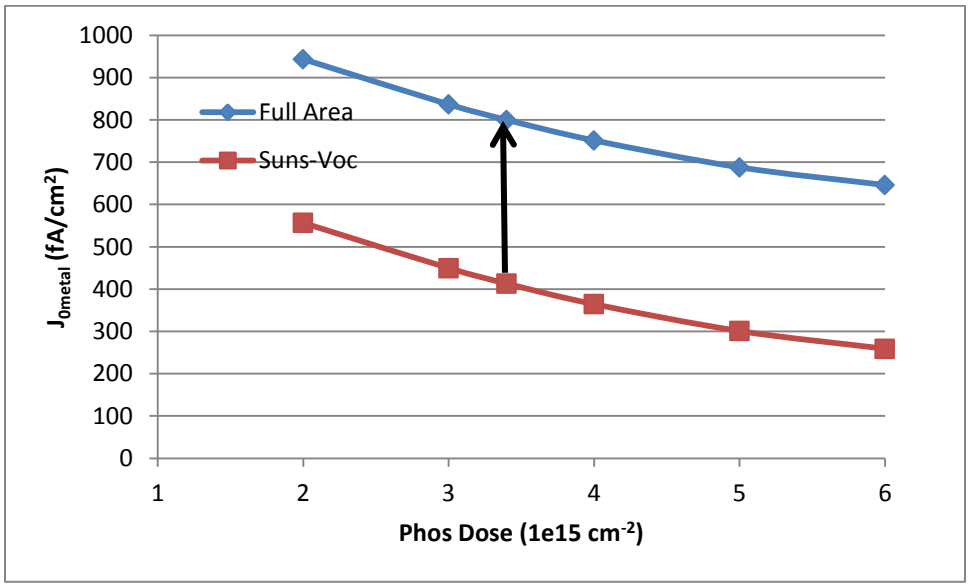


Figure 7: Assumed functional dependence of J_{0metal} on implant dose.

The Suns-Voc data were measured and the full area cell results are modelled except at the 3.4e15 cm^{-2} dose level. We simply add the difference between the two curves at 3.4e15 to the Suns-Voc curve.

Once we incorporate these findings into our model, we can predict the cell performance at any dose.

Table 7: Model assumptions

Parameter	Value
Fritless busbars	No extra series resistance
	No recombination
Selective BSF	1.6e15/2.4e15 cm^{-2} field/selective dose
Front implant	1.8e15 cm^{-2}
Passivation	SiO_2/SiN_x (no AlO_x)
# Front Gridlines	100
# Rear Gridlines	130
Busbars	Five busbars, each 0.8 mm wide
Selective BSF width	300 µm
J_{0base}	25 to 50 fA/cm^2
Gridline width	50 to 65 µm

Table 7 above shows the assumptions used in the model. We have also varied the number of rear gridlines. In order to make our goal of $J_{0b} \leq 120$ fA/cm^2, we must make one assumption which is only partially justified. In a previous task we achieved gridline widths of 50 µm and we have used this width in the model results presented below.

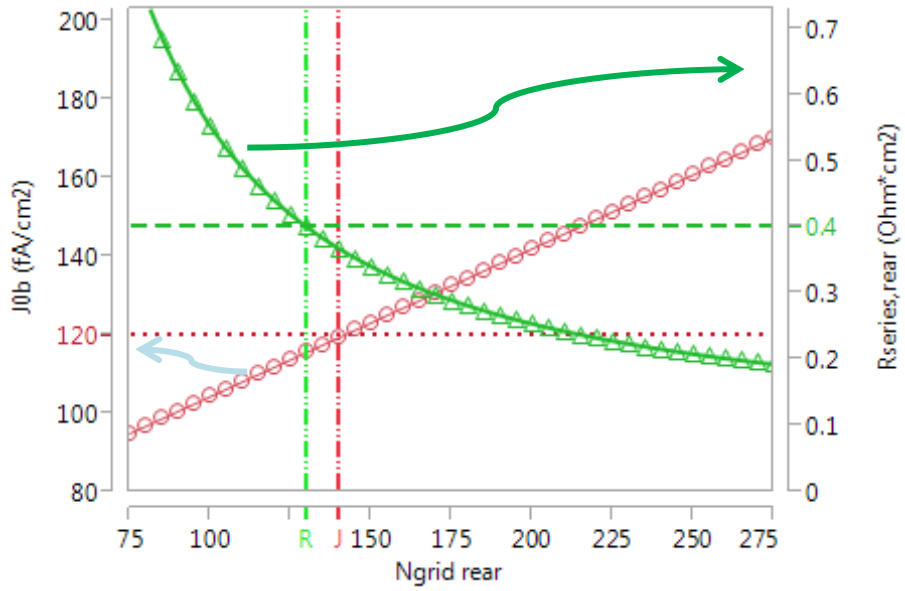


Figure 8: Model results with the recombination (J_{0b}) on the left hand axis and the red line and the rear series resistance in green and on the right hand axis.

For a rear number of gridlines between 130 and 140, we achieve both our goals of r_{series} < 0.4 Ω·cm^2 and J_{0b} ≤ 120 fA/cm^2.

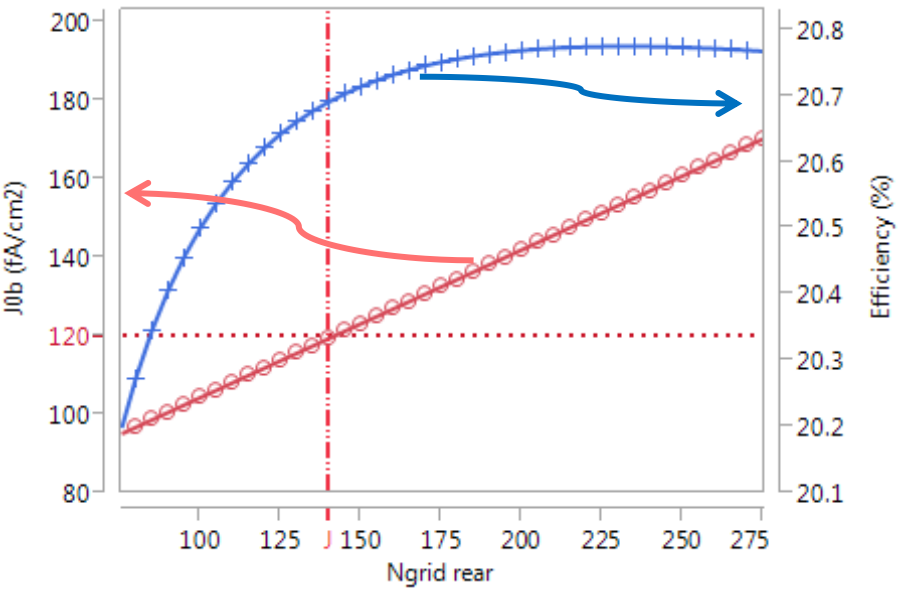


Figure 9: Job and efficiency as a function of the number of grid lines on the rear.

At 130-140 gridlines we would achieve an efficiency of 20.7% and this would increase to nearly 20.8% if we increased to about 240 gridlines.

Task 4 – Back surface metallization via screen printing

Subtask 4.1 *– Design and optimize the laser ablation process*
Milestone: Established high-volume manufacturing compatible laser ablation process and finalize the approach for integrating laser ablation into the process flow.
Deliverable: Presentation to DOE of data and definition of the requirements for high volume manufacturing compatible laser ablation process

Status: Complete

Subtask 4.2 *– Demonstrate PVD capability on low-volume tool*
Milestone: Data Collected. Deliverable: Presentation to DOE, with pull strength on metal stack meeting Suniva Spec of >1.0 N/mm and Rseries for Cell <0.8ohm.cm2

Status: Complete

Subtask 4.3– Design and Optimize (lowest Cost/Wp) back metal pattern for homogenous or selective BSF
Milestone: Bifacial Metal Pattern Optimized with Rseries contribution from back metal + BSF <0.4 Ω.cm2

Subtask 4.4 – Select between Single vs Dual print approaches optimized for selective (or homogeneous) BSF layers
Milestone: Select and qualify pastes for Front and back prints. Finalize a bifacial print configuration that targets <350mg Ag weight on the cell.

Task 4 Summary:

The original work plan for Task 4 involved the developed of PVD metal films on the back surface to form the back contact with low Job'. However, we found a lack of compatibility between PVD and standard module integration. We viewed screen printing on both sides with a bifacial print pattern as a suitable alternative to PVD since it is cost effective at current silver prices, and offers a reliable module integration solution. After modification of the project, optimization of the bifacial metallization was included in Subtask 4.3 and 4.4. We designed the back surface metallization layout by optimizing cost and cell performance. The following was determined for each component of the series resistance:

- Base resistivity will be in the range 1-7 Ω·cm and thus the resistance from the base will be 0.13 $\Omega \cdot cm^2$ or below.
- Gridlines have a line resistance of approximately 1.8 Ω/cm. For 120 gridlines this translates to about 0.17 $\Omega \cdot cm^2$.
- The sheet resistance goes as the inverse square of the number of gridlines and should be about 0.1 $\Omega \cdot cm^2$ for a sheet resistance of 70 Ω/□.
- Together these pieces sum to approximately 0.4 $\Omega \cdot cm^2$ (slightly more for 7 Ω·cm and slightly less for 1.0 Ω·cm material).

We fabricated cells with 360 gridlines on the rear which have well below the goal of 0.4 $\Omega \cdot cm^2$.

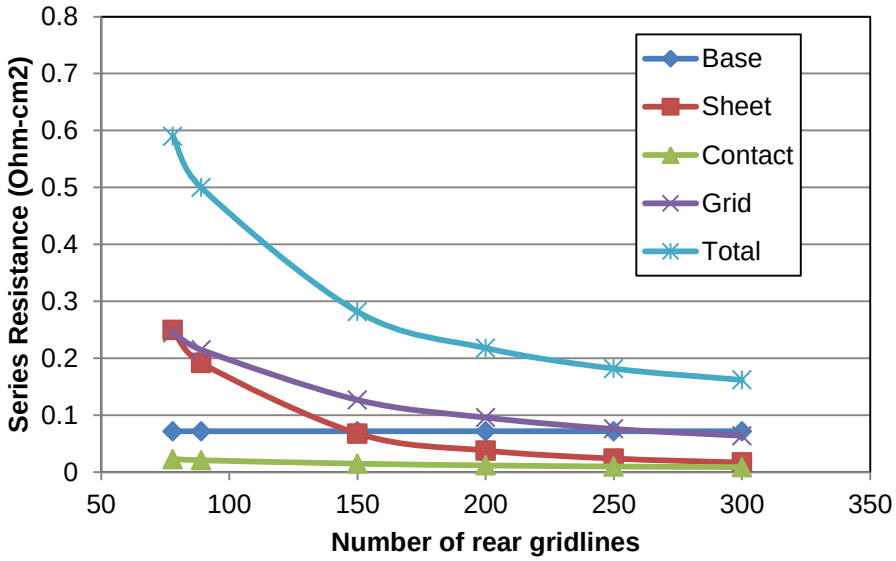


Figure 10: Decrease in the components of the rear series resistance as a function of increasing number of gridlines. A base resistivity of 4 Ω·cm is used for this calculation.

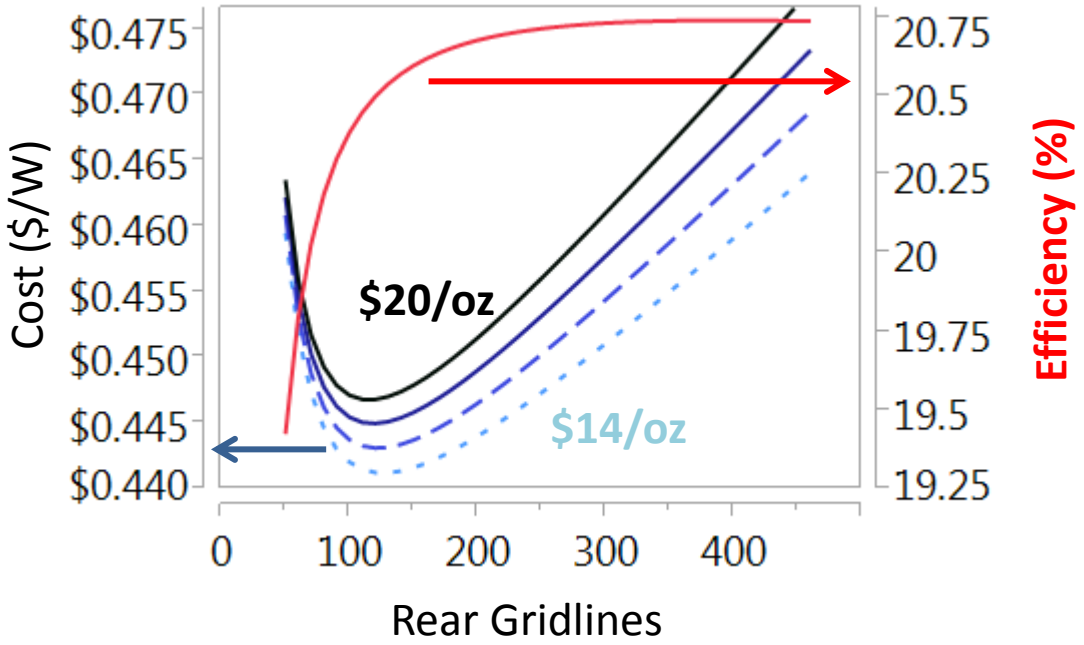


Figure 11: Cell efficiency and cell conversion cost as a function of the number of rear gridlines (in red, on the right hand axis). Conversion cost is also calculated as a function of silver price.

Figure 11 shows the efficiency as a function of the number of rear gridlines (in red, on the right hand axis). It also shows the conversion cost of the solar cell as a function of the number of rear gridlines for silver at $14/oz up to $20/oz in $2/oz increments (in blue/black on the left hand axis). At $14/oz silver the cost of this process per Watt is a minimum at about 130 gridlines. Beyond that the efficiency gains are outweighed by the cost of the silver in the extra gridlines. The minimum cost is approximately 44.1¢/W_p. At higher silver prices the cost minimum shifts slightly to fewer gridlines. For instance at $20/oz the optimum occurs at 120 gridlines.

Task 5 – Front surface metallization via screen printing optimization

Subtask 5.1 – Improve baseline screen printing performance

Milestone: Established process to reduce shading and line spreading on textured samples to reach printed line width of 85+/-5um.

Status : **Complete**

Subtask 5.2 – Improve Texturing process (reduce size), upgrade screens to enable fine prints

Milestone: Implement new processes, test/validate performance in production, and demonstrate printed line widths of 70+/-5um.

Status: Complete

Subtask 5.3 - Qualify new texture process to enable fine line printing

Milestone: New Texture process with pyramid sizes less than 4 um that meets production requirements

Status: Complete

Subtask 5.4 - *Evaluate new Pastes/screens optimized to take advantage from the improved texture process*

Milestone: Select and qualify pastes for front side contact formation (and limit the increase in printed Linewidth after firing to <5um)

Status: Complete

Subtask 5.5 –Optimized screen printing process

Milestone: Present the results validating the screen printing improvements measured by demonstrating printed line widths ≤50±5μm and front metal coverage =6% with a step processing cost ≤$0.07/Wp (assuming Ag price <$30/t.oz.)

Status: Complete

Task 5 Summary:

The focus of Task 5 is to enable finer line printing through implementation of an improved texturing process that reduces average pyramid size ≤4μm and enables a reduction in printed linewidths in conjunction with new screens and pastes optimized for contacting B emitters. The texture pyramid size in manufacturing was ~9 um, which does not support fine line screen printing and the line width targets in this project. We conducted a DOE around the texture process in the R&D wetbench, identified a new chemical additive, and established conditions that result in a texture pyramid size of 3-4 um. This process has been rolled out to production wet benches with production fully transitioned to the new texturing additive

Figure 12 below shows data for first long pilot run on bath 1 showing excellent control over etch depth for bath age up to 600 (60000 wafers). Samples were picked periodically to validate pyramid size. Profilometer images of these samples are shown in Figure 13.

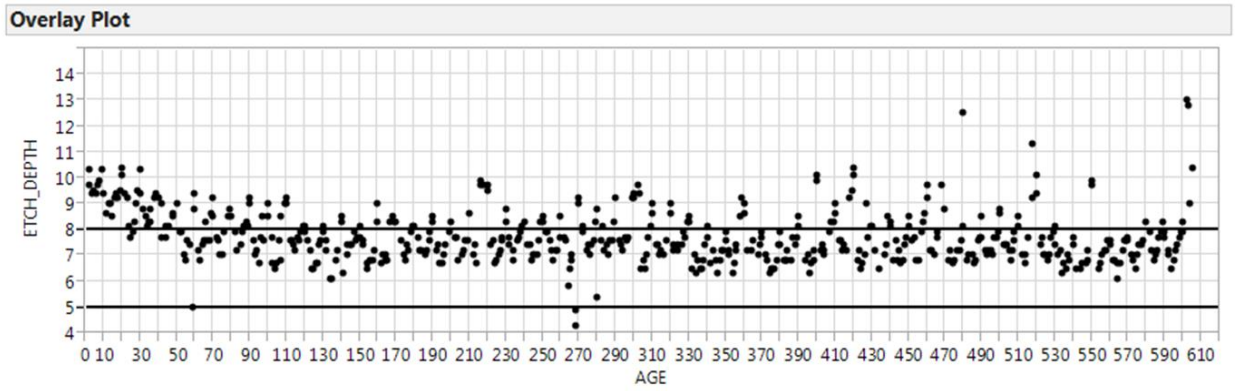


Figure 12: Etch depth as a function of bath age.

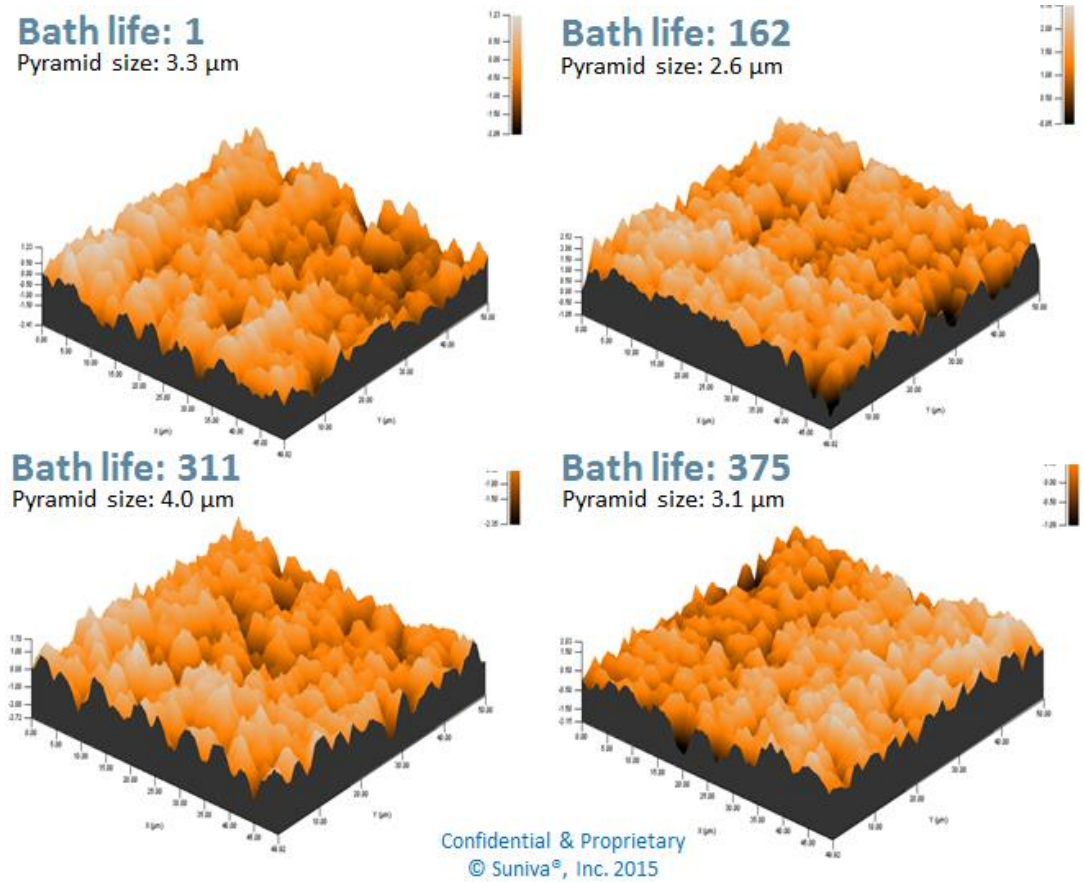


Figure 13: Profilometer images of wafers at different bath ages showing pyramid size <4µm

In combination with the new texturing process, we tested new pastes that enable finer line printing and much reduced paste spread. We identified pastes for both Boron and Phosphorus contacts that limit the spread in line width between printing and firing to less than 5um. In addition, by optimizing the screen mesh and EOM conditions, fired line widths of 50um were achieved for both pastes.

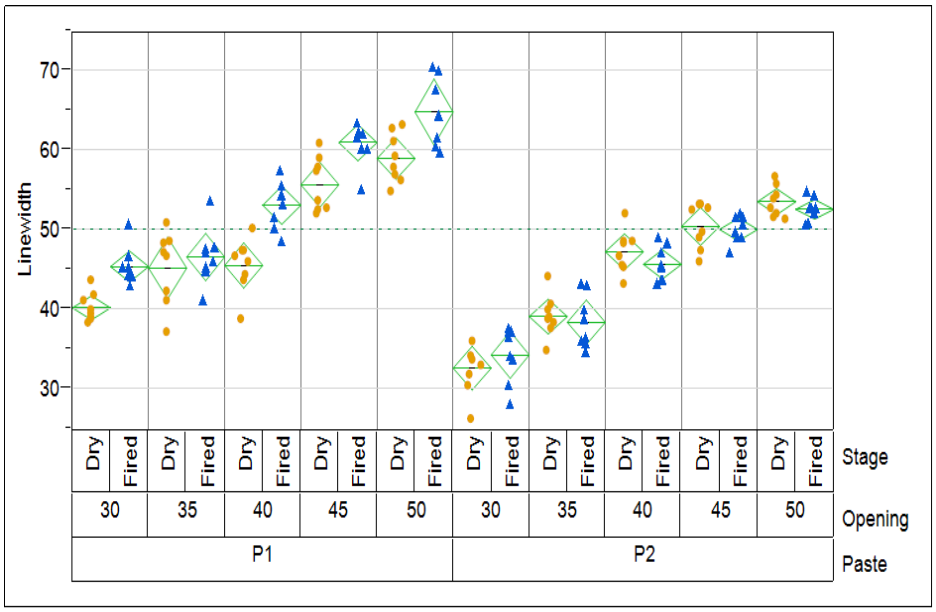


Fig. 14: Comparison of line widths after print and after firing for phosphorus pastes.

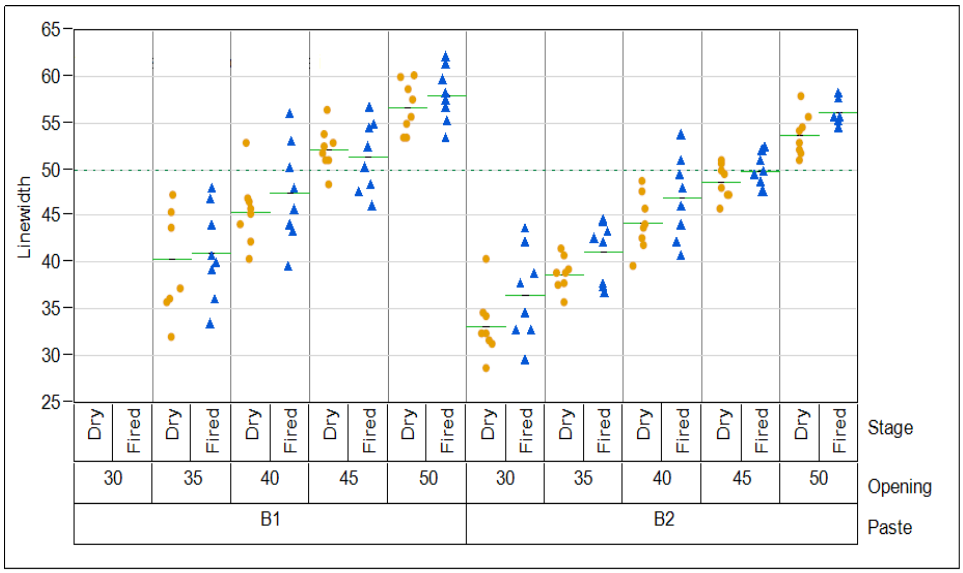


Fig. 15: Comparison of line widths after print and after firing for boron pastes.

As shown in the Fig. 14 and 15 above, we have identified new paste formulations that do not spread much between print and firing. As it can be seen, except for paste P1, other pastes do not show any significant increase in line width after firing. However, even with pastes P1, by reducing the opening in the screen, fired line widths of 50um can be achieved. For all pastes, screen openings in the range of 40-45um are optimal to achieve fired line widths of 50um.

Task 6 – HVM demonstration with Front and back process integration and demonstration via module production

Subtask 6.1– Validate CoO and CoC for PECVD processes for B Emitter Passivation

Milestone: Demonstrate >2400wph processing capability with production system and verify that the processing cost for the PECVD step is ≤$0.02/Wp

Status: Not complete

Subtask 6.2– Marathon cell production run (150 kW, 30k of 239 cm2 cells)

Milestone: Pilot production validation with at least 30000 cells produced on 6" pseudo-square substrates with production targets of median cell efficiency ≥ 20.9% (5 W per cell) and Cell Electrical Yield ≥95% (minimum cell efficiency = 19.5%) in addition to the actual costs of pilot manufacturing line as the final deliverable of this project.

Status: Not complete

Subject inventions developed: None

Significant Accomplishments and Conclusions:

- Developed and calibrated process and performance models to define seven device structures capable of reaching >21.7% cell efficiency.
- Identified that the poor uniformity of the APCVD AlOx/TiO2 front side ARC does not meet customer requirements. The tool vendor also recognizes this shortcoming but has no short term solution.
- Identified a chemical additive, and established conditions that result in a texture pyramid size of 3-4 um. Process was rolled out to production wet benches and manufacturing lines have been fully transitioned to the new texturing additive.

Inventions, Patents, Publications, and Other Results: None

Path Forward: N/A

References: None