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PROBLEMS

SUMMARY
THE IMPLEMENTATION OF SOLID STATE SWITCHES IN A PARALLEL CONFIGURATION TO GAIN OUTPUT CURRENT CAPACITY IN A HIGH CURRENT CAPACITIVE DISCHARGE UNIT (CDU)

MARIO CHAVES

UNIVERSITY OF NEW MEXICO
SCHOOL OF ELECTRICAL AND COMPUTER ENGINEERING

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1 Part 1 Circuit Simulation

1.1 Introduction

For my project I have selected to research and design a high current pulse system, which will be externally triggered from a 5V pulse. The research will be conducted in the region of paralleling the solid state switches for a higher current output, as well as to see if there will be any other advantages in doing so. The end use of the paralleled solid state switches will be used on a Capacitive Discharge Unit (CDU). For the first part of my project, I have set my focus on the design of the circuit, selection of components, and simulation of the circuit.

1.2 Requirements

First, I would like to list some of the design requirements. Each of these requirements could pertinent in the end use of a High Current CDU. The final circuit will meet the following requirement criteria:

1. The High Current CDU will be triggered by an external 5V pulse
2. The High Current CDU will be charged by a maximum of 3KV DC voltage source
3. The High Current CDU will be able to deliver a minimum of 1KA peak
4. The High Current CDU will deliver a minimum of 1µs pulse width
5. The High Current CDU will be capable of delivering the stored energy into a low impedance load
6. The High Current CDU driver circuit will be powered by a 5V DC source

1.3 Design and Component Selection

1.3.1 Solid State Switch Selection

For the circuit design process, I shall begin by selecting a solid-state switch that will be capable of delivering a current pulse of greater than 1KA from the capacitor, then into a low impedance load. This solid-state switch will have a low propagation time from low to high (T_{PLH}). I have researched Insulated-Gate Bipolar Transistors (IGBT) and found that they have high current throughputs- the IXYS IGBT (P/N: IXEL40N400) had a specification of I_{CM} = 400A, for a maximum of 1ms and a low T_{PLH}. However, I selected the IXYS BiMOSFET (P/N: IXBL60N360) due to its greater current capability of I_{CM} = 720A. Furthermore, I selected the BiMOSFET because of its lower required gate voltage (V_{GE}) to reach the maximum current rating. See below specifications for I_{CM} and V_{GE} from their datasheets.

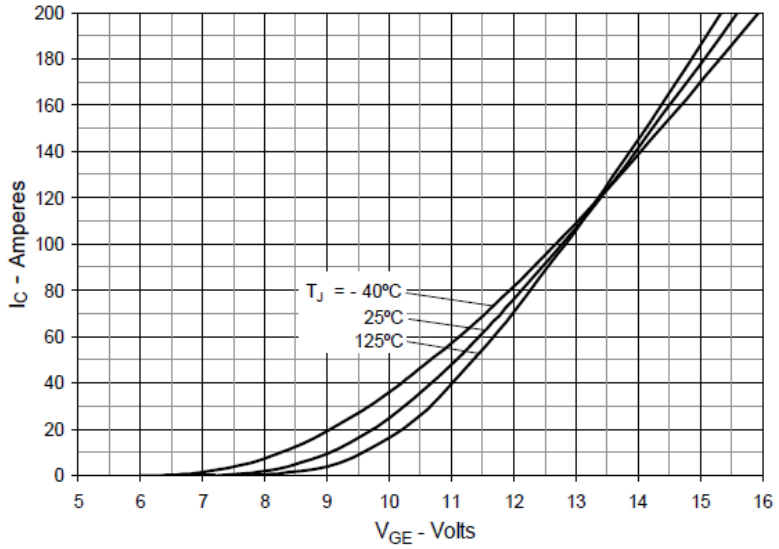
I_{C25}	T_C = 25°C	90	A
I_{C110}	T_C = 110°C	40	A
I_{CM}	Pulse Width Limited by T_{JM}, 1ms, V_{GE} = 25V	400	A

1.3.1.1 Current capability of IGBT IXEL40N400

I_{C25}	T_C = 25°C	92	A
I_{C110}	T_C = 110°C	36	A
I_{CM}	T_C = 25°C, 1ms	720	A

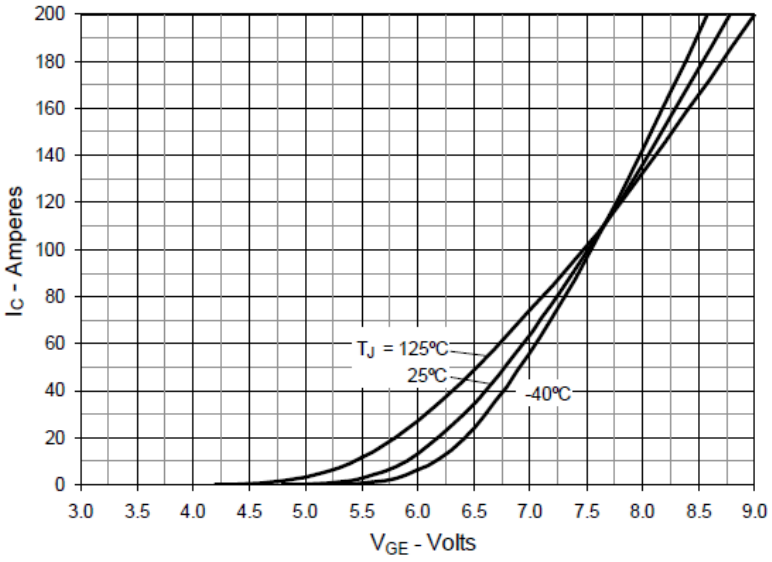
1.3.1.2 Current capability of BiMOSFET IXBL60N360

Fig. 6. Input Admittance



1.3.1.3 I_C versus V_{GE} of the IGBT IXEL40N400

Fig. 6. Input Admittance



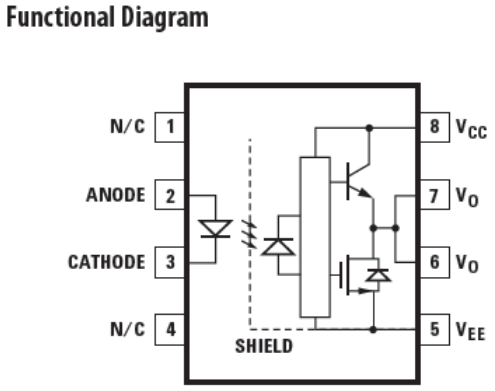
1.3.1.4 I_C versus V_{GE} of the BiMOSFET IXBL60N360

1.3.2 DC/DC Converter Selection

The next step was my selection of the 15V DC converter, which was sourced by the 5V DC. This power supply is a boost converter that will convert the 5V DC input into a 15V DC regulated output. For this application I've selected a Recom DC/DC converter (P/N: RKZ-0515S) that is capable of delivering 2W to the load. This converter was designed for IGBT driver applications.

1.3.3 High Speed Gate Drive Selection

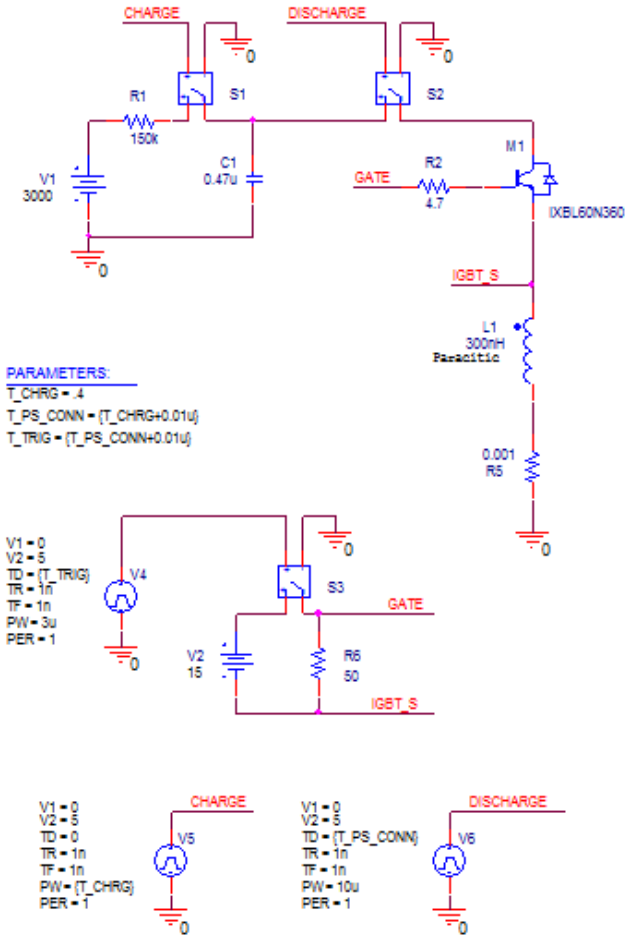
The next component selection was a high speed gate driver. For the driver I wanted to use an optocoupler, so that the external trigger source would be isolated from the pulse circuit. For this reason, I selected a high speed gate drive optocoupler from Avago (P/N: HCPL-3180). I preferred this gate driver because of its high speed response and its low pulse width distortion of 20ns.



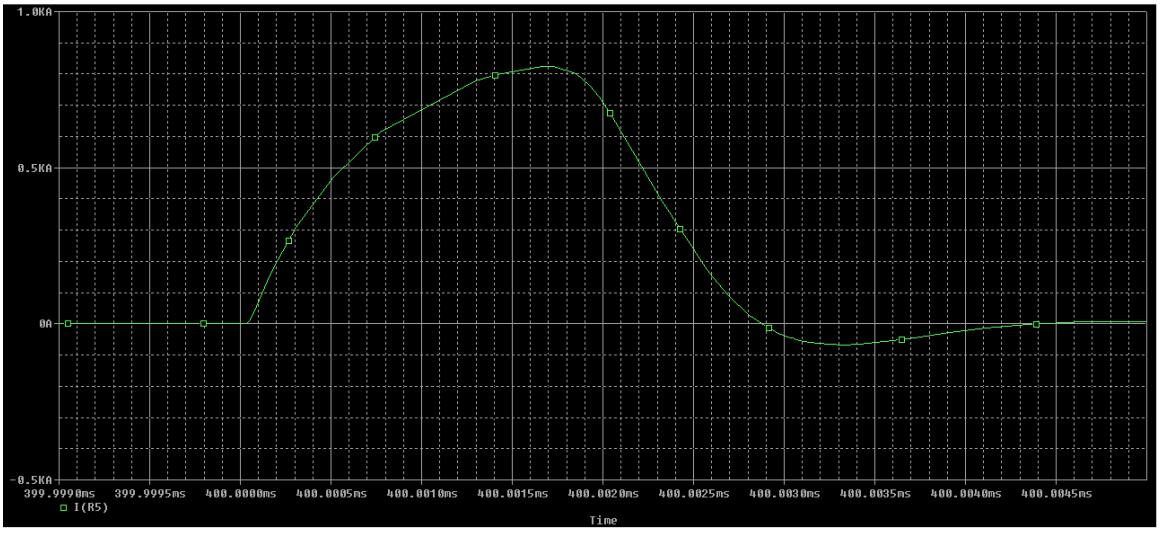
1.3.3.1 Avago high speed gate drive optocoupler

1.4 Schematic Capture and Simulation

Now having selected the major components of the CDU, capturing the circuit schematic and simulating it were my next steps. I started my research with a single BiMOSFET for discharging the capacitor into a low impedance load, and once that was accomplished, I had the ability to expand it into additional BiMOSFETs in parallel. I was also able to get a model for the BIMOSFET from IXYS. For the purpose of simulation, I feel that the major part of my research was directed toward the advantages of utilizing the BiMOSFETs in a parallel fashion. I designed circuitry, which for the most part, only took into account the capacitive discharge of the CDU with the BiMOSFETs into the low impedance load. For my simulations, I used a 3KV charging source and a 0.47μF capacitor. I also put in series between the power supply and capacitor a 150KΩ charge limiting resistor. My rational for this, is because of the power supply I will be using is a 120W supply, and it will crowbar if the current limit of 20mA is exceeded. Lastly, I placed a 1mΩ resistor for the load and a 300nH inductor to accommodate for any inductive parasitics in the output connection. See the below figures for the circuit configuration and current output waveform.



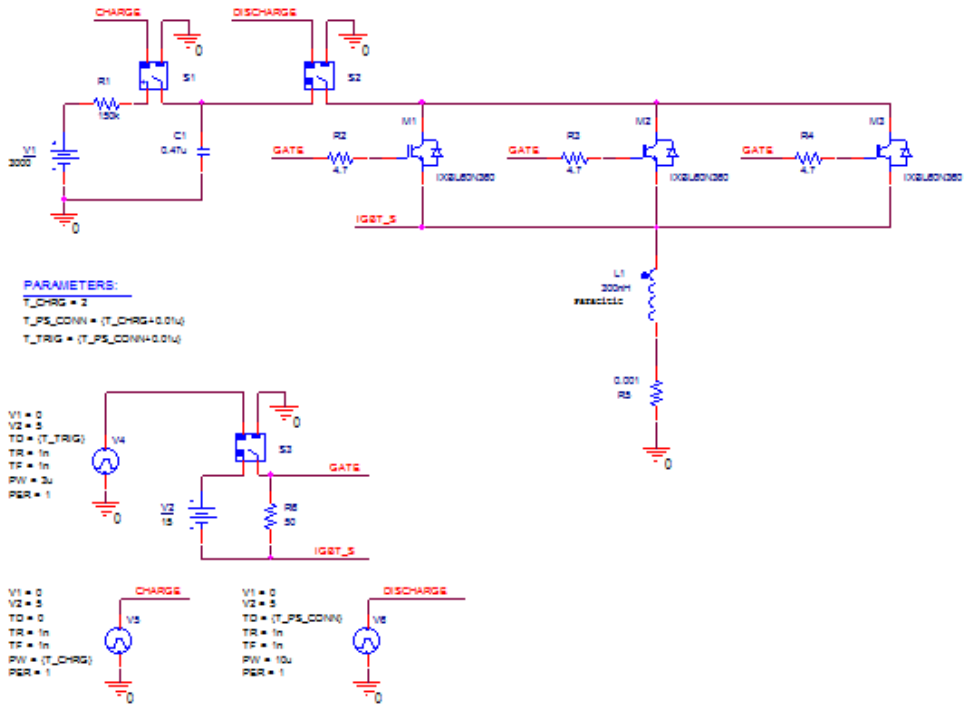
1.4.1.1 Single BiMOSFET CDU Circuit



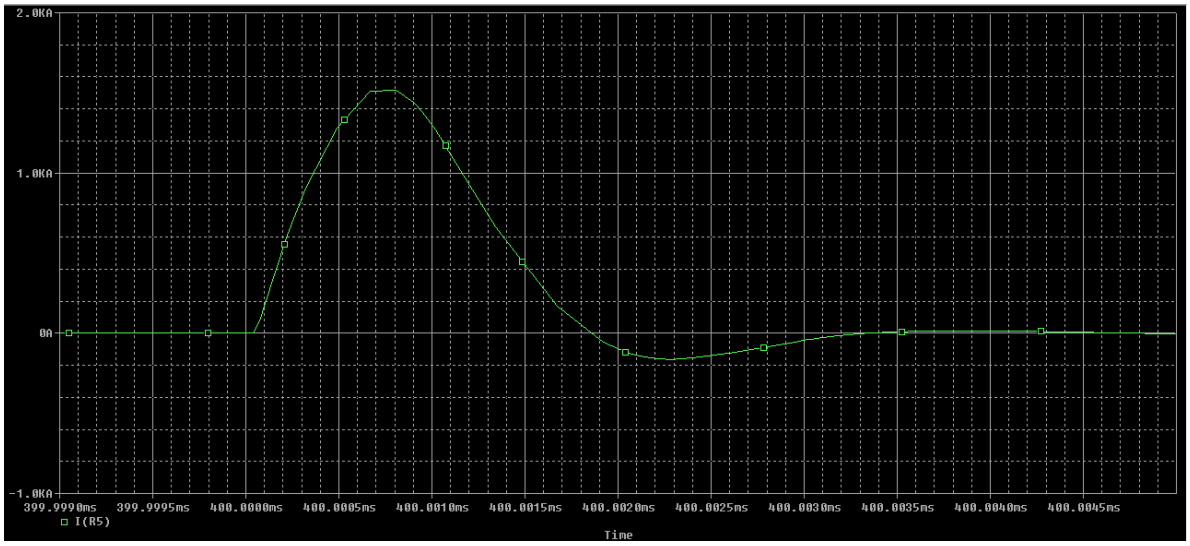
1.4.1.2 Single BIMOSFET CDU Circuit Simulation Current Output

The simulations from the single BiMOSFET CDU showed a max output current of 824.57A. The simulations also showed a rise time of 1.102µs and a pulse width of 1.945µs. These simulations are very promising to the capability of BiMOSFETs being used for the CDU application.

After the successful single BiMOSFET simulations, I added two more BiMOSFETs in parallel with the first and re-ran the simulations. See the below figures for the circuit configuration and current output waveform.



1.4.1.3 Paralleled BIMOSFET CDU Circuit



1.4.1.4 Paralleled BIMOSFET CDU Circuit

The simulations from the paralleled BiMOSFET CDU showed a max output current of 1.517KA, a rise time of 502.424ns, and a pulse width of 1.087µs.

1.5 Part 1 Conclusion

According to the simulations, the use of the BiMOSFETs in both the single and paralleled configurations, for the use in a high current pulse system, is very plausible. By connecting three BiMOSFETs in parallel the maximum current output increased by 84% and the rise time decreased by 45%. The pulse width shortened due to the same amount of energy being dissipated at a faster rate. Therefore according to my simulations, all of my requirements have been met with substantial margin. The pulse width can be increased or decreased by changing the capacitance in order to store more or less energy. These results proved (in simulation) that by adding additional BiMOSFETs in parallel, you can increase the current output capacity and reduce the rise time.

2 Part 2 Introduction

During the second part of my project, the discharge capacitor was selected; a Printed Circuit Board (PCB) was designed, fabricated, and tested. The test results were compared to my original simulations and requirements to see if the final design proved that the hypothesis of a higher current output capability could be achieved by paralleling BiMOSFETs in a High Current Capacitive Discharge Unit (CDU).

2.1 Final Circuit Design and Component Changes

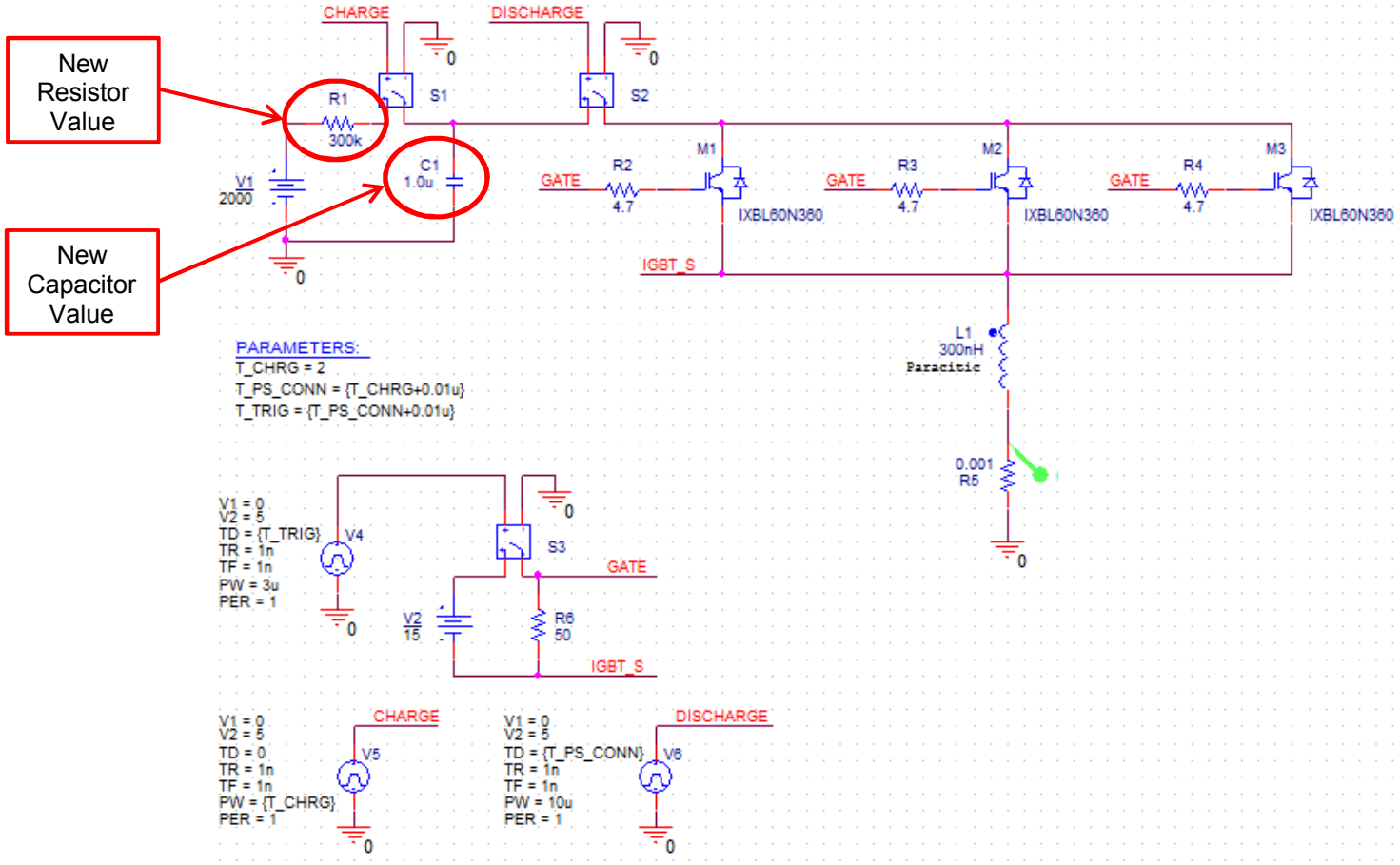
The High Current BiMOSFET CDU circuit was designed with components found at common electronic component distributors. Due to the lack of availability, some components changed value or parameters from the circuit designed in the first part of the project.

2.1.1 Discharge Capacitor

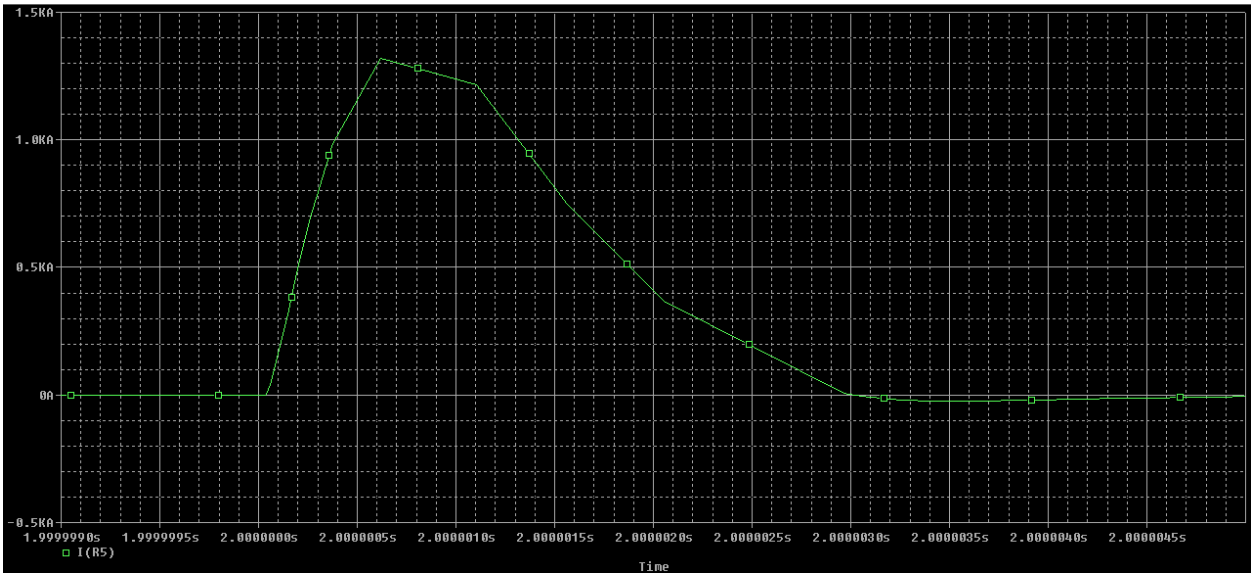
For the discharge capacitor, I chose a capacitor comprised of a Polypropylene dielectric material because its typical applications include high power and pulse discharge. The discharge capacitor value changed from the original design due to the availability of high voltage Polypropylene capacitors did not include the 0.47uF value from my original design. Instead of the 0.47uF, I selected a 1.0uF capacitor from Cornell Dubilier Electronics (P/N: 940C20W1K-F). Secondly, I decided to add a second set of discharge capacitor pads on the circuit board to accommodate any changes to the design if it did not meet the set requirements (Otherwise the part will remain uninstalled on the circuit board).

2.1.2 Current Limiting Charge Resistor

The current limiting charge resistor value was changed due to distributor stock availability. The original 150KΩ value was selected because the high voltage power supply I will be using had a max current output of 20mA. Using Ohms Law $V = I * R$ then, $R = \frac{V}{I}$ and $\frac{3KV}{20mA} = 150K\Omega$. Instead of stressing the high voltage power supply, I chose the available 300KΩ High voltage resistor from TE Connectivity passive components (P/N: HB1300KFZRE). This value would give a maximum charge current of 10mA and a charge time of 1.5 seconds. The charge time was calculated by 5τ, Where τ is the R*C time constant and$5\tau = 5 * 300K\Omega * 1\mu F = 1.5\ seconds$. This charge time seemed to be reasonable as I do not intend for the high current pulse system to be used in a highly repetitious fashion. See the figures below for the adjusted simulation schematic and current output.



2.1.2.1 Adjusted simulation of the Parallel BiMOSFET CDU Circuit



2.1.2.2 Current Output of the Adjusted Parallel BiMOSFET CDU Circuit

The adjusted simulations from the paralleled BiMOSFET CDU delivered a max output current of 1.320KA, a rise time of 437.373ns, and a pulse width of 1.446µs. These results still meet/exceed the original requirements.

2.2 Printed Circuit Board (PCB) Design

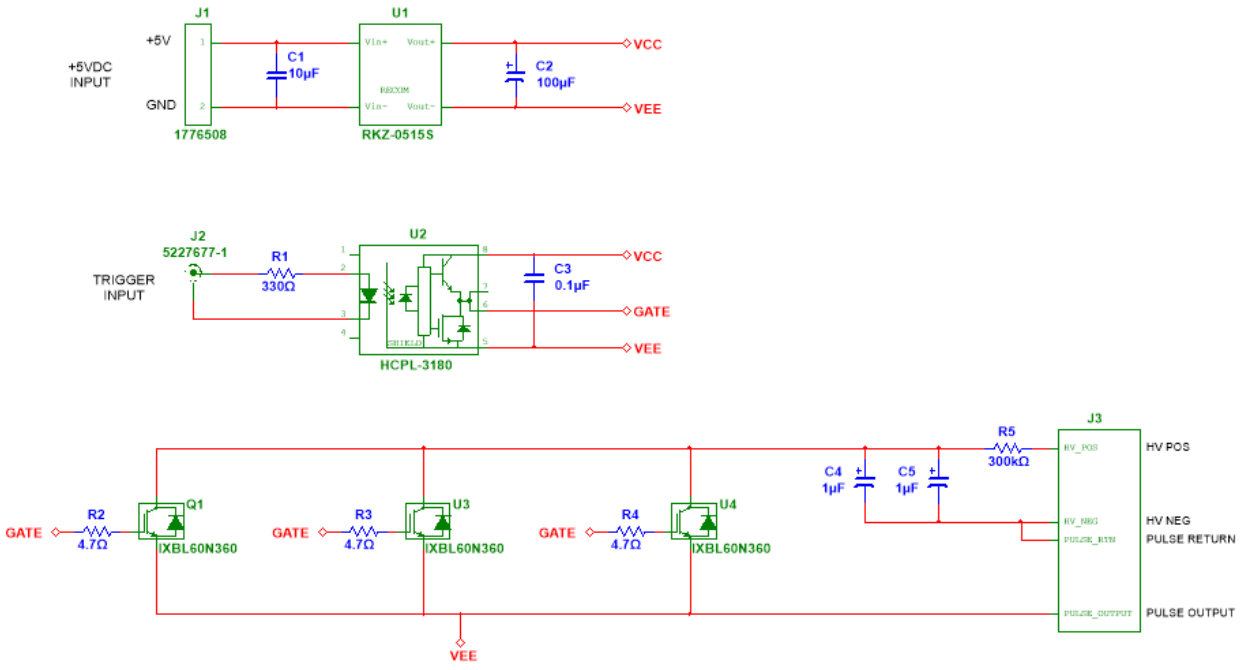
I was not able to export the netlist from the ORCAD/PSPCIE simulation software I used in part 1 of the project into a format that the circuit board layout software packages I have were able to read. Therefore, I chose the National Instruments (NI) Multisim for schematic capture and Ultiboard for the circuit board layout. I chose the NI package because I have the software at my disposal and it is easy to use.

2.2.1 Additional Components

Additional components were added to the circuit per the datasheet circuit requirements for nominal operation. These components include decoupling capacitors and gating resistors (shown in below schematic).

2.2.2 Schematic capture

In order to capture the circuit schematic in Multisim, I used the components datasheets to create their respective circuit symbols and footprints to build the parts. See the Multisim schematic capture below.

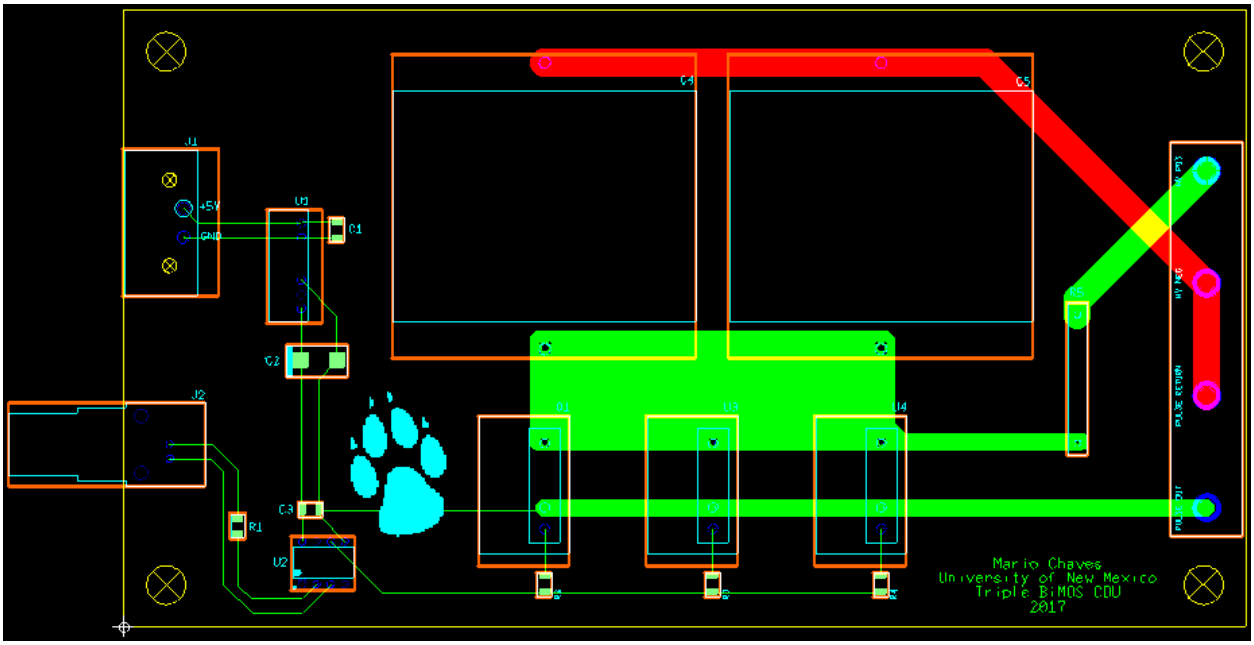


2.2.2.1 National Instruments Schematic Capture

2.2.3 Circuit Board Layout

While designing the High Current BiMOSFET CDU circuit board there were some parameters I needed to take into consideration. These parameters are loop inductance, trace widths, component placement and spacing. In order to keep loop inductance at its minimum the discharge capacitors and BiMOSFETs were placed as close to each other as possible keeping in mind the required high voltage standoff distance. The copper traces used in the high current/voltage section were 3mm in order to attain maximum ampacity and still keep minimum standoff distance. The copper traces in the trigger section were 0.5mm since it did not require high current or high voltage. A BNC connector

interface (P/N: 5227677-1) was used for the external trigger pulse input since it is a common pulse system interface. For the external +5VDC external supply that powers the DC/DC converter, the Phoenix contact (P/N: 1776508) terminal block was chosen because it would easy to adapt to any +5V source. As for the High voltage input and high current pulse output, I used screw terminal holes because I could not find circuit board mountable high voltage connectors.



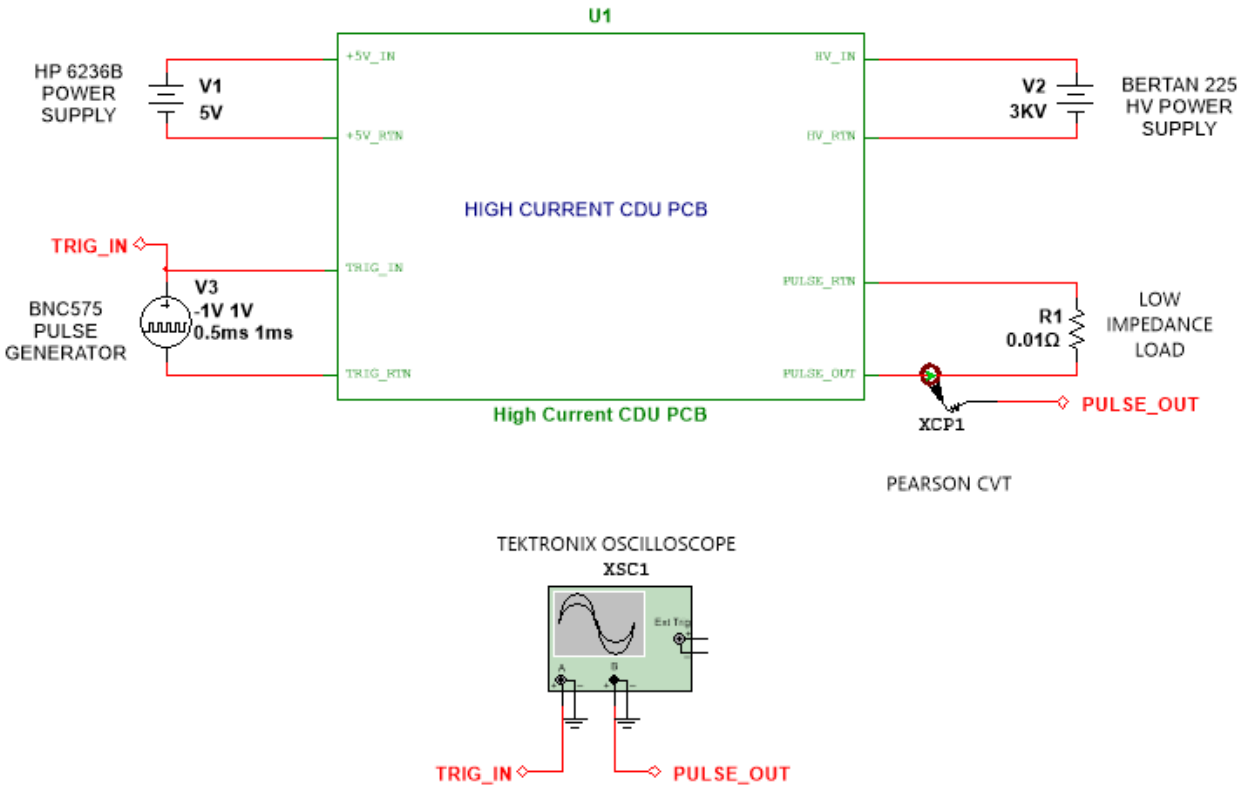
2.2.3.1 National Instruments Ultiboard PCB Layout

2.3 Pulse circuit testing and comparison

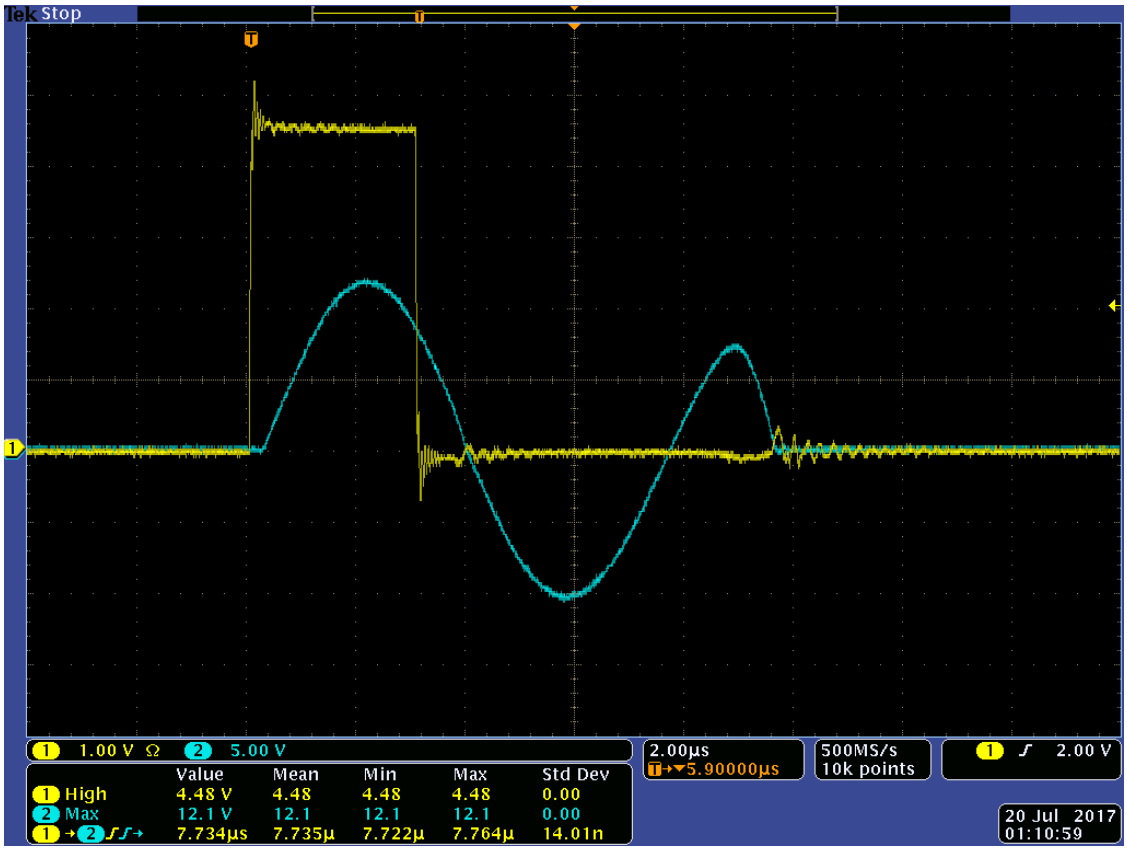
In order to test the High Current BiMOSFET CDU I will use the following test equipment:

- Bertan 225 series 3KV programmable power supply
- Berkeley Nucleonics BNC575 pulse generator
- HP 6236B Triple output, +6V adjustable power supply
- Tektronix DPO4034B 350MHz, 2.5Gs/s oscilloscope
- Pearson Model 110 (0.01V/A) Current Viewing Transformer (CVT)

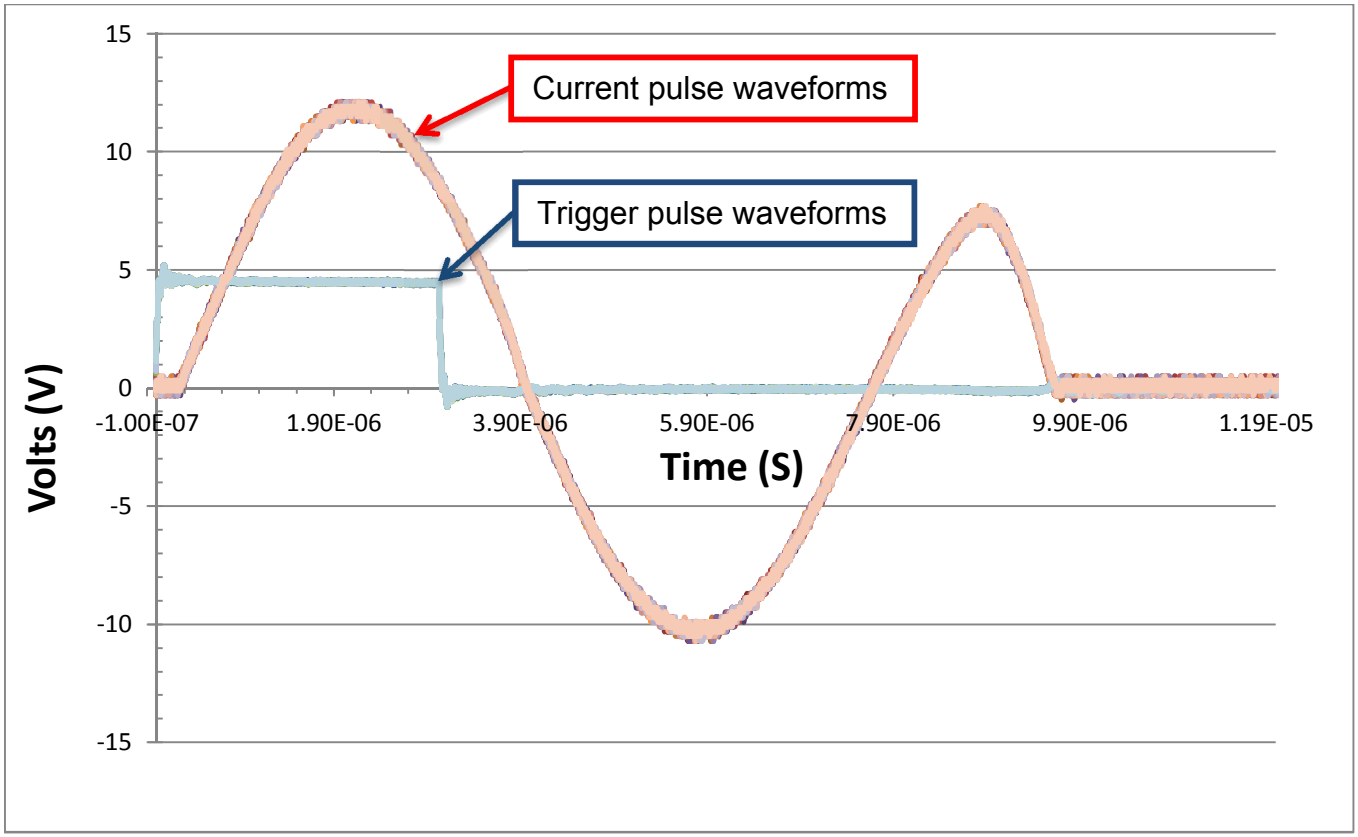
After connecting the test equipment and also connecting a 0.01Ω resistor load to the CDU circuit board per the CDU test setup, I programmed the BNC575 pulse generator to output a 5V pulse with a 3µs pulse width. Next, the Tektronix oscilloscope channel 1 was set to 1MΩ, 1V/div, and full bandwidth. Channel 2 of the Tektronix oscilloscope was set to 1MΩ, 5V/div, and full bandwidth. The Tektronix oscilloscope was also set to a horizontal resolution of 2µs/div with a single shot trigger from channel 1 at a threshold of 2V. Lastly, the Glassman power supply was set to 1.5KV and maximum current (20mA) output. See below test circuit for connections to the circuit board.



2.3.1.1 CDU Test Setup



2.3.1.2 Single pulse from High Current CDU



2.3.1.3 CDU Output: 30 pulse overlay

A total of 30 pulses were captured and plotted in Microsoft Excel for waveform overlaying. In the above waveform plots, the current pulse waveforms were measured and scaled using a Pearson 0.01 V/A CVT so the waveform could be viewed on the oscilloscope. This means the actual output current amplitude is 100 times larger than the plot displays. Using Microsoft Excel, the Maximum current on all 30 waveforms was 1.21KA. At 50% of the maximum current output or 605V, I calculate 68ns of jitter with a standard deviation of σ=0.124. I also measure 1.27μs of rise time and 2.47μs of pulse width. The rise time was slower and the pulse width was wider than my simulations but this could be due to my output connections having a higher inductance than originally believed for the simulations.

2.4 Part 2 Conclusion

In conclusion, although there were differences from the simulations to the actual built circuit, the output current waveforms from the BiMOSFET High Current CDU met all set requirements. After reviewing the results from testing the final High Current BiMOSFET CDU by paralleling BiMOSFETs, the circuit proved that it is a viable solution to attaining a High Current CDU. The design presented here met and exceeded the set requirements and is capable of delivering a high current pulse to a low impedance load with outstanding performance.