SAND2016-7073PE

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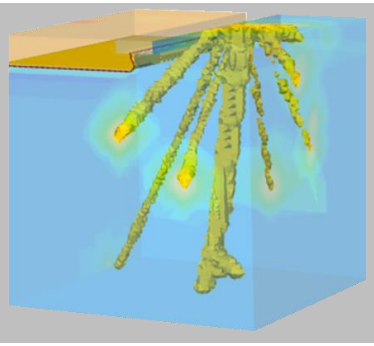
CHARON

Xyce™ PARALLEL ELECTRONIC SIMULATOR



Happy Flag Day

Single Event Effects in Sandia's CMOS7 Devices and *Acceptance* Testing in Integrated Circuits

Lawrence C Musson

Dolores Black

Jeffrey Black

U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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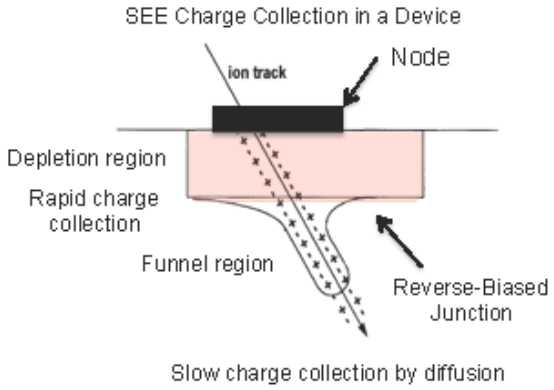
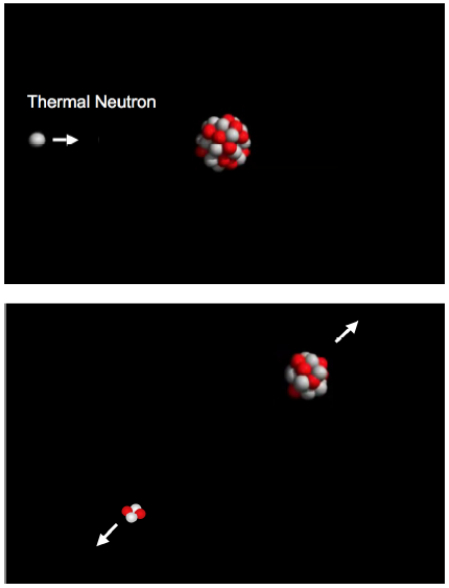
Case Study – CMOS7 Eiger Platform

- NW Single Event Environment
  - Direct ionization from heavy ions during flight
  - Indirect ionization from heavy ions, protons, and neutrons
- CMOS7 Eiger Platform Mitigation
  - Harden logic gates with linear energy transfer (LET) onset of upsets > XX MeV-cm^2/mg
    - Semiconductor elements from nuclear reactions has LETs < XX MeV-cm^2/mg
    - W (contact plugs) has higher LET but exists over highly doped regions with low charge collection efficiency
  - Design Implementations
    - Increased drive transistors and higher nodal capacitance – density impact
    - Resistive feedback – density and timing impact

Direct ionization from heavy ion



Nuclear reaction in semiconductor, leading to ionization



Case Study – CMOS7 Eiger Platform

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- Eiger V5 (Production version) was completed after 5 iterations including the initial platform prototype V0
  - 3 iterations were the result of designs attempting to meet radiation requirements while improving performance – evaluated after fabrication
  - Each iteration took 1 year and cost at least $XX
  - Next Generation Platforms in CMOS8 face same and new challenges
  - Memory element radiation hardening versus performance optimization
    - Same as Eiger issue described above
    - Increased importance since hardening techniques used in CMOS7 do not scale well
  - Standard logic cell layout
    - Commercial logic cell use innovative layouts that have larger Si islands, but save on overall density
    - The layouts have larger charge collection volumes and increased body contact resistance (both bad for single event effects)
    - We are not likely to take the risk without a validated predictive modeling option

*Proposed effort would enable design trades to optimize IC performance while meeting radiation requirements and validate designs prior to fabrication.

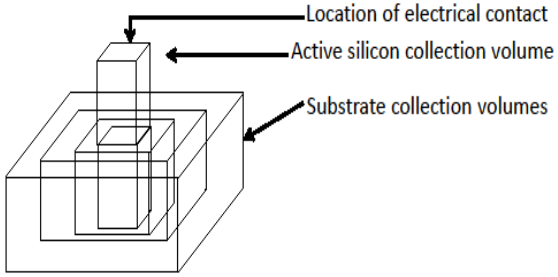
The Team

Sandia National Laboratories

- **Jeffrey Black**
  - Circuit designer for Sandia for 5 years with more than 12 years of prior experience.
  - 15 years of researching single event effects and developing mitigation approaches.
  - Currently leading Sandia's development of CMOS8 circuit designs to meet radiation requirements
- **Dolores Black**
  - Circuit analyst for Sandia for 3 years working with Xyce with more than 15 years of prior experience as a Circuit and ASIC designer.
  - More than 10 years experience as a System/Design Verification Engineer.
  - Researching Single Event Effects for 8 years working with MRED.
- **Lawrence Musson**
  - Charon developer for more than 10 years and a Xyce developer for 5 years.
  - Developed software to model drift-diffusion and associated models in semiconductors.
  - Has developed all the neutron radiation models for Charon 2.
- **Patrick Griffin**
  - Sandia Senior Scientist
  - Consultant to this LDRD
- **Vanderbilt**
  - Ron Schrimpf
    - Director, Institute for Space and Defense Electronics
  - Graduate student

High Altitude View

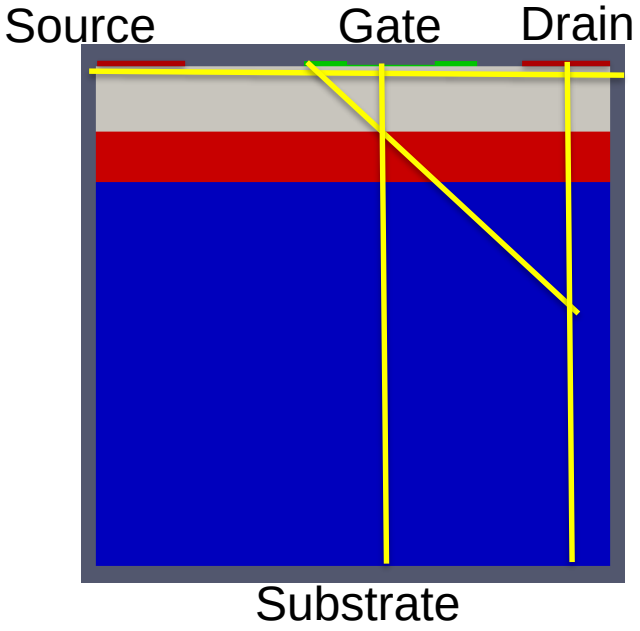
- **We anticipate a union of tools & activities to satisfy the goals of what we intend in the LDRD**
- **Charon**
  - Device physics
    - Drift-Diffusion Model
    - Finite Element / Finite Volume
    - Recombination / Charge generation
  - *How to inform secondary effects due to parasitic bipolar enhancement
- **Monte-Carlo Radiative Energy Deposition (MRED)**
  - Particle physics (Geant 4)
  - Nested Sensitive Volumes
    - Provides approximation for device physics at reduced cost
  - *How are nested sensitive volumes defined for silicon-on-insulator (SOI) devices
- **Xyce**
  - Circuit simulation
    - Charon/ MRED SEE informed netlists
  - *Explain current anomalies in existing CMOS7 data
- **Experiments**
  - Design of experiments
  - *Validation data for research and publication

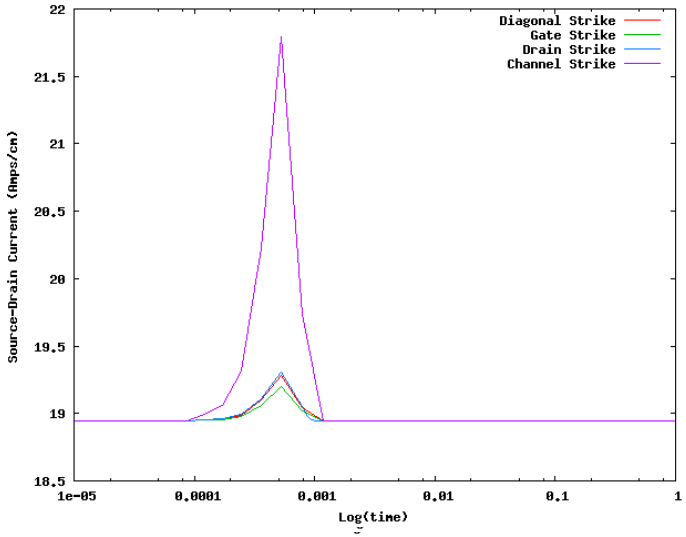


*Overall integrated, validated workflow from TCAD to IC evaluation

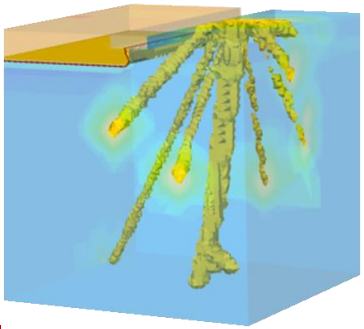
*Research Aspects

Charon





- Real strikes are not user-defined
  - There is scattering
  - Energy is lost along the way
  - Use Cascade / Marlowe input?



MOSFET manufactured in CMOS7 SOI technology

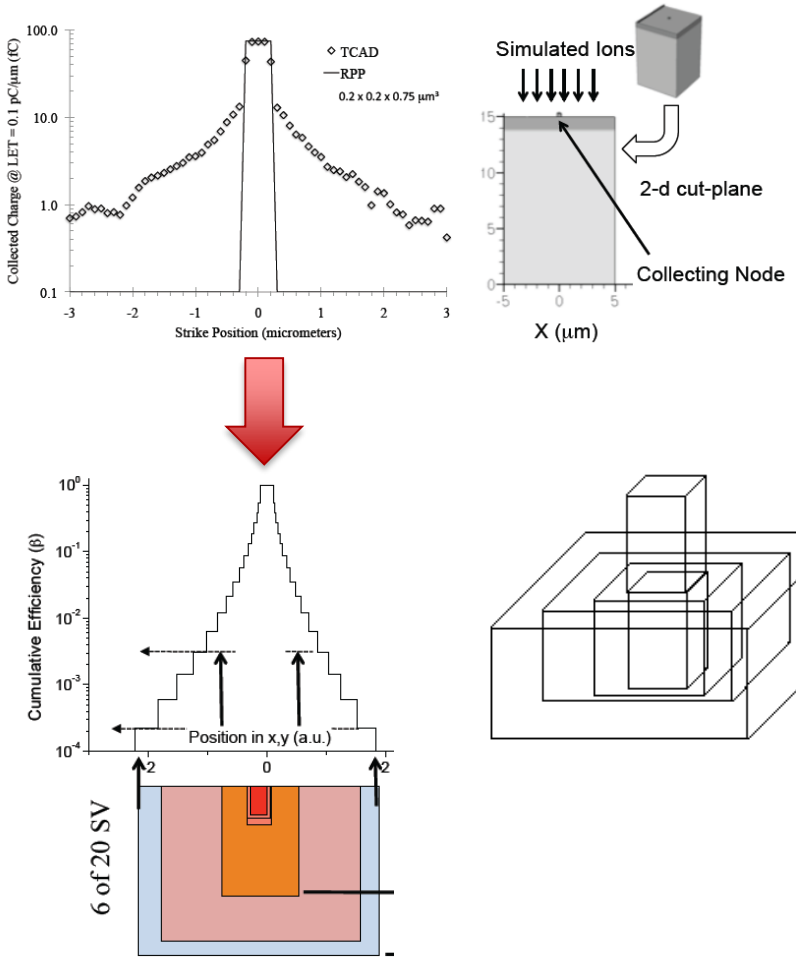
- User defined particle strike
  - Shape/location of the strike
  - Intensity of the strike
  - 0th order approximation to SEE

- Real analysis requires many evaluations
  - Must examine broad spectrum of strikes
  - Must examine multiple devices that provide identical function, but have different SEE response

***The problem is not deterministic; it is stochastic**
There is a better, more efficient way… Use TCAD informed MRED

Charon->MRED (in SOI)

- Charon
  - Computationally intensive – Monte Carlo simulations are computationally intractable
  - Implements ion strikes at line of charge – actual deposition is random and involves nuclear interactions
- MRED device physics approximation
  - Overcomes computation and single event simulation limitations
  - Charon is used to calibrate volumes and efficiencies



CMOS7/8 devices present unique challenges for this conversion

Research Contribution – Charon to MRED to Xyce Single Integrated Simulation Tool Flow

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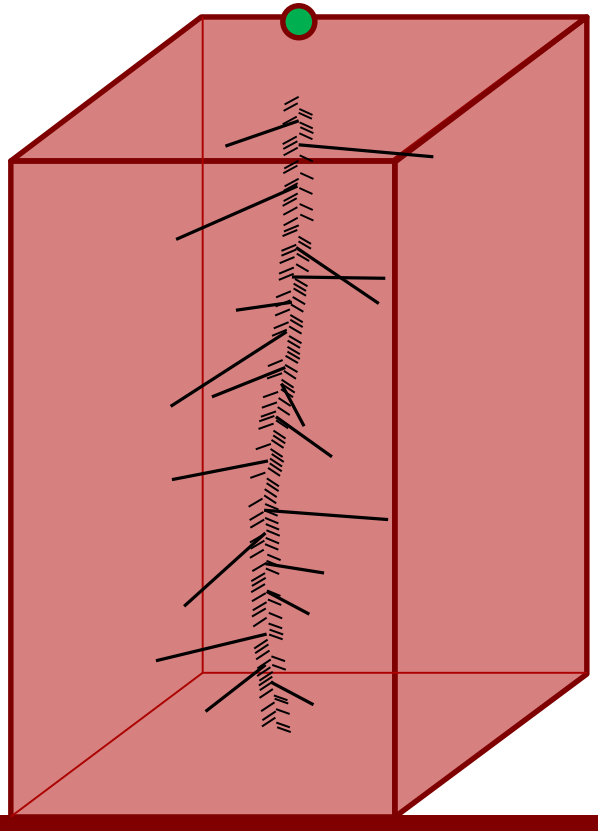
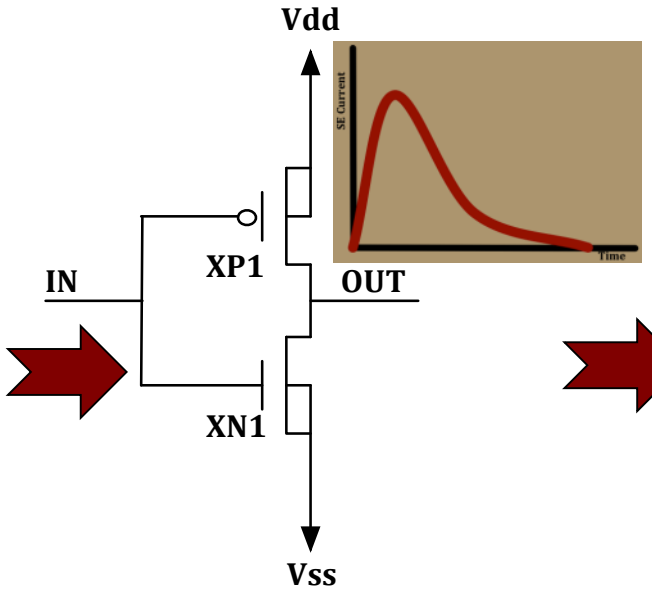
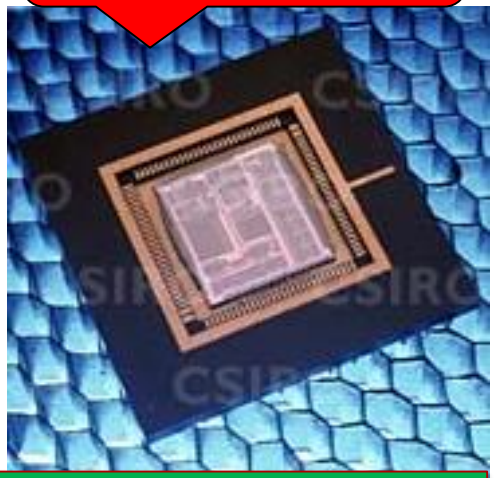
- Radiation transport to IC response for ionizing particles.
- Translation across several layers of abstraction

Radiation transport **Circuit-level simulation** **IC-level simulation**





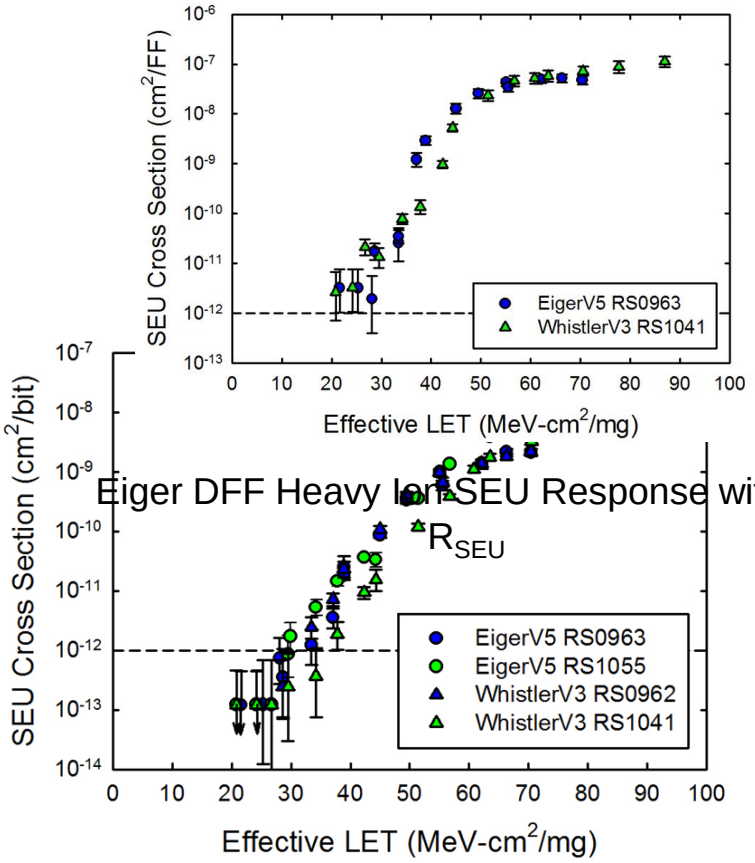
Meet Rad Requirement? Yes/No?



*Results in the reduction of test space across boundaries

Experimental Validation

- Existing CMOS7 Test Data
  - D Flip-Flops (DFF)
    - With and without feedback resistance
    - Large transistors, mainly BUSFETs, but no transistor variations
  - Dual Port SRAM (DPSRAM)
    - With and without feedback resistance
    - Smaller transistors with large shallow implant islands for access ports
  - Analog Blocks
    - Lots of transistor sizes and variations in each block
    - Not good for calibration, but good for validation



Eiger DFF Heavy Ion SEU Response without R_{SEU}

Eiger DPSRAM Heavy Ion SEU Response with R_{SEU}

Experimental Validation

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- Calibration with existing data
  - Currently provides two layout variations (DFF vs. DPSRAM) with some circuit variations (with or without feedback resistance)
  - Layout differences include different size transistors, use of shallow implants in extended drains in DPSRAM, and transistors in the same island
  - It will be difficult to extract these layout differences independently with this test data – too many variations and not enough distinct data sets
  - *Explanation of anomalous responses in existing data
- We propose the development and evaluation of new test structures
  - Perform a design of experiments to better distinguish responses due to layout variations
  - Experiment data then used to validate the radiation modeling
  - *Validation of parasitic bipolar enhancement model

Research & Risks

- *Proposed effort would enable design trades to optimize IC performance while meeting radiation requirements and validate designs prior to fabrication.
  - *How to inform secondary effects due to parasitic bipolar enhancement (Charon)
  - *How are nested sensitive volumes defined for SOI devices (MRED)
  - *Explain current anomalies in existing CMOS7 data (Xyce)
  - *Validation data for the research and publication & bipolar enhancement model (Experiments)
  - *Overall integrated, validated workflow from TCAD to IC evaluation
    - *Results in the reduction of test space across boundaries
    - *CMOS7/8 devices present unique challenges for this conversion

- Too much uncertainty in the model
  - Is it sufficiently predictive?
  - Can we capture the bipolar effect?
- Scheduling build & test

- The whys, what-fors, outputs
  - In the call, “introduce advanced models for single-event effects.”
  - Should save years and $Ms
  - Validated process w/ mod-sim to assess ICs for radiation susceptibility prior to build & test
    - No one else has taken this approach

Objectives & Milestones

Sandia National Laboratories

- **Year 1**
  - Develop sensitive volumes and their associated parameters in CMOS7 & CMOS8 silicon-on-insulator transistors
  - Validate the Charon TCAD models to CMOS7 & CMOS8 transistor layout variations in a normal, non-irradiated environment
  - Determine the transistor layout variations which significantly affect charge collection due to single events
- **Year 2**
  - Develop MRED to Xyce Process
  - Demonstrate simple circuit netlist (flip-flop) being exercised with MRED using Xyce
  - Validate flip-flop and SRAM circuit response in MRED to Xyce with test data.
- **Year 3**
  - Develop SEE evaluation process for designed schematics and layouts
  - Demonstrate Monte Carlo sampling of a circuit netlist for single event effects evaluation
  - Validate process with integrated circuit single event prediction against existing test data

Planning & Reporting

- Phenomena Identification Ranking Table (PIRT)
  - These have been developed for most CMOS7 devices inre dose rate
  - Should be straightforward to modify for SEE
- Predictive Capability Maturity Model (PCMM)
  - V&V Planning documents
  - Comprehensive framework including verification, validation, UQ…
  - …but was not developed with smaller research projects in mind
  - Will follow the framework, but likely without the detailed formalism
- Reporting
  - Briefing as appropriate
  - Annual SAND Report

Code Verification (CVER)		
Apply Software Quality Engineering (SQE) processes	1	0.5
Provide test coverage information	2	1.5
Physics and Material Model Fidelity (PMMF)		
Assess interpolation vs. extrapolation of physics and material model	3	2
Technical review of physics and material models	2	1.5
Representation and Geometric Fidelity (RGF)		
Characterize Representation and Geometric Fidelity	3	2.5
Geometry sensitivity	2	1
Solution Verification (SVER)		
Quantify numerical solution errors	3	2.5
Quantify Uncertainty in Computational (or Numerical) Error	2	2
Validation (VAL)		
Define a validation hierarchy	2	2
Apply a validation hierarchy	3	3
Uncertainty Quantification (UQ)		
Aleatory and epistemic uncertainties identified and characterized.	2	1
Perform sensitivity analysis	2	2

Summary

- Target BUSFETs in Single Event Environments
  - Should work for other environments (dose rate)
  - Methods employed can be brought to bear on other devices or materials (GaAs, GaN)
  - 1700 currently has single event test articles
    - Data not created to discriminate by device specifics, i.e. in layout-vs-schematic, devices of different doping depths, for example, appear identical even though they have varied SEE responses.
- Simulation Informs Decision Making in Layout
  - TCAD (Charon) models charge transport
  - Monte Carlo Radiative Energy Deposition (MRED) tool is informed by TCAD
    - Nested sensitive volumes
    - Bringing this tool to SNL from Vanderbilt
  - Xyce
    - Radiation informed netlists
- Partner with Academia
  - Ron Schrimpf, Vanderbilt
    - Fund Graduate Student