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Readout Electronics for a Single-Volume Neutron Scatter Camera

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INTRODUCTION

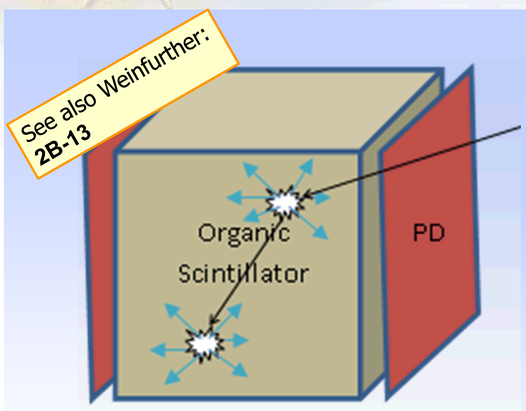
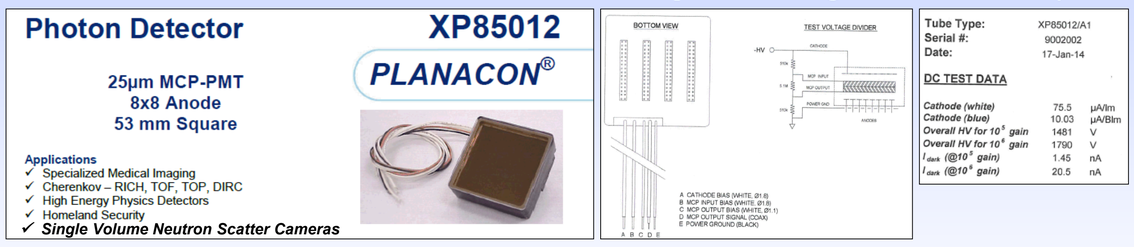


Figure 1: A neutron double-scatter interaction in a single-volume scatter camera. Two or more high-resolution photodetectors (PDs) are coupled to a large scintillator volume.

We are developing a single-volume double-scatter neutron imager. The detection concept involves the use of kinematic information from two neutron-hydrogen elastic scattering events in organic scintillator. In the single-volume detector, both neutron scatters can occur in the same large active volume (see Figure 1). The ability to detect and resolve two interactions of a fission-energy neutron in a single volume of organic scintillator would yield dramatically better intrinsic efficiency than the multi-cell-based geometry used in current double-scatter neutron imagers. However, building such a detector presents several challenges to standard photo-detection and signal collection practices. The spatial and temporal separations of successive neutron scattering interactions are of order 1 cm and 1 ns. A fast scintillator, preferably with sub-ns decay time, is needed to resolve closely spaced interactions, but there is a tradeoff between scintillator speed and light output. These constraints lead to a regime wherein the photons from related scatters overlap in time and position at the face of the scintillator volume. A solution to this overlap is to record the position and time of arrival of each photon and apply knowledge of photon production and transport mechanisms to reconstruct a likely series of scattering events leading to the observed photons. Simulations using realistic physical assumptions have shown that possessing such a list of photon positions and arrival times leads to a detector with useful performance. This leaves the problem of realizing hardware capable of generating the necessary photon list.

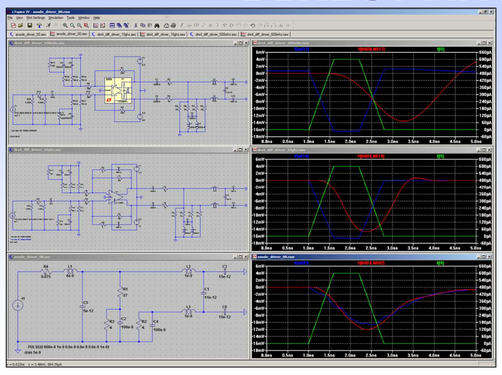
PHOTO-DETECTION

The central task of resolving two nearby proton recoils in a single volume of scintillator would not be possible using traditional photomultiplier tubes. Recent advances in photodetector (PD) technology, however, have made the approach conceivable. PDs based on micro-channel plate electron multipliers (MCPs) rather than dynode structures have inherently good spatial and temporal resolution. We used commercially available Photonis Planacon MCP-PMTs for initial laboratory studies, and have selected the Photonis XP85012 8x8 anode MCP-PMT as the basis for an experimental single volume detector system.



Because it remains difficult to distinguish multiple overlapping photon induced charge pulses on a given anode, a reduction in average anode occupancy is desirable and can obviously be achieved with finer anode pixelization. Photonis offers a 32x32 anode Planacon that is attractive in this respect. However, the density of the necessary readout electronics was not practically achievable in the time and budget scope offered us forcing us to eschew ASICs, etc., and turn to accessible commercial IC and PCB technologies. The ongoing work developing SPADs integrated directly to readout electronics within a pixel for PET applications is of significant interest to us for the SVSC application.

DIRECT ANODE CONNECTION

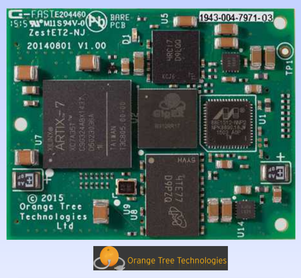


We chose to drive the inputs single-endedly to eliminate the significant space, power and bandwidth constraints entailed by using an input single-to-differential op-amp buffer stage, since linearity and cross-talk are not as important to our application as these other factors. Single ended drive is not recommended by PSI. However, simulations suggest that given a low enough load resistance an adequate frequency response is possible. There is no practical way to simulate the loss of noise and cross-coupling immunity due to single-ended input drive. This is certainly one of the highest risk decisions made in the design.

TRIGGER / CALIBRATION

System triggers are generated from the OR-ed fan-in and subsequent fan-out of a threshold discriminator attached to each Planacon's "MCP Out" signal. "MCP Out" acts similarly to the last dynode of a conventional PMT and presents a signal that is a negative fraction of the sum of the anode signals, providing a simple, opportunistic coincidence function. We employ a siamesed use of the 9-th channel on one DRS4 to digitize each Planacon's PMT Out signal. The 9-th channel of both DRS4 chips is also used to digitize a low distortion sine wave enabling a calibration of each DRS4's fixed pattern aperture jitter.

SYNCHRONIZER / DATA CONCENTRATOR



Orange Tree Technologies

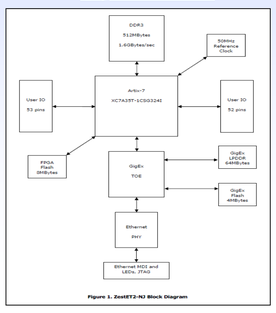
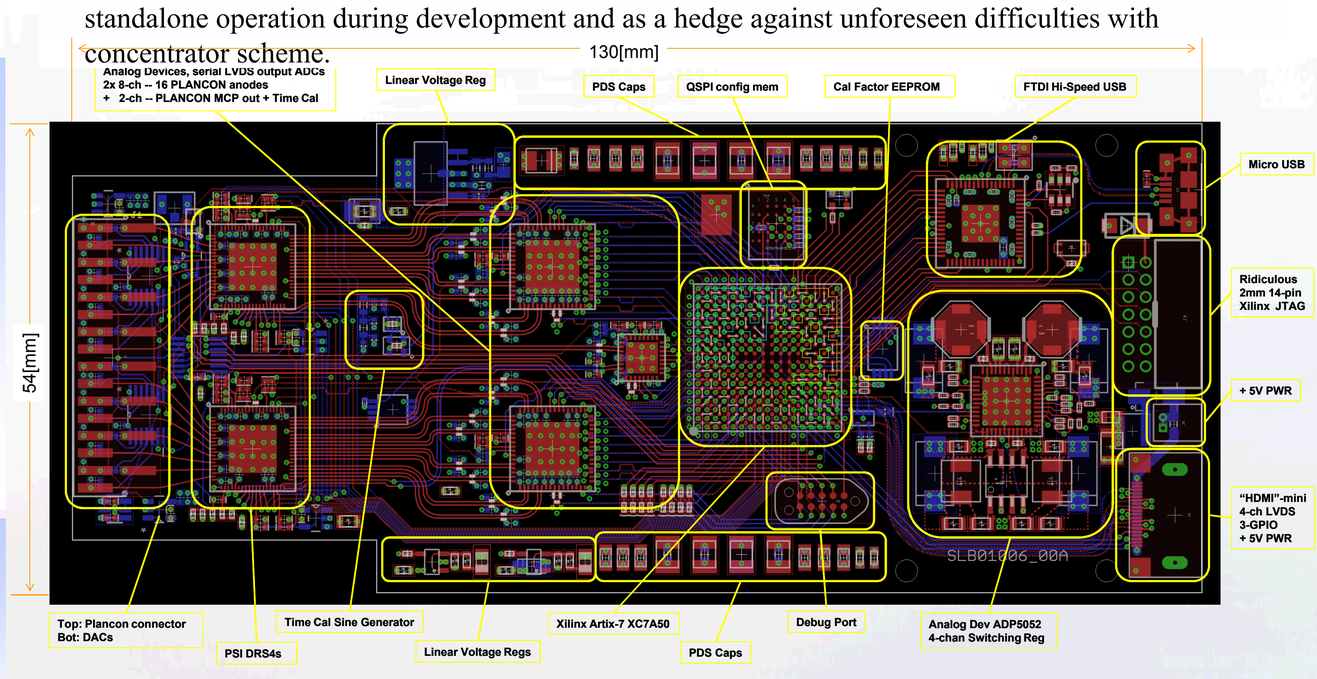


Figure 1. ZestET2-NJ Block Diagram

A prototype detector system configured with four Planacons requires a total of 16 digitizer assemblies. To coordinate control, triggering and data transfer, the 16 digitizer assemblies will communicate via a high-speed serial link architecture using a star topology with a central system concentrator node. In lieu of expending a significant effort to design and build a custom printed circuit assembly for the system concentrator node, we selected for this function the ZestET2 Gigabit Ethernet interface module produced by Orange Tree Technologies. In addition to Orange Tree's GigExpedite TCP/IP offload engine (TOE)--a dedicated hardware TCP/IP solution delivering sustained full gigabit speed--the ZestET2 includes a user programmable Xilinx Artix-7 XC7A35T FPGA and 512Mbytes of DDR3 memory in which we will implement our control logic, serial links and data buffering. We will use Xilinx's SERDES resources in each Atrix FPGA to realize the distribution of common clock and trigger synchronization signals as well as sample data transfer. Given 256 channels digitizing 1024 samples per channel at 12-bits per sample and given the ultimate 1[Gb/s] Ethernet speed limit should yield a maximum system trigger rate of ~300[Bq].

WAVEFORM CAPTURE

The XP85012 presents its 64 anode signals through four 2x16 pin 2mm connectors, 16 anodes per connector. We designed and are building a very compact custom digitization printed circuit assembly that plugs directly to these Planacon connectors—four of these digitizer assembles being needed for each Planacon. Each digitizer assembly provides 16 channels of 5 [GS/s] sampling with a buffer depth of up to 1024 samples per trigger by utilizing two Paul Scherrer Institute (PSI) DRS4 switched capacitor array chips. Each DRS4 chip has nine channels of which eight are driven in single-ended mode directly by the Planacon anodes (*see Direct Anode Connection section*) and the 9th channel is used to digitize a calibration sine wave and the Planacon's "MCP Out". (*see Trigger/Calibration section*) To maximize event-to-event throughput, each DRS4 is read out using an Analog Devices AD9257 Octal ADC for the 8 anode channels and one channel of a common AD9645 Dual ADC for the timing calibration channel. Both digitizer types are 14-bit units of which we will deliver 12 bits in the data payload. A sampling rate of 33 [MS/s] is recommended by PSI for best DRS4 SNR and integral nonlinearity. Both ADC types use fast serial LVDS connections on data outputs to minimize the pins and routing needed to connect to the Xilinx Artix-7 XC7A50T FPGA, in which we will implement the control, trigger distribution, local data buffering and fast serial connection with the data concentrator node. (*see Synchronizer/Data Concentrator section*) HDMI connectors and cables are used for the fast serial connections. In addition to these connections, each digitizer assembly has an FTDI FT2232H USB 2.0 High Speed (480[Mb/s]) FIFO chip to allow full standalone operation during development and as a hedge against unforeseen difficulties with concentrator scheme.



DISCUSSION / FUTURE WORK

One reproducible observation is things always take longer than one would like. For example, at the time of this poster's printing we have yet to lay hands on a physical example of the circuit assembly suggested above. The PC boards have been fabricated and are in the process of being loaded with components. We anticipate doing a smoke test within two weeks. As many of the sub-circuits as possible were directly copied from known working designs. The design as a whole was subjected to review by knowledgeable folks outside the project team. No obvious red flags were raised. Elements of the FPGA firmware are under development using surrogate hardware. We continue to become familiar with the DRS4's characteristics as revealed by its operations in a several PSI DRS4 Evaluation Kits used in our lab experiments to date. We are developing computer signal post-processing code based on the data gathered by the Kits. Our hardware effort here is geared towards the proof of principle goal of this project and not to produce an optimal design for a practical production system. To that end, we encourage the production, transmission and storage of much more data than we hope will ultimately prove necessary to successfully deploy the single volume concept. Substantial work remains in identifying a minimal set of analysis processing steps and pushing those as close as possible to the surfaces of the volume.

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