SAND2016-5085D

xdm

Xyce Data Model

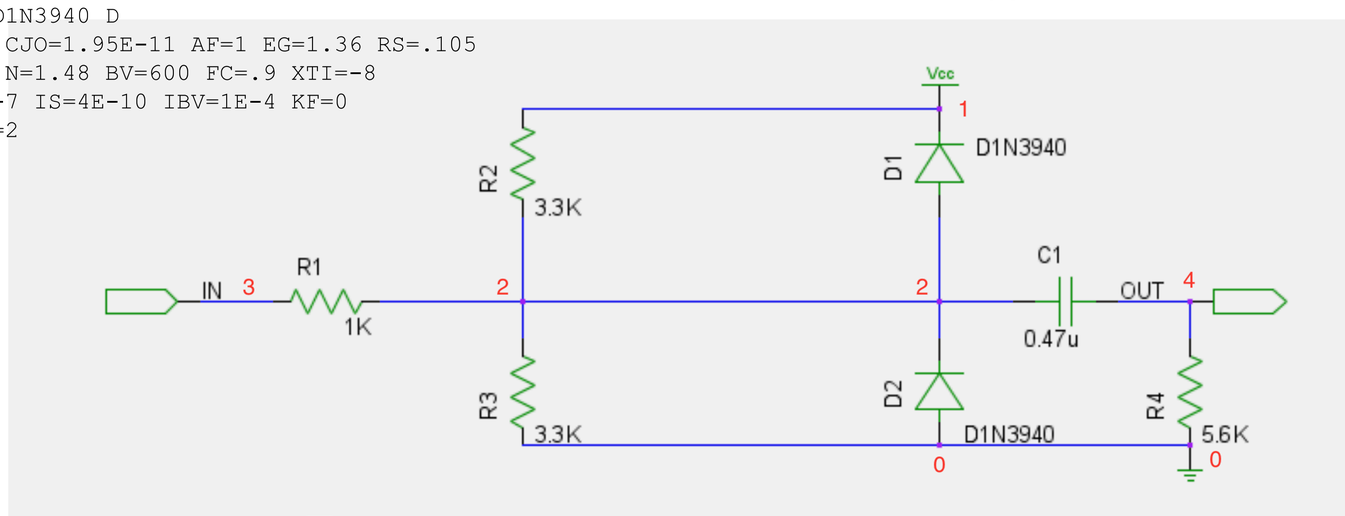
Xyce **D**ata **M**odel (**xdm** – Org. 5561/8943) is an enabling technology that connects electrical circuit designers (Org. 434, 1350, and 1700) with powerful high-performance computing electrical modeling capabilities (Xyce™ Parallel Electronic Simulator – Org. 1355). All Sandia circuit data originates in one of the commercial design-capture tools (OrCAD, Mentor Graphics) in netlist formats that do not translate into the Sandia Xyce code directly – **xdm** bridges this gap using a graph based abstract data model to allow rapid data conversion from multiple commercial formats into the Xyce netlist modeling format.

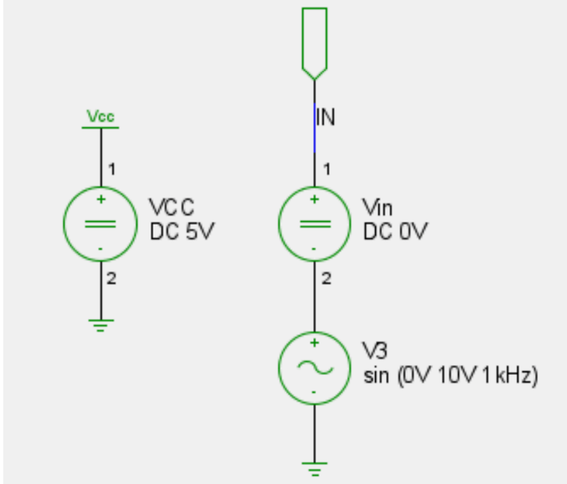
DC Diode Clipper circuit (example Xyce simulation post-**xdm** netlist conversion)

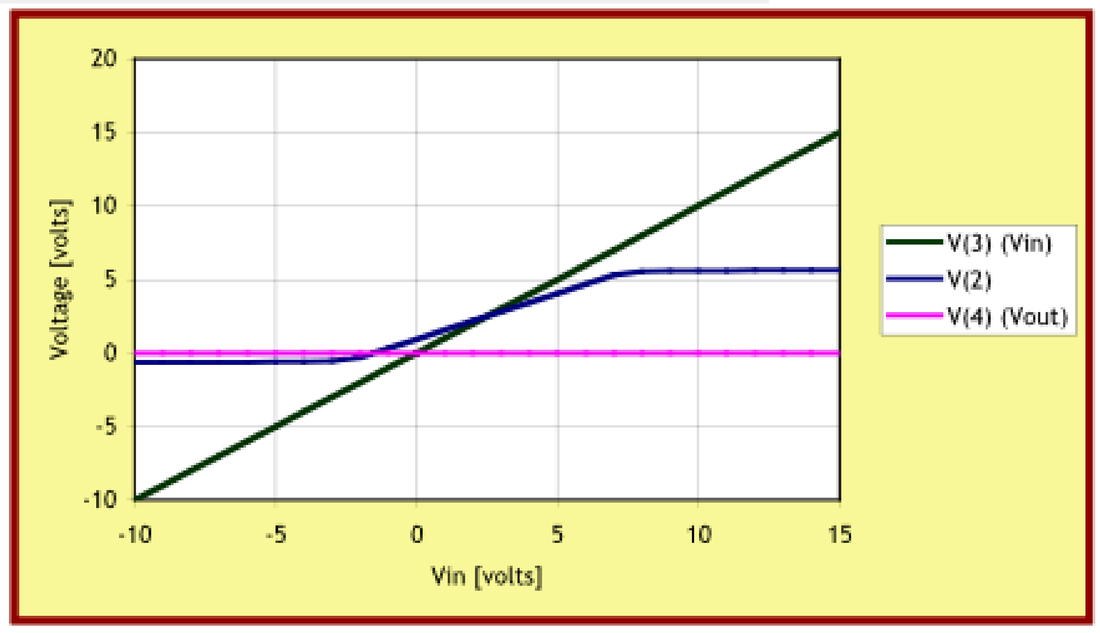
```
** Translated using xdm 1.10 on May_15_2016_22_15_08_PM
** from /Users/rrlober/xdm_new/bin/pspice_16_6.xml
** to /Users/rrlober/xdm_new/bin/xyce_6_4.xml

* Diode Clipper Circuit
* Voltage Sources
VCC 1 0 DC 5V
VIN 3 0 DC 0V
* Diodes
D1 2 1 D1N3940
D2 0 2 D1N3940
* Resistors
R1 2 3 R=1K
R2 1 2 R=3.3K
R3 2 0 R=3.3K
R4 4 0 R=5.6K
* Capacitor
C1 2 4 C=0.47u
* Analysis Control (-10 volts to 15 by 1)
.DC LIN VIN -10 15 1
.PRINT DC V(3) V(2) V(4)
* GENERIC FUNCTIONAL EQUIVALENT = 1N3940
* TYPE: DIODE
* SUBTYPE: RECTIFIER
.MODEL D1N3940 D
+ VJ=.4 CJO=1.95E-11 AF=1 EG=1.36 RS=.105
+ M=.38 N=1.48 BV=600 FC=.9 XTI=-8
+ TT=8E-7 IS=4E-10 IBV=1E-4 KF=0
+ LEVEL=2
*

.END
```

xdm 1.1 Features:

- Graph based abstract data model
- Netlist device query capability
- XML based format definitions
- Supported circuit formats:
  - OrCAD PSpice
  - OrCAD Spectre (alpha)
  - Mentor T-Spice (in devel)
- Sandia Analysis Workbench (SAW/8953) integration
- Boost Spirit C++ parser, Python Xyce Writer







Abstracting Data to connect Users to Capabilities

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