SAND2016-5047C

Readout Electronics for a Single-Volume Neutron Scatter Camera

James Brennan, Erik Brubaker, John Steele, Melinda Sweany
Sandia National Laboratory, Livermore, CA
John Mattingly, Kyle Weinfurther
North Carolina State University

INTRODUCTION

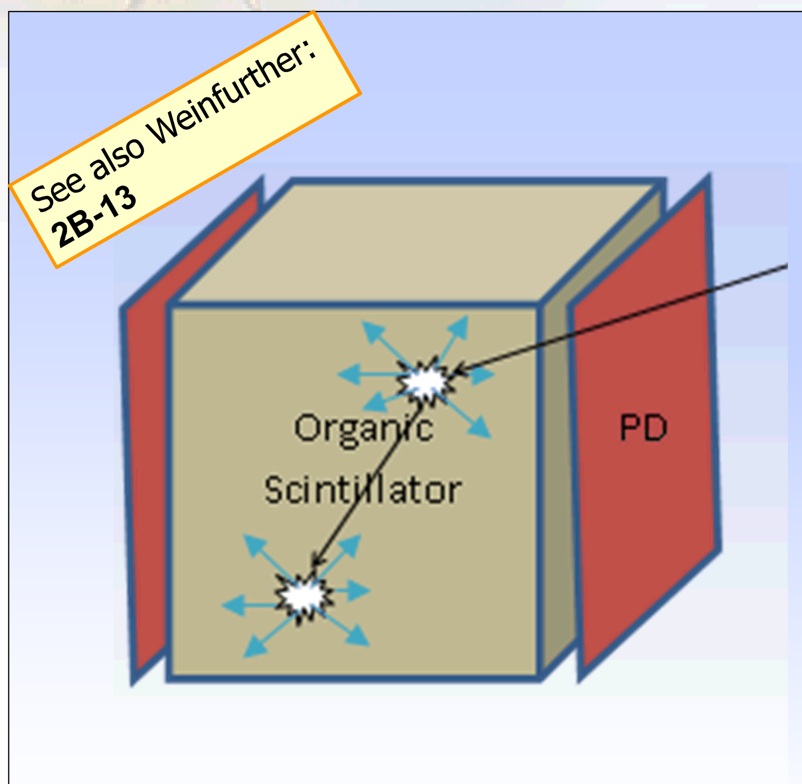


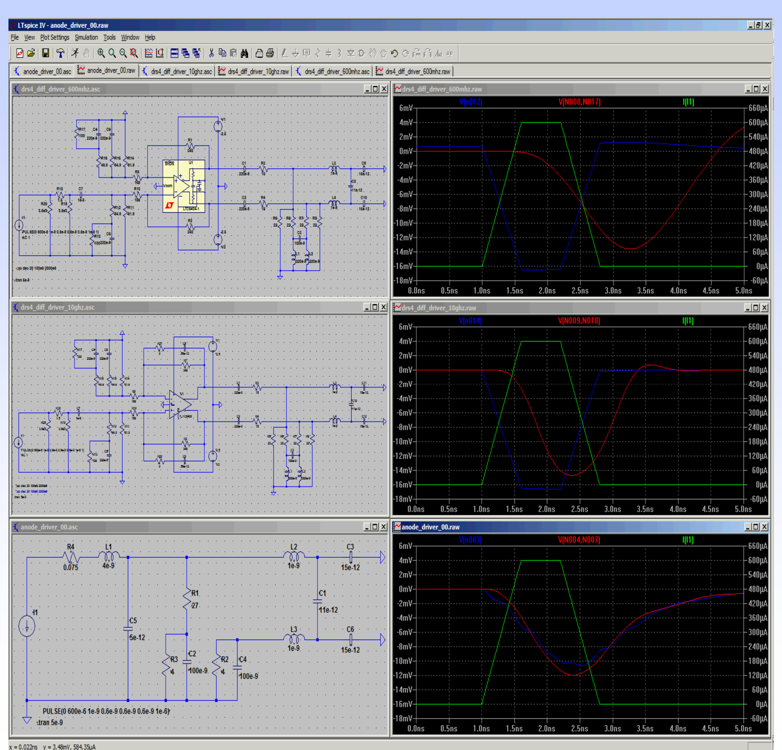
Figure 1: A neutron double-scatter interaction in a single-volume scatter camera. Two or more high-resolution photodetectors (PDs) are coupled to a large scintillator volume.

We are developing a single-volume double-scatter neutron imager. The detection concept involves the use of kinematic information from two neutron-hydrogen elastic scattering events in organic scintillator. In the single-volume detector, both neutron scatters can occur in the same large active volume (see Figure 1). The ability to detect and resolve two interactions of a fission-energy neutron in a single volume of organic scintillator would yield dramatically better intrinsic efficiency than the multi-cell-based geometry used in current double-scatter neutron imagers. However, building such a detector presents several challenges to standard photo-detection and signal collection practices. The spatial and temporal separations of successive neutron scattering interactions are of order 1 cm and 1 ns. A fast scintillator, preferably with sub-ns decay time, is needed to resolve closely spaced interactions, but there is a tradeoff between scintillator speed and light output. These constraints lead to a regime wherein the photons from related scatters overlap in time and position at the face of the scintillator volume. A solution to this overlap is to record the position and time of arrival of each photon and apply knowledge of photon production and transport mechanisms to reconstruct a likely series of scattering events leading to the observed photons. Simulations using realistic physical assumptions have shown that possessing such a list of photon positions and arrival times leads to a detector with useful performance. This leaves the problem of realizing hardware capable of generating the necessary photon list.

PHOTODETECTION

The central task of resolving two nearby proton recoils in a single volume of scintillator would not be possible using traditional photomultiplier tubes. Recent advances in photodetector (PD) technology, however, have made the approach conceivable. PDs based on micro-channel plate electron multipliers (MCPs) rather than dynode structures have inherently good spatial and temporal resolution. We used commercially available Photonis Planacon MCP-PMTs for initial laboratory studies, and have selected the Photonis XP85012 8x8 anode MCP-PMT as the basis for an experimental single volume detector system.

DIRECT ANODE CONNECTION



One potentially high pay-off, in terms of simplicity and PC board area, gambits is to directly drive the DRS4 inputs with the Planacon anodes in a single-ended fashion. This is not recommended by PSI. However, simulations suggest that given a low enough load resistance an adequate frequency response is possible. There is no practical way to simulate the loss of noise and cross-coupling immunity due to single-ended input drive. But since our application does not require the highest fidelity waveform reproduction as well as significant cross-talk arising in the Planacons themselves, we felt the advantages outweighed the risks. TBD. We are crossing our fingers.

SYNCHRONIZER/DATA CONCENTRATOR

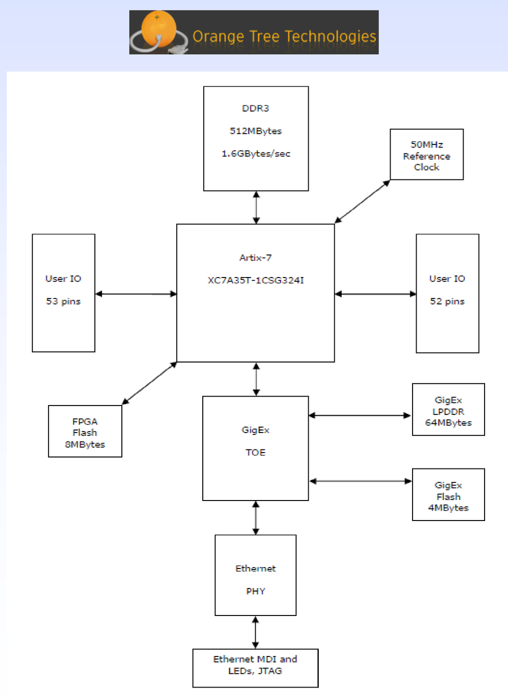
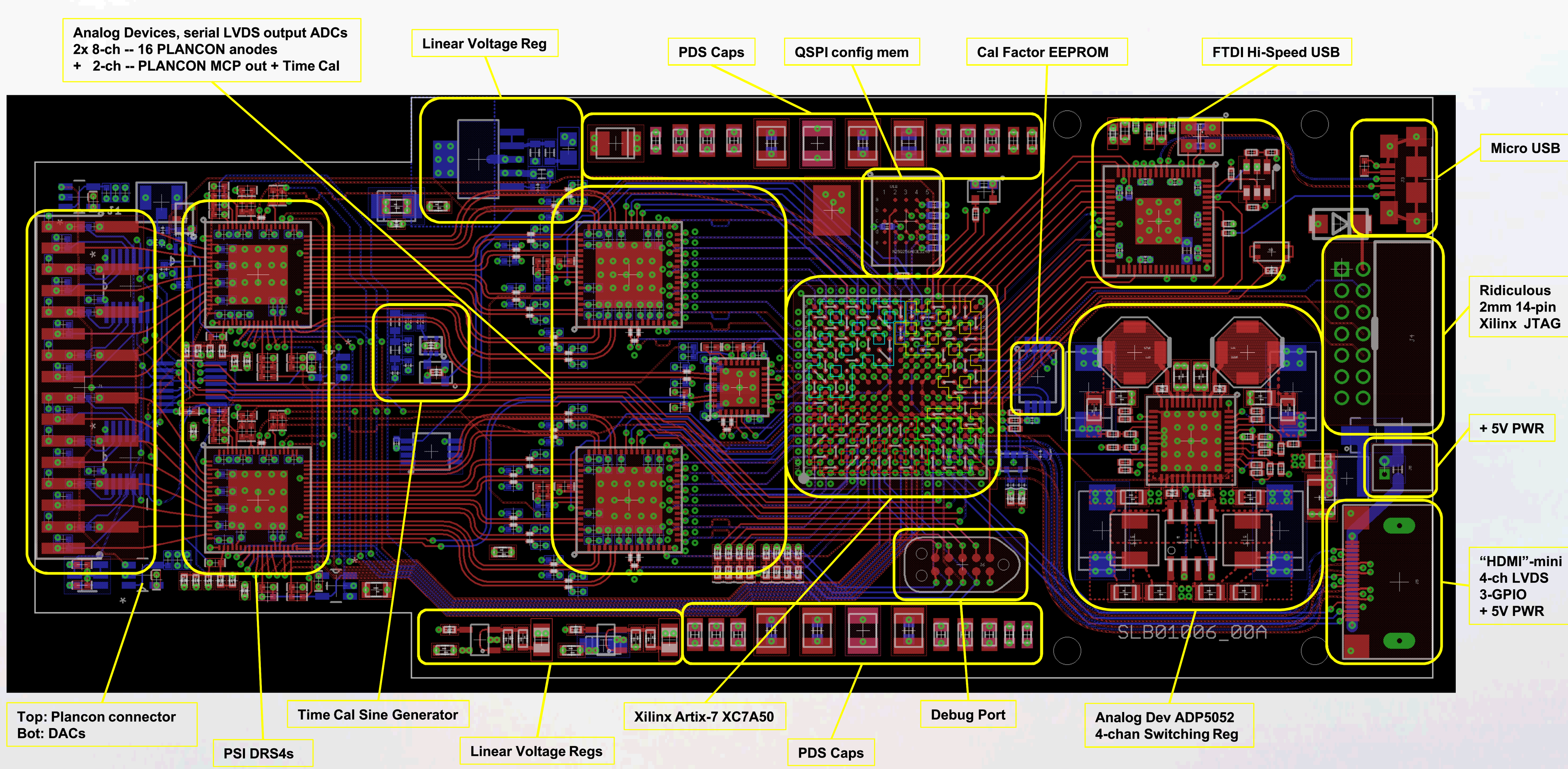


Figure 1. ZestET2-NJ Block Diagram

The detector system configured with four Planacons requires a total of 16 digitizer assemblies. To coordinate control, triggering and data transfer, the 16 digitizer assemblies communicate via a high-speed serial link architecture using a star topology with a central system concentrator node. In lieu of expending a significant effort to design and build a custom printed circuit assembly for the system concentrator node, we selected for this function the ZestET2 Gigabit Ethernet interface module produced by Orange Tree Technologies. In addition to Orange Tree's GigExpedite TCP/IP offload engine (TOE)--a dedicated hardware TCP/IP solution delivering sustained full gigabit speed--the ZestET2 includes a user programmable Xilinx Artix-7 XC7A35T FPGA and 512Mbytes of DDR3 memory in which we implement our control logic, serial links and data buffering. We used Xilinx's SERDES resources in each Atrix FPGA to realize the distribution of common clock and trigger synchronization signals as well as sample data transfer. Given 256 channels digitizing 1024 samples per channel at 12-bits per sample and given the ultimate 1[Gb/s] Ethernet speed limit yields a maximum system trigger rate of ~300[Bq].

WAVEFORM CAPTURE

The XP85012 presents its 64 anode signals through four 2x16 pin 2mm connectors, 16 anodes per connector. We designed and built a very compact custom digitization printed circuit assembly that plugs directly to these Planacon connectors—four of these digitizer assembles being needed for each Planacon. Each digitizer assembly provides 16 channels of 5 [GS/s] sampling with a buffer depth of up to 1024 samples per trigger by utilizing two PSI DRS4 switched capacitor array chips. Each DRS4 chip has nine channels of which eight are driven in single-ended mode directly by the Planacon anodes and the 9th channel is used to digitize a low distortion sine wave enabling a calibration of each DRS4's fixed pattern aperture jitter. We chose to drive the inputs singled-endedly to eliminate the significant space, power and bandwidth constraints entailed by using an input single-to-differential op-amp buffer stage, since linearity and cross-talk are not as important to our application as these other factors. (see Direct Anode Connection section.) To maximize event-to-event throughput, each DRS4 is read out using an Analog Devices AD9257 Octal ADC for the 8 anode channels and one channel of a common AD9645 Dual ADC for the timing calibration channel. Both digitizer types are 14-bit units of which we deliver 12 bits in the data payload. The sampling rate is 33 [MS/s] as recommended by PSI for best DRS4 SNR and integral nonlinearity. Both ADC types use fast serial LVDS connections on data outputs to minimize the pins and routing needed to connect to the Xilinx Artix-7 XC7A50T FPGA, in which we implement the control, trigger distribution, local data buffering and fast serial connection with the data concentrator node. (see Synchronizer/Data Concentrator section.) HDMI connectors and cables are used for the fast serial connections. In addition to these connection, each digitizer assembly has an FTDI FT2232H USB 2.0 High Speed (480[Mb/s]) FIFO chip to allow full standalone operation during development and as a hedge against unforeseen difficulties with concentrator scheme.



TRIGGER/CALIBRATION

System triggers are generated from the OR-ed fan-in and subsequent fan-out of a threshold discriminator attached to each Planacon's "MCP Out" signal. "MCP Out" acts similarly to the last dynode of a conventional PMT and presents a signal that is a negative fraction of the sum of the anode signals, providing a simple, opportunistic coincidence function. We employ a siamesed use of the 9-th channel on one of the DRS4 to digitize each Planacon's PMT Out signal. The 9-th channel of both DRS4 chips is also used to digitize a timing calibration sine wave such that the fixed pattern aperture jitter can be measured.

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SAND2016-xxxxxxxx

National Nuclear Security Administration