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# Miniature High Voltage, High Temperature Component Package Development

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***Abstract*— With the next generation of semiconductor materials in development, significant strides in the Size, Weight, and Power (SWaP) characteristics of power conversion systems are presently underway. In particular, much of the improvements in system-level efficiencies and power densities due to wide-bandgap (WBG) and ultra-wide-bandgap (UWBG) device incorporation are realized through higher voltage, higher frequency, and higher temperature operation. Concomitantly, there is a demand for ever smaller device footprints with high voltage, high power handling ability while maintaining ultra-low inductive/capacitive parasitics for high frequency operation. For our work, we are developing small size vertical gallium nitride (GaN) and aluminum gallium nitride (AlGaN) power diodes and transistors with breakdown and hold-off voltages as high as 15kV. The small size and high power densities of these devices create stringent requirements on both the size (balanced between larger sizing for increased voltage hold-off with smaller sizing for reduced parasitics) and heat dissipation capabilities of the associated packaging. To accommodate these requirements and to be able to characterize these novel device designs, we have developed specialized packages as well as test hardware and capabilities. This work describes the requirements of these new devices, the development of the high voltage, high power packages, and the high-voltage, high-temperature test capabilities needed to characterize and use the completed components. In the course of this work, we have settled on a multi-step methodology for assessing the performance of these new power devices, which we also present.**

***Keywords—packaging; power components; testing; temperature effects; voltage breakdown; 3D printing; WBG devices***

## I. INTRODUCTION

New Wide-Bandgap (WBG) materials, such as Gallium Nitride (GaN) and Silicon Carbide (SiC) have bandgaps of 3.2-3.4 eV. The WBG nature of these materials allow for improvements over conventional Si devices in voltage hold-off (as the critical field scales with bandgap), high temperature operation (as the number of free carrier decreases markedly with bandgap), and high frequency operation (as size and therefore capacitance decreases) [1]-[2]. This higher frequency operation is especially noteworthy, as they enable system-level SWAP improvements. As these devices have matured into commercial products, they are being utilized for application spaces as diverse as grid-connected power electronic systems [3], electric vehicle inverters [4], space [5], and military applications [6] and even applications in extreme environments such as geothermal [7].

One of the major motivating factors in adopting these WBG and UWBG devices is in reducing circuit size by reducing the size of passive elements [3]. However, packaging high voltage WBG or UWBG semiconductor devices in large power modules could offset the gains made from this size reduction in passive components. A miniature high voltage package capable of operating in high temperature environments is therefore needed to fully take advantage of the UWBG semiconductor devices currently in development. Since these new devices are equipped to operate at higher voltages and temperatures than conventional Si-based power devices, challenges exist in characterizing and/or validating the performance of new materials and packaged devices utilizing conventional characterization equipment.

As the operational voltage of UWBG devices is far above conventional packaging designs (e.g. To-220), a novel device package is presented that balances the needs for high-voltage operation (large dimensions to limit arcing) with high frequency operation (small dimensions to limit parasitics). In additional to an optimized layout, these packages utilize 3D printed advanced manufacturing capabilities, which allow for low-cost, high-throughput, mass manufacturing of high-voltage, high-performance packages. A designed and testing methodology for parts placed in the package is outlined.

The high operational voltage of UWBG devices also requires new instrumentation for characterization that is able to operate at extremely high voltages while providing accurate and precise measurements of voltage and current. A design for a high voltage IV tracer is presented here that uses commercially available components to analyze the behavior of a reverse-biased diode under high voltage conditions. While other designs such as [8] have been presented to accomplish testing at high voltage, the proposed design uses a modular approach with commercially available components and measures voltage with a finer resolution; specifically, the supply can regulate the steady-state output voltage to within 5V, but the measurement setup can resolve voltage to within 100 mV and sample the voltage and current during transitions between steps in supply voltage. The proposed design also allows for testing over a wide range of parts by using socket mounts. Though the proposed design is currently limited to 20 kV, the safety features and ancillary components will support testing above 50 kV; thus, the operational range may be expanded by merely replacing the power supply. Finally, high temperature voltage breakdown was tested in a high voltage oven.

## II. Objectives for Device Packages

The goal of this work is to develop device packages that complement the characteristics of WBG and UWBG devices, in particular, GaN and AlGaN diodes and transistors for power applications. Our goals are to fabricate devices in materials with much higher bandgaps and theoretical device figures-of-merit (most commonly, breakdown voltage and series resistance) which can provide much higher converter power densities. GaN, used extensively in radio frequency applications, is beginning to become commercially available as power components. Work began with the fabrication of vertical GaN diodes and lateral high electron mobility transistors (HEMTs). We fabricated GaN PIN diodes with breakdown voltages as high as 3900V and the best unipolar FOM demonstrated thus far [9]. Consequently, our present fabrication development work has shifted to AlGaN devices. AlGaN, depending on its alloy concentration, has a bandgap between the 3.4 eV bandgap of GaN and the 6.2 eV bandgap of AlN. We have fabricated the first high-Al content ($Al_{0.3}Ga_{0.7}N$) AlGaN PIN diodes with breakdown voltages in excess of 1600V [10].

Both GaN and AlGaN devices operate at high voltages and high frequencies in order to achieve high power densities in converter applications. As a demonstration test circuit, we created a GaN transistor-based 92V voltage converter switching at 1MHz with a power density of over 200 $W/in^3$. Since we are in the early stages of our device development cycle, we are not yet fabricating high current devices. However, work continues to extend operating capabilities to higher currents, voltages, and frequencies. To support this ongoing work, a test methodology has been developed that is both thorough and extendable.

## III. Testing Methodology

A multi-step test methodology has been developed for evaluating package performance and for de-embedding key performance metrics from underlying component performance metrics. The test plan contains the following steps:

1. Pre-packaging DC sweep of bare die components.
2. DC sweep of the empty package to determine breakdown voltage.
3. S-parameter testing of the empty package to determine frequency performance limiting package parasitics.
4. Packaged parts high voltage DC sweep test.
5. Testing of packaged components in the Buck Converter Tester to obtain operational frequency response characteristics of packaged components.
6. Testing of packaged components in the Double Pulse Tester for high current/ high voltage packaged component operational characteristics.

This test regime involves the use of three custom testers which we have developed specifically for this work. These are the 20-kV IV Tracer Tester, for performing high voltage DC sweeps; the Buck Converter Tester, for testing components in an operating power supply; and the Double Pulse Tester for obtaining high current and high temperature stress test results.

Our test capability and methodology has been under development concurrently with our semiconductor device development. Consequently, we have not tested all of the devices that we have fabricated with all of the same tests, and both our methodology and our testers are still under development.

## IV. 3D Printed Electronic Packages

When first starting development of (U)WBG semiconductor devices, we searched for high voltage electronic packages and found few commercially available options. As the processing and materials challenges of devices production yielded high voltage devices that did not carry very high currents, we needed packages with high breakdown voltages but only moderate current and power handling capabilities. Furthermore, packages with minimal parasitic capacitances and inductances were of extreme importance due to the high switching speeds needed for extreme SWaP improvements. It was determined that creating our own electronics packages was the most viable option for obtaining the necessary packages. To accomplish this, we developed a methodology for creating electronics packages using commercially available pins embedded in custom 3D printed insulating bodies.

A wide variety of pins suitable for use in electronics packages are available from manufacturers such as Amphenol, Keystone, Mill-Max, TE Connectivity, etc. As with most electronics packages, wire bonds are used for making at least some of the electrical connections from the pin to the die. In order to make an effective wire-bond contact, it is important to have a clean, oxide-free surface. This usually means that the pins used in the package should be plated with gold.

Our complete package fabrication methodology is as follows: Suitable pins for the package design are selected. Next, a model for that pin is created using the modeling software that will be utilized for the complete package. The main requirements of the modeling software are (1) that it is capable of generating 3D drawings, (2) that it can be used to create assemblies of separately created parts, and (3) that it can output a file format that is acceptable to the 3D printer that will be used. The most commonly used 3D file formats are STL and VRML. Most 3D printers will support either or both of these formats. After a model has been created for the pin(s), we create a model for the package body. For most 3D printers, the package body will be printed from a single material. Most materials available for 3D printers are low temperature thermoplastics, such as polyvinyl chloride (PVC). Packages made from PVC should not see temperatures higher than 140 $^oC$. If the package will see higher temperatures, it is important to use a high temperature thermoplastic, such as Ultem. Ultem uses a flame resistant resin and has a continuous service temperature of 170 $^oC$.

Once the 3D model for the package body has been created, at least five copies are printed in order to obtain data on package tolerance variations. We then assemble the complete

electronics package by pressing the pins into the package body. In order to obtain a good fit between pin and body, it is important to have the pin aperture sized to be slightly smaller than the pin diameter. The thermoplastic used for the body typically has adequate elasticity to hold the pin during subsequent use.

Figure 1 shows an example of a high voltage package developed for our wide bandgap semiconductor devices. This package is specifically designed to hold high voltage diodes. It uses three circular pins for each diode terminal, in order to increase the current carrying capability of the overall assembly. The high walls around the central cavity form a potting shell. We use DP270, Scotch Weld, a 3M product, for potting the devices, after they have been installed and wire-bonded to the package pins. The fin added to the bottom of the package is intended to increase the package breakdown voltage by creating a longer, more tortuous discharge path between the exposed package pins.

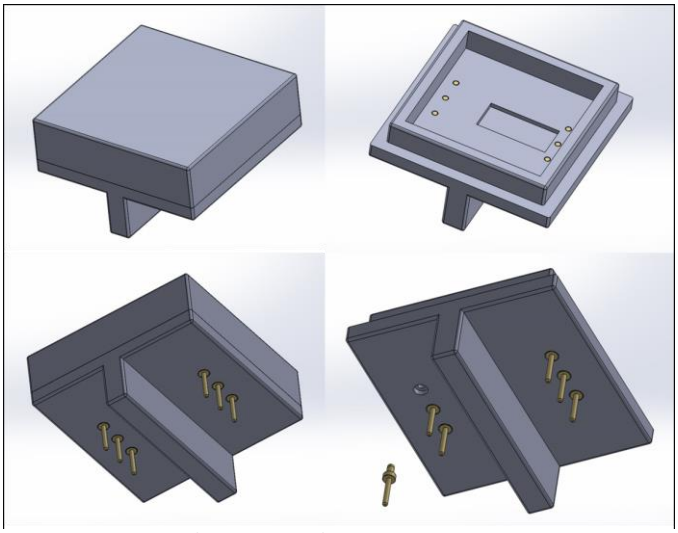


**Figure 1: (clockwise from upper left) 3D printed high voltage package, top view; package with lid removed; bottom view showing pin insertion; bottom view fully assembled**

## V. Package Impedance

One of the advantages of WBG and UWBG materials are the very fast rise times for power electronic devices on the order of 10 ns [3]. In conjunction with other features of the devices, this allows much higher frequency switching than is possible with more mature devices. However, placing these devices into a package with excess parasitic inductance would slow the response and prevent the gains that could be achieved. Given the relationship of $t_r \cong 0.34/\omega_C$, which relates rise time $t_r$ to the cut-off frequency $\omega_C$, a 10 nsec rise time would correspond to a cut-off frequency of approximately 34 MHz. It is therefore necessary that the package impedance be consistent with the desired frequency response to achieve the target device rise time.

A network analyzer was used to find the frequency dependent behavior of the package under different conditions. Calibration of the analyzer was done in a two phased manner. First, the analyzer was calibrated to the end of an SMA cable. Then it was calibrated with the cable connected to printed circuit boards (PCBs) with an open circuit, short circuit, and 50 Ω load over a 5 Hz to 2.2 GHz range. These boards were designed to mount the HVPackage6 and provide an output to a slip-on SMA connector.

Once the analyzer had been calibrated for the board, the package was mounted and tested with an open circuit, short circuit, and a 50 Ω load over a 5 Hz to 2.2 GHz range. The S11 measurement of the reflection coefficient is shown in the Smith chart of Figure 2. As seen in the open circuit plot, the package is a mostly capacitive device that has a noticeable loss component and negligible inductive component. However, this loss doesn't become an issue until higher frequencies. A rise time on the order of 10 ns would require a bandwidth of approximately 34 MHz.

Figure 3 shows the impedance magnitude and phase for the three cases as found from the measure reflection coefficients by the equation: $Z = Z_0(1-S_{11})/(1+S_{11})$ where $S_{11}$ is the reflection coefficient as read by the network analyzer and $Z_0$ is the cable impedance of 50 Ω. As seen in the graph, none of the effects due to impedance are really noticeable until above 100 MHz which is well above the 34 MHz required for UWBG semiconductor devices. There is a noticeable change in the phase angle of the short circuit case due primarily to numerical error in 2 points.

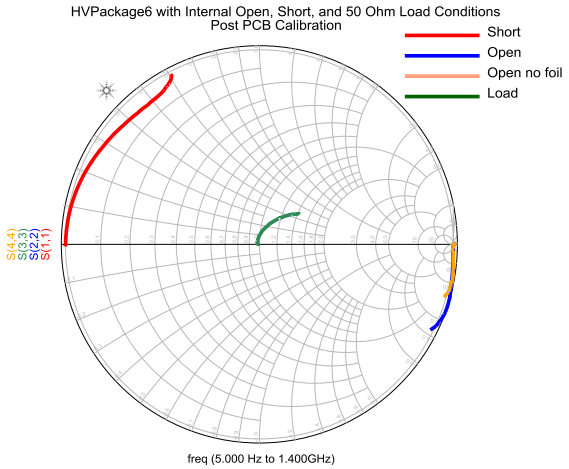
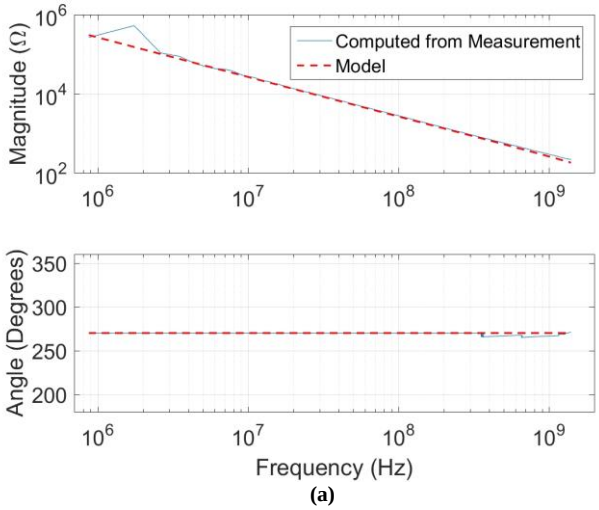
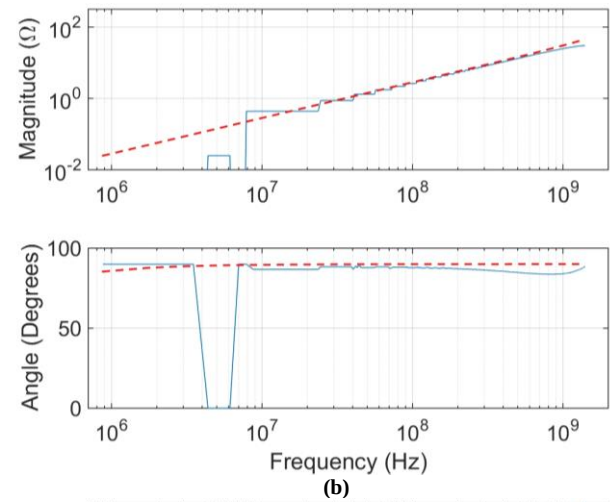


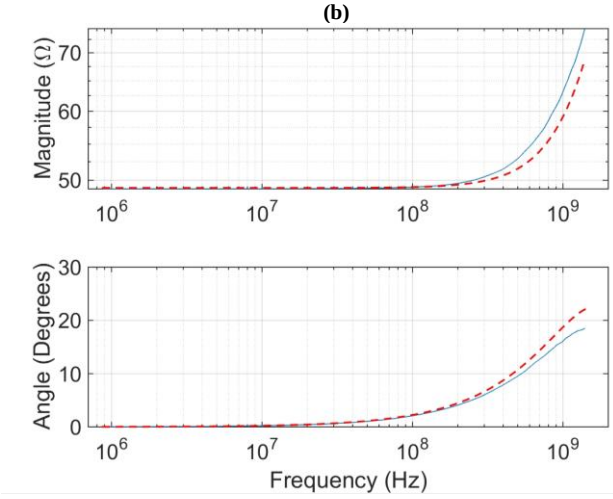

**Figure 2: HVPackage6 with Internal Open, Short, and 50 Ohm Load**




**(a)**




(b)




(c)

**Figure 3: Impedance magnitude and phase for (a) Internal Open, (b) Short and (c) 50 Ohm Load**

In order to find the package impedance at high frequency and construct an equivalent circuit, parameters were fit to the impedances. The resulting equivalent circuit is shown in Figure 4 with R equal to 0.001 Ω, $L_1$ equal to 1 nH, $L_2$ equal to 3.5 nH, and a C or 0.6 pF.

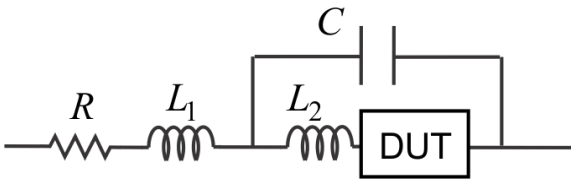



**Figure 4: Package Parasitic Model**

## VI. 20 kV IV-Tracer Testbed

In order to test the voltage breakdown of high voltage devices and packaging, a 20 kV IV tracer was constructed by connecting a high-voltage power supply, a digital multimeter, and a picoammeter to a supervisory computer through GPIB and USB interfaces, as illustrated in Figure 5. Specifically, a Glassman EJ series high voltage supply applies a commanded voltage across the device under test (DUT).

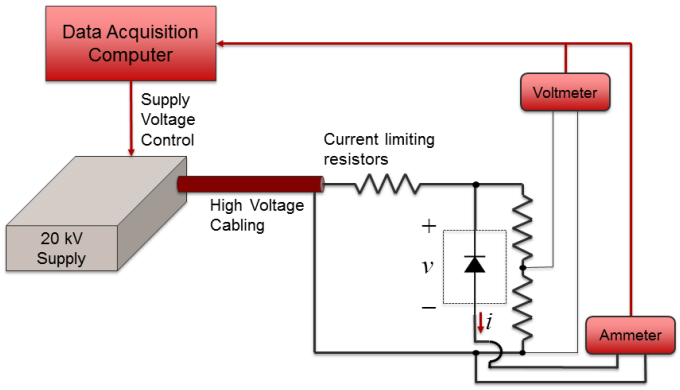



**Figure 5: IV tracer schematic**

The selected power supply has a 20 kV range and can supply up to 600 W to the circuit. Additionally, the power supply can be operated from a standard 120 V 60 Hz AC plug [11]. An Agilent 34401 precision digital multimeter is used to measure the voltage drop across the diode. The multimeter is limited to 1000 V [12], so a calibrated voltage divider was placed in parallel with the DUT. The voltage divider uses a 100 MΩ KDI Pyrofilm PVC resistor in series with a total of 10 MΩ resistance [13]. Accounting for the multimeter input impedance, the divider scales down the applied voltage by approximately 21:1. The circuit also includes a 10 MΩ current limiting resistor at the output of the power supply. This ensures that even if the device under test fails as a short at full voltage no more than 2 mA will be drawn from the power supply. A Keithley 6485 picoammeter is connected in series with the DUT to measure current [14].

To ensure worker safety, several precautions have been added to the test bench. An enclosure (see Figure 2) has been constructed around the power supply, test circuit, and measurement equipment so that the high voltage is isolated when in operation. The power supply has an interlock connected to the door of the enclosure that will prevent the application of high voltage. Warning signs are also posted and a light will flash when the power supply is active.


**Figure 6: IV tracer hardware**

A data acquisition computer is used to obtain data from the meters and to control the supply voltage. This computer runs a LabVIEW program to set the voltage through a USB interface while obtaining measurement information through a GPIB (IEEE-488) interface. The method of applying voltage can be modified to accommodate either a continuously increasing voltage or a pulsed voltage. Data is captured in MATLAB-compliant data files. To mitigate ionization and corona effects on the IV tracer components themselves, the circuit design incorporates brass balls at each point of connection, large distances between components, and a well-isolated base to support each component.

In order to test the effects of temperature, the device under test has been placed inside of a high voltage oven. The oven is capable of heating components above 800 ºC and applied voltages over 20 kV.

## VII. Voltage Sweep of Parts at High Temperature

Due to the availability, the empty packages were mounted on Kapton film that had been laminated to copper sheets using SAC305 lead free solder. Since the melting range of SAC305 is 217 ºC-220 ºC, temperature was limited to 200 ºC to avoid melting the solder. This is also a little above the glass transition temperature of the package material to push the capabilities of the package. Voltage sweeps of the part were then conducted with the oven set to 40 ºC, 75 ºC, 100 ºC, 150 ºC, and 200 ºC. To reduce signal noise added by the oven, the data was then put through a 5-point fast average filter.

Figure 7 shows the currents as voltage is swept. Room temperature breakdown for the part is around 13 kV. This breakdown through air, as shown in Figure 8, is caused by the geometry of the part. As temperature is increased the hold off voltage significantly decreases. Additionally, at higher temperatures there is an increased leakage current. This leakage is probably through the part, since the magnitude of the current approaches 4 µA without causing avalanche.

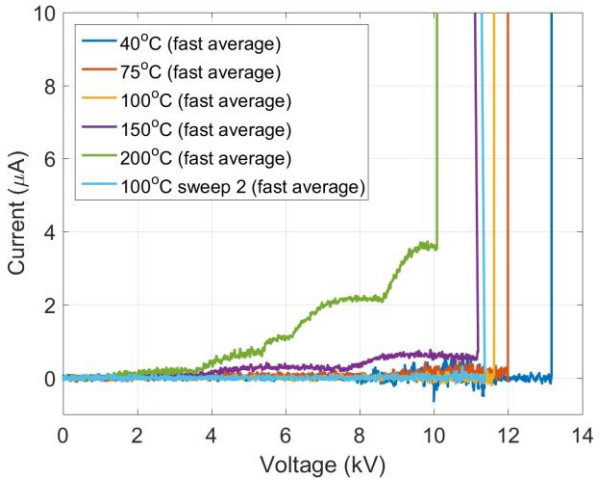



**Figure 7: Voltage hold-off over a range of external temperatures**

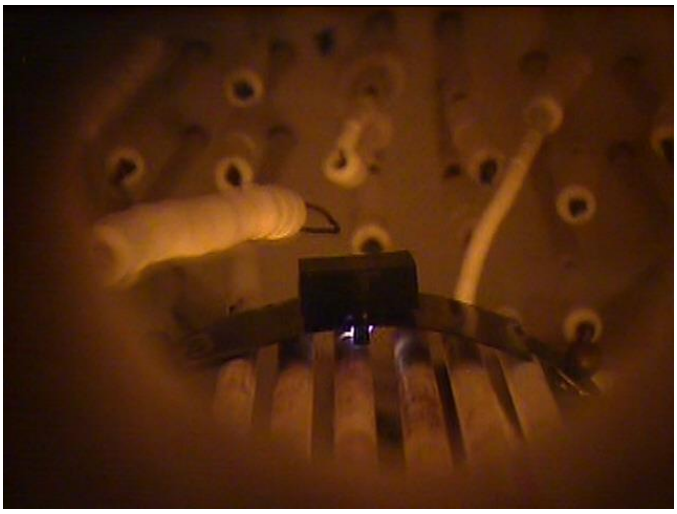


**Figure 8: Voltage breakdown through air for a part held at 200 ºC**

## VIII. Conclusions and Future Work

This paper shows the development of a miniaturized high voltage part for use with wide bandgap semiconductors. The part was constructed using high temperature resistant materials and tested under extreme conditions. In addition, to prevent the parasitic impedance of the package from slowing device switching, the package was designed to have very low insertion impedance at frequencies below 100 MHz. Test results using a Network analyzer verify the low impedance characteristic. High-temperature/high-voltage test results show that increasing temperature results in lower voltage hold-off and greater leakage current.

In order to support the future developments of WBG and UWBG semiconductor devices, packaging such as that presented in this paper will need to be additionally tested before wide use. Long duration application of high voltage and temperature conditions will be needed to test reliability. The resiliency of packaging to ultraviolet light and radiation should also be studied.

## IX. Acknowledgements

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