Tribological Reliability of Multi-Layer Thin Films on MEMS

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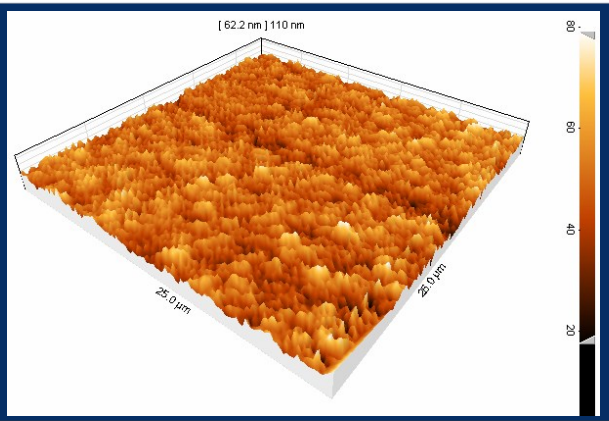

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Motivation

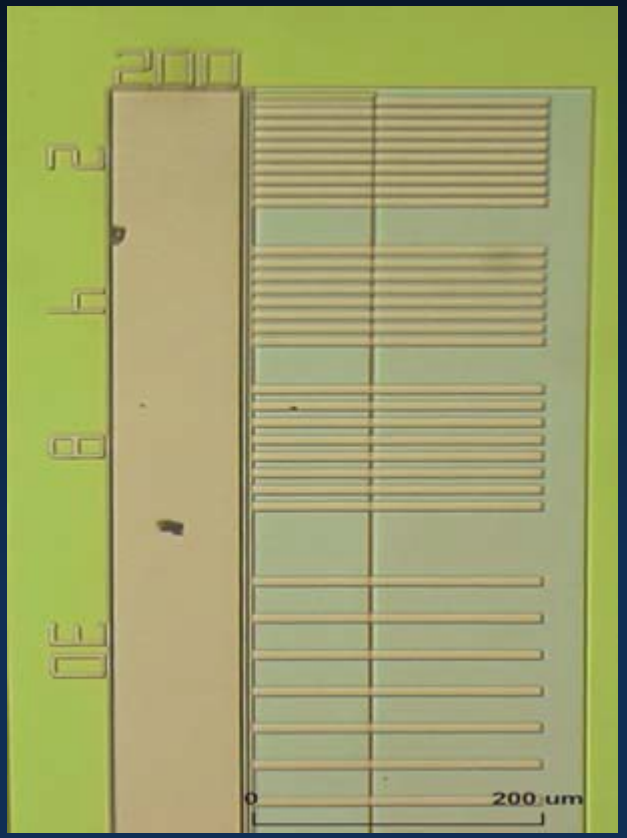
- The Au coating must resist damage due to friction in the microelectromechanical systems (MEMS) applications.
- The purpose of the study was to examine the tribological reliability of the Au coating on a polysilicon substrate with a layer of Cr between the two – resistance to indenter scratching in particular.

Work done

1. Nano-scratch tested poly-Si MEMS substrate (baseline)
2. Vapor deposited Cr and Au on the poly-Si
3. Nano-scratch tested the tri-layer Si-Cr-Au thin film
4. Investigated the failure (scratch) mechanism.

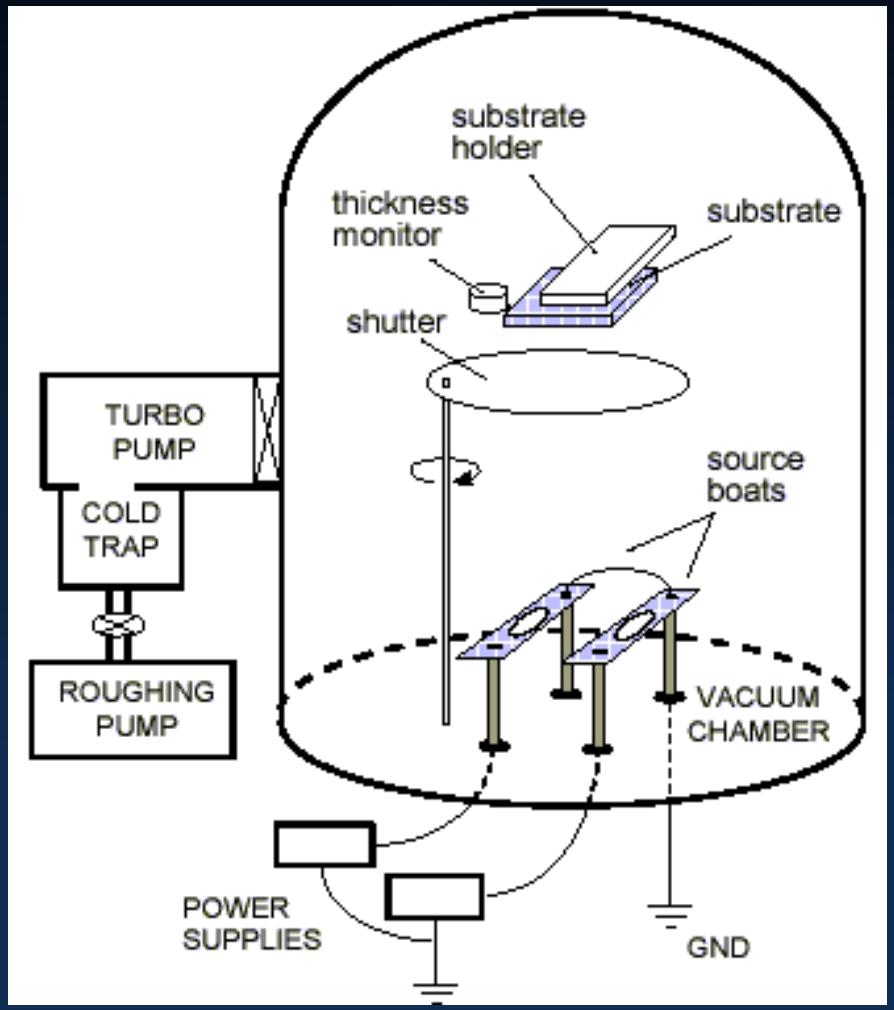
A sliding electrical contact on a MEMS needed gold-plating.

- Au-plating was needed for consistently low electrical contact resistance.
- The Au layer will rub against a rough Si surface in the operation of the MEMS.
- Au is much softer than Si.
- Wear must be minimized.
- Question: is Au-plating comparable to Si in scratch resistance?



On the poly-Si, Physical Vapor Deposition (PVD) deposited Cr and Au

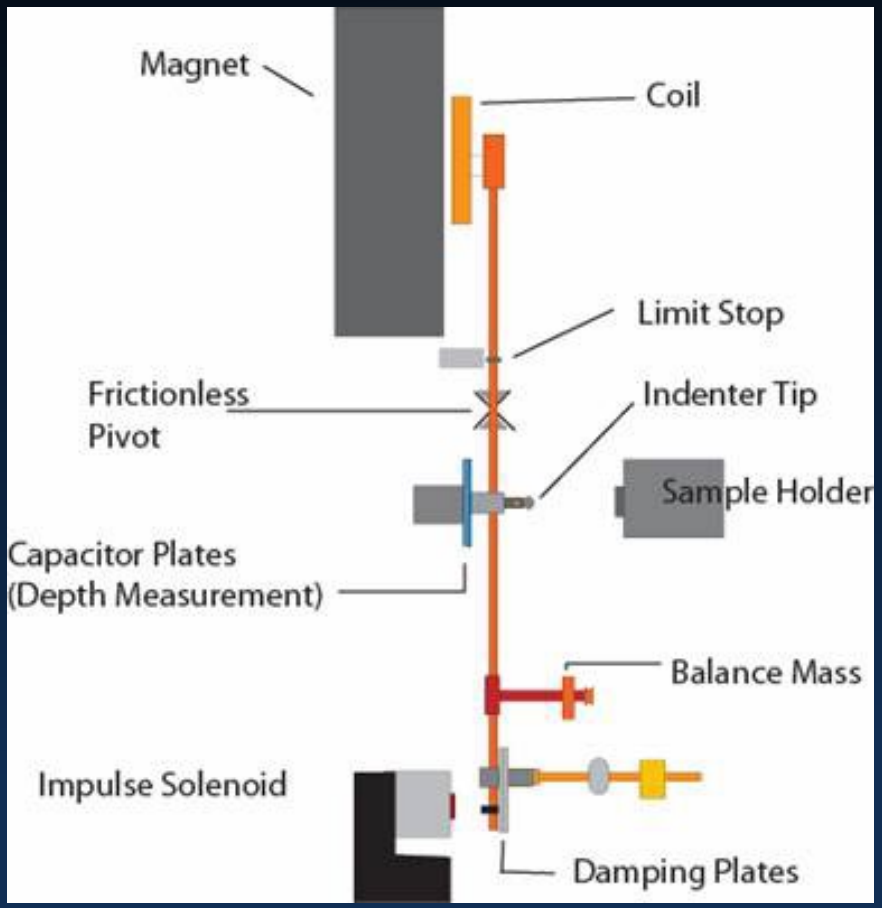
- Joule-heating melted and evaporated the coating metal in a source boat.
  - ~1600^{o}C
- Vacuum facilitated evaporation and travel of metal vapor from the boat to the target substrate.
  - 10E-5Torr.
- Very thin layer of Cr enhances adhesion between Si substrate and Au top layer.
  - Dendritic structure



https://stuff.mit.edu/afs/athena.mit.edu/course/3/3.082/www/team2_f02/Pages/PVD.gif

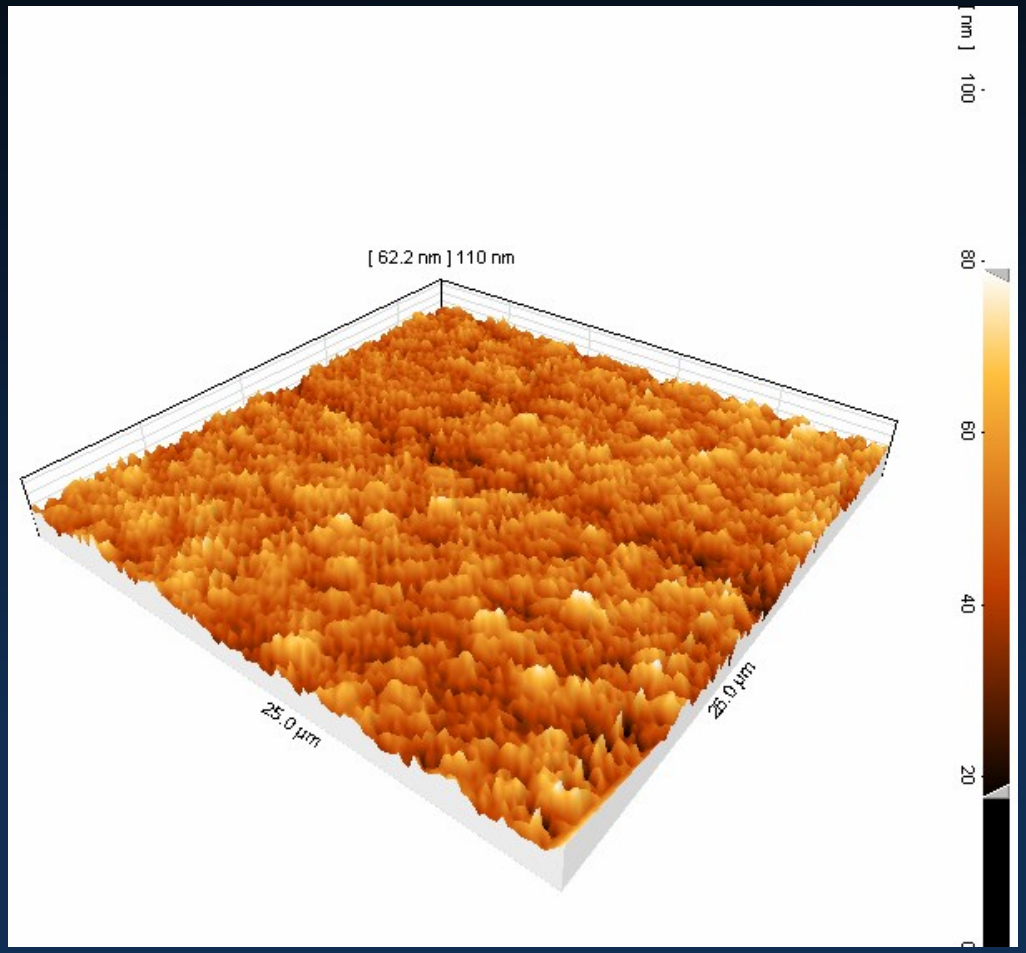
A nano test system measured scratch resistance

- Scratch testing used a nano test system
- Three-pass mode
- Linear ramp-up load
- Measured poly-Si substrate (baseline) and Si-Cr-Au tri-layers.



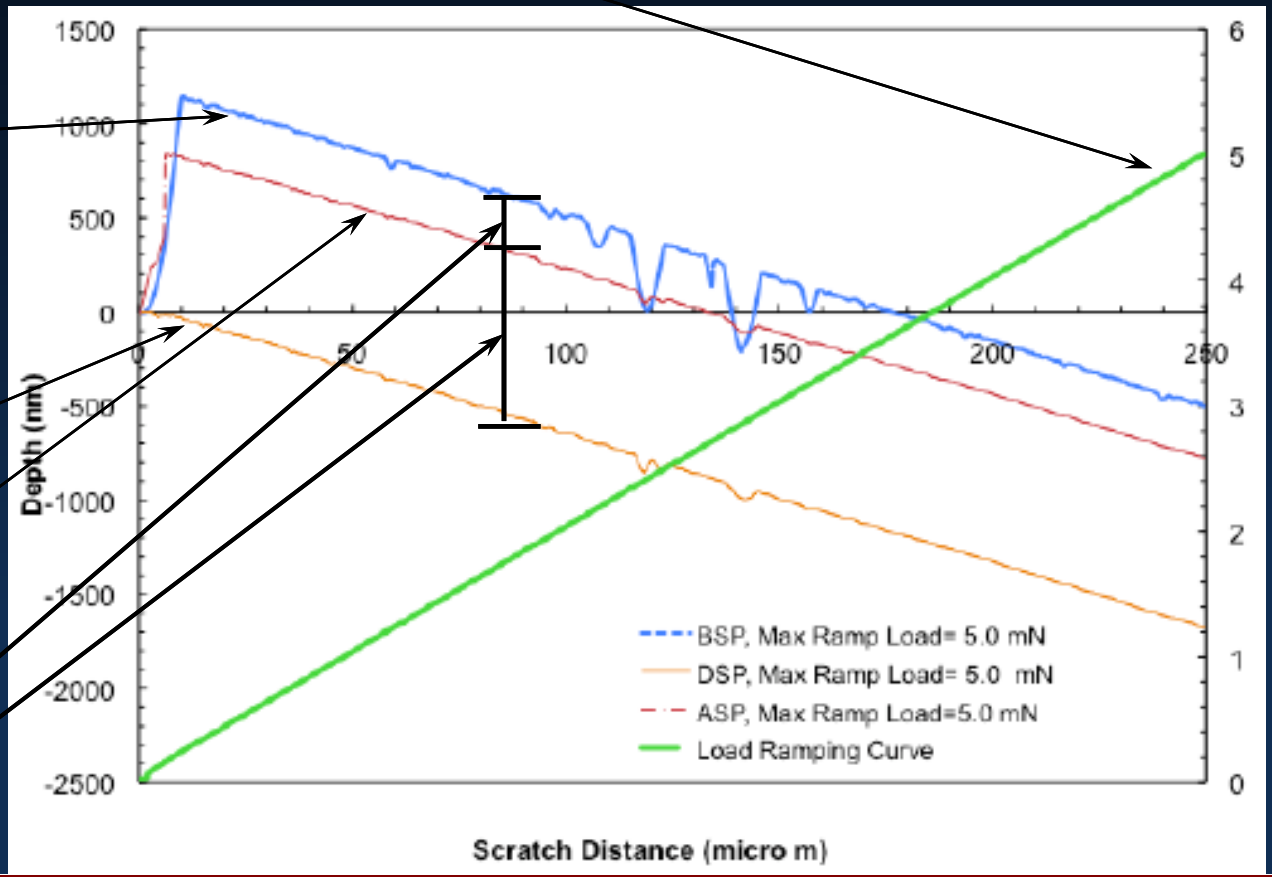
The Si-Cr-Au tri-layers were scratched with a linearly increasing load

- Spherical indenter dragged on surface.
- Atomic Force Microscope (AFM) scans the surface *in-situ* during the scratching.
- Scratch length 100 µm.
- Speed 500 nm/s



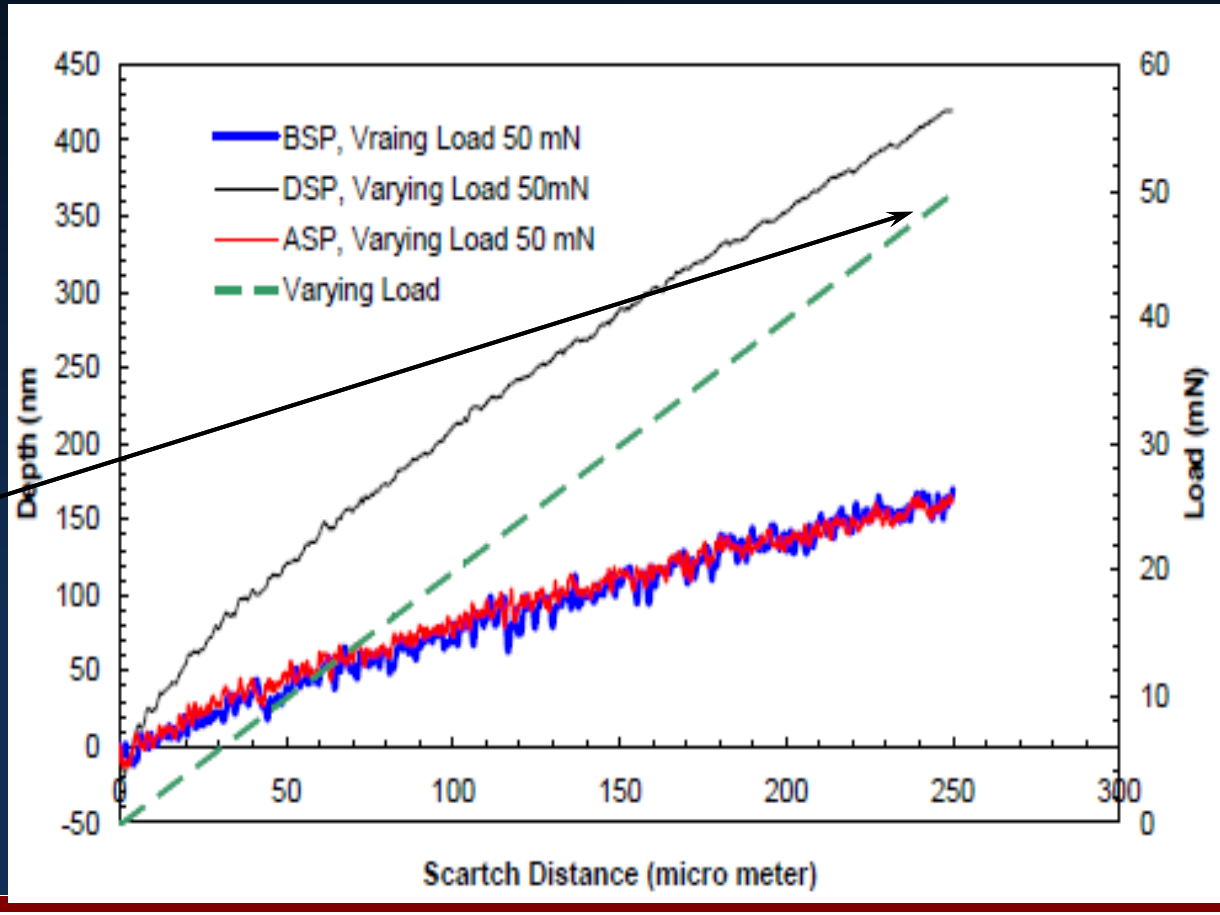
The tri-layers suffered permanent scratch

- On the Si-Cr-Au tri-layers, the normal load on the nano-scratcher was ramped up from ~0 to 5mN.
- Before scratching, the position (tilt) of the tri-layers was scanned.
- In-situ scanning during scratching
- After scratching
- Plastic deformation
- Elastic recovery



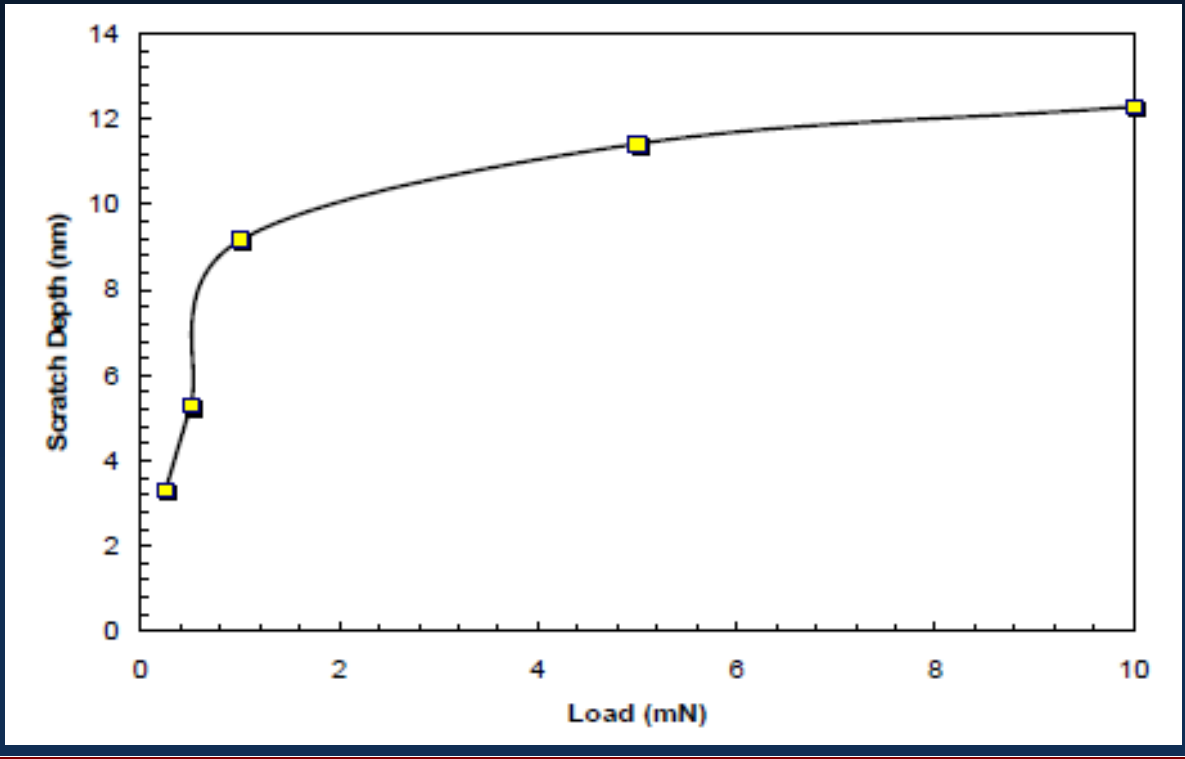
For baseline hardness data, Poly-Si substrate had also been scratched

- To cause a scratch depth of 400 nm On the Si-Cr-Au tri-layers, the normal force was 5mN.
- On the Si substrate, that force was 50mN.
- Moreover, the Si substrate recovers elastically.



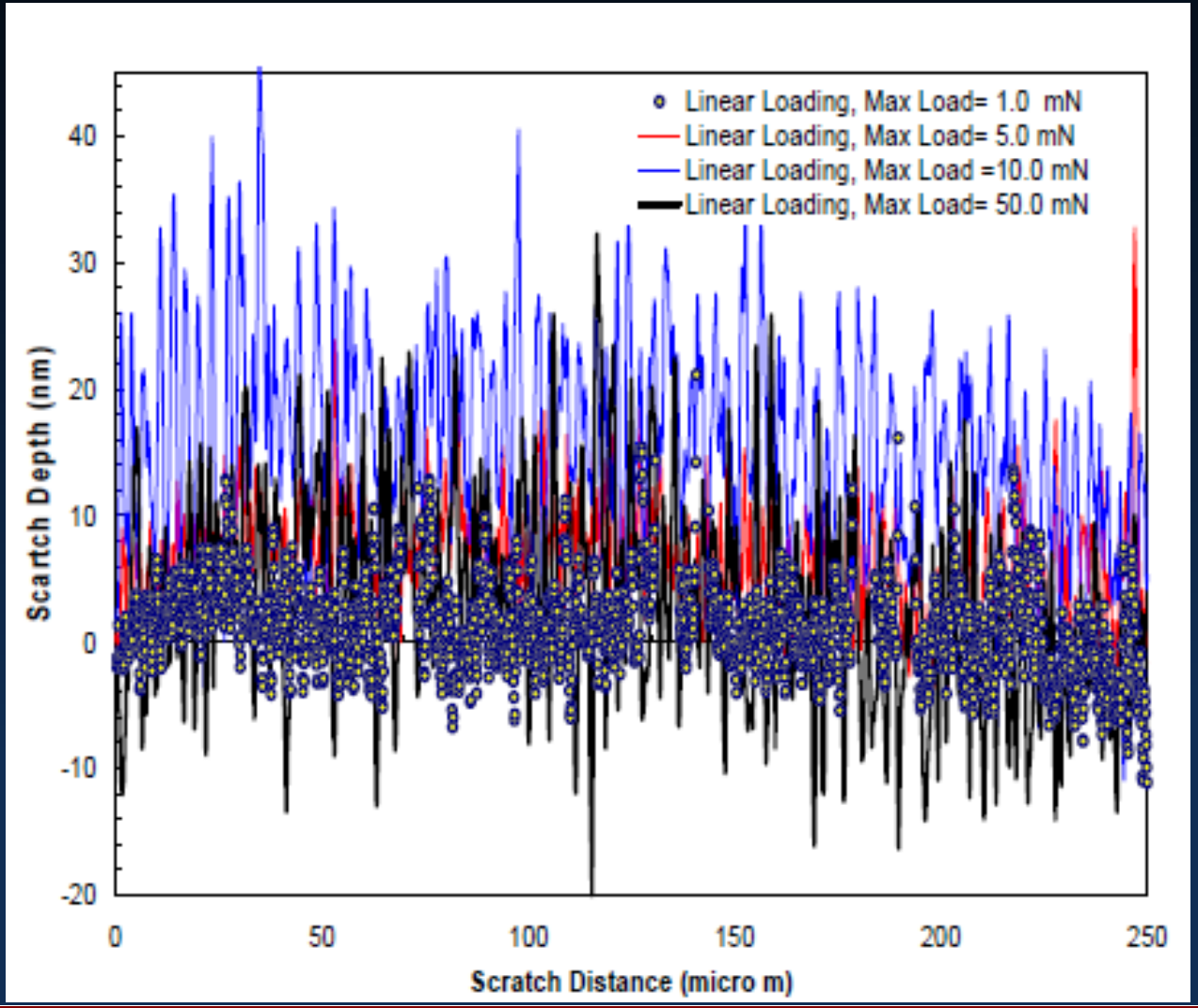
The scratch on the Si substrate does not increase linearly with load.

- Increasing load from 0 to 1.5 mN resuled in rapid increase in scratch depth
- Further load increase resulted in slow increase in scratch depth.
- Scratches in Si substrate << scratch depth in Cr+Au.
- Hardness of Si >> hardness of Cr+Au.



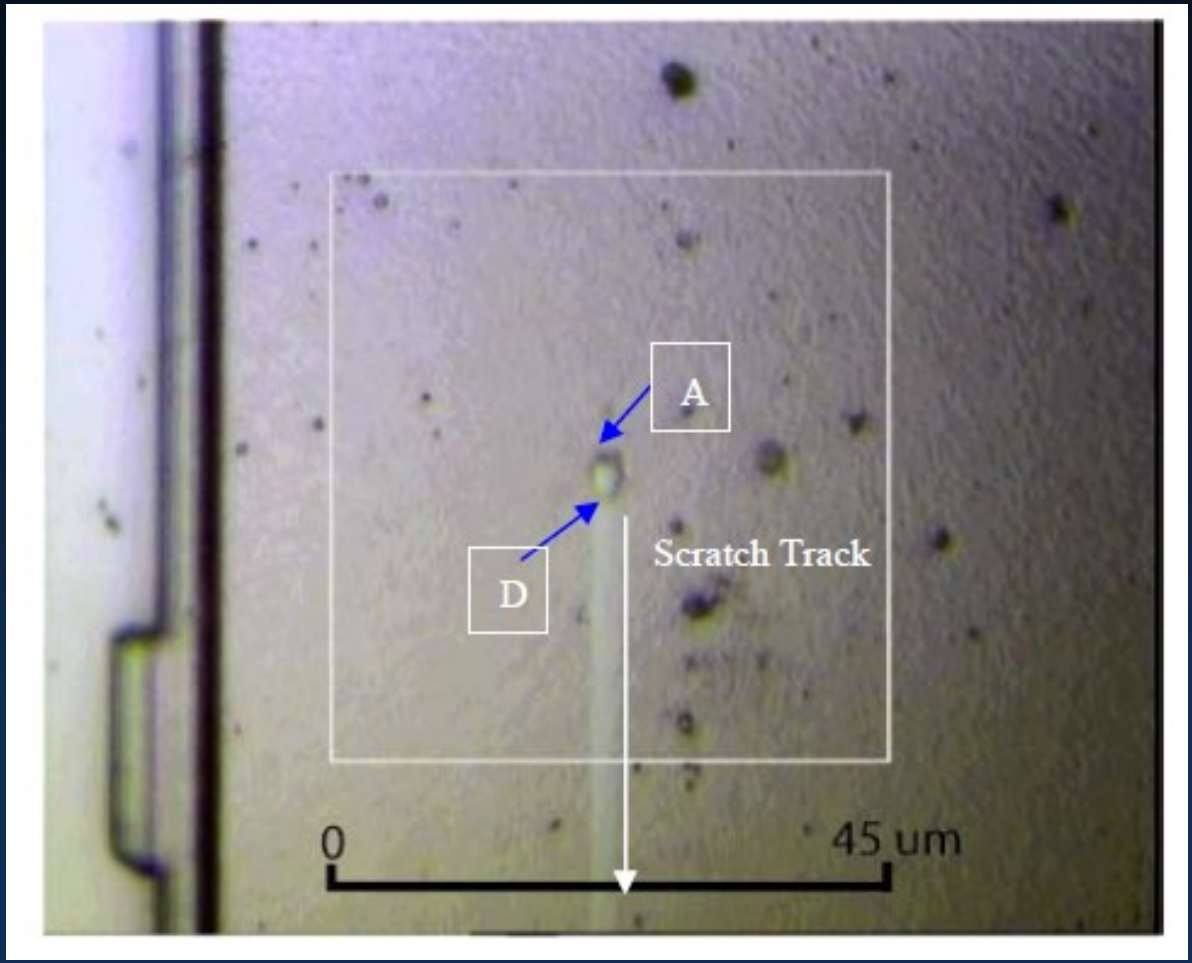
Gold plating degrades the scratch resistance of the MEMS device by a lot.

- Constant loads verified further that Poly-Si substrate shows little/no plastic deformation below 10 mN load.
- In contrast, the Si-Cr-Au tri-layers was damaged at < 1mN



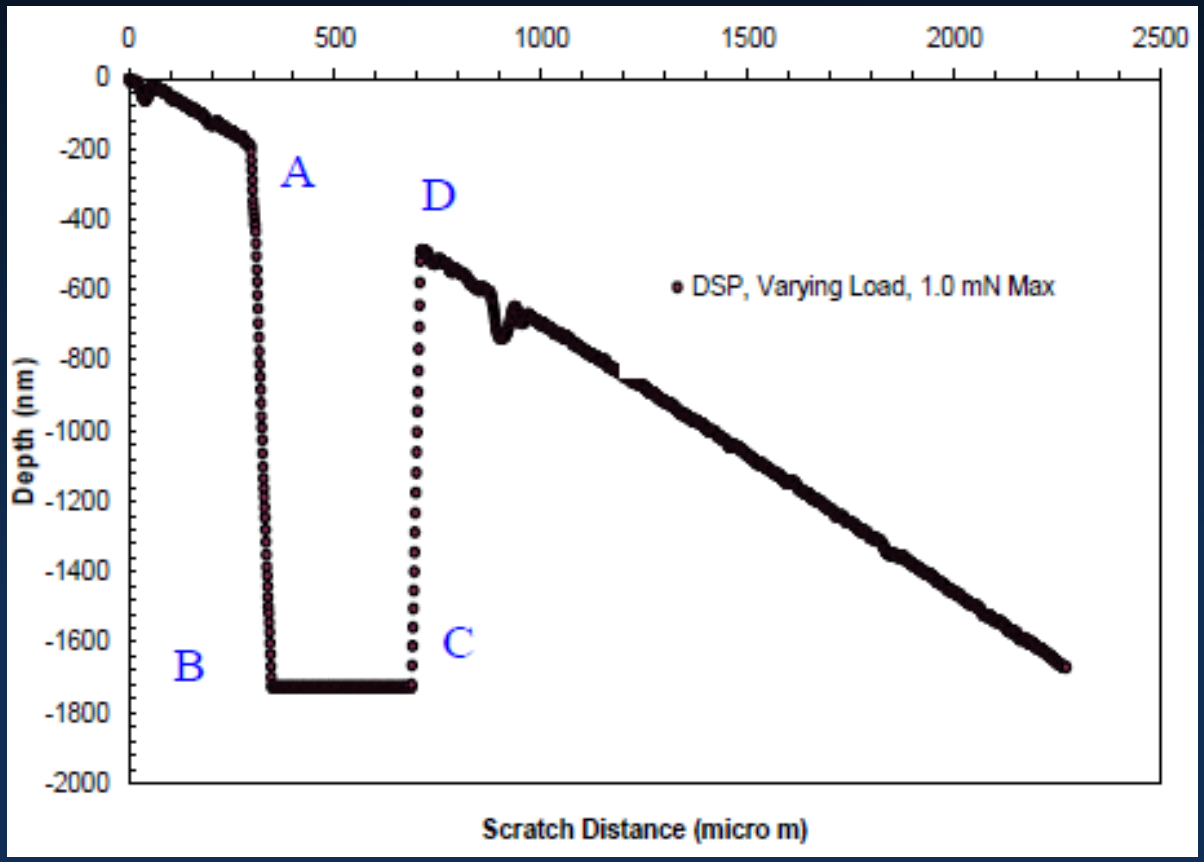
Porosity is another problem with the gold plating process.

- Porosity flaws were visible with an optical microscope.
- (How) did porosity affect the nano-scratch test?



The Nano-Scratch test procedure is robust against porosity.

- Outside of the porosity hole (A-B-C-D), the *in-situ* AFM profile measurement under test follows a fairly smooth line.



Conclusions

- Gold plating degrades the scratch resistance of the MEMS device by a lot.
- The Si substrate deformed at ~10X the force on the Au layer.
- Moreover, most of the Si deformation recovers elastically, while the Au is damaged permanently.
- Nano-scratching has decisively differentiated the scratch resistance of the gold plating against the scratch resistance of the Si substrate.
- Nano-scratching is robust against holes in the gold plating layers.