Analysis of Fixed Duty Cycle Hysteretic Flyback Converter for Firing Set Applications

Tom Love, Sandia National Laboratories

***Abstract* -- This paper analyzes several performance aspects of the fixed-duty-cycle, hysteretic flyback converter topology typically used in firing sets. Topologies with and without active pulse-by-pulse current limiting are considered, and closed-form expressions in terms of basic operating parameters are derived for each of the following:**

1. **Peak switch current, I_p**
2. **Amplitude of output ripple, ΔV_{out}**
3. **Ripple in output capacitor stored energy, ΔE_{out}**
4. **Period of output ripple, T_{hyst}**
5. **Output voltage at i^{th} switch cycle, $V_{out}(i)$**
6. **Number of cycles, n, for output to charge to a given voltage**

Theoretical results are then verified by comparison with both simulation and measurement data.

I. Introduction

Detonator ignition depends on short, high-energy pulse(s), typically delivered from a capacitor charged to several kilovolts and then discharged abruptly into the detonator(s) via special switches. In the system considered here, this high-voltage charge is developed by means of a fixed-duty-cycle, hysteretic flyback converter. Though the flyback converter topology is well-documented, the hysteretic, fixed-duty cycle control approach is somewhat unusual, and while a handful of SAND reports [see references (1) (2) (3) (4)] discuss aspects of its operation, none offers derivations of the equations provided here, the goal being not only to provide such equations in terms of basic variables, but also to give their derivations starting from first principles.

Figure 1 provides a functional diagram of a simple flyback converter with one secondary output and active pulse-by-pulse current limiting. Switch current is sensed by current sense resistor R_s, and the resulting current sense waveform is fed back to a current-sense comparator. Output voltage is passed through an attenuator of gain K and the resulting waveform fed back to a voltage-sense comparator. As long as neither the current sense waveform nor the output voltage feedback waveform exceed their respective comparator thresholds, a gate-drive pulse drain of fixed duty cycle, D, exercises the primary power switch. If in the course of a single switching period the sensed inductor current reaches the current limit threshold, switch on-time is terminated for the remainder of that switching period. If the current limit is not reached during a given switching period, the power switch remains on until on-time reaches $D*T_{sw}$, at which point it turns off for the remainder of the cycle. A typical value for switching period is around 20usec, implying a switching frequency, f_{sw}, of around 50 kHz.

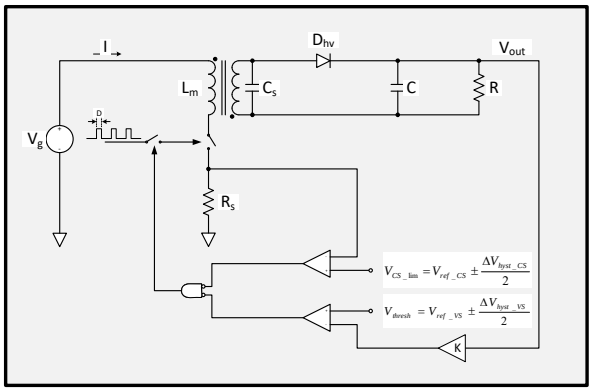

Figure 1, Functional Diagram, Flyback Converter

During the switch on-time, the input voltage, V_g, is applied across the flyback transformer's primary, causing current to build up in the inductor. If the switching period is much smaller than the primary time constant, the increase in inductor current is essentially linear, reaching some peak value, I_p, by the end of the switch on-time. Noting that the negative polarity of the flyback transformer secondary relative to the primary, and noting the orientation of the high-voltage rectifier, D_{hv}, it is apparent that no current flows in the transformer secondary winding during the switch on-time. Instead, energy is stored in the transformer's magnetic field. As the primary-side power switch opens and the current ceases to flow in the primary, inductive behavior causes the transformer secondary voltage to rise to a diode drop above the voltage across the high-voltage output capacitor, C. As it

Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

does, the current ending in the primary begins to flow in the secondary, reduced in amplitude by the transformer turns ratio.

When the output voltage across C reaches the upper threshold of the voltage sense comparator, the gate-drive pulse train to the primary power switch is terminated, effectively holding the converter off. During this interval, small current flows in bleed resistor, R, causing the voltage across C to fall until it crosses the lower voltage sense threshold, at which point the comparator turns off and the gate-drive pulse train is again applied to the primary power switch. The hysteretic charge-discharge cycle causes a steady-state hysteretic ripple in the output voltage waveform. This continues until such time as a trigger pulse is received and the capacitor is discharged completely into the detonator(s). Figure 2 shows a typical output voltage waveform, exhibiting both the exponential rise as the capacitor charges from zero volts to the upper voltage level, and the steady-state hysteretic ripple. Figure 3 shows the same data again, but zoomed in to show the hysteretic ripple in more detail.

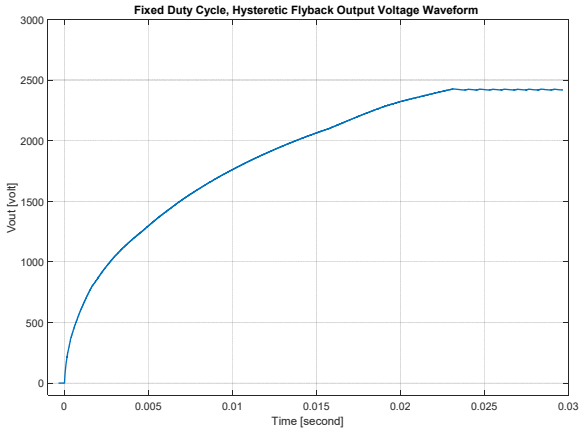

Figure 2, Waveform, Flyback Output Voltage

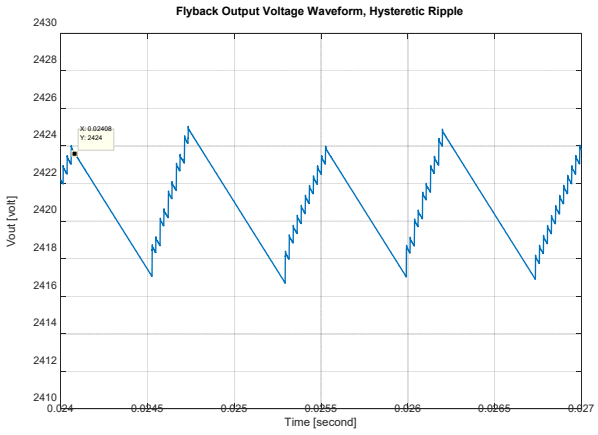

Figure 3, Waveform, Hysteretic Ripple, Output Voltage

II. VARIABLE DEFINITIONS

Variables used herein are defined as follows:

C.....Load capacitance [farad]

C_s.....Sum of transformer secondary winding capacitance and junction capacitance of high-voltage diode [farad]

D.....Fixed, programmed duty-cycle of the converter power switch [unitless]

ΔE_{cycle}.....Net increase in energy stored in load capacitance during a single switching period

ΔE_{cycle_Cs}.....Energy stored in C_s during a single switching period

ΔE_{cycle_n}.....Energy lost each switching cycle (in C_s and R)

ΔE_{cycle_p}.....Energy delivered to converter's secondary network during a single switching period

ΔE_{cycle_R}.....Energy lost to dissipation in R during a single switching period

ΔE_{out}.....Change in energy stored in C due to steady-state hysteretic ripple in output voltage

E.....Energy, or specifically, the energy stored in a capacitance

E_{max}.....Maximum energy stored in C, corresponding to V_{out_max}

E_{min}.....Minimum energy stored in C, corresponding to V_{out_min}

f_{sw}.....Switching frequency as measured at the converter power switch

i.....Index used to count consecutive switching cycles

I_{disch}.....Discharge current in C due to R

I_p.....Peak inductor current

I_{p_CL}.....Peak inductor current programmed by the chosen current sense comparator threshold

I_{p_D}.....Peak inductor current that would flow if switch on-time were allowed to reach $D*T_{sw}$

K.....Gain of voltage feedback attenuator, typically a resistive divider

K_1.....Coefficient on $V_{out}(i-1)^2$ associated with output energy lost each cycle

K_{2_CL}.....Term added to $V_{out}(i-1)^2$ associated with output energy gained on the ith cycle in the case that the active pulse-by-pulse current limit is reached (i.e. if $I_{p\_CL} < I_{p\_D}$)

K_{2_D}.....Term added to $V_{out}(i-1)^2$ associated with output energy gained on the ith cycle in the case that the active pulse-by-pulse current limit is NOT reached (i.e. case when full programmed duty cycle is reached, $I_{p\_CL} > I_{p\_D}$)

L_m.....Primary magnetizing inductance of flyback transformer

n.....Number of switching cycles required for C to charge to $V_{out}(n)$

n_{CL} ..... Number of switching cycles required for C to charge to $V_{out}(n)$, assuming active pulse-by-pulse current limiting ($I_{p\_CL} < I_{p\_D}$)
n_D ..... Number of switching cycles required for C to charge to Vout(n), assuming switch on-time of $D*T_{sw}$ (i.e. $I_{p\_CL} > I_{p\_D}$)
n_{rise} ..... Number of switching cycles required for C to charge from V_out_min to V_out_max
R ..... Load resistance
R_{lower} ..... Resistance of lower leg of output voltage feedback divider
R_s ..... Current sense resistance
R_{upper} ..... Resistance of upper leg of output voltage feedback divider
Δt_{fall} ..... Time associated with the portion of hysteretic output voltage ripple when voltage falls from V_{out_max} to V_{out_min}
Δt_{rise} ..... Time associated with the portion of hysteretic output voltage ripple when voltage rises from V_{out_min} to V_{out_max}
t_{chg} ..... Time required for C to charge from 0V to V_{out}
t_{chg_CL} ..... Time required for C to charge from 0V to V_{out} assuming, assuming active pulse-by-pulse current limiting ($I_{p\_CL} < I_{p\_D}$)
t_{chg_D} ..... Time required for C to charge from 0V to V_{out} assuming, assuming switch on-time of $D*T_{sw}$ (i.e. $I_{p\_CL} > I_{p\_D}$)
T_{sw} ..... Switching period as measured at the converter's power switch
ΔV_{hyst_cs} ..... Total hysteresis in current sense comparator reference voltage
ΔV_{hyst_vs} ..... Total hysteresis in voltage sense comparator reference voltage
ΔV_{out} ..... Peak-to-peak change in V_{out} associated with steady-state hysteretic ripple
V_{CSlim} ..... Threshold or reference voltage at the current sense comparator, which determines at what current sense voltage comparator terminates switch on-time
V_g ..... Converter input voltage
V_{out_avg} ..... Steady-state average of output voltage waveform
V_{out_max} ..... Maximum output voltage associated with the peak of the hysteretic ripple
V_{out_min} ..... Minimum output voltage associated with the valley of the hysteretic ripple
$V_{out}(n)$ ..... Output voltage at the end of the n^{th} switching cycle

III. PEAK INDUCTOR CURRENT

Assuming that the switch on-time is small compared to the effective time constant associated with the flyback transformer's primary magnetizing current, the rise in inductor current will be governed by the following equation:

$$V = L_m \frac{\Delta I}{\Delta t} \quad (1)$$

Solve (1) for ΔI:

$$\Delta I = \frac{V \cdot \Delta t}{L_m} \quad (2)$$

Assuming discontinuous conduction mode wherein inductor current returns to zero before the end of each switching period, peak current equals the total change in current during the switch on-time. Treating first the case where the primary switch remains on for the full programmed duty cycle (i.e. the current limit threshold is not reached), designate this peak current as I_{p_D}, and rewrite (2) as follows:

$$I_{p\_D} = \frac{V \cdot \Delta t}{L_m} \quad (3)$$

Letting the input voltage be designated as Vg, and noting that $\Delta t = D*T_{sw} = D/f_{sw}$ (since $T_{sw} = 1/f_{sw}$), (3) becomes the following:

$$I_{p\_D} = \frac{V_g \cdot D}{L_m \cdot f_{sw}} \quad (4)$$

In the case when the current limit is reached, let the peak current be designated as I_{p_CL}, and note that at the current limit threshold, the current sense comparator's reference voltage equals $I_{p\_CL}*R_s$, where R_s is the current sense resistance. This allows I_{p_CL} to be defined in terms of the current limit reference, V_{CS_lim}, and R_s:

$$I_{p\_CL} = \frac{V_{CS\_lim}}{R_s} \quad (5)$$

Then for general operating conditions, the peak current, Ip, equals the lesser of I_{p_D} and I_{p_CL}:

$$I_p = \min\left(I_{p\_D}, I_{p\_CL}\right) \quad (6)$$

IV. OUTPUT VOLTAGE RIPPLE

As described earlier, after the output voltage first crosses the level, V_{out_max}, corresponding to the upper voltage sense comparator threshold, the converter shuts off and the output falls approximately linearly until it crosses the level, V_{out_min}, corresponding to the lower voltage sense comparator threshold. It then oscillates between these upper and lower limits, causing the output voltage waveform to ripple between V_{out_max} and V_{out_min}. This behavior was shown in the simulation waveform provided in Figure 3, above, and is diagramed below in Figure 4.

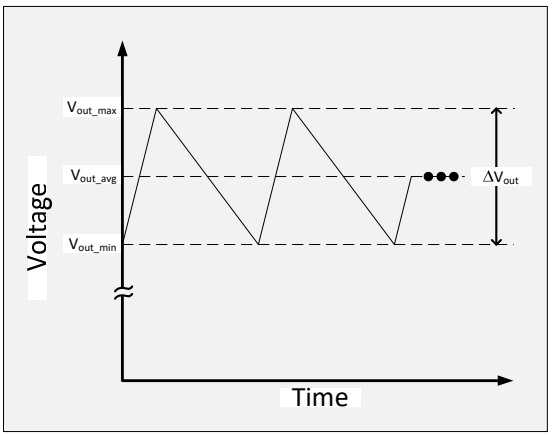

Figure 4, Waveform Diagram, Output Voltage Ripple

Let the amplitude of the ripple be designated ΔV_{out}, and let the difference between the upper and lower voltage sense comparator thresholds be designated ΔV_{hyst_vs}. If the gain of the voltage feedback attenuator is called K, then ΔVout and ΔV_{hyst_vs} are related by the following equation:

$$\Delta V_{out} = \frac{\Delta V_{hyst\_vs}}{K} \quad (7)$$

If the feedback attenuator is a resistive divider made of upper and lower resistances, R_{upper} and R_{lower}, respectively, then K can be written as follows:

$$K = \frac{R_{lower}}{R_{lower}+R_{upper}} \quad (8)$$

Substitute (8) into (7) and simplify:

$$\Delta V_{out} = \left(1 + \frac{R_{upper}}{R_{lower}}\right) \cdot \Delta V_{hyst\_vs} \quad (9)$$

V. Change in Output Capacitor Energy

Referring to Figure 4, wish to derive expression for the change in output capacitor energy associated with steady-state ripple in output voltage.

First, write expression for energy stored in a capacitor charged to voltage, V:

$$E = \frac{1}{2} C V^2 \quad (10)$$

Energy stored at V=V_{out_max}:

$$E_{max} = \frac{1}{2} C {V_{out\_max}}^2 \quad (11)$$

Energy stored at V=V_{out_min}:

$$E_{min} = \frac{1}{2} C {V_{out\_min}}^2 \quad (12)$$

Change in stored output energy:

$$\Delta E_{out} = E_{max} - E_{min} \quad (13)$$

Substitute (11) and (12) into (13) and simplify:

$$\Delta E_{out} = \frac{1}{2} C \left({V_{out\_max}}^2 - {V_{out\_min}}^2\right) \quad (14)$$

Referring again to Figure 4, V_{out_max} and V_{out_min} can be expressed as follows:

$$V_{out\_max} = V_{out\_avg} + \frac{1}{2}\Delta V_{out} \quad (15)$$

$$V_{out\_min} = V_{out\_avg} - \frac{1}{2}\Delta V_{out} \quad (16)$$

Substitute (15) and (16) into (14) and simplify:

$$\Delta E_{out} = C \cdot V_{out\_avg} \cdot \Delta V_{out} \quad (17)$$

VI. Period of Output Voltage Ripple

Wish to derive an expression for the period, T_{hyst}, of output voltage ripple. First write expression for energy delivered from the transformer primary to the secondary network, which includes the transformer secondary capacitance, diode junction capacitance, output load capacitor, and bleed resistor:

$$\Delta E_{cycle\_p} = \frac{1}{2} L_m {I_p}^2 \quad (18)$$

where

$$I_p = \begin{cases} \frac{V_{CS\_lim}}{R_s} \; if \; I_{p\_CL} < I_{p\_D} \\ \frac{V_g \cdot D}{L_m \cdot f_{sw}} \; otherwise \end{cases} \quad (19)$$

Substitute (19) into (18):

$$\Delta E_{cycle\_p} = \begin{cases} \frac{L_m {V_{CS\_lim}}^2}{2{R_s}^2} \; if \; I_{p\_CL} < I_{p\_D} \\ \frac{{V_g}^2 \cdot D^2}{2{L_m \cdot f_{sw}}^2} \; otherwise \end{cases} \quad (20)$$

Now, write expression for energy dissipated in secondary circuit each switching period. Energy stored in transformer's secondary capacitance, C_s, is lost, as is that dissipated in bleed resistance, R:

$$\Delta E_{cycle\_n} = \Delta E_{cycle\_Cs} + \Delta E_{cycle\_R} \quad (21)$$

where

$$\Delta E_{cycle\_Cs} = \frac{1}{2} C_s {V_{out\_avg}}^2 \quad (22)$$

$$\Delta E_{cycle\_R} = \frac{{V_{out\_avg}}^2}{R} T_{sw} = \frac{{V_{out\_avg}}^2}{R \cdot f_{sw}} \quad (23)$$

Substitute (22) and (23) into (21) and simplify:

$$\Delta E_{cycle\_n} = {V_{out\_avg}}^2 \left(\frac{C_s}{2} + \frac{1}{R \cdot f_{sw}}\right) \quad (24)$$

Net energy accumulated in output capacitor each switching period is then the difference between the energy delivered by the transformer primary and energy dissipated in the secondary network:

$$\Delta E_{cycle} = \Delta E_{cycle\_p} - \Delta E_{cycle\_n} \quad (25)$$

Substitute (20) and (24) into (25):

$$\Delta E_{cycle} = \begin{cases} \frac{L_m {V_{CS\_lim}}^2}{2{R_s}^2} - {V_{out\_avg}}^2 \left(\frac{C_s}{2} + \frac{1}{R \cdot f_{sw}}\right) & if\ I_{p\_CL} < I_{p\_D} \\ \frac{{V_g}^2 \cdot D^2}{2L_m \cdot {f_{sw}}^2} - {V_{out\_avg}}^2 \left(\frac{C_s}{2} + \frac{1}{R \cdot f_{sw}}\right) & otherwise \end{cases} \quad (26)$$

As illustrated in Figure 5, the net energy delivered to the output capacitor while the converter is switching causes the output voltage to rise from V_{out_min} to V_{out_max} in a time Δt_{rise}:

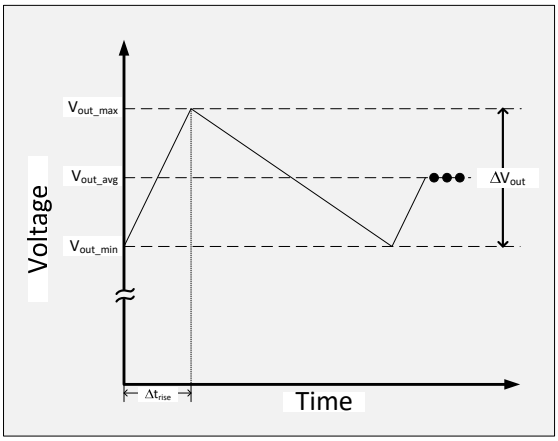

Figure 5, Waveform Diagram, Output Ripple Rise Time

The number of switching cycles required to cause the rise from V_{out_min} to V_{out_max} can be computed by dividing total change in energy, ΔE_{out}, by the net energy delivered to the output capacitor each cycle, ΔE_{cycle}:

$$n_{rise} = \frac{\Delta E_{out}}{\Delta E_{cycle}} \quad (27)$$

Time to rise is then number of cycles multiplied by time per cycle:

$$\Delta t_{rise} = n_{rise} \cdot T_{sw} = \frac{\Delta E_{out}}{\Delta E_{cycle}} \cdot T_{sw} \quad (28)$$

Substitute (17) and (26) into (28) and simplify:

$$\Delta t_{rise} = \begin{cases} \frac{2RC \cdot V_{out\_avg} \cdot \Delta V_{out} \cdot {R_s}^2}{L_m {V_{CS\_lim}}^2 R f_{sw} - {V_{out\_avg}}^2 \left(C_s {R_s}^2 R f_{sw} + 2{R_s}^2\right)} & if\ I_{p\_CL} < I_{p\_D} \\ \frac{2RC \cdot V_{out\_avg} \cdot \Delta V_{out} \cdot L_m \cdot f_{sw}}{{V_g}^2 D^2 R - {V_{out\_avg}}^2 \left(C_s L_m {f_{sw}}^2 R + 2L_m f_{sw}\right)} & otherwise \end{cases} \quad (29)$$

Next, derive expression for time for capacitor to discharge from V_{out_max} to V_{out_min}. When the converter is off, no energy is delivered to output capacitor, so discharge time is governed by RC time constant – assume that $\Delta t_{fall} << RC$:

$$I_{disch} = \frac{C \cdot \Delta V_{out}}{\Delta t_{fall}} \quad (30)$$

Where, assuming $\Delta V_{out} << V_{out\_avg}$,

$$I_{disch} \approx \frac{V_{out\_avg}}{R} \quad (31)$$

Set (31) equal to (30), and solve for Δt_{fall}:

$$\Delta t_{fall} = RC \cdot \frac{\Delta V_{out}}{V_{out\_avg}} \quad (32)$$

The period of the output voltage ripple, T_{hyst}, is then the sum of the rise time and the fall time:

$$T_{hyst} = \Delta t_{rise} + \Delta t_{fall} \quad (33)$$

Substitute (29) and (32) into (33):

If Ip_CL < Ip_D:

$$T_{hyst} = \frac{2RC \cdot V_{out\_avg} \cdot \Delta V_{out} \cdot {R_s}^2}{L_m {V_{CS\_lim}}^2 R f_{sw} - {V_{out\_avg}}^2 \left(C_s {R_s}^2 R f_{sw} + 2{R_s}^2\right)} + RC \frac{\Delta V_{out}}{V_{out\_avg}}$$

Otherwise, if Ip_CL ≥ Ip_D:

$$T_{hyst} = \frac{2RC \cdot V_{out\_avg} \cdot \Delta V_{out\cdot} \cdot L_m \cdot f_{sw}}{{V_g}^2 D^2 R - {V_{out\_avg}}^2 \left(C_s L_m {f_{sw}}^2 R + 2L_m f_{sw}\right)} + RC \frac{\Delta V_{out}}{V_{out\_avg}}$$

(34)

VII. OUTPUT VOLTAGE AT i^th SWITCHING CYCLE

Next, wish to find expression for output voltage after i^th switching cycle. Rewrite (26) for the i^th cycle, replacing V_{out_avg} with voltage after i^th cycle:

$$\Delta E_{cycle}(i) = \begin{cases} \frac{L_m {V_{CS\_lim}}^2}{2{R_s}^2} - V_{out}(i)^2\left(\frac{C_s}{2} + \frac{1}{R \cdot f_{sw}}\right) & if\ I_{p\_CL} < I_{p\_D} \\ \frac{{V_g}^2 \cdot D^2}{2L_m \cdot {f_{sw}}^2} - V_{out}(i)^2\left(\frac{C_s}{2} + \frac{1}{R \cdot f_{sw}}\right) & otherwise \end{cases} \quad (35)$$

Write expressions for energy stored in output capacitor after i^{th} and $(i-1)^{th}$ cycles:

$$E_{out}(i) = \frac{1}{2} C V_{out}(i)^2 \quad (36)$$

$$E_{out}(i-1) = \frac{1}{2} C V_{out}(i-1)^2 \quad (37)$$

By definition, the net energy delivered to the output capacitor after the i^{th} cycle is the difference between the stored output energy after the i^{th} and $(i-1)^{th}$ cycles:

$$\Delta E_{cycle}(i) = E_{out}(i) - E_{out}(i-1) \quad (38)$$

Substitute (36) and (37) into (38) and simplify:

$$\Delta E_{cycle}(i) = \frac{1}{2} C\left[{V_{out}}^2(i) - {V_{out}}^2(i-1)\right] \quad (39)$$

Set (39) equal to (35), solve for $V_{out}^2(i)$, and simplify:

If Ip_CL < Ip_D:

$${V_{out}}^2(i) = \left[\frac{1}{2}(C + C_s) + \frac{1}{R \cdot f_{sw}}\right]^{-1} \cdot \left[\frac{C}{2}{V_{out}}^2(i-1) + \frac{L_m \cdot {V_{CS\_lim}}^2}{2{R_s}^2}\right]$$

Otherwise, if Ip_CL ≥ Ip_D:

$${V_{out}}^2(i) = \left[\frac{1}{2}(C + C_s) + \frac{1}{R \cdot f_{sw}}\right]^{-1} \cdot \left[\frac{C}{2}{V_{out}}^2(i-1) + \frac{{V_g}^2 \cdot D^2}{2L_m \cdot {f_{sw}}^2}\right] \quad (40)$$

VIII. NUMBER OF CYCLES, n, TO CHARGE TO Vout(n)

Referring to (40), define K_1 and K_2 as follows:

$$K_1 = \left[1 + \frac{C_s}{C} + \frac{2}{RC \cdot f_{sw}}\right]^{-1} \quad (41)$$

$$K_2 = \begin{cases} \left[\frac{1}{2}(C + C_s) + \frac{1}{R \cdot f_{sw}}\right]^{-1} \cdot \frac{L_m {V_{CS\_lim}}^2}{2{R_s}^2} & if\ I_{p\_CL} < I_{p\_D} \\ \left[\frac{1}{2}(C + C_s) + \frac{1}{R \cdot f_{sw}}\right]^{-1} \cdot \frac{{V_g}^2 \cdot D^2}{2L_m \cdot {f_{sw}}^2} & otherwise \end{cases} \quad (42)$$

Rewrite (40) for $Vout^2(i)$ in terms of K_1 and K_2:

$${V_{out}}^2(i) = K_1 \cdot {V_{out}}^2(i-1) + K_2 \quad (43)$$

Define $V_{out}(n)$ to be output voltage after nth cycle, and seek to derive closed-form expression for n, number of cycles to reach $V_{out}(n)$ -- expand (43):

$$i = 0: {V_{out}}^2(0) = 0 \quad (44)$$

$$i = 1: {V_{out}}^2(1) = K_2 \quad (45)$$

$$i = 2: {V_{out}}^2(2) = K_2(1 + K_1) \quad (46)$$

$$i = 3: {V_{out}}^2(3) = K_2\left({K_1}^2 + K_1 + 1\right) \quad (47)$$

$$i = 4: {V_{out}}^2(4) = K_2\left({K_1}^3 + {K_1}^2 + K_1 + 1\right) \quad (48)$$

$$\vdots$$

$$i = n: {V_{out}}^2(n) = K_2\left({K_1}^{n-1} + \cdots + {K_1}^3 + {K_1}^2 + K_1 + 1\right) \quad (49)$$

$$i = n: {V_{out}}^2(n) = K_2 \sum_{i=1}^{n} {K_1}^{i-1} \quad (50)$$

Let j=i-1 and rewrite (50):

$${V_{out}}^2(n) = K_2 \sum_{j=0}^{n-1} {K_1}^j \quad (51)$$

Since the right side of (51) represents a geometric series, it can be written in closed form as follows:

$${V_{out}}^2(n) = K_2 \frac{1 - {K_1}^n}{1 - K_1} \quad (52)$$

Solve (52) for n in terms of $V_{out}(n)$:

$$n = log_{K_1}\left[1 - {V_{out}}^2(n) \cdot \frac{1 - K_1}{K_2}\right] \quad (53)$$

Define α to be equal to the argument of the log function in (53):

$$\alpha = 1 - {V_{out}}^2(n) \cdot \frac{1 - K_1}{K_2} \quad (54)$$

From properties of algorithms:

$$log_{K_1}[\alpha] = \frac{ln(\alpha)}{ln(K_1)} \quad (55)$$

Use (54) and (55) to rewrite (53) in final form:

$$n = \frac{1}{ln(K_1)} ln\left[1 - V_{out}{}^2(n) \cdot \frac{1-K_1}{K_2}\right] \quad (56)$$

where K_1 and K_2 are as defined in (41) and (42), respectively.

It is worth noting that (56) is similar in form to an equation provided without derivation in reference (3).

IX. VERIFICATION OF RESULTS

Equation (56) supports prediction of expected charge-time performance given a converter described by a certain set of parameters. For example, Figure 6 shows an Excel spreadsheet that accepts input parameters and computes values for n_{CL}, n_D, n, t_{chg_CL}, t_{ch_D}, and t_{chg}. To check prediction against measurements made using development hardware, input parameters were set within reasonable tolerances of as-designed values, as follows:

C = 0.495 uF
C_s = 5.6 pF + 20 pF = 25.6 pF
D = 38.8 % (nominal programmed, no current limiting)
f_{sw} = 43 kHz
L_m = 41 uH
R = 3.33 megohm
R_s = 0.135 ohm
V_{CSlim} = 0.35 volt
V_g = 22 V, 26V, and 33 V
$V_{out}(n)$ = 2340 volt

	Parameter	Value	Units	Description
Inputs	C	4.95E-07	farad	Load Capacitance
	Cs	2.56E-11	farad	Flyback transformer secondary capacitance
	D	3.88E-01	unitless	Duty cycle
	f_sw	4.30E+04	Hz	Switching frequency
	Lm	4.10E-05	henry	Primary magnetizing inductance
	R	3.33E+06	ohm	Load Resistance
	Rs	1.35E-01	ohm	Current sense resistance
	V_CSlim	3.50E-01	volt	Current sense comparator threshold
	Vg	2.80E+01	volt	Input voltage
	Vout_n	2.34E+03	volt	Output voltage after nth switching cycle
Outputs	Ip_CL	2.593	amp	Ip_CL < Ip_D)
	Ip_D	6.162	amp	Peak primary current achieved if active pulse-by-pulse current limit threshold is NOT reached (i.e. if full programmed duty cycle is reached, Ip_CL > Ip_D)
	K1	0.999920	unitless	Coefficient on Vout(i-1)^2 associated with output energy lost each cycle
	K2_CL	556.69	volt^2	Term added to Vout(i-1)^2 associated with output energy gained on the ith cycle in the case that the active pulse-by-pulse current limit is reached (i.e. if Ip_CL < Ip_D)
	K2_D	3144.99	volt^2	the active pulse-by-pulse current limit is NOT reached (i.e. case when full programmed duty cycle is reached, Ip_CL > Ip_D)
	n_CL	19378	unitless	Theoretical number of cycles to reach Vout_n if active pulse-by-pulse current limit is reached each cycle (i.e. Ip_CL < Ip_D)
	n_D	1878	unitless	Theoretical number of cycles to reach Vout_n if active pulse-by-pulse current limit is NOT reached each cycle (i.e. Ip_CL > Ip_D)
	n	19378	unitless	Number of switching cycles to charge to Vout
	t_chg_CL	0.451	second	Ip_CL < Ip_D)
	t_chg_D	0.044	second	Theoretical time to reach Vout_n if active pulse-by-pulse current limit is NOT reached each cycle (i.e. Ip_CL > Ip_D)
	t_chg	0.451	second	Time to charge to Vout

Figure 6, Theoretical Model, Excel Implementation

Figure 7 and Figure 8 compare measurement data taken from development hardware at 25degC to the values computed by the spreadsheet for Vg = 22V, 26V, and 33V. At low input voltage, the theoretical charge time is within 1%, or approximately 4.5 msec of measurement. The theoretical model predicts the same charge time across input voltages, whereas measured charge times decrease noticeably as input voltage increases, and error increases to 8.2% at nominal input, 12.7% at high input. Nevertheless, prediction remains within 15% error, so that theoretically predicted values are useful approximations of measured performance.

t_charge vs Vg (Vout = 2340V, C = 0.495uF, Rs=0.135ohm, 25degC)			
Vg [volt]	t_charge (theory, closed form) [second]	t_charge (measured) [second]	% error
22	0.4488	0.446	-0.6%
26	0.4488	0.412	-8.2%
33	0.4488	0.392	-12.7%

Figure 7, Table, Measurement Data vs Prediction

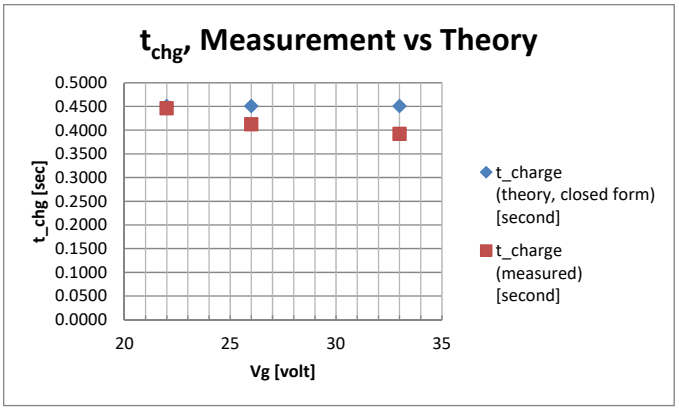

Figure 8, Plot, Measurement Data vs Prediction

Figure 9 and Figure 10, below, show the simulation model used to investigate the accuracy of (56). The first shows the flyback converter itself, and the second shows the control logic as implemented in the Sandia-designed Peladon control chip [see reference (5)], including both voltage sense and current sense comparator functions.

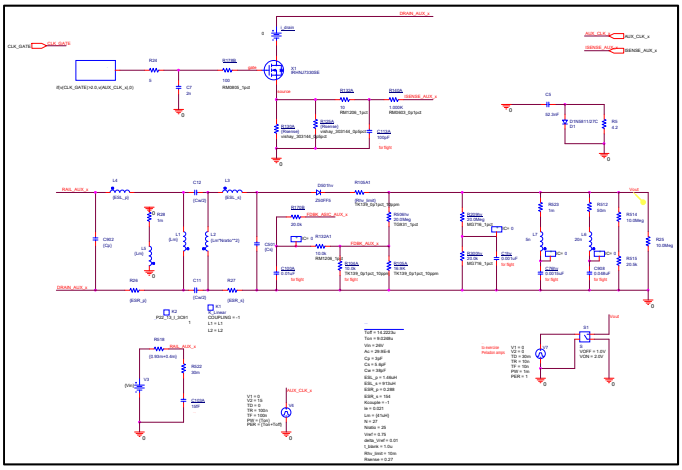

Figure 9, Simulation Model, Flyback Converter

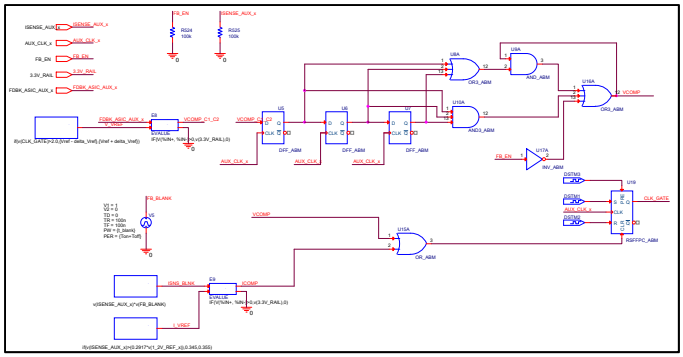

Figure 10, Simulation Model, Control Logic

To compare theory to simulation, key parameters were set to the following values in the respective models, where C_s is the parallel combination of transformer capacitance (5.6pF) and high-voltage diode junction capacitance (22.76pF) [see reference (6)], and load capacitance was reduced by a factor of ten to shorten simulation time (both simulation and theory show charge time to be proportional to C, so results can simply be scaled, meaning that both simulation and theory predict 10x increase in charge time for a 10x increase in output capacitance):

C = 0.0495 uF
C_s = 5.6 pF + 22.76 pF = 30.4 pF
D = 38.8 % (nominal programmed, no current limiting)
f_{sw} = 43 kHz
L_m = 41 uH
R = 3.33 megohm
R_s = 0.1 ohm
V_{CSlim} = 0.35 volt
V_g = 26 volt
$V_{out}(n)$ = 2425 volt

t_charge vs Vg (Vout = 2420V, C = 0.0495uF, Rs=0.1ohm, 25degC)			
Vg [volt]	t_charge (theory, closed form) [second]	t_charge (simulation) [second]	% error
22	0.0185	0.0155	-16%
26	0.0185	0.0151	-18%
27	0.0185	0.0158	-15%
28	0.0185	0.0149	-20%
29	0.0185	0.0154	-17%
30	0.0185	0.0173	-7%
31	0.0185	0.022	19%
32	0.0185	0.0258	39%
33	0.0185	0.0267	44%

Figure 11, Table, t_{chg}, Theory vs. Simulation

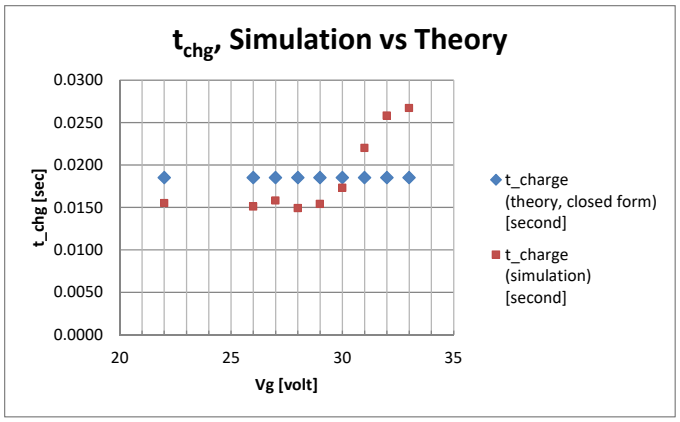

Figure 12, Plot, t_{chg}, Theory vs. Simulation

Figure 11 and Figure 12 provide a summary of simulation results vs. theoretical prediction. While measurements taken on development hardware showed a decrease in charge time with an increase in converter input voltage, simulation predicts charge times faster by about 20% until the input voltage reaches about 29V, at which point simulation results show a sudden and significant increase in charge time for input voltages above 29V, with the percentage error increasing to a positive (slower) 44% at Vg = 33V.

Figure 13 overlays simulation results at Vg=26V with the theoretical waveform computed using (40). The MATLAB code used to make the computation is provided in Figure 14. The theoretical waveform is consistent with the time predicted using (56), again exceeding simulation by about 4msec.

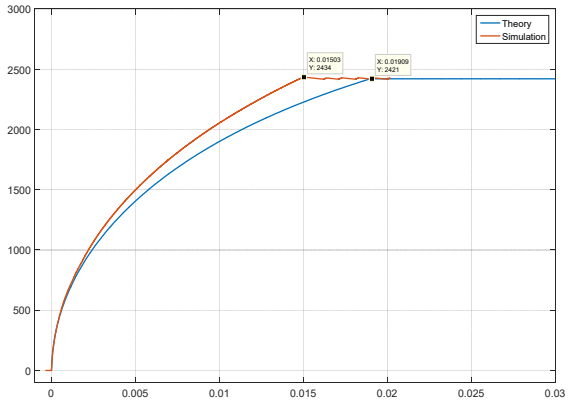

Figure 13, Waveform, Vout, Theory vs. Simulation

```
%% Plot Vout vs Time
% Wish to plot the variation of Vout versus time.  Based on simulation and lab
% results, the Vout waveform should look approximately exponential as it
% rises toward its steady-state value.  Equation (40) provides
% an expression for Vout(i) in terms of circuit parameters and Vout(i-1),
% the output voltage after the previous cycle.
Vout_charge_nom = zeros(12500,1);
Vout_charge_min = zeros(12500,1);
Vout_charge_max = zeros(12500,1);
t_nom = zeros(12500,1);
t_min = zeros(12500,1);
t_max = zeros(12500,1);
for i=2:i=12500
    if (Vout_charge_nom(i-1)<Vout_nom)
        if (V_CS1in_nom/Rs_nom) < ( (Vg_nom*Ci_nom / (Lm_nom*fsw_nom) )
            Vout_charge_nom(i)  = sqrt(( (C_nom*Ca_nom/2 + 1/(H_nom*fsw_nom) )^-1 *  (C_nom/2*Vout_charge_nom(i-1)^2 +  (Lm_nom*V_CS1in_nom^2 / (2*Rs_nom^2) ));
        else
            Vout_charge_nom(i)  = sqrt(( (C_nom*Ca_nom/2 + 1/(H_nom*fsw_nom) )^-1 *  (C_nom/2*Vout_charge_nom(i-1)^2 +  (Vg_nom^2*Ci_nom^2 / (2*Lm_nom*fsw_nom^2) ));
        end
    else
        Vout_charge_nom(i)  = Vout_charge_nom(i-1);
    end
    if (Vout_charge_min(i-1)<Vout_min)
        if (min_V_CS1in/min_Rs) < ( (min_Vg*min_Ci / (min_Lm*min_fsw) )
            Vout_charge_min(i)  = sqrt(( (min_C*min_Ca)/2 + 1/(min_H*min_fsw) )^-1 *  (min_C/2*Vout_charge_min(i-1)^2 +  (min_Lm*min_V_CS1in^2 / (2*min_Rs^2) ));
        else
            Vout_charge_min(i)  = sqrt(( (min_C*min_Ca)/2 + 1/(min_H*min_fsw) )^-1 *  (min_C/2*Vout_charge_min(i-1)^2 +  (min_Lm*(Vg^2*min_D^2) / (2*min_Lm*min_fsw^2) ));
        end
    else
        Vout_charge_min(i)  = Vout_charge_min(i-1);
    end
    if (Vout_charge_max(i-1)<Vout_max)
        if (max_V_CS1in/max_Rs) < ( (max_Vg*max_Ci / (max_Lm*max_fsw) )
            Vout_charge_max(i)  = sqrt(( (max_C*max_Ca)/2 + 1/(max_H*max_fsw) )^-1 *  (max_C/2*Vout_charge_max(i-1)^2 +  (max_Lm*max_V_CS1in^2 / (2*max_Rs^2) ));
        else
            Vout_charge_max(i)  = sqrt(( (max_C*max_Ca)/2 + 1/(max_H*max_fsw) )^-1 *  (max_C/2*Vout_charge_max(i-1)^2 +  (max_Lm*(Vg^2*max_D^2) / (2*max_Lm*max_fsw^2) ));
        end
    else
        Vout_charge_max(i)  = Vout_charge_max(i-1);
    end
    t_nom(i)  = i/fsw_nom;
    t_min(i)  = i/fsw_min; % conditions for shortest time to steady-state
    t_max(i)  = i/fsw_nom; % conditions for greatest time to steady-state
end
fig1 = figure;
plot(t_nom,Vout_charge_nom,'-g');
hold on
plot(t_min,Vout_charge_min,'-r');
plot(t_max,Vout_charge_max,'-b');
xlabel(gca,'Time [s]','fontsize',6,'fontweight','b');
ylabel(gca,'Converter Output Voltage, Vout [volt]','fontsize',6,'fontweight','b');
set(gca,'fontsize',10);
title('Vout Charge Profile','fontsize',14,'fontweight','b');
grid on;
my_legend = legend('Vout Charge Profile, Nominal','Vout Charge Profile, Fastest','Vout Charge Profile, Slowest');
set(my_legend,'Location','East')
hold off
```

Figure 14, MATLAB Code to Plot Theoretical Vout vs Time

X. CONCLUSIONS

Closed-form expressions for key operating parameters allow analyst and designer to gain insight into the expected operation of the fixed duty cycle, hysteretic flyback converter often used in firing set applications. As switch-mode power conversion is a non-linear process with many variables, such theoretical models are necessarily, like all models, approximations. By strategically combining theoretical modeling, Pspice modeling, and measurements from representative hardware operating in representative conditions, the designer can gain insights into the weaknesses of the models being used, and ultimately into the hardware itself. This can help the designer avoid being misled by models, and can lead to early detection of necessary design changes, thereby shortening the design process, and allowing the designer to develop in herself and others confidence that the design will meet mission objectives with requisite margin.

XI. REFERENCES

1. **Nagel, Robert.** *Transformer Design Considerations for Non-continuous Mode, Boost, Flyback Converters.* Albuquerque, NM : Sandia National Laboratories, 1995.

2. **William C. Curtis, Victor Rimkus, Gregory Lyons.** *Isolated Flyback Converter Electronics -- Generic Models Developed/Simulations Performed;Specific Models/Simulations Being Incorporated.* Albuquerque, NM : Sandia National Laboratories, 1999. SAND99-3099C.

3. **Curtis, William C.** *Isolated Flyback Converter Electronics -- Using Simulation, Mathematics, and Prototype Hardware to Predict Performance.* Albuquerque, NM : Sandia National Laboratories, 2000. p. 11. SAND2000-1125C.

4. **Alexander W. Roesler, Joshua M. Schare, S. Jill Glass, Kevin G. Ewsuk, George Slama, Dave Abel, Daryl Schofield.** *Planar LTCC Transformers for High Voltage Flyback Converters.* Albuquerque, NM : Sandia National Laboratories, 2007. SAND2007-2591.

5. **Pearson, Sean.** *Peladon PPI ASIC Hardware Description Document.* 01753. Albuquerque, NM : Sandia National Laboratories, 2016. pp. 5-6.

6. **Voltage Multipliers, Inc.** *Spice Model, Z50FF5.* Visalia, CA : Voltage Multipliers, Inc., 2016. p. 1.