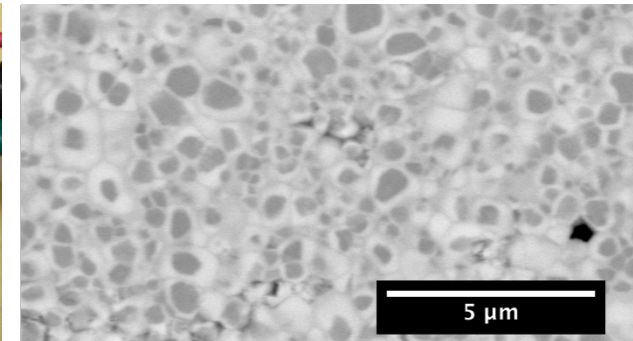
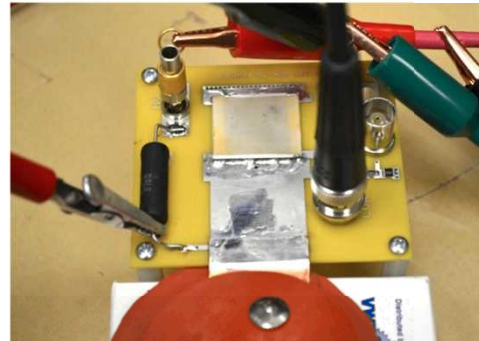
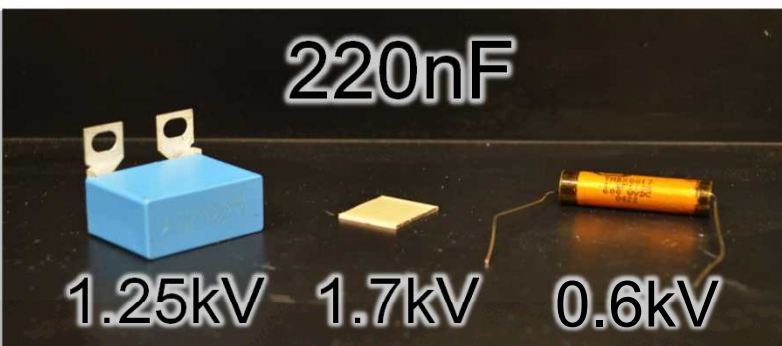


Exceptional service in the national interest



Design of high voltage ceramic and glass capacitors for pulse forming networks

Harlan J. Brown-Shaklee, A. Cook, T. Garino,

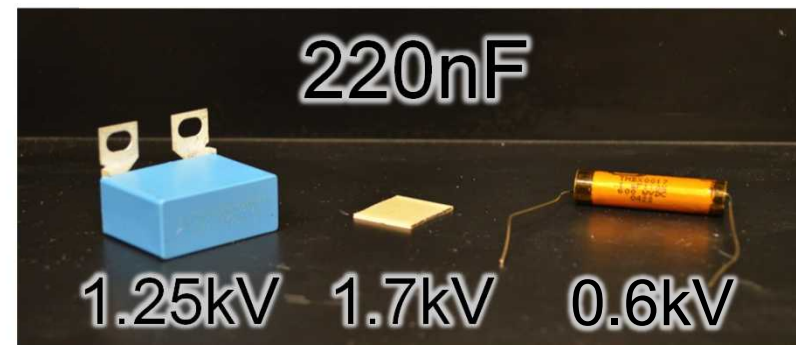
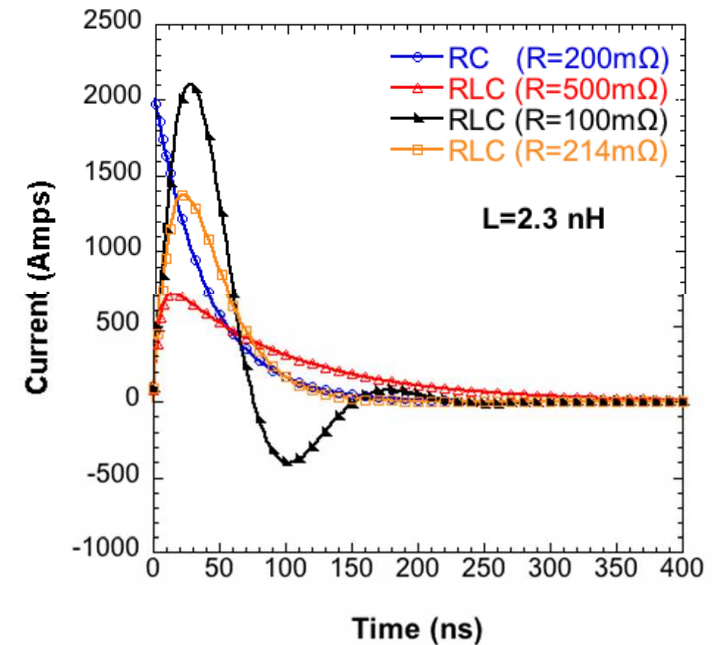
P.G. Clem, R. Johnson, and **Rudeger H.T Wilke**

Material Science and Engineering Center

Sandia National Laboratories, Albuquerque, NM USA

Outline

- Application space for high voltage capacitors
- Circuit considerations
- High ϵ' dielectrics for HV capacitors
- Low ϵ' dielectrics for HV capacitors
- Path forward



Applications for high voltage capacitors

DC/DC and DC/AC Power Inverters



Motor Drives



Raytheon Zumwalt-Class Destroyer



Z-Machine at SNL



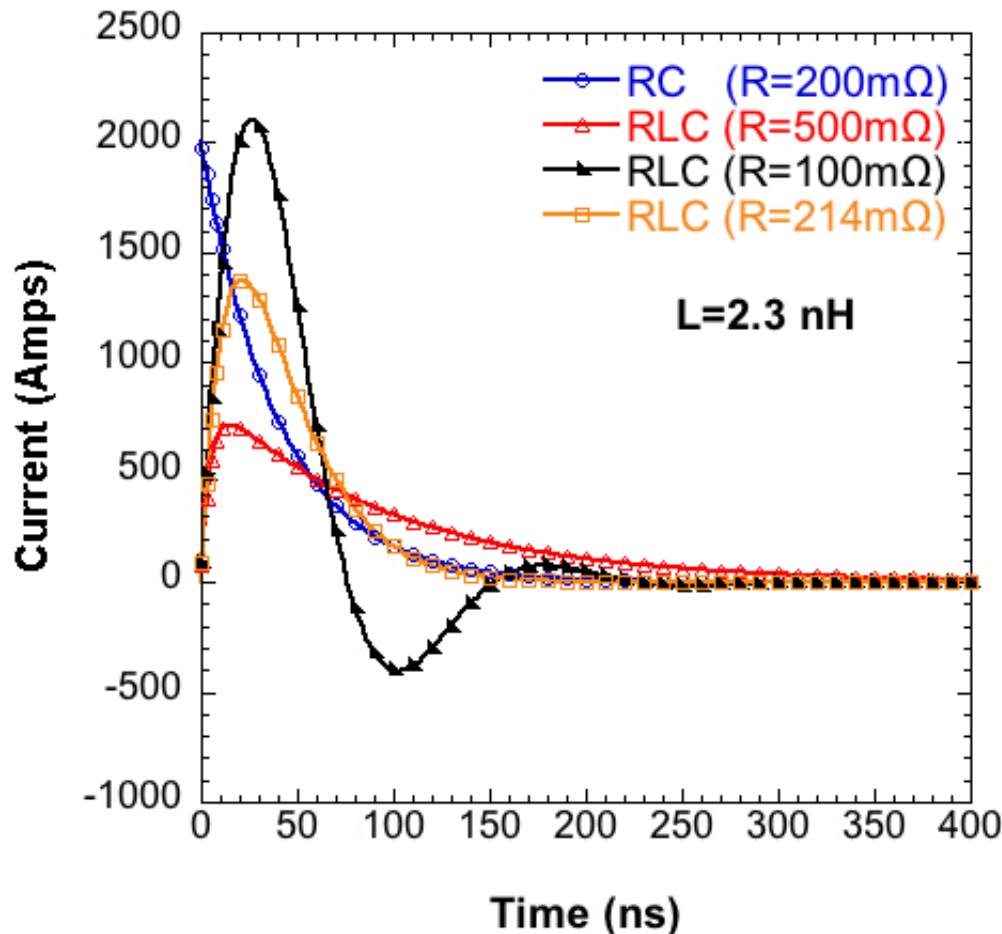
*Voltage, energy, power, lifetime, reliability and cost requirements are
application specific*

http://gpelectric.com/files/gpelectric/images/products/GP_Pure_Series_Horz_Reflection_web2.png

<http://www.abb-conversations.com/wp-content/uploads/2012/11/ABB-IE4-Synchronous-Reluctance-Motor-SynRM-480x301.jpg>

<http://www.raytheon.com/capabilities/products/zumwalt/>

Capacitors can be charged and discharged using RC or RLC circuits



$$i(t)_{RC} = \frac{V_0 e^{\frac{-t}{RC}}}{R_{load}}$$

$$i(t)_{RLC-OD} = \frac{V_0}{L\omega_2} e^{\left(-\frac{Rt}{2L}\right)} \sinh(\omega_2 t)$$

$$i(t)_{RLC-UD} = \frac{V_0}{L\omega_1} e^{\left(-\frac{Rt}{2L}\right)} \sin(\omega_1 t)$$

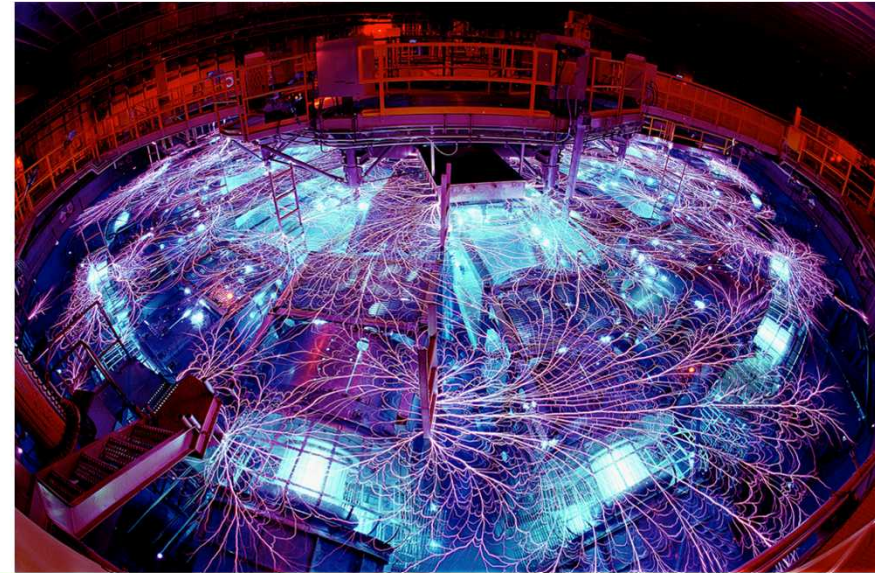
$$i(t)_{RLC-CD} = \frac{V_0 t}{L} e^{-\omega_0 t}$$

For high C and targeted fast discharge, one encounters circuit inductance which requires design of low inductance circuits.

Must manage capacitor ESR and ESL!

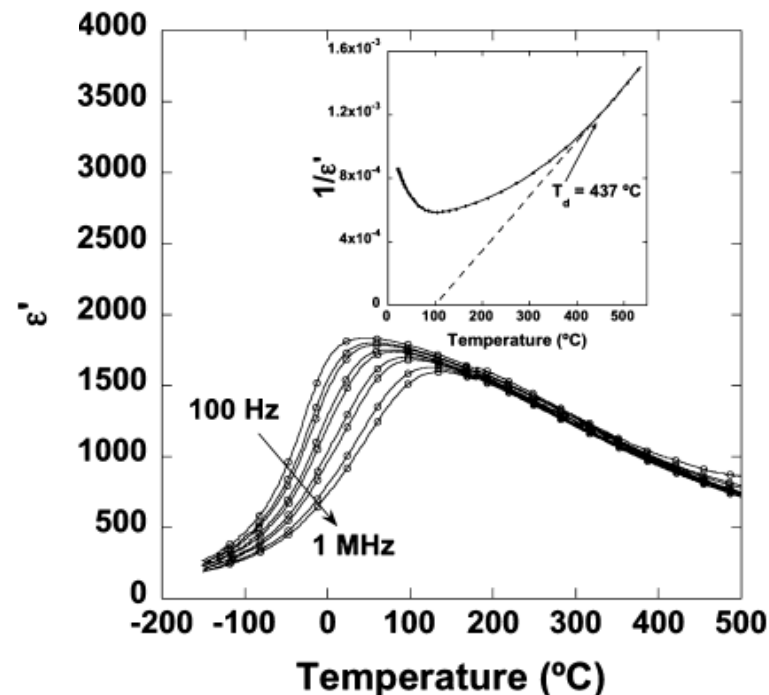
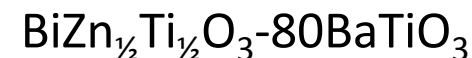
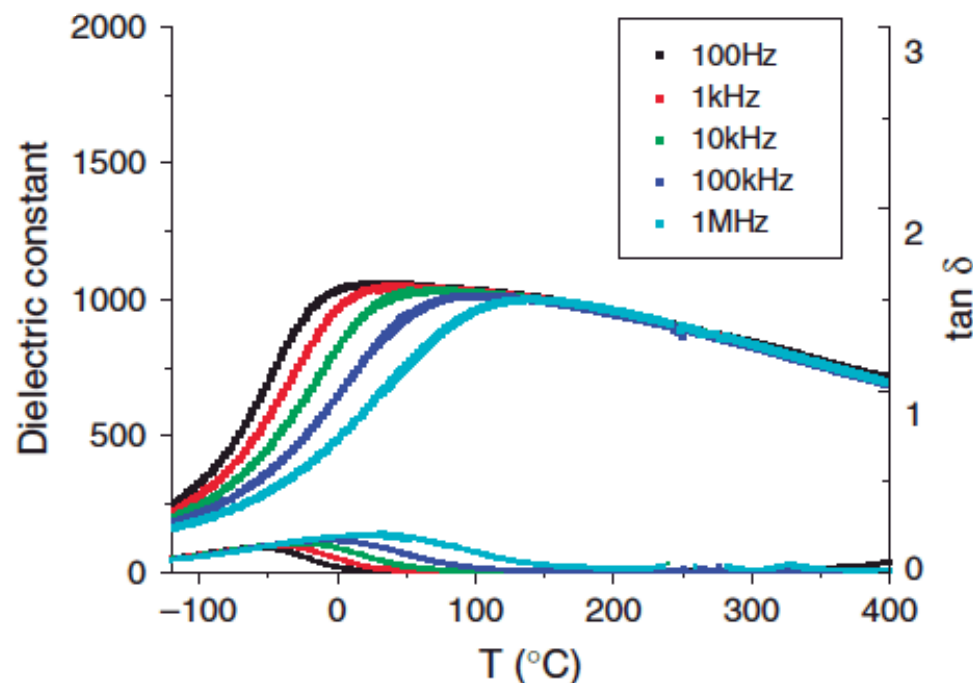
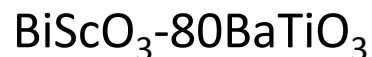
Considerations for capacitor design

- Electromechanical stability
- Operating frequency
- Shot life and duty cycle
- Temperature
- Package volume
- Cost



High K dielectrics for high voltage capacitors

We are studying weakly coupled relaxors for high energy density capacitors



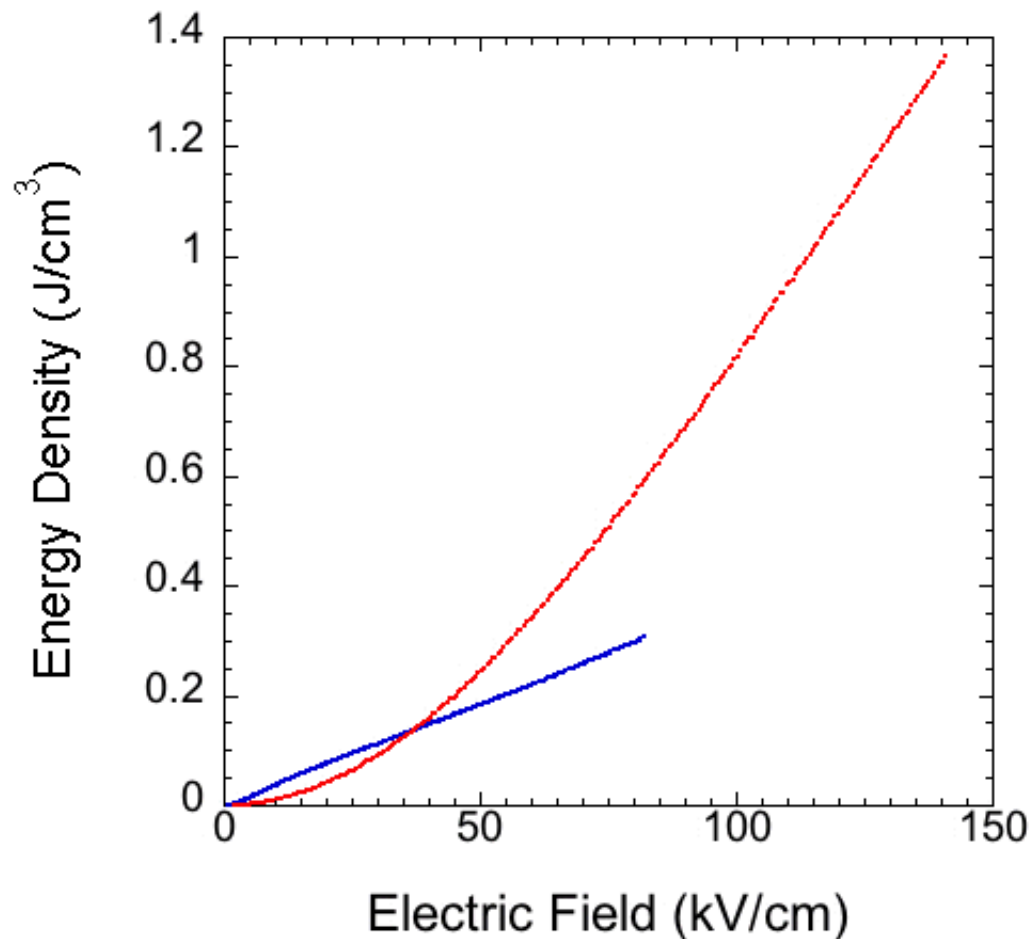
These so called weakly coupled relaxors exhibit high permittivity and can exhibit low $d\epsilon'/dT$ above the relaxation temperature

PSU Ogihara, Randall, and Troler-McKinstry, JACerS **92** [1] 3554-61 (2009)

OSU Raengthon and Cann, JACerS **95** [11] 3554-61 (2012).

Can't we just use BaTiO₃?

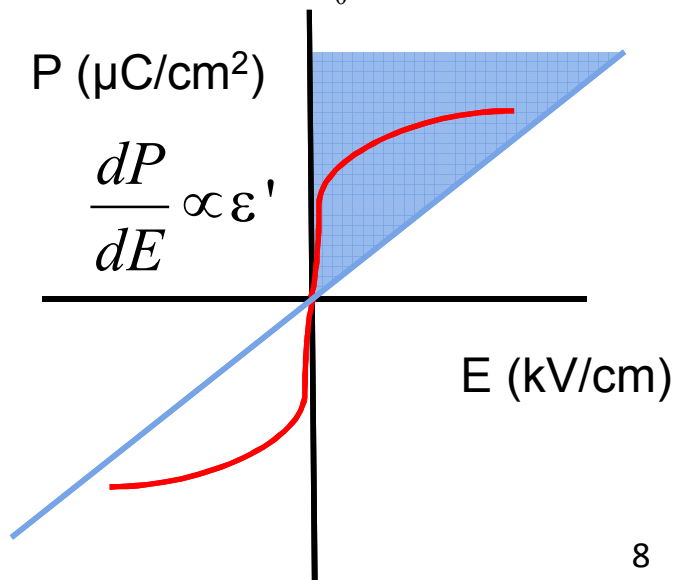
- Commercial capacitors exhibit electric field tuning
 - Dielectric constant changes with applied field
 - Commercial capacitors are optimized for high ϵ' but not energy density



Energy stored in a capacitor is:

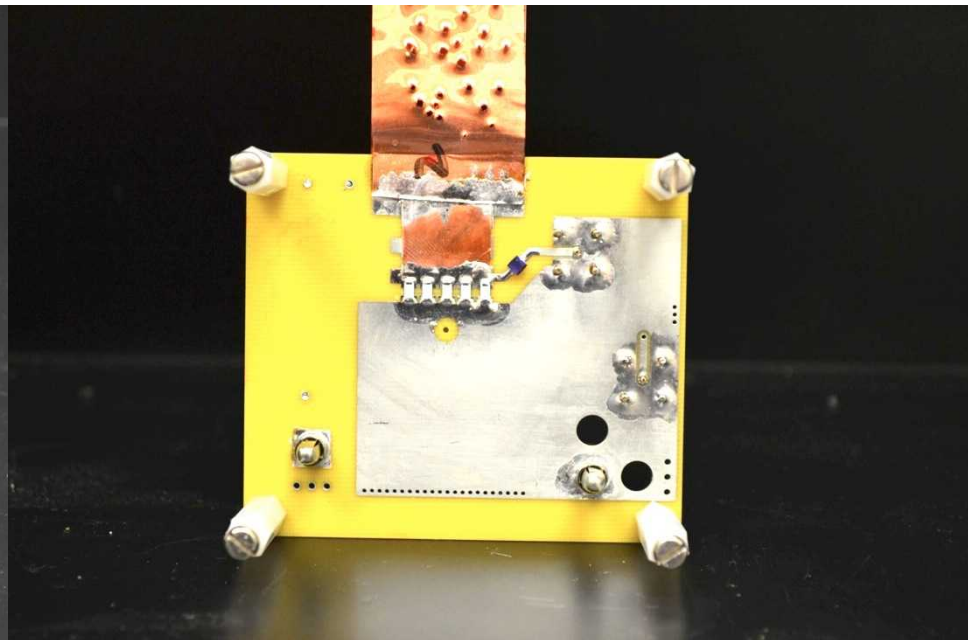
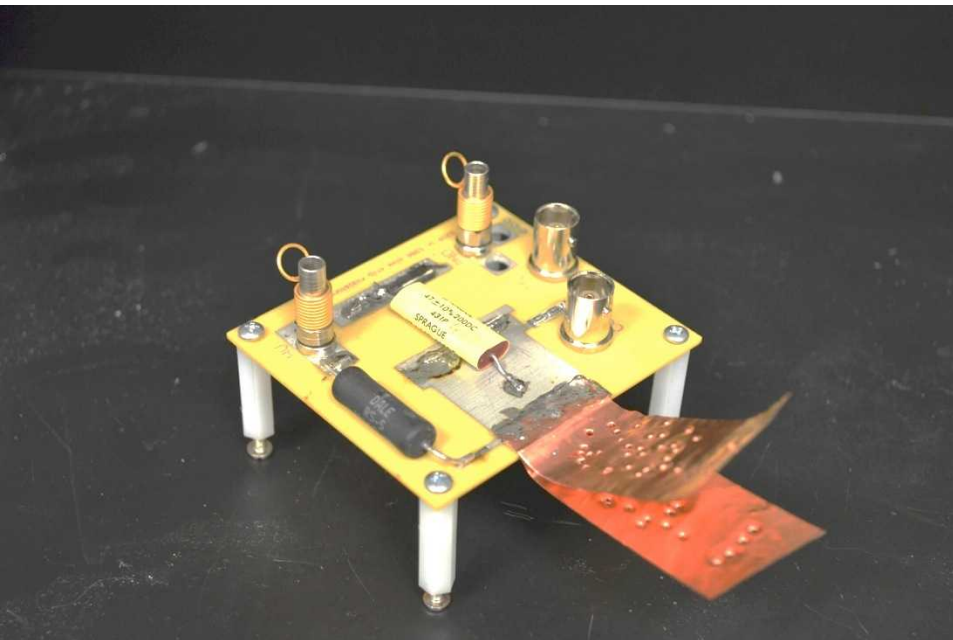
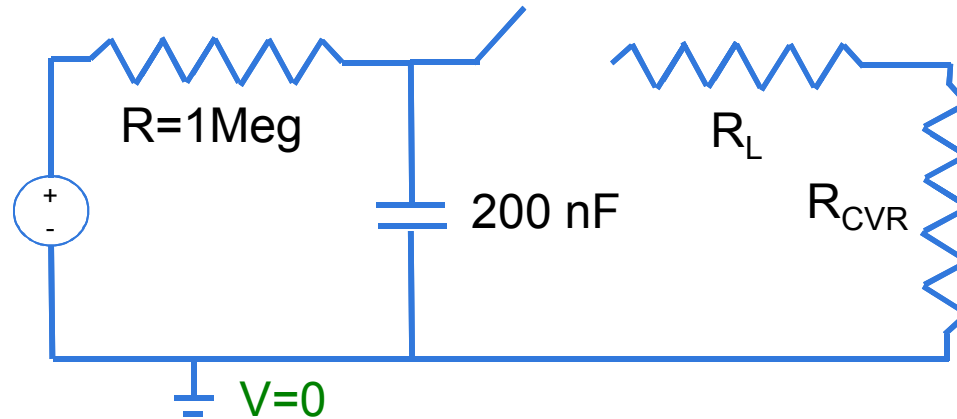
$$W = \frac{1}{2} \epsilon_r \epsilon_0 \frac{A}{d} V^2$$

$$\left(\frac{J}{cm^3} \right) = \int_{E_0}^{E_{max}} P(E) dE$$

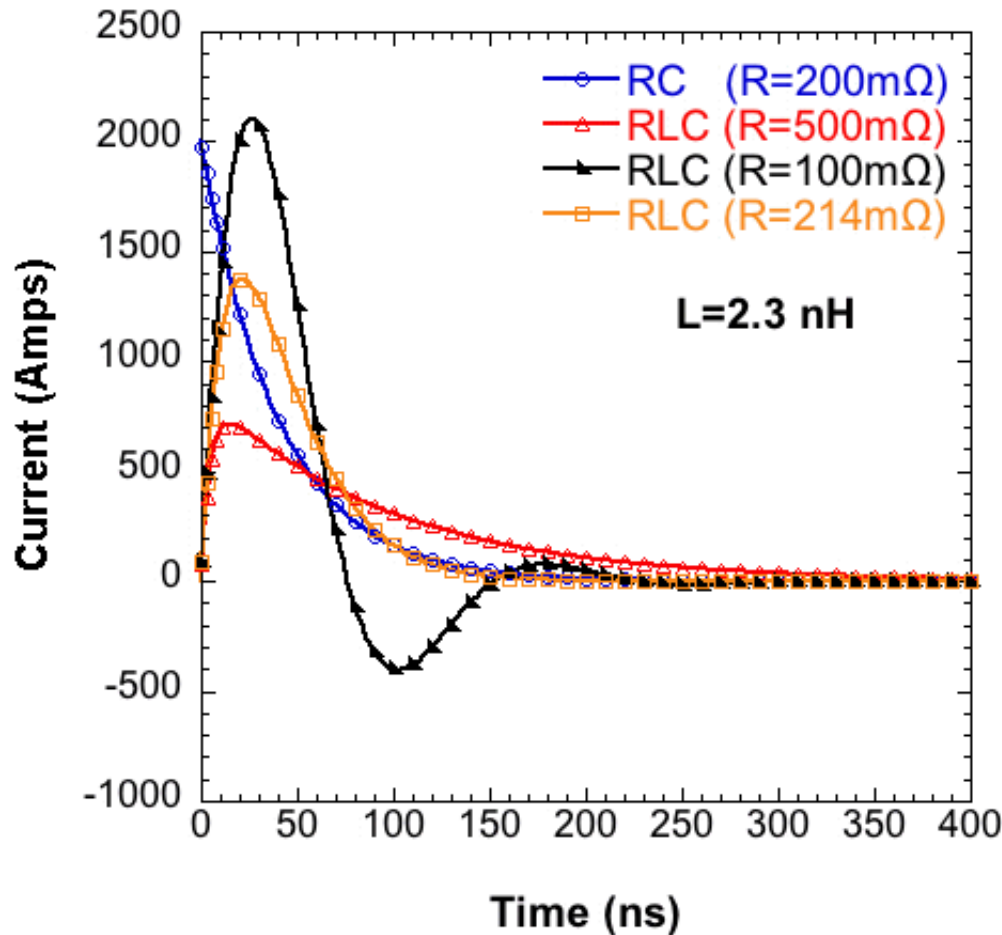


Pulse discharge requires purpose built circuits

Most measurements we make are in frequency domain but pulse discharge occurs in the time domain...



Capacitors can be charged and discharged using RC or RLC circuits



$$i(t)_{RC} = \frac{V_0 e^{\frac{-t}{RC}}}{R_{load}}$$

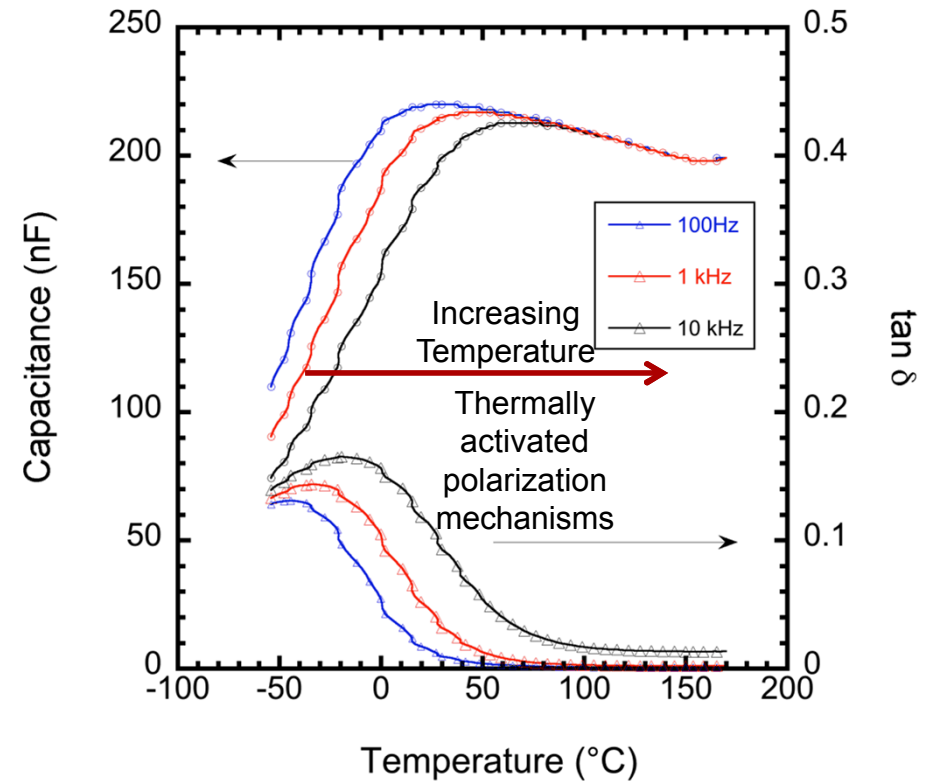
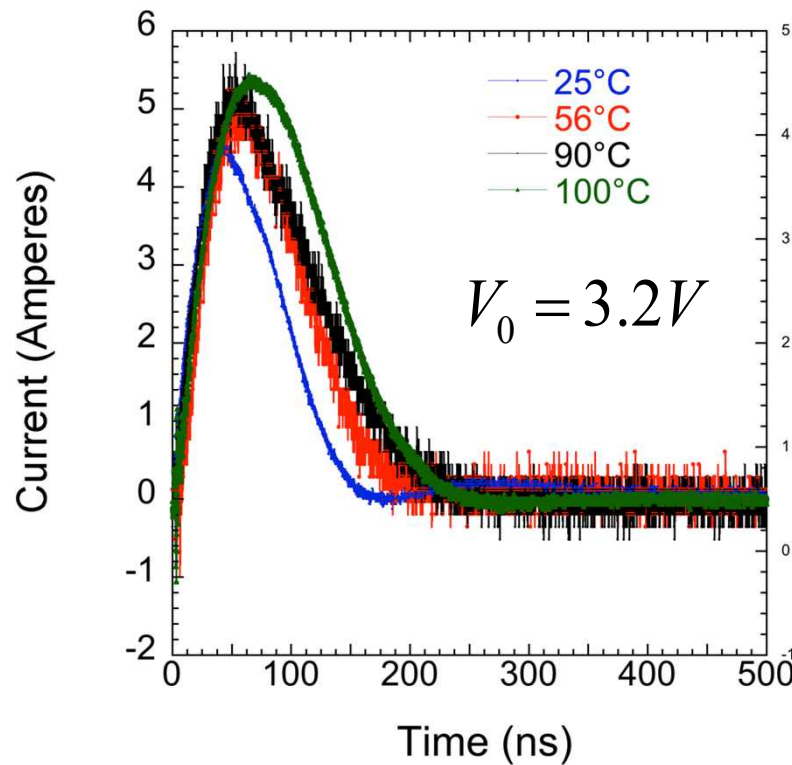
$$i(t)_{RLC-OD} = \frac{V_0}{L\omega_2} e^{\left(-\frac{Rt}{2L}\right)} \sinh(\omega_2 t)$$

$$i(t)_{RLC-UD} = \frac{V_0}{L\omega_1} e^{\left(-\frac{Rt}{2L}\right)} \sin(\omega_1 t)$$

$$i(t)_{RLC-CD} = \frac{V_0 t}{L} e^{-\omega_0 t}$$

For high C and targeted fast discharge, one encounters circuit inductance which requires design of low inductance circuits.

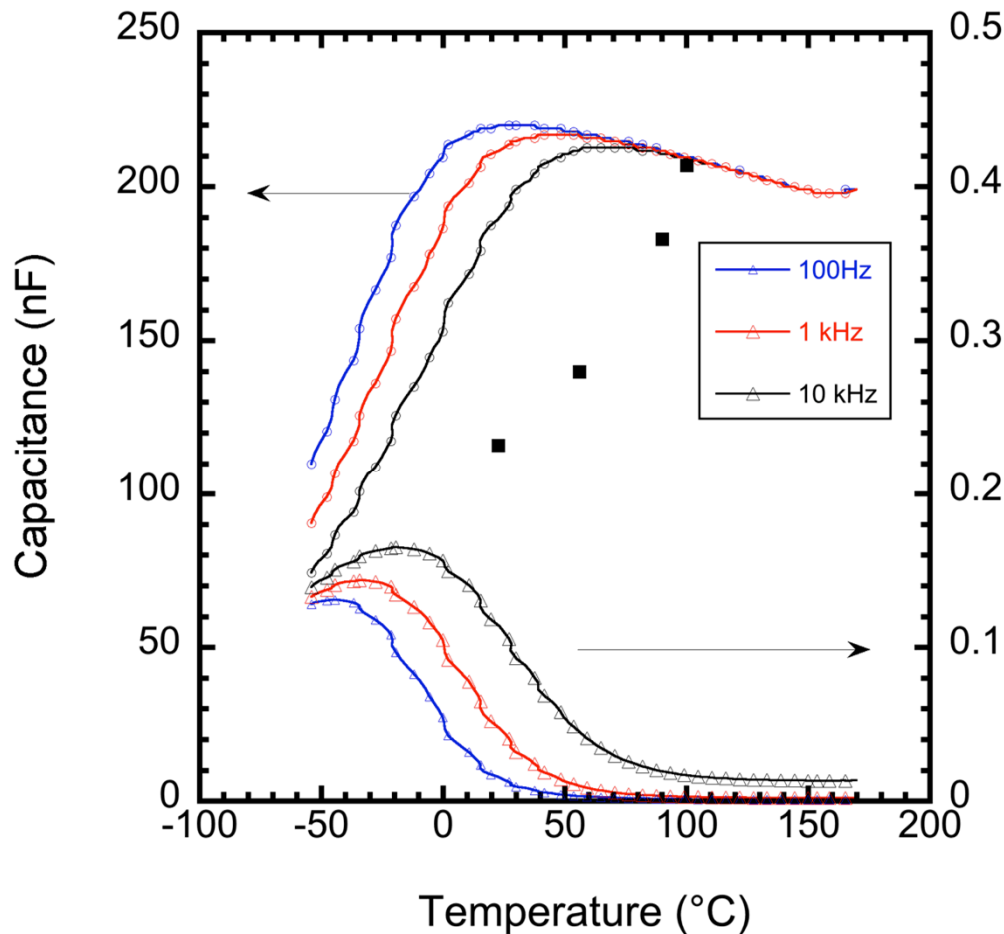
Waveform shapes changed with increasing temperature



Loss of small signal between 200 and 300 ns with increasing temperature...thermal activation of slow polarization mechanisms and increases capacitance is observed
Capacitance appears to increase with temperature (higher peak current)

Dielectric relaxation was also shown at elevated temperatures

Frequency Domain

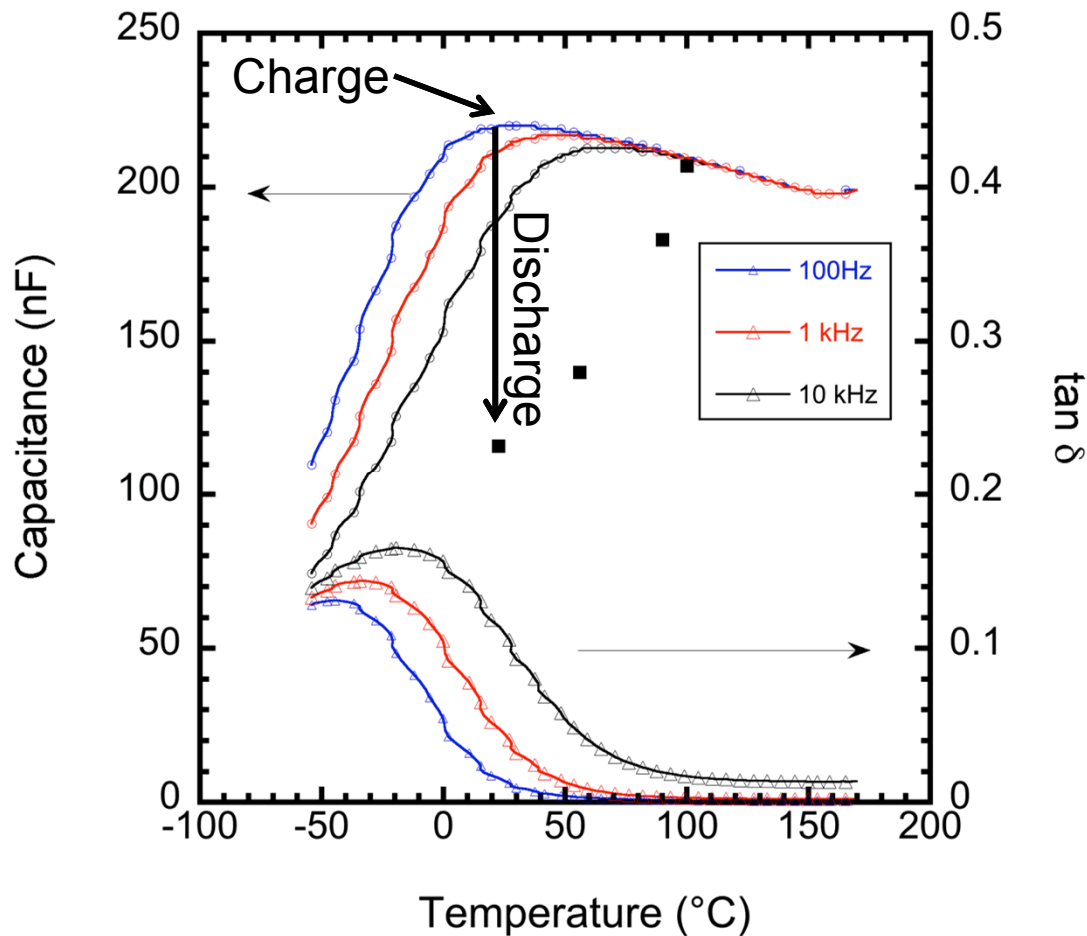


Time Domain

Temperature (°C)	C _{2-5MHz} (nF)	C _{10mHz} (nF)
-55	-	170
-40	-	159
-30	-	214
10	-	-
22.5	116	208
56	140	-
90	183	-
100	207	-

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

Combining frequency and time domain data



The charge capacitance should be:

$$E = \frac{1}{2} c_{low-f} V^2$$

The discharge capacitance should be:

$$E = \frac{1}{2} c_{high-f} V^2$$

Dielectric loss only accounts for <15%

The energy stored by the MLCC must equal the energy dissipated during discharge

Stored (DC charge)

Discharged

$$E = \frac{1}{2} c V^2 = 1.23 \mu J \quad E = \frac{1}{2} 142 nF (3.34 Volts)^2 = 7.92 \times 10^{-7} Joules$$

Dissipated during discharge
by circuit resistance

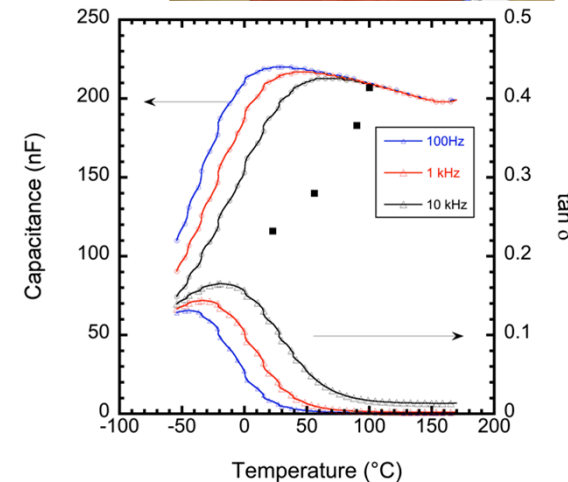
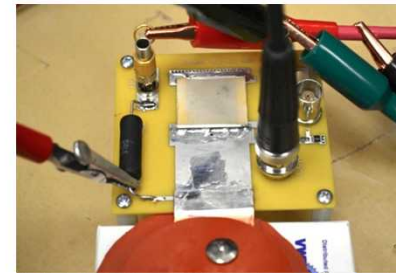
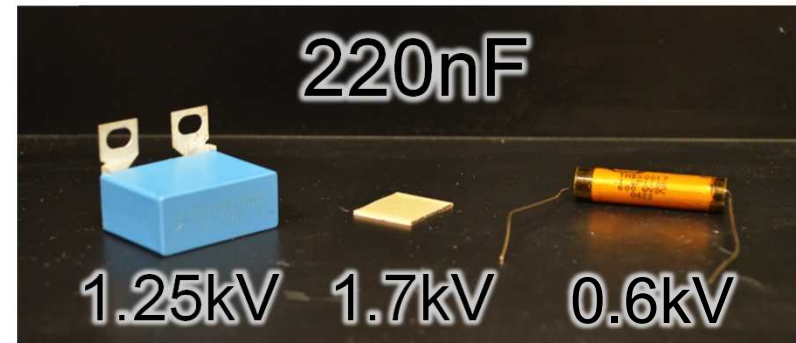
$$E_{discharged} = R \int_{t=0}^{t=dis.} i_{CVR}^2 dt \quad E = 474 \Omega \int i(t)^2 dt = 8.22 \times 10^{-7} Joules$$

The values agree to within 96%
220nF polymer cap agrees to within 99%

We still don't know where 40% of the
energy went from the effective low- f
charge and high- f discharge

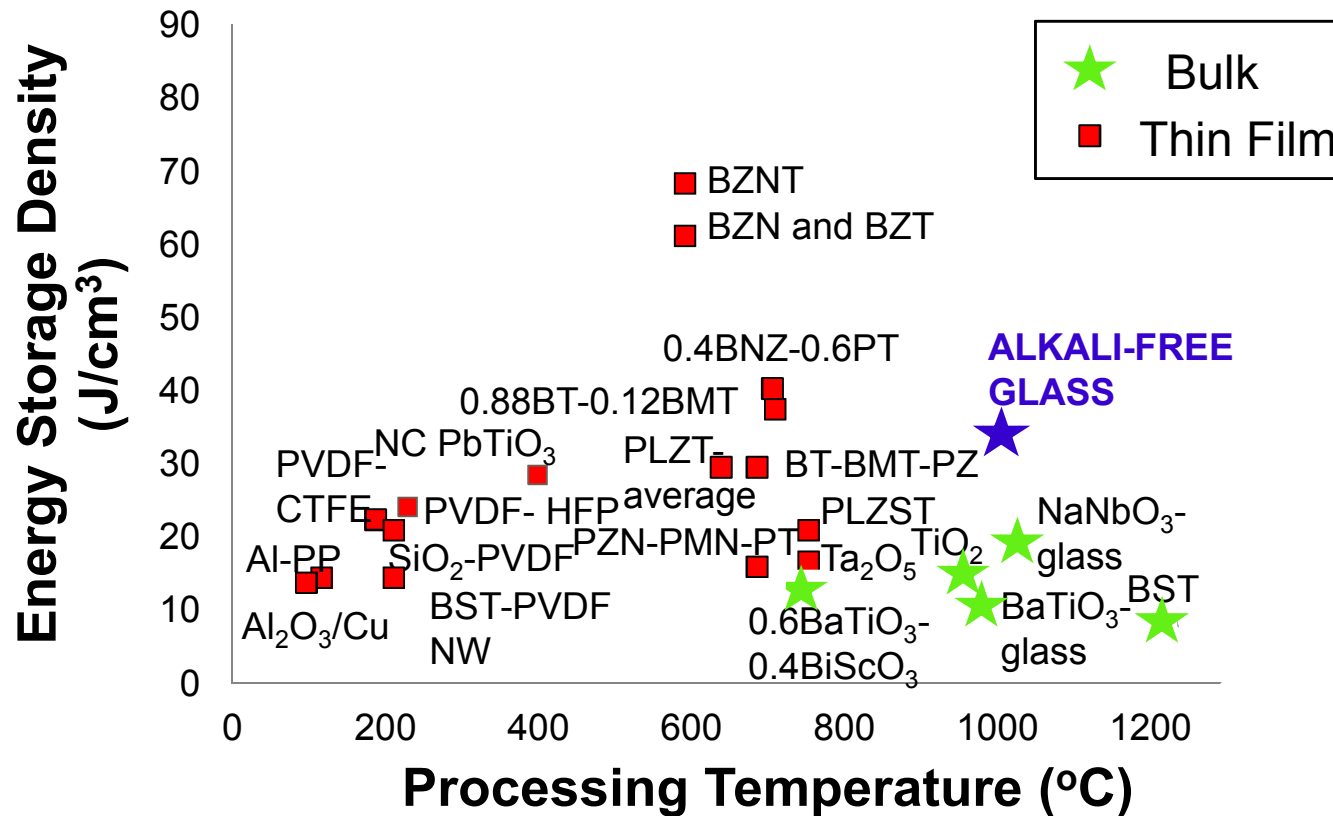
Summary

- 200 nF MLCCs were successfully fabricated from BZT-80BT
- Capacitance values calculated from pulse discharge data reveals that the dielectric relaxation is observable in the time domain
- We can reduce the temperature of the dielectric relaxation through solid solution formation



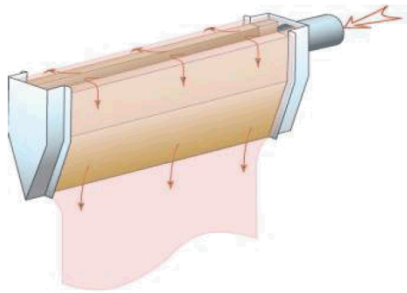
Low K dielectrics for high voltage capacitors

Comparison of Capacitive Energy Storage Materials



- Alkali-free glass competitive with many emerging materials
- May have an advantage in manufacturing
- Packaged capacitors: 0.3-3 J/cc (depending on voltage rating)
 - Can we make 1 kV, 100 nF capacitors?

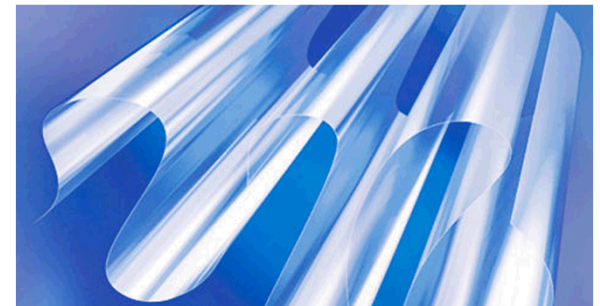
Alkali-Free Glasses



- “Overflow drawn down process”

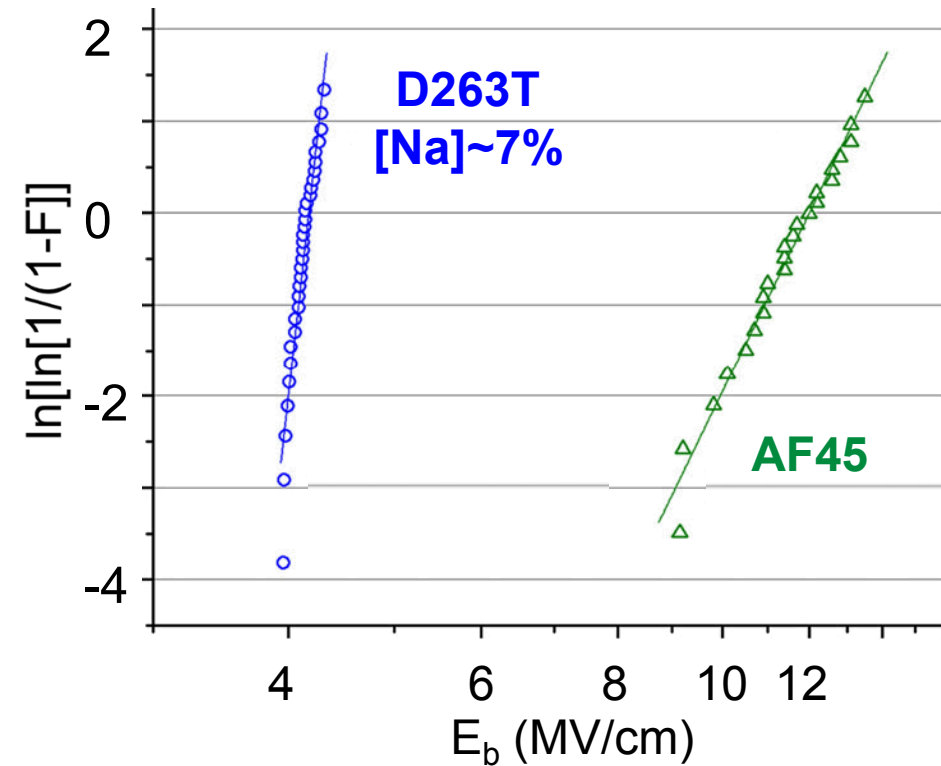


Parameter	Value
Density (g/cm ³)	2.3-2.5
Young's Modulus (GPa)	73-75
ϵ_r	5-6
$\tan \delta$	0.001
ρ ($\Omega \cdot \text{cm}$ @ 250 °C)	$>10^{12}$
Strain Point	650-700 °C

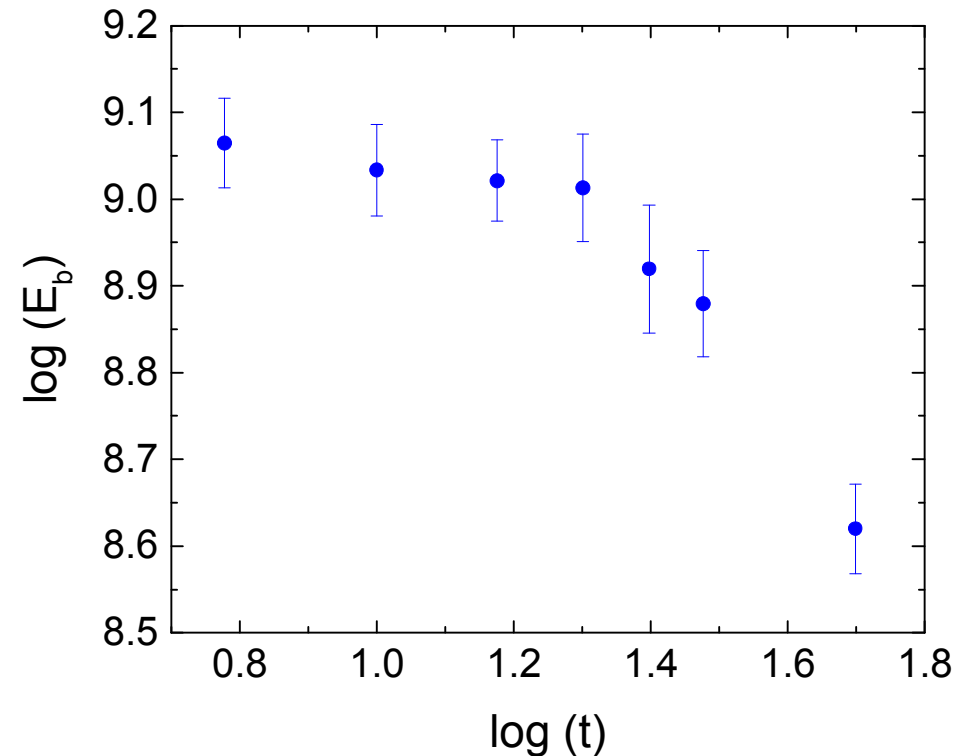


- Sold by many vendors world wide
- Boro-alumino-silicate glass system
- Sold in thicknesses $\sim 100 - 200 \mu\text{m}$
- $[\text{Na}] < 350 \text{ ppm}$ (typical)

Breakdown Strength of Alkali-free Glass



Parameter	D263T	AF45
t (μm)	30	19
E_b (MV/cm)	4.2	12
β	47.9	10.7



- Schott AF45 glass etched via sonicating in HF
- For $t < 20 \mu\text{m}$, $E_b > 10 \text{ MV/cm}$
- $U_{\text{dielectric}} \sim 35 \text{ J/cc}$

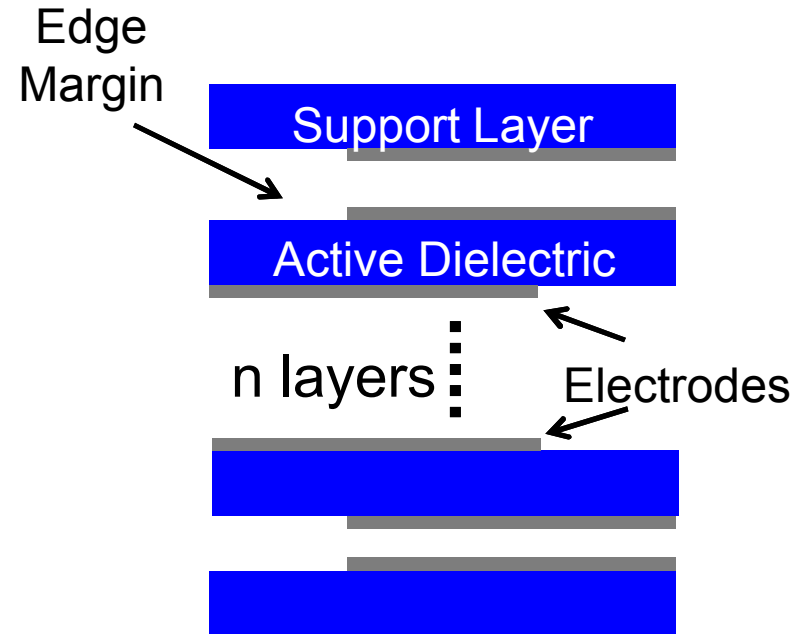
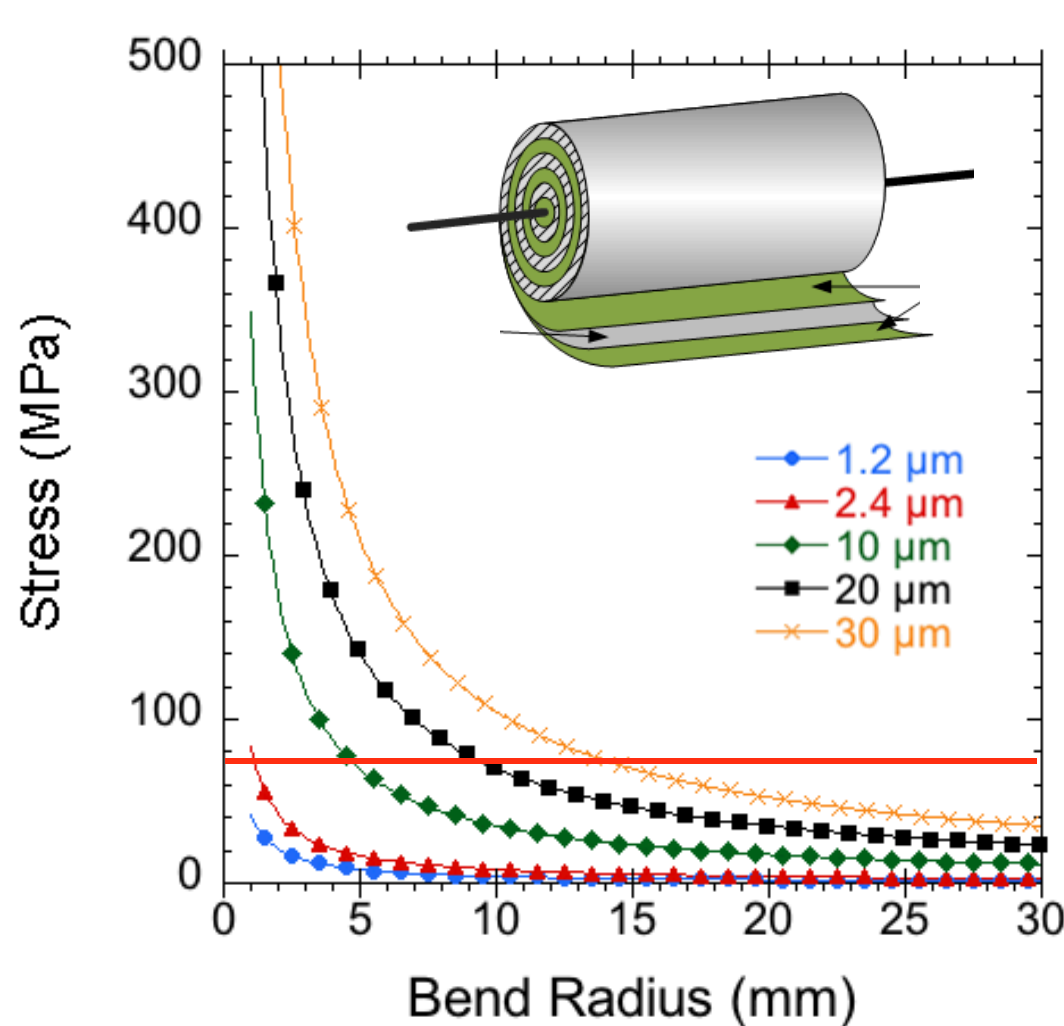
Thinning of Glass - Motivation



5 μm thick, 8 mm diameter

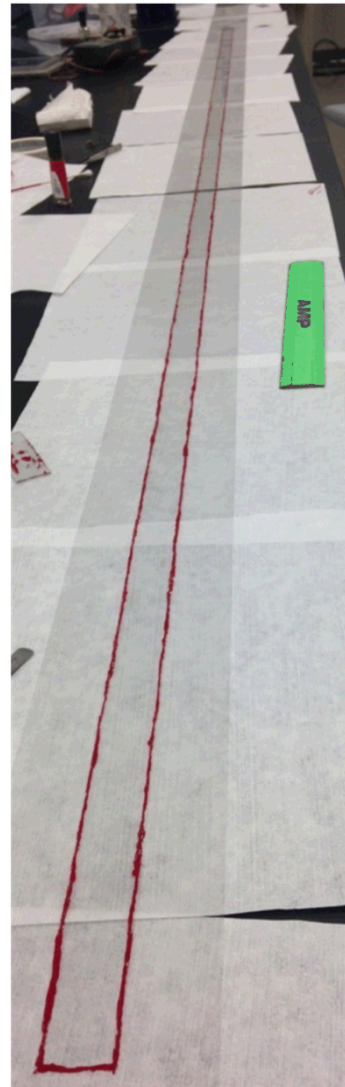
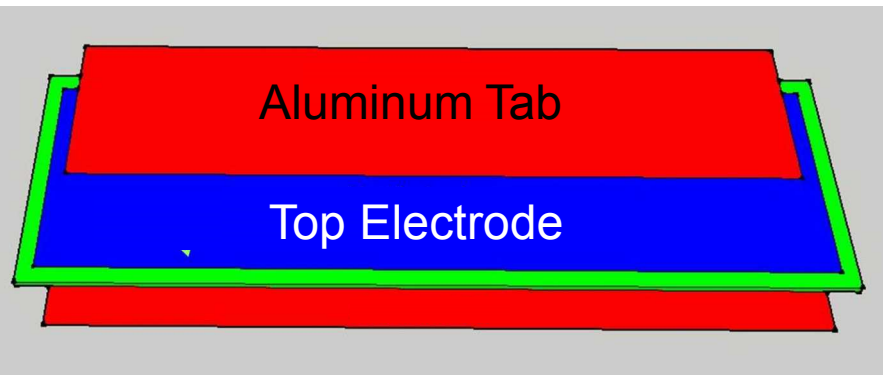
- Alkali-free glass has found broad application in mobile device and display applications
- Commercially sold in thickness $> 100 \mu\text{m}$ (1.3 x 300 m rolls)
- $\epsilon_r \sim 5-6 \Rightarrow$ Need massive area ($> 20 \text{ cm}^2$) to achieve 1 nF capacitance

Thinned Glass Capacitors Designs



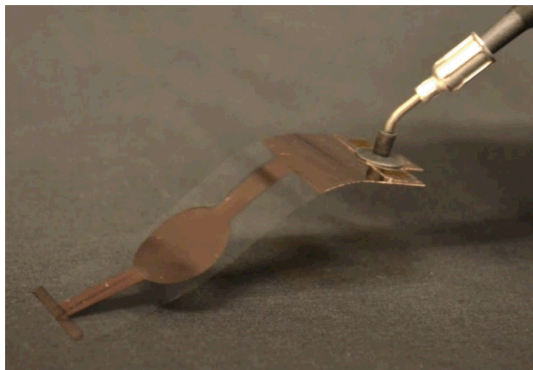
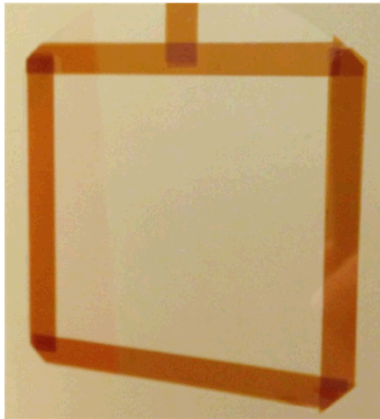
- Top/Bottom sheets for physical support
- Edge margin to avoid flashover
 - Needs insulating fluid to avoid triple points

Fabrication of a Wound Capacitor



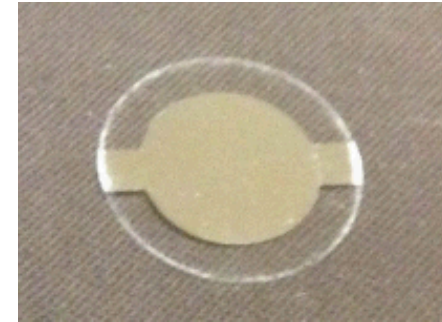
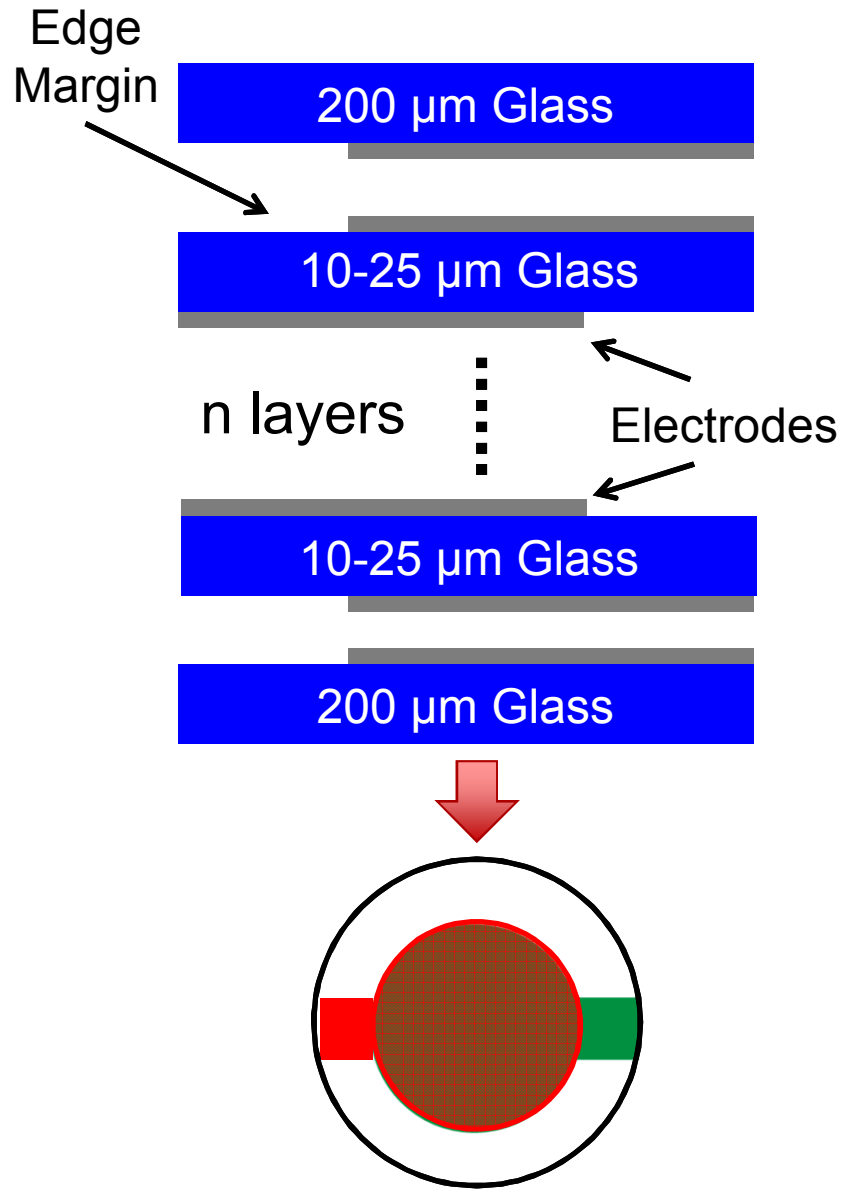
- 2.7 m long piece of 50 μm thick NEG Glass
- Designed to have electrode tabs to limit electrode resistance and inductance effects
- Wound around 14 cm diameter spool
- 1 kV: $U_{\text{dielectric}} \sim 10 \text{ mJ/cc}$, $U_{\text{capacitor}} \sim 0.5 \text{ pJ/cc}$

Thinning of Glass - Process



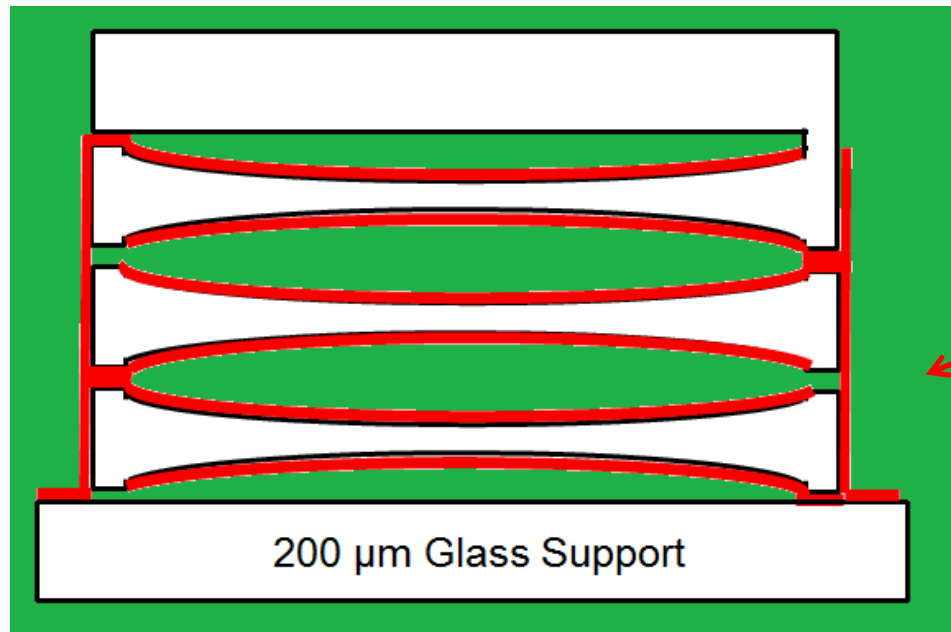
- Glass is masked on edges – provide mechanical structure for thinned samples
- Etched in 2.5% HF solution ($0.01 \mu\text{m}/\text{s}$)
- Sputter electrodes (100 nm)

Fabrication Approach for Multi-layer Glass Capacitor

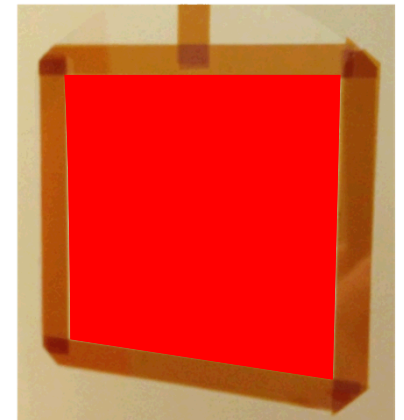


- Pattern 0.75" diameter electrode with edge tab
 - Electrode deposition top and bottom – rotated 180°
- Laser cut glass to form individual capacitor layer
 - Edge margin is 0.125" (~ 10 kV hold off voltage in air)

Fabrication of Large Area/Multi-Layer Capacitor

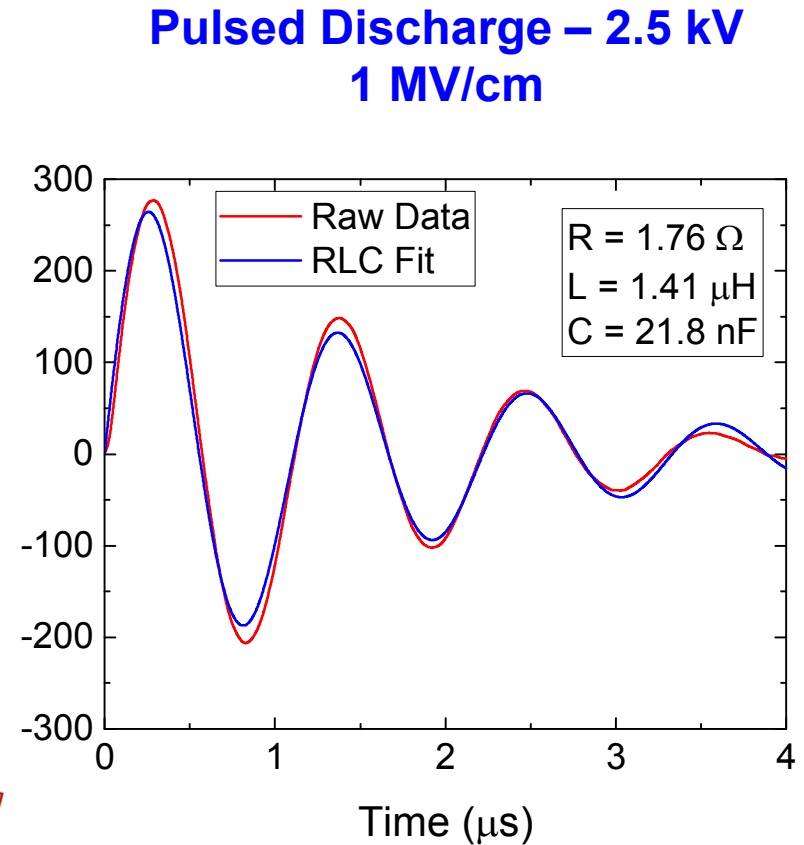
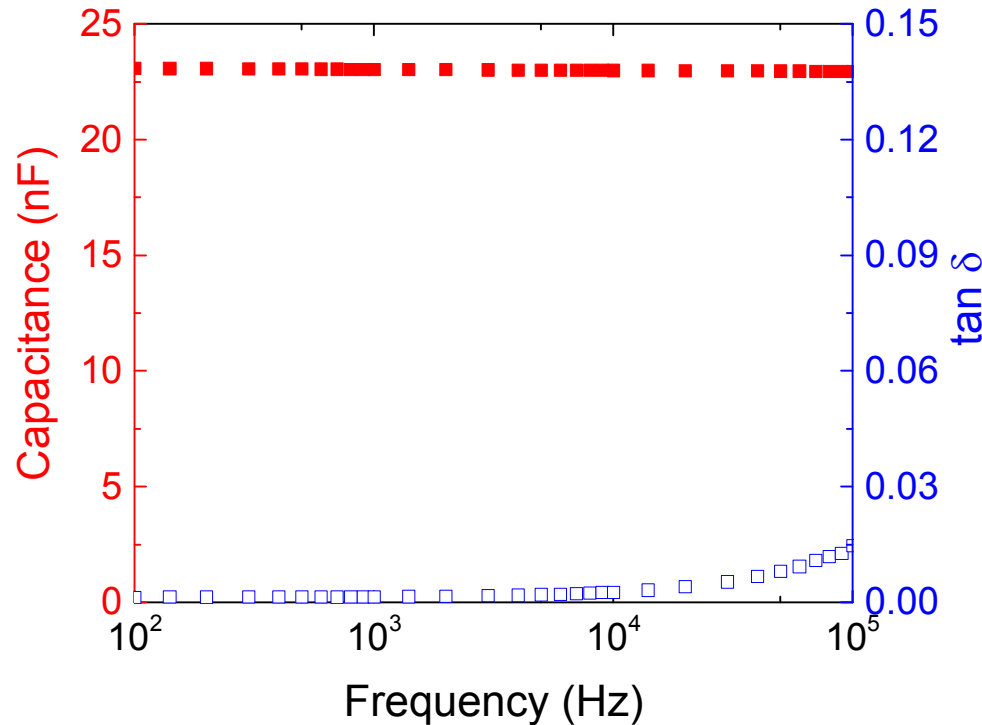


← Fluorinert
Cu Electrodes



- Left 200 μm thick support frame around 25 μm thick thinned glass (60 mm \times 60 mm)
- Immersed in Fluorinert for measurement
- Layers bonded together using air dried silver paint

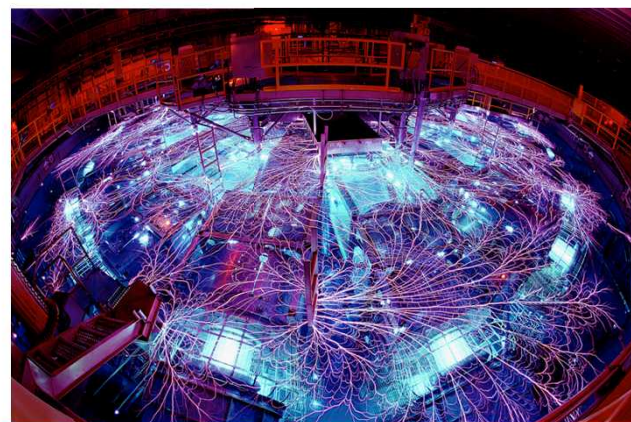
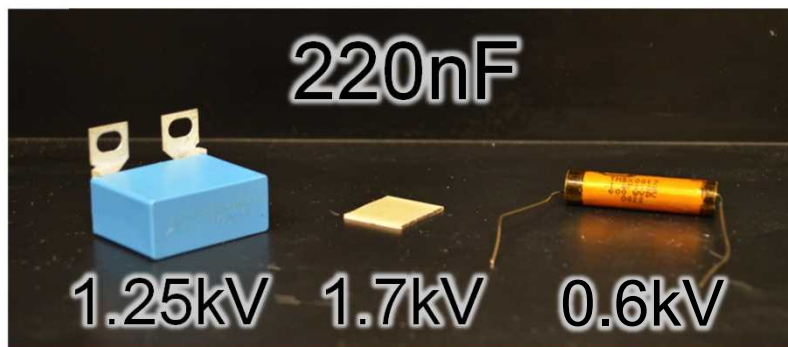
Properties of Multi Layer Glass Capacitor



- $C(1 \text{ kHz}) = 23.0 \text{ nF}$, $\tan \delta = 0.001$
- $U_{\text{dielectric}} \sim 0.24 \text{ J/cc}$ – need to improve end termination to push E_{applied}
- $U_{\text{capacitor}} \sim 70 \text{ mJ/cc}$ - can increase by increasing n , decreasing edge margin, using thinner support layers

Path Forward

- Partner with commercial entities to develop system specific disruptive technologies
- Continue to refine glass post processing to achieve packages relevant to high power electronics
- Continue to evaluate material and package response in pulsed power environments



Acknowledgements

- Adrian Casias and Adrian Wagner
- Prof. Geoff Brennecka
- Mia Blea

Funding Sources

- The authors acknowledge the support of
 - Dr. Imre Gyuk and the Department of Energy's Office of Electricity Delivery and Energy Reliability

Questions?

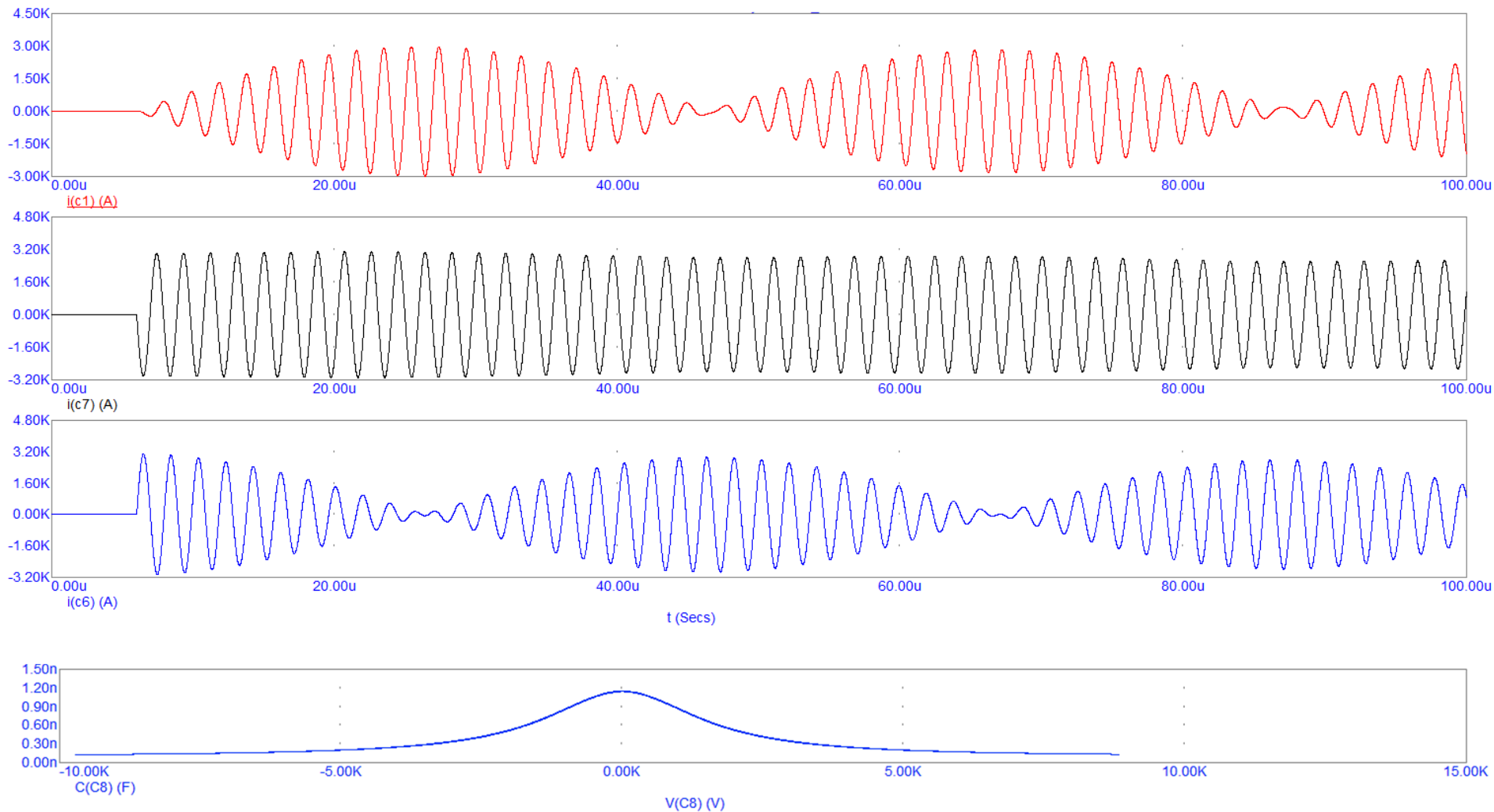
Derek Wilke

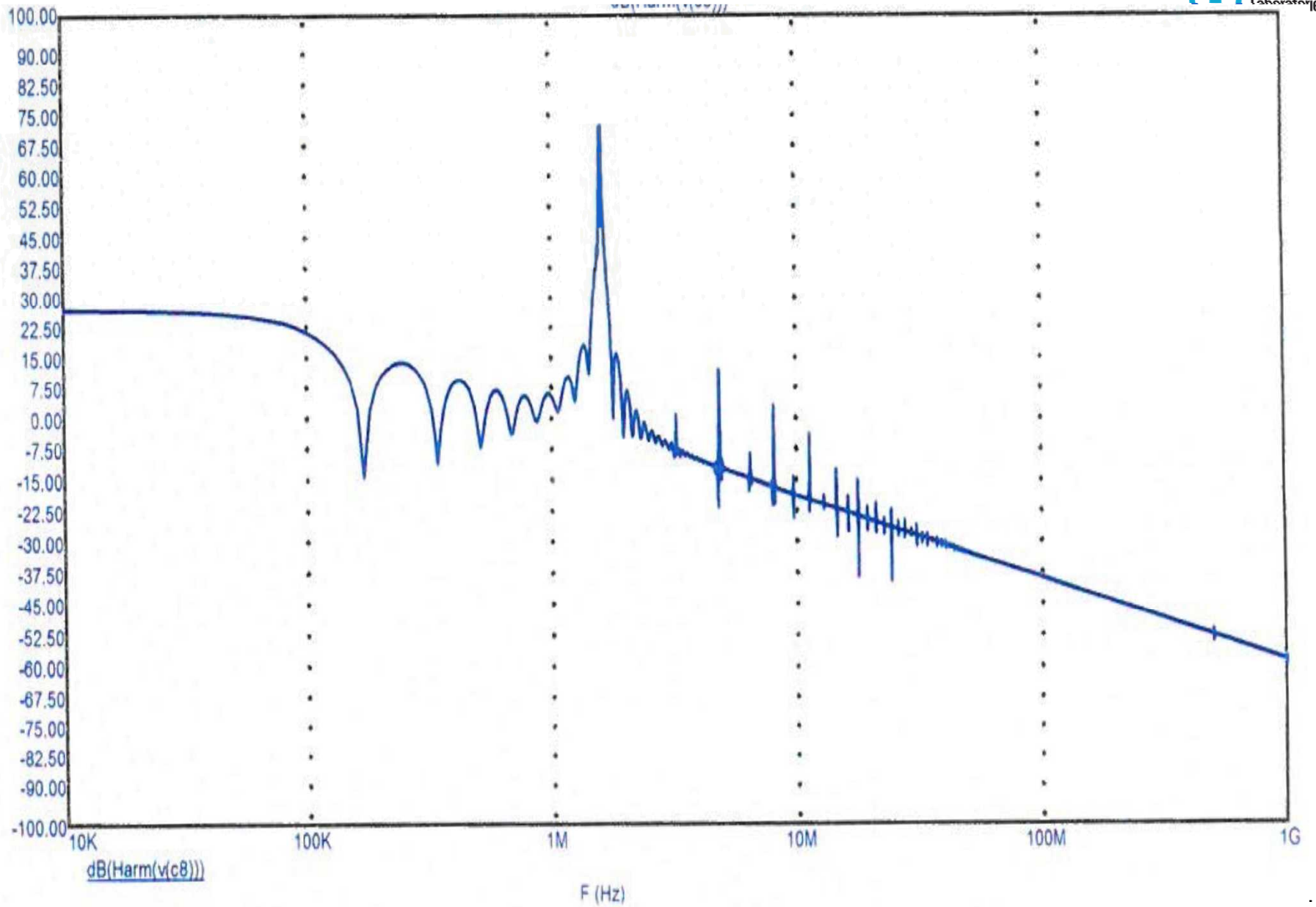
rhwilke@sandia.gov

Harlan Brown-Shaklee

hjbrown@sandia.gov

Underdamped case with non-linear dielectrics Sandia National Laboratories



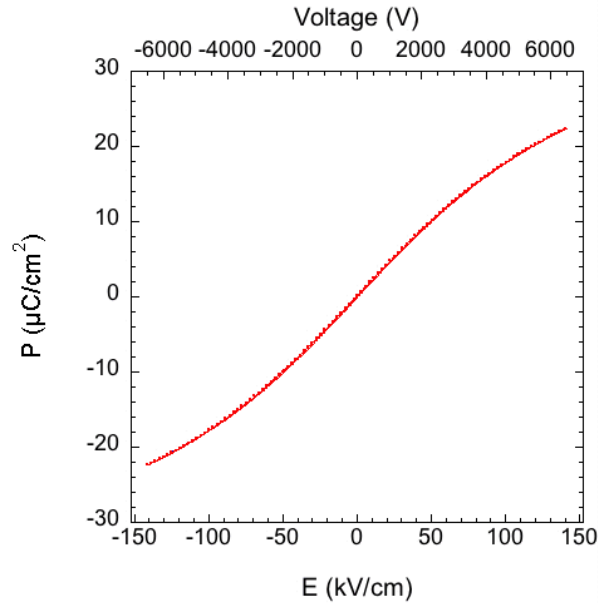


200nF MLCCs were fabricated in house



- BZT-BT powder was synthesized from BaCO_3 , Bi_2O_3 , ZnO , and TiO_2
- Powders were calcined at 950°C for 12 hrs in air
- Particle size was reduced by ball milling
- Milled powders were blended with Ferro B-73305 PVB-based binder
- 15.25 cm wide tapes were cast on a heated bed
- Tapes were printed with DuPont 9894 Pt-Ink
- Sample burnout in flowing O_2 and sintering in stagnant air

Energy densities of >1.3 J/cc have been demonstrated



Dimpled Electrode

$$t=460\mu\text{m}$$

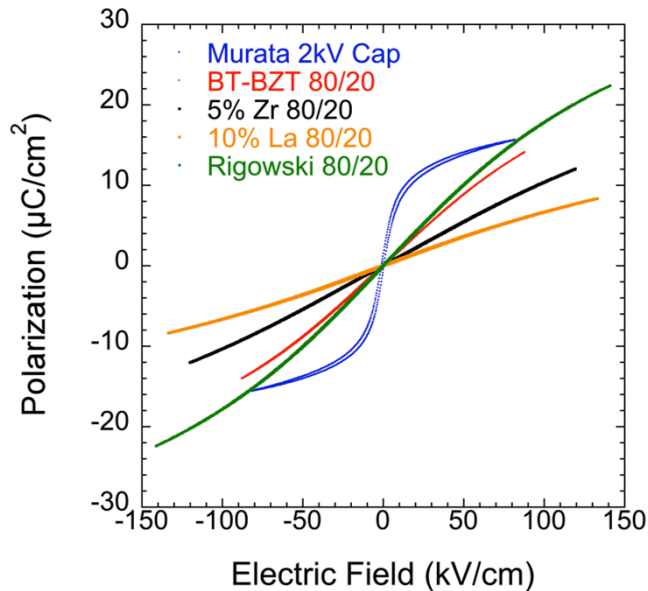
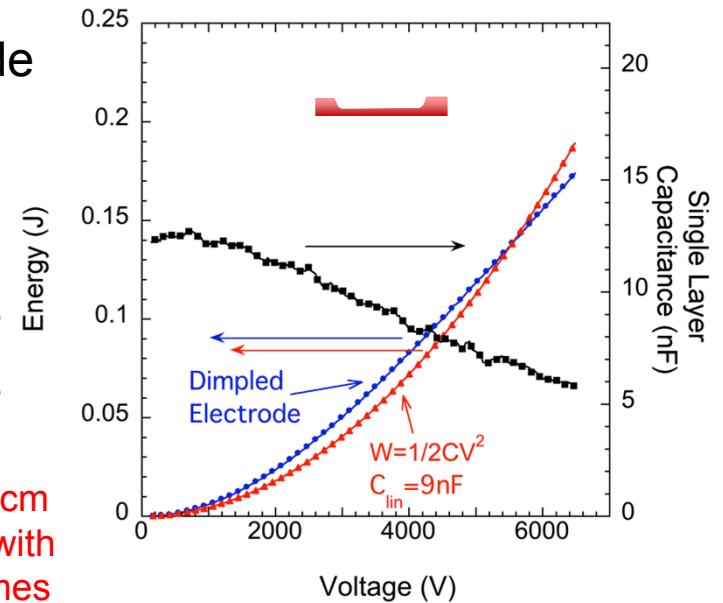
$$A=2.77\text{cm}^2$$

$$v=0.127\text{cm}^3$$

$$E/v_{100\text{kV/cm}}=0.82\text{ J/cm}^3$$

$$E/v_{140\text{kV/cm}}=1.35\text{ J/cm}^3$$

Breakdown >230 kV/cm
have been achieved with
smaller sample volumes



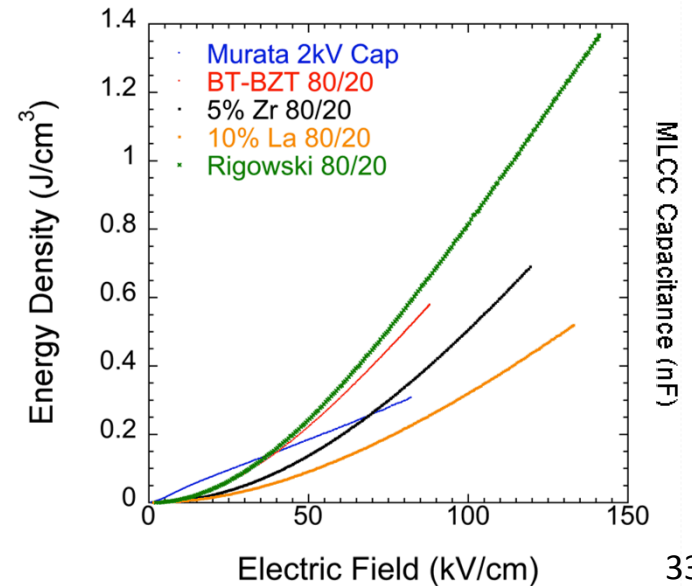
200nF MLCC

$$t=135\mu\text{m}$$

$$A=18.1\text{cm}^2$$

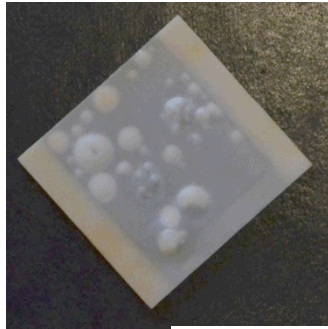
$$v=0.262\text{cm}^3$$

$$E/v_{100\text{kV/cm}}=0.69\text{ J/cm}^3$$

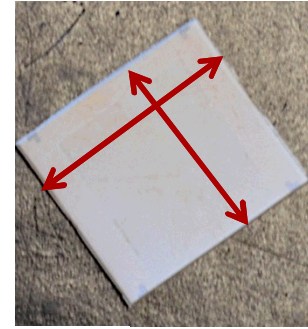


Blistered 200 nF MLCC were fabricated initially

MLCC sintered at 1210°C



MLCC sintered at 1040°C

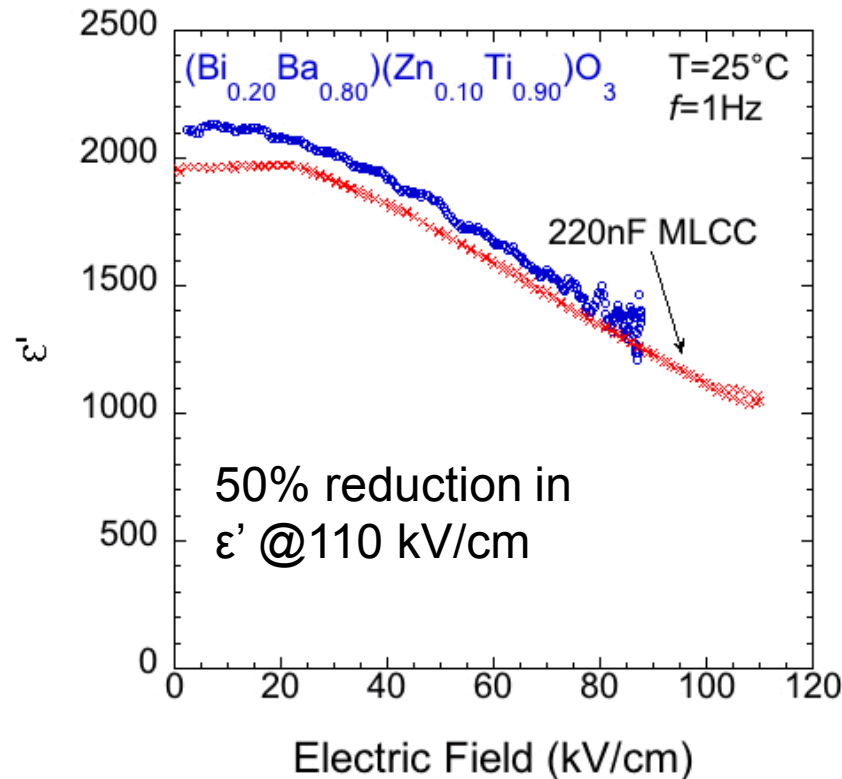


Reduced sintering temperature

No blisters

Systematic study eliminated blisters in MLCCs

RGA indicated that O_2 was released above 1000°C



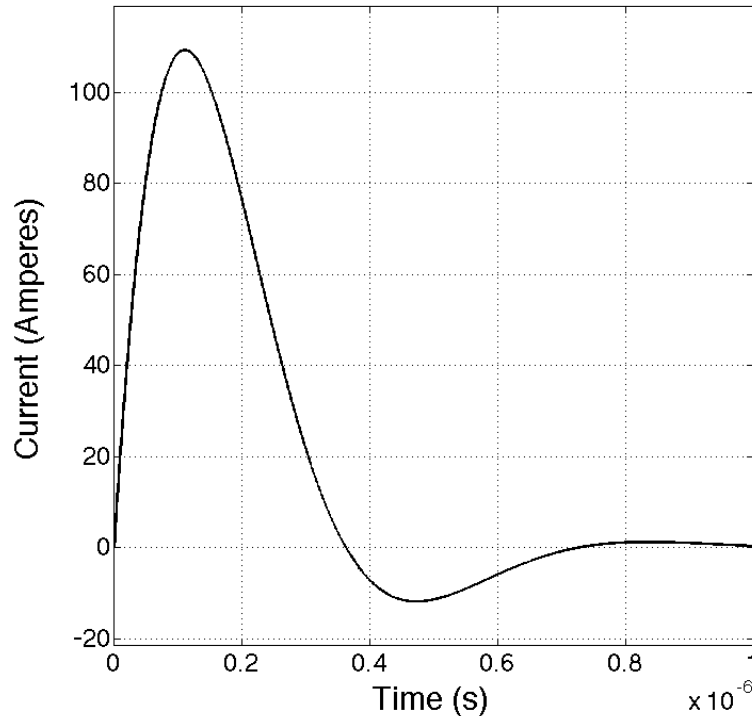
$L = 22.68$ mm
 $w = 24.4$ mm
 $t = 1.12$ mm

6 active layers
9894 Pt ink with BZT-80BT dielectric

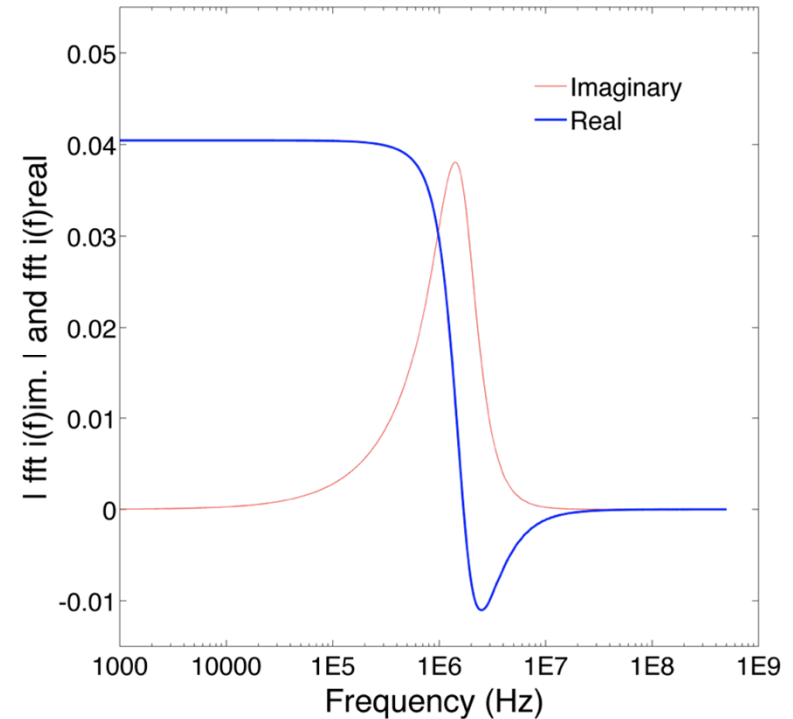
Final dicing can reduce package size (fiducials painted in Pt on top of MLCC)

Dominant frequencies from a current pulse can be extracted using a Fourier transform

Current Waveform from Underdamped RLC Circuit Fourier Transform $\sim 1.4 \text{ MHz}$



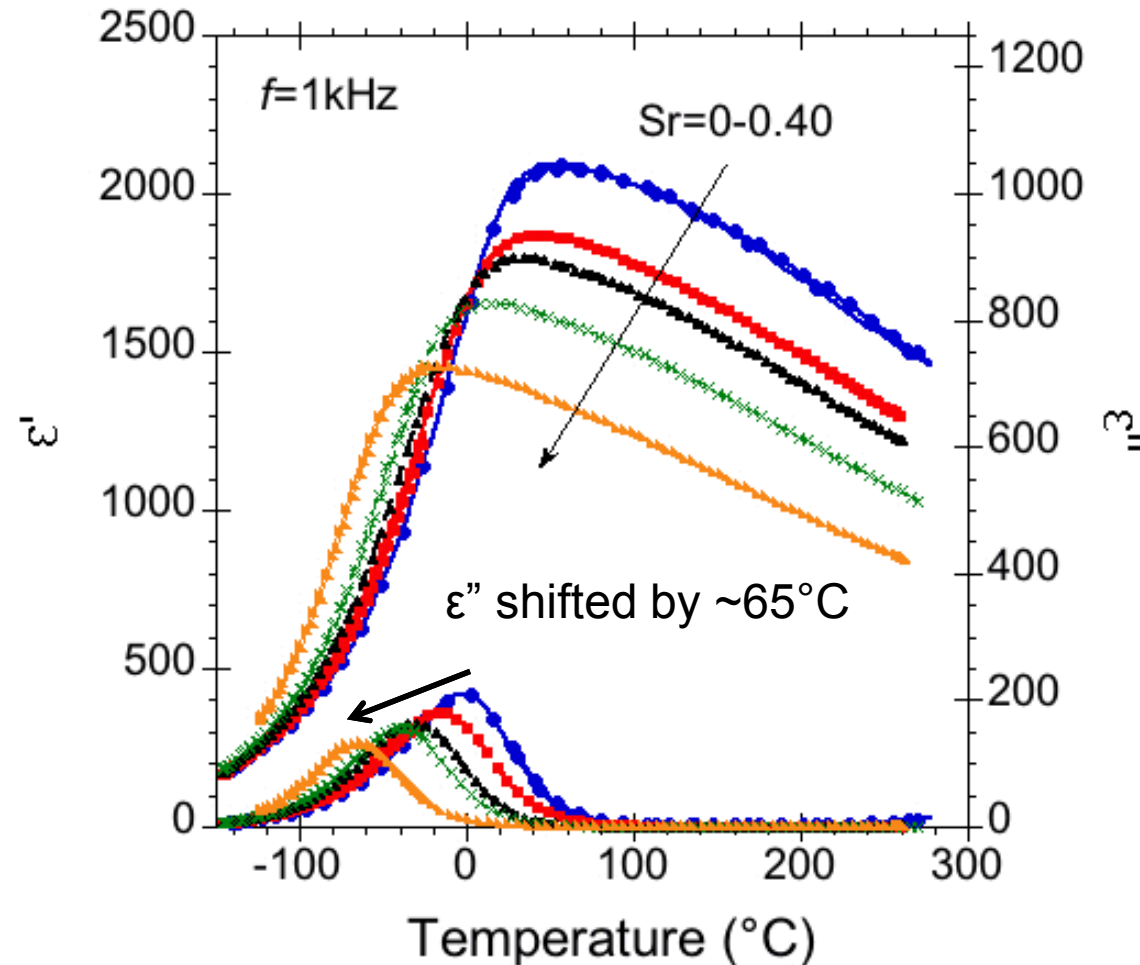
Time Domain



Frequency Domain

Dominant frequency ($\sim 1.4 \text{ MHz}$) of the current pulse measured with a CVR agrees well with that calculated from $\omega_0 = 2\pi f$

Sr shifts T_{\max} below room temperature



Sr (%)	$\text{TC}\epsilon'$ (ppm/K)
0	-1338
5	-1464
10	-1479
20	-1474
40	-1603

$$\text{TC}\epsilon' = \frac{-(\epsilon'_{\max} - \epsilon'_{\max@+180^{\circ}\text{C}})}{\epsilon'_{\max@+90^{\circ}\text{C}}(180^{\circ}\text{C})}$$

- Dielectric relaxation should be below 0°C for high frequency and fast pulse applications