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Models for Total-Dose Radiation Effects in Non-Volatile Memory

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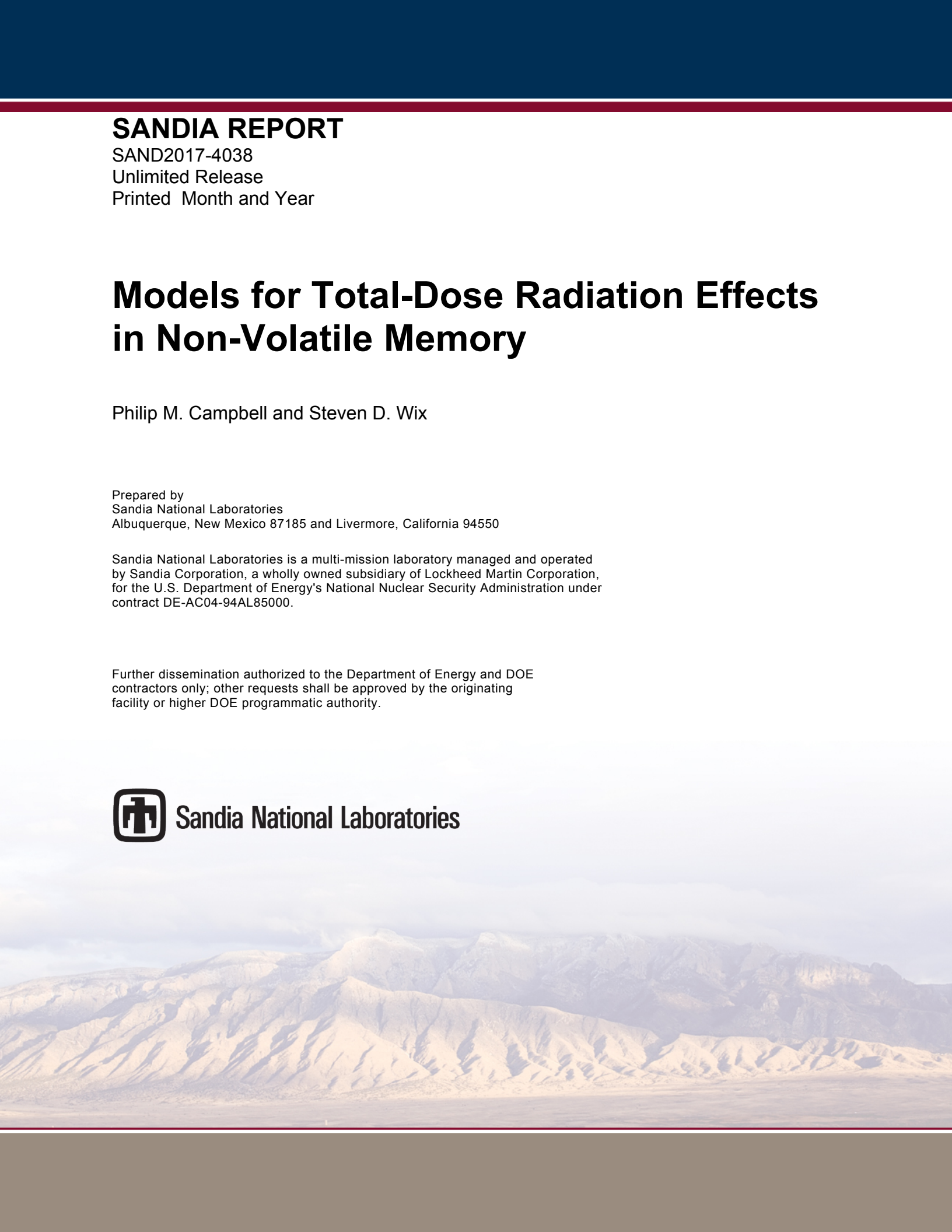

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Models for Total-Dose Radiation Effects in Non-Volatile Memory

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Abstract

The objective of this work is to develop models to predict radiation effects in non-volatile memory: flash memory and ferroelectric RAM. In flash memory experiments have found that the internal high-voltage generators (charge pumps) are the most sensitive to radiation damage. Models are presented for radiation effects in charge pumps that demonstrate the experimental results. Floating gate models are developed for the memory cell in two types of flash memory devices by Intel and Samsung. These models utilize Fowler-Nordheim tunneling and hot electron injection to charge and erase the floating gate. Erase times are calculated from the models and compared with experimental results for different radiation doses. FRAM is less sensitive to radiation than flash memory, but measurements show that above 100 Krad FRAM suffers from a large increase in leakage current. A model for this effect is developed which compares closely with the measurements.

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ACKNOWLEDGMENTS

The authors are grateful to Guy Chun for providing a report on radiation effects in a Ramtron ferroelectiic device.

TABLE OF CONTENTS

FIGURES

TABLES

NOMENCLATURE

Abbreviation	Definition
FG	Floating Gate
FRAM	ferroelectric RAM
PZT	lead zirconate titanate
NMOS	N-doped Metal Oxide Semiconductor
VDD	Label for externally applied voltage
FE	Ferroelectric

1. INTRODUCTION

In this work, we develop models for total dose radiation effects in non-volatile memory (Flash and FRAM). A flash memory cell consists of a MOSFET with a floating gate as shown in Figure 1.

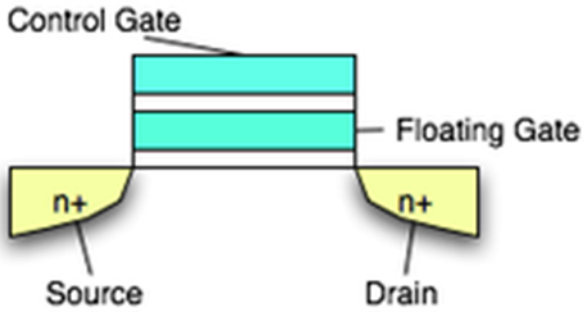

Figure 1. Structure of a flash memory cell.

When the floating gate (FG) is charged with electrons (programmed) the threshold voltage rises and the drain current shuts off. This represents a logical state 0. When the FG is discharged, the drain current resumes, and this is logical state 1. Radiation data is available for two types of flash memory technology, one by Samsung and one by Intel [1]. The Samsung device uses Fowler-Nordheim tunneling both to charge and discharge the FG. The Intel device uses hot electron injection to charge the FG and Fowler-Nordheim for discharge as illustrated in Figure 2.

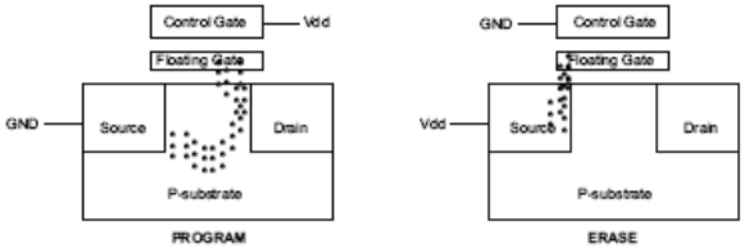

Figure 2. Flash memory cell programmed by hot electron injection and erased by Fowler-Nordheim tunneling.

These devices operate with a logic voltage of either 3.3 V or 5 V, but programming and erase require higher voltages, 20 V for the Samsung device and 12 V for the Intel. The high voltages are obtained from an on-chip high voltage generator or charge pump. Experiments show that the MOSFETs in the charge pump are the most sensitive to radiation damage. Even if the internal charge pump is bypassed, the charge retention properties of the cell may also be affected by radiation.

Another non-volatile memory device of interest is ferroelectric RAM or FRAM [2]. A FRAM chip contains a capacitor formed with a thin ferroelectric film of lead zirconate titanate, usually referred to as PZT. The Zr/Ti atoms in PZT change polarity

in an electric field producing a binary switch. This device offers the same functionality as flash memory. The design of an FRAM memory cell compared with DRAM is shown in Figure 3. Below we look at how total-dose-effects influence the FRAM device to predict where functionality is affected due to radiation damage.

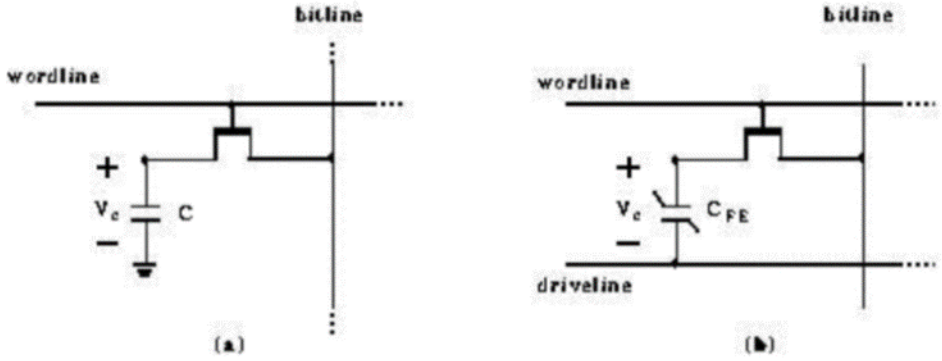

Figure 3. An FRAM memory cell (b) compared to DRAM (a).

2. CHARGE PUMP OPERATION WITH RADIATION EFFECTS

The basic Dickson charge pump [3] is constructed with diodes as shown in Figure 4, and we have developed models for these structures.

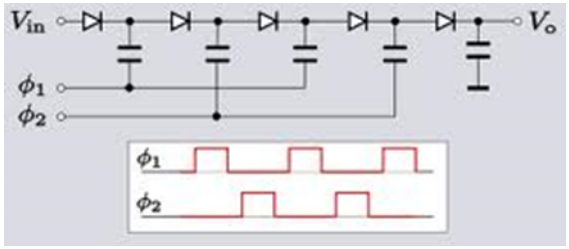

Figure 4. Basic four-stage Dickson charge pump.

Because of fabrication issues in flash memory, the diodes are replaced with MOSFETs wired to function as a diode as shown in Figure 5. The MOSFET-based charge pump is usually less efficient than the diode version, because there is a voltage drop in each stage which depends on the threshold voltage. To a first approximation, the output voltage V_{out} is given in terms of the logic voltage V_{DD} and the threshold voltage V_{th} by,

$$V_{out} = V_{DD} - V_{th} + N \times \left(V_{DD} - V_{th}\right) \qquad 1$$

where N is the number of stages. A more detailed analysis of charge pump circuits can be found in the references [4] [5] which include the effects of stray capacitance and the body effect which modifies the threshold voltage in MOSFETs.

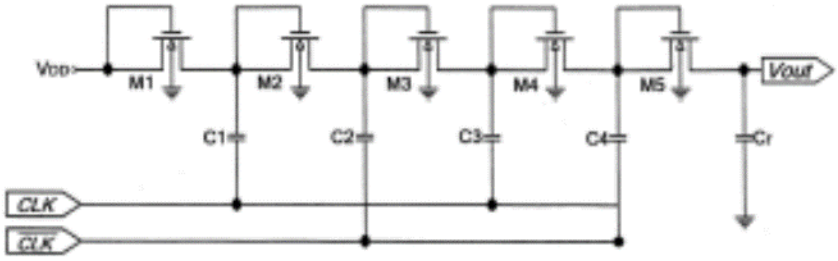

Figure 5. A four-stage voltage multiplier utilizing MOSFETs operating as diodes.

Total dose radiation effects in the MOSFET [6] can increase the threshold voltage to the point where the efficiency of the charge pump is too low to charge and discharge the FG in a flash memory cell effectively. To model these effects, we begin with a brief summary of threshold shifts due to trapped charge in the gate oxide of MOSFETs.

When a gate oxide is exposed to ionizing radiation, electron-hole pairs are formed uniformly throughout the oxide. Electrons are extremely mobile and are quickly swept out of the oxide under the gate electric field. The holes that escape initial recombination drift toward one of the two interfaces, $gate / SiO_2$ or $Si/Si\,O_2$, depending on the sign of the applied field. Holes will be trapped in the strained region of the oxide near the interface creating a positive oxide-trapped charge. The trapping centers are neutral oxide defects (oxygen vacancies) that can trap holes and hold them for long periods. In radiation-hardened gate oxides the distribution of trapped holes is normally within a few nanometers of the interface.

As a result of the hole transport and trapping process, hydrogen (H^+) is released from hydrogen-containing defects in the oxide. The hydrogen will drift to the $Si/Si\,O_2$ interface where it can interact to form interface traps (dangling bonds in Si). For n-channel devices interface traps are negatively charged, and for p-channel devices interface traps are positively charged.

A positive oxide-trapped charge distribution introduces a negative threshold voltage shift given by [6]

$$\Delta V_{ot} = -\frac{q}{\varepsilon_{ox}} \bar{x} \Delta N_{ot} \qquad 2$$

where $\varepsilon_{ox} = 3.45 \times 10^{-13}$ F/cm is the oxide permittivity, q is the electron charge, ΔN_{ot} is the sheet density of trapped charge in cm^{-2}, and $\bar{x}$ is the centroid of the charge distribution where x is distance from the gate electrode. With a positive gate bias, the trapping sites are usually located within a few nanometers of the Si/SiO_2 interface. In this case $\bar{x} \cong t_{ox}$, where t^{ox} is the oxide thickness, and the threshold shift becomes,

$$\Delta V_{ot} = -\frac{q}{C_{ox}} \Delta N_{ot} \qquad 3$$

where $C_{ox} = \varepsilon_{ox} / t_{ox}$ is the oxide capacitance per unit area. With a negative gate bias where the holes are trapped near the $gate / SiO_2$ interface, $\bar{x} << t_{ox}$. The voltage shift due to interface-trapped charge is given by

$$\Delta V_{it} = \frac{q \Delta N_{it}}{C_{ox}} dtype, \qquad 4$$

where q is the electron charge, ΔN_{it} is the sheet interface charge density in cm^{-2}, and dtype is +1 for n-channel devices and -1 for p-channel devices. The total threshold voltage shift is the sum of the two contributions,

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \qquad 5$$

The shift for holes trapped in the oxide is always negative, but the shift due to interface-trapped charge can be either positive or negative depending on the type of device.

The key component in Equations (2) and (4) is the trapped charge density as derived from the radiation dose. As shown in reference [6], the oxide-trapped charge can be written,

$$\Delta N_{ot} = N_T [1 - \exp(-G_0 DY \sigma_T t_{ox})], \qquad 6$$

where N_T is the sheet density of trapping sites, $\sigma_T = \sigma_0 E^{-0.55}$ is the field-dependent cross section for the capture of a hole at a trapping site, D is the radiation dose, $G_0 = 8.1 \times 10^{12} cm^{-3} / rad$ is the generation rate of e-h pair formation in SiO_2, and Y is the yield of e-h pairs that escape initial recombination. The cross section for capture of a hole is on the order of $\sigma_0 = 3 \times 10^{-14} cm^2$, where E is given in MV/cm.

The hydrogen reactions involved in interface-trap formation are described in reference [6]. Consideration of the hydrogen reactions in the bulk, transport of the protons released and their interactions with dangling bonds at the interface lead to an expression for the interface-trap density,

$$\Delta N_{it} = N_D\left[1 - \exp\left(-G_0 DY\sigma_H t_{ox}\right)\right] \qquad 7$$

In this expression, N_D is the sheet density of hydrogen-containing defects in the oxide, σ_H is the cross section for H^+ formation by holes, and it is assumed that all the hydrogen released in the bulk eventually forms interface traps. The value for σ_H lies in the range of 6×10^{-14} to 1.2×10^{-13} cm^2.

As reported in reference [1], the Intel device showed functional failure at a total dose of about 25 Krad. Although a detailed construction analysis of the charge pump used in the Intel device is not available, we can try to construct a model using the limited information given in reference [1] together with some of the details given in reference [7]. The Intel charge pump has an input value of 5.0 V with an output of 12 V. We adopt a value of 20 pf for the capacitors in each stage with an output capacitor of 10 pf in a configuration similar to Figure 5. We assume the clocks operate a 12.5 Mhz. The model parameters for the MOSFETs are derived as a variation of the SA3000 device and are given in Table 1.

Table 1. Model Parameters for MOSFETs in the Intel Charge Pump Simulation

U0 = 526.4	VTO = 2.60	NFS = 3.776E+11	TOX = 38.68E-09	TMOM = 27
NSUB = 9.408E+15	VMAX = 1.156E+05	RSH = 2.12	RS = 2.5	RD = 2
IS = 1E-11	THETA = 0.01035	ETA = 1.121	KAPPA = 0.05993	XJ = 6E-07

We ran a charge pump model in Xyce based on these parameters. Results for NMOS are shown in Figure 6. With eight stages the output is 12.0 V, which is the value required for programming and erasing the Intel memory cell. We lack measured values for the parameters in Equations (6) and (7) from which to obtain estimates for the trapped charge, but we can make some educated guesses based on the results given in Reference [6]. In Reference [6] radiation effects in several MOSFETs were analyzed with the key parameters in Equations (2) – (7) extracted. Referring to Table 2 in that report and assuming values near the low end of the range for N_T and N_D gives:

$N_T = 1.0\times10^{11}$, $\sigma_T = 2.60\times10^{-14}$, $Y = 0.55$, $t_{ox} = 38.7\times10^{-7}$, $D = 25\times10^3$

$N_D = 5.0\times10^{11}$, $\sigma_H = 1.2\times10^{-13}$, $Y = 0.55$, $t_{ox} = 38.7\times10^{-7}$, $D = 25\times10^3$

Comment [SJD]: definition

Using these parameters from Reference [6] as trial values for the Intel device, we get the following estimates for trapped charge: $\Delta N_{ot} = 1.13 \times 10^{9}\ \ cm^{-2}$, $\Delta N_{it} = 2.54 \times 10^{10}\ \ cm^{-2}$. When these values for a trapped charge are used in the simulation of the 8-stage charge pump, the output voltage falls to 11.74 V. The netlist for this simulation is given in Appendix 1. Whether this is enough of an effect to fail the device depends on calculated values for charging and erasing the cell. In the following section, we see that the oxide field appears in exponentials for both erase and write operations, and so a relatively small degradation of the charge pump can have a relatively large effect on programming and erasing the cell.

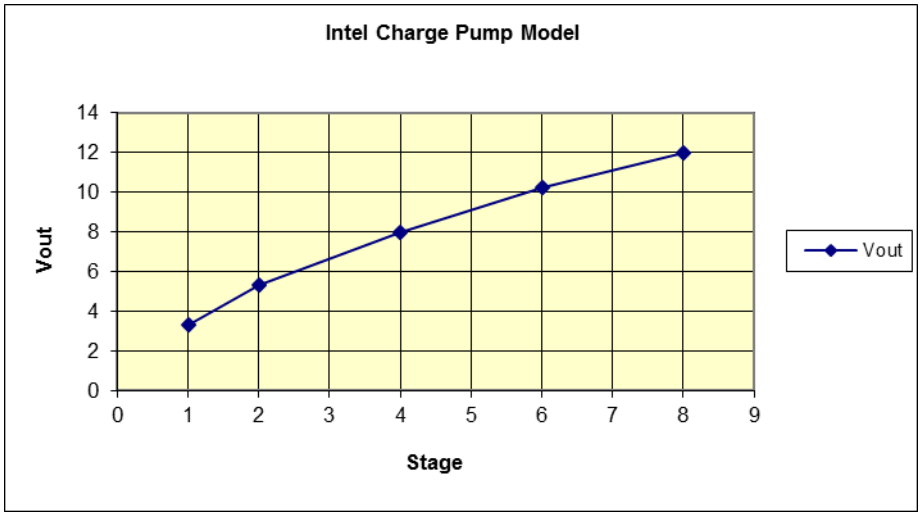

Figure 6. Output voltage of the Intel charge pump model with $V_{DD} = 5.0$ V.

3. MODELS FOR THE FLASH MEMORY CELL

Flash memory is generally produced in two architectures, NAND and NOR. We will look at two different devices, one by Intel which uses the NOR structure as shown in Figure 7, and one by Samsung which uses the NAND structure shown in Figure 8.

The Intel device is programmed with hot electron injection and erased with Fowler-Nordheim tunneling as shown in Figure 2. Programming and erase both require 12 V which can be applied externally, or 5 V can be applied externally with the charge pump activated. The Samsung device uses Fowler-Nordheim tunneling for both programming and erase, both of which require 20 V obtained from the charge pump with 5 V applied externally.

We first look at the Intel device using a Verilog-A model for the memory cell with the parameters given in Table 2. Since we do not have construction analysis on this device, we must make educated guesses for many of the parameters based on information given in Reference [1].

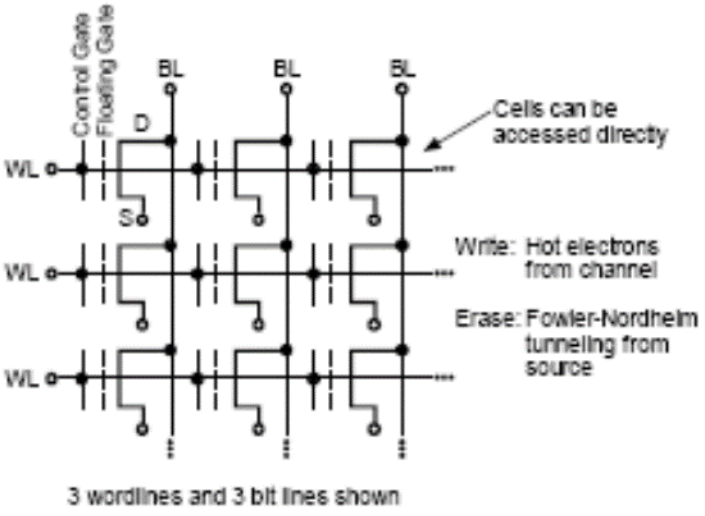

Figure 7. NOR architecture used in the Intel device.

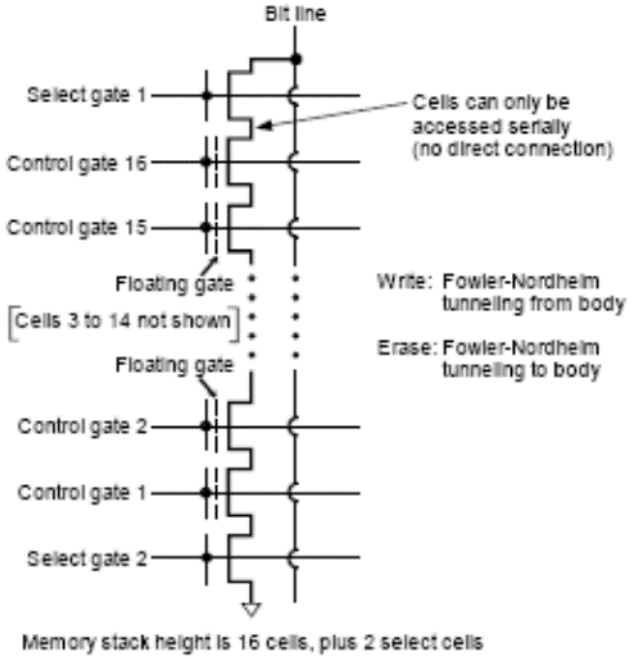

Figure 8. NAND architecture used in the Samsung device.

Table 2. Model Parameters for the Intel Cell Structure

UO = 526.4 VTO = 2.6 NFS = 3.776E+11 TOX = 8E-9 W=50u L=3u NSUB = 9.408E+15 VMAX = 1.156E+5 RSH = 2.812 RS = 25 RD = 7.762
IS = 1E-11 THETA = 0.01035 ETA = 1.121 KAPPA = 0.05993 XJ = 6E-7

Measured threshold voltages for the Intel device are given in Reference [1] and shown in Figure 9. Based on the figure, we assume a nominal threshold voltage of 2.6 V in the erased state and 5.6 V in the programmed state. With an oxide thickness of 8 nm for this device, we can estimate the capacitance of the floating gate as $C_{ox} = \varepsilon_{ox} / t_{ox} = 0.004316 \;\; F/m^2$. This means that with a threshold voltage in the programmed state of 5.6 V, the charge density on the FG will be $Q_{FG} = -0.0129$ with $V_{FG} = -3.0\,\text{V}$. These figures should be close to those obtained from a more detailed formulation of the model.

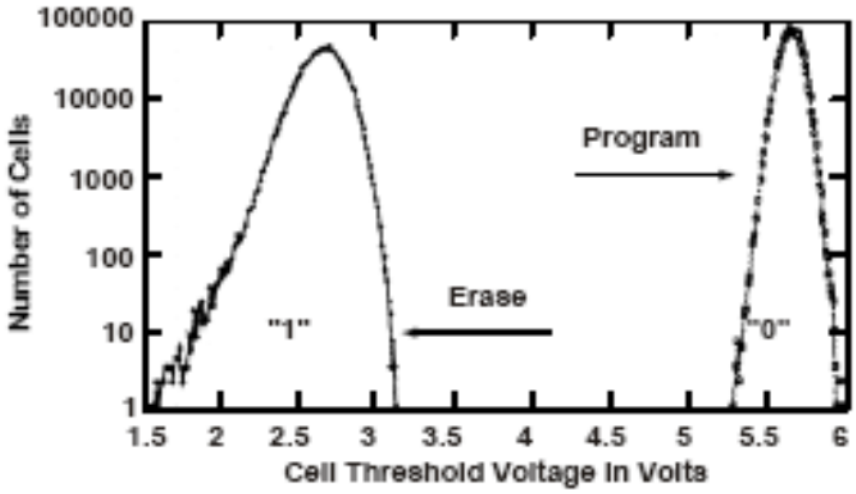

Figure 9. Threshold voltage distributions in the Intel device after programming and erase [1].

The Intel device is programmed by hot-electron injection from the channel. This process is described by the lucky-electron model which is developed in References [8] and [9]. A channel electron can reach the gate if, after gaining energy in the channel, it is scattered towards the Si/SiO_2 interface with enough energy to overcome the potential barrier there. After being redirected toward the interface, the hot electron must not lose energy through collisions before encountering the potential barrier. A lucky electron that has passed the barrier will be swept toward the floating gate by the oxide field.

The current into the FG from this process is given by,

$$I_{gate} = -0.5 I_{DS} (tox + tunox) \left(\frac{\lambda E_m}{\phi_b} \right)^2 \frac{P(E_{ox})}{\lambda_T} \exp\left(\frac{-\phi_b}{\lambda E_m} \right) \qquad 8$$

where E_m is the maximum channel field at the drain end, I_{DS} is the drain current, φ_b is the interface barrier potential, and $P(E_{ox})$ is the combined probability that the

electron does not suffer an energy–stripping collision in the silicon or the oxide before reaching the peak of the potential barrier. The redirection scattering mean free path is $\lambda_T = 6.16\times10^{-6}$ cm, and the hot-electron scattering mean free path is $\lambda = 1.05\times10^{-6}$ cm. The Si/SiO_2 interface potential in volts is given by,

$$\phi_b = 3.2 - 2.6\times10^{-4}\sqrt{E_{ox}} - 4\times10^{-5}E_{ox}^{2/3} \qquad 9$$

where,

$$E_{ox} = \frac{V_G - V_D - V_{fb}}{tox + tunox} \text{ V/cm} \qquad 10$$

The maximum electric field at the drain end of the channel can be expressed in terms of the drain voltage as,

$$E_m \cong \frac{V_D - V_{Dsat}}{L} \quad L = 0.22(tox + tunox)^{0.33} X_j^{0.5} \qquad 11$$

where the source/drain junction depth is $X_j = 3.25\times10^{-7}$ cm, and the voltage where the carriers reach saturation velocity V_{Dsat} is given by,

$$V_{Dsat} = \frac{|V_G - Vth|E_{sat}L_{eff}}{|V_G - Vth| + E_{sat}L_{eff}} \qquad 12$$

with $E_{sat} = 2\times10^4$ and $L_{eff} = 3\times10^{-4}$. All of the above is developed in more detail in References [8] and [9].

Fowler-Nordheim tunneling is described in Reference [10]. The current density into and out of the FG is given by,

$$I_{gate} = -\frac{q^2E_{ox}|E_{ox}|}{8\pi h\phi_b}\exp\left(\frac{-8\pi\sqrt{2m^*}(q\phi_b)^{3/2}}{3hq|E_{ox}|}\right) \qquad 13$$

In this expression

$$E_{ox} = (V_{GS} + Q_{fg}/C_{ox})(tox + tunox) \qquad 14$$

where initially $Q_{fg} = -0.0130$ as calculated from Equation (8) to give a threshold voltage of 5.6 V. E_{ox} varies during erase as $Q_{fg} \to 0$.

We have developed Verilog-A models for both the Intel and Samsung memory cells that contain the FG with the processes listed above for programming and erase. However, it is sometimes easier to work with a subsidiary calculation of these functions. A code that includes programming by hot-electron injection and erase by Fowler-Nordheim tunneling for the Intel device is listed in Appendix 2. This code calculates write and erase times close to those quoted in the literature. For the Intel device the calculated time to bring Vth up to 5.6 V in Figure 9 is 13.7 μsec with a quoted time of 8 μsec, and the calculated erase time is 27 μsec which is almost exactly the value quoted in Reference [1]. Times are not given for the Samsung device, but our calculated times are 12 msec for programming and 0.15 msec for erase.

4. RADIATION EFFECTS IN FLASH MEMORY

Figure 10 shows erase times as a function of radiation exposure in the Intel device reported in Reference [1]. Large differences are observed between individual memory cells, and the figure shows the best and worst cases. When 12 V is applied externally and the charge pump is not used, no effect of the radiation is apparent. This indicates that the charge pump is the component most sensitive to radiation damage. Evidently no effects of trapped charge occur in the memory cell itself.

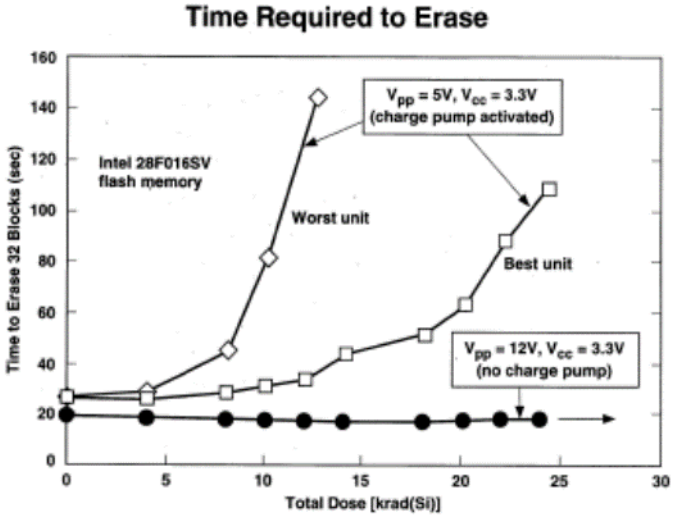

Figure 10. Measured erase times in the Intel device as a function of total dose [1].

Figure 11 shows a comparison of the measured values with the model described above: the trapped charge and threshold shifts in the charge pump from Equations (2) – (7) and the erase times derived from F-N currents in Equation (13). For the best case simulation we assumed a PMOS device in the charge pump with $N_D = 1.22 \times 10^{10}$,

$N_T = 1.26 \times 10^{13}$, $tox = 38.68$ nm and the cross sections mentioned earlier in connection with Figure 6. For the worst case, we used $N_D = 2.42 \times 10^{10}$ and $N_T = 2.53 \times 10^{13}$, with $tox = 38.68$ nm. In the memory cell, we used $tox = tunox = 8$ nm. We were unable to get nearly as good a match to the measured erase times by assuming the charge pump was NMOS. Without error bars on the measurements, it is not clear how well the model reproduces the data, but the calculated points are fairly close.

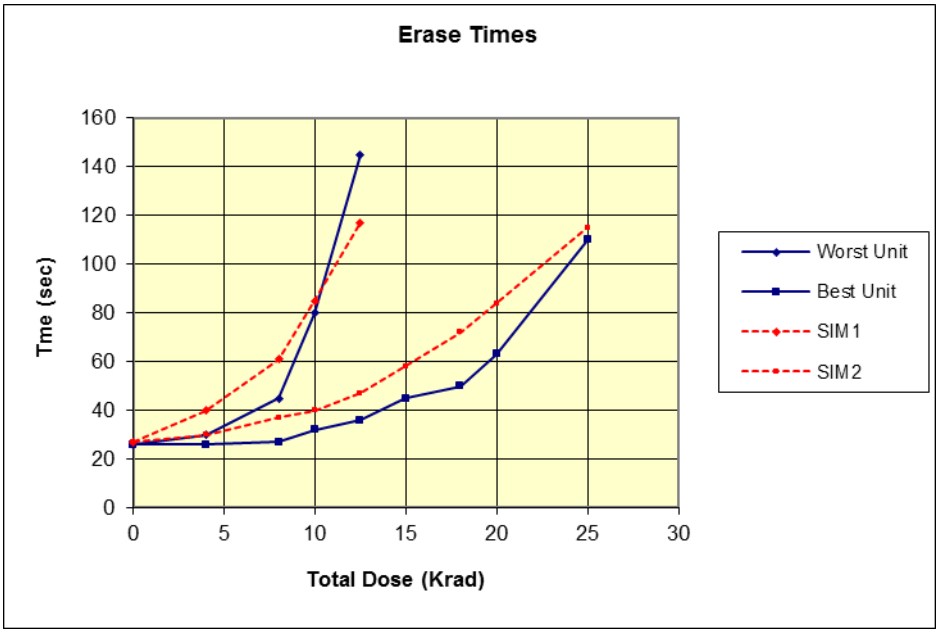

Figure 11. Model calculation of erase times compared with measurements.

5. STRUCTURE AND DESIGN OF THE FRAM CELL

In contrast to flash memory, the information in an FRAM cell is not stored in the form of charge carriers in a FG. The bits—logically 0 or 1—are contained in the reversible electric polarization of the ferroelectric material lead zirconate titanate, PZT (Pb (ZrTi)O3). A thin film of this material is placed between two electrodes to form a ferroelectric capacitor.

The ferroelectric material has a crystal structure with an atom at the center. This atom has two equal and stable low energy states which determine the position of the atom as shown in Figure 12. When an electric field is applied to the crystal the atom will move in the direction of the field. The polarization of the crystal layer can then be used to store information. Ferroelectric materials are switched only by electric fields and are not affected by magnetic fields. The FRAM has a higher resistance to radiation than the floating gate memory, since radiation has little or no effect on the crystal structure.

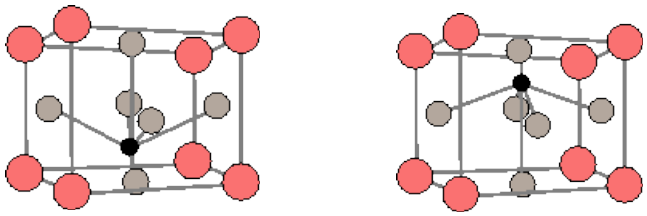

Figure 12. Ferroelectric crystals in down polarization and up polarization.

A 1T-1C memory cell is shown in Figure 13. To write a binary digit 0 (positive polarization state) to a cell, a positive voltage VDD is applied to the bitline while the plateline is grounded and the wordline is asserted. In writing a binary digit 1 (negative polarization state), a positive voltage VDD is applied to the plateline while the bitline is grounded and the wordline is asserted. Note that a negative voltage would be required on the bitline to produce the same voltage across the FE capacitor if the plateline were grounded. The equivalent circuit in the write operation is the FE capacitor in series with the access transistor ON resistance.

A cell can be read by floating the bitline and applying a positive voltage VDD to the plateline while asserting the wordline. If the initial polarization state of the capacitor is negative (positive), reading the cell develops a relatively large (small) signal on the bitline, typically around 250 mV. Since this operation is destructive, the data must be written back into the cell after a read. The equivalent circuit in the read operation is the FE capacitor in series with the bitline capacitance.

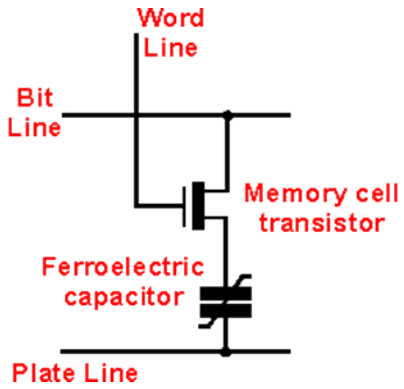

Figure 13. Basic ferroelectric memory cell.

6. RADIATION EFFECTS IN FRAM

Total dose radiation measurements were made on the Ramtron FM23MLD16 ferroelectric memory [11]. The measurements show total dose tolerance under biased irradiation to about 100 Krad with no significant changes to the parametric response. Under unbiased irradiation the part shows no parametric degradation up to 300 Krad. Sizeable parametric degradation was observed in the biased parts up to 300 Krad, although the stored information was not corrupted. However, the parts only remained

functional because the tester supplied the high input currents required by the device at the higher radiation levels. Functional failure could occur at a lower dose if the surrounding circuitry is unable to supply the higher currents required by a system in actual use.

Figure 14 shows the standby leakage current as a function of total dose for biased and unbiased irradiation. Also shown is return to normal parametric function after 16 weeks of room temperature anneal.

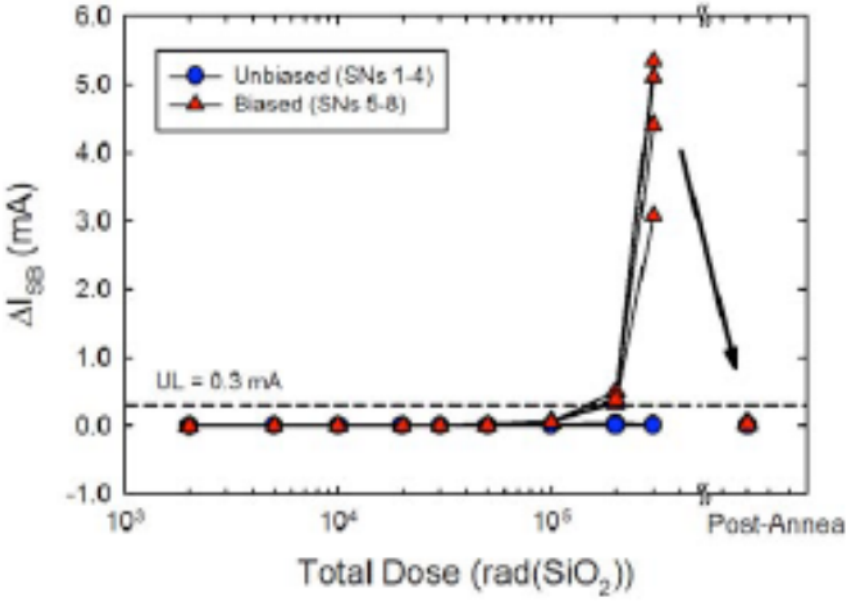

Figure 14. Change in standby leakage current in the FM23MLD16 FRAM as a function of total dose [11].

A model was developed earlier for the effect of radiation on subthreshold leakage current in MOSFETs [12]. Some of that work can be applied to the total dose degradation of the access transistor in each FRAM cell. In this model the radiation effects represented in Equations (2) – (7) are combined with a unified expression for drain current which is valid both above and below threshold. The model includes leakage currents from weak inversion in the channel and leakage from the reverse-biased P-N junction in the drain-substrate well.

In Reference [13] a basic MOSFET model is developed that provides a natural transition between below and above threshold regimes. The unified expression for drain current is,

$$I_D = \frac{g_{chi} V_{gte}}{1 + g_{chi} R_s + \sqrt{1 + 2 g_{chi} R_s + \left(V_{gte} / V_L\right)^2}} \qquad 15$$

In Equation (15), the intrinsic channel conductance is,

$$g_{chi} = \frac{W}{L}\mu_{eff}C_{ox}\eta\frac{kT}{q}\ln\left[1+\frac{1}{2}\exp\left(\frac{qV_{gt}}{\eta kT}\right)\right] \quad 16$$

and the combined gate voltage swing is,

$$V_{gte} = \frac{kT}{q}\left[1+\frac{qV_{gt}}{2kT}+\sqrt{\delta^2+\left(\frac{qV_{gt}}{2kT}-1\right)^2}\right] \quad 17$$

where R_s is the series resistance, $V_{gt} = (V_{gs} - V_t)\times dtype$, where dtype=1 for n-channel and dtype=-1 for p-channel, and

$$V_L = v_{\max}\frac{L}{\mu_{eff}} \quad 18$$

where $v_{\max} = 7\times10^6$ is the saturated carrier velocity. The two adjustable parameters in these expressions are η which adjusts the subthreshold slope and δ which determines the width of the transition region. A typical value for δ is 3, and when $\delta = 0$, $V_{gte} = V_{gt}$.

There are two effects that contribute to reverse bias leakage at the junction of the drain well implant; diffusion current and generation current. Consider first the diffusion current. In a reverse-biased junction, the applied voltage causes a gradual depletion of electrons in the neutral p-region just outside the depletion region boundary. The resulting concentration gradient leads to electron diffusion into the depletion region. This current together with the corresponding diffusion of holes out of the n-region constitutes the leakage current in a reverse-biased junction. The reverse current from diffusion in a diode is [14],

$$I_{diff} = qA\left[\frac{D_n}{L_n}\frac{n_i^2}{N_A}+\frac{D_p}{L_p}\frac{n_i^2}{N_D}\right]\left[\exp(qV_a/kT)-1\right] \quad 19$$

where D_n is the diffusion coefficient, and $L_n = \sqrt{D_n\tau_n}$ is the diffusion length for electrons in the p-region and D_p is the diffusion coefficient, and $L_p = \sqrt{D_p\tau_p}$ is the diffusion length for holes in the n-region. In these expressions τ is the recombination lifetime. In Equation (19), $V_a < 0$ for reverse bias, and the reverse current is $I_{diff} < 0$.

Now consider the generation current. When a junction is reverse biased, carrier concentrations in the depletion region are below their equilibrium values; this leads to thermal generation of electrons and holes. The field in the depletion region sweeps these carriers into the neutral regions thereby adding to the reverse current. From Reference [14] we find that the combined forward and reverse bias recombination-generation current is,

$$I_{rg} = qA\frac{n_i}{2\tau_g}W_{dep}\frac{\left[\exp(qV_a/kT)-1\right]}{\left(1+\frac{V_{bi}-V_a}{kT/q}\frac{\sqrt{\tau_n\tau_p}}{2\tau_g}\exp(qV_a/2kT)\right)} \quad 20$$

where W_{dep} is the width of the depletion region and the generation lifetime is given by,

$$\tau_g = \frac{1}{2}\left[\tau_p\exp\left(\frac{\phi_T-\phi_i}{kT/q}\right)+\tau_n\exp\left(\frac{\phi_i-\phi_T}{kT/q}\right)\right] \quad 21$$

In Equation (21) the carrier lifetimes are given by,

$$\tau_p = \frac{1}{\sigma_p v_{th} N_T} \text{ and } \tau_n = \frac{1}{\sigma_n v_{th} N_T} \quad 22$$

where the cross sections are, $\sigma \approx 1\times10^{-14}\,cm^2$, the thermal speed is, $v_{th} \approx 1\times10^{7}\,cm/\sec$, and the bulk trap concentration is $N_T \approx 1\times10^{14}\,cm^{-3}$. In Equation (21) we assume the energy of the traps is near the middle of the bandgap and $\varphi_T - \varphi_i \cong 0.20$ ev.

The combined reverse-bias leakage current is a combination of equations (19) and (20). Except for a very low reverse bias voltage the exponential terms can be neglected, in which case,

$$I_{leak} \cong -qA\left[\frac{D_n}{L_n}\frac{n_i^2}{N_A}+\frac{D_p}{L_p}\frac{n_i^2}{N_D}\right]-qA\frac{n_i}{2\tau_g}W_{dep} \quad 23$$

The drain current model represented by Equations (15) – (23) has been implemented in the code subt1.c which appears in Appendix 3. The equations for trapped charge are included in the code. If we assume the transistor is irradiated under bias of 3.3 V with the following values for density of trapping centers and hydrogen defects,

$N_{tr} = 3 \times 10^{11} cm^{-2}$ and $N_{hd} = 2 \times 10^{11} cm^{-2}$, the model gives an almost exact match to the measured leakage currents as shown in Figure 15.

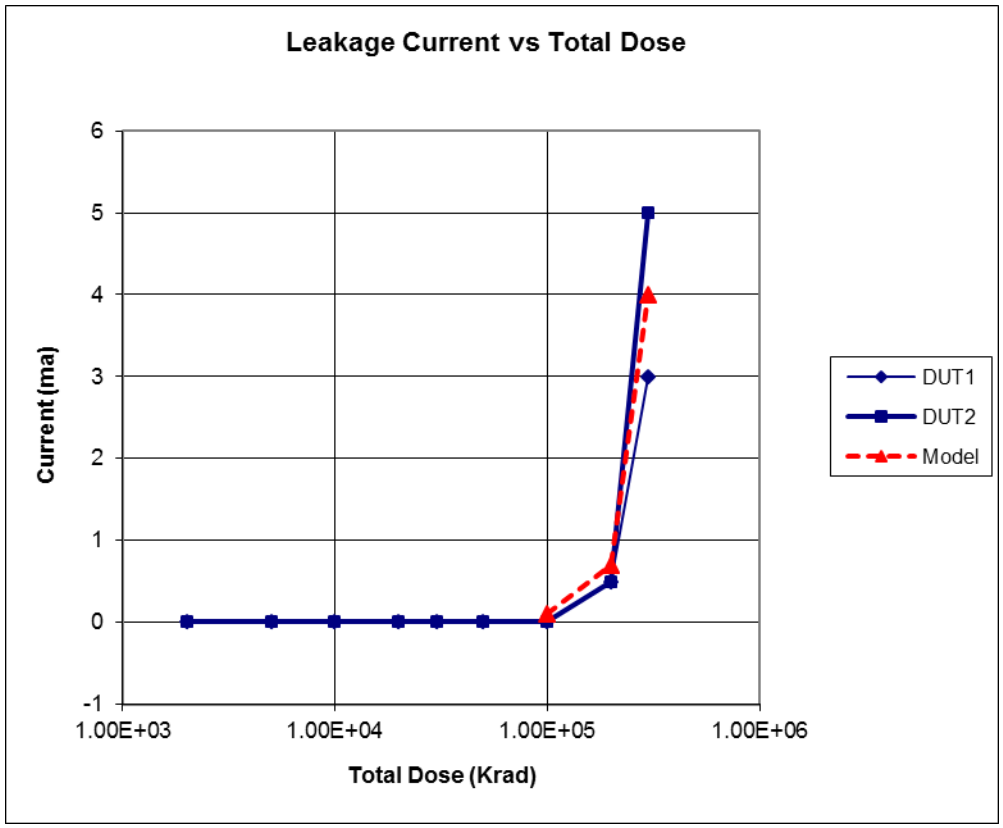

Figure 15. Model compared with measured leakage current in the FM23MLD16.

Measurements show that if the device is unbiased during irradiation, no effect is seen. Expressions for trapped charge in the unbiased case were derived in Reference [6] and given by,

$$\Delta N_{ot} = N_T[1 - \exp(-G_0 \sigma_T \delta D)], \tag{24}$$

$$\Delta N_{it} = N_D\left[1 - \exp\left(-G_0 \sigma_H \delta D\right)\right] \tag{25}$$

$$\delta = 0.5\sqrt{\frac{\varepsilon_{ox} kT}{q^2 G_0 D}} \tag{26}$$

When these expressions are applied to the irradiations in Figure 14 and Figure 15, the leakage current at D=300 Krad is a little over 0.1 ma. This is somewhat higher than shown in Figure 14, but still quite small.

7. SUMMARY AND CONCLUSIONS

This work looks at measurements of radiation effects in flash memory and ferroelectric RAM and develops models that reproduce the observed effects. Two flash memory devices are considered, one by Intel and one by Samsung. The FRAM device studied is the Ramtron FM23MLD16.

In flash memory, the internal high voltage generator, or charge pump, is most sensitive to radiation. Trapped charge from the radiation affects the threshold voltage which lowers the output from the charge pump. When the output falls far enough the device fails. The model compares favorably to measured erase times in the Intel device which increase with total dose. The Samsung device fails at about 10 Krad, and the Intel device fails between 25 Krad and 50 Krad.

In the FRAM, no parametric degradation is observed up to 100 Krad at which point a strong increase of leakage current is observed. This increase continues up to 300 Krad. Functional failure did not occur below 300 Krad, because the tester could supply the large currents drawn by the irradiated device. In actual use the support circuitry may not be able to supply the increased current requirement resulting from doses over 300 Krad. A model was developed for the device that reproduces the leakage current increase due to radiation exposure.

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APPENDIX 1: NETLIST FOR EIGHT-STAGE CHARGE PUMP IN THE INTEL DEVICE

```
Dickson Charge Pump Test Circuit - eight stages
* this is the Huang, Cheng, Liou test

*  Vout = 11.74
.param  dose = 2.5e4
.param  nint = 2.54e+10
.param  noxt = 1.13e+09

*  Vout = 12.01
*.param  dose = 0
*.param  nint = 0
*.param  noxt = 0

C2 2 16 20pf
C3 3 17 20pf
C4 4 16 20pf
C5 5 17 20pf
C6 6 16 20pf
C7 7 17 20pf
C8 8 16 20pf
C9 9 17 20pf
C10 10 0 10pf
R10 10 0 1.0meg

V1 1 0 5.0v
V16 16 0 PULSE(0 5.0 40n 1n 1n 40n 80n)
V17 17 0 PULSE(0 5.0  0n 1n 1n 40n 80n)

M1 1 1 2 0 SA3000N W=150u L=3u  dose={dose} nint={nint} noxt={noxt}
M2 2 2 3 0 SA3000N W=150u L=3u  dose={dose} nint={nint} noxt={noxt}
M3 3 3 4 0 SA3000N W=150u L=3u  dose={dose} nint={nint} noxt={noxt}
M4 4 4 5 0 SA3000N W=150u L=3u  dose={dose} nint={nint} noxt={noxt}
M5 5 5 6 0 SA3000N W=150u L=3u  dose={dose} nint={nint} noxt={noxt}
M6 6 6 7 0 SA3000N W=150u L=3u  dose={dose} nint={nint} noxt={noxt}
M7 7 7 8 0 SA3000N W=150u L=3u  dose={dose} nint={nint} noxt={noxt}
M8 8 8 9 0 SA3000N W=150u L=3u  dose={dose} nint={nint} noxt={noxt}
M9 9 9 10 0 SA3000N W=150u L=3u  dose={dose} nint={nint} noxt={noxt}

.MODEL SA3000N NMOS (  LEVEL=23  TNOM=27
+ UO = 526.4  VTO = 2.60 NFS = 3.776E+011   TOX = 3.868E-008
+ NSUB = 9.408E+015  VMAX = 1.156E+005  RSH = 2.812  RS = 2.5  RD = 2
+ IS = 1E-011 THETA = 0.01035 ETA = 1.121 KAPPA = 0.05993 XJ = 6E-007 )

*.TRAN 1ns 800ns
.TRAN 1ns 8us
.PRINT TRAN V(1) V(16) V(2) V(4) V(10)

.END
```

APPENDIX 2: CODE FOR CALCULATING INTEL PROGRAMMING AND ERASE

```
/*
 *  File name:   HEI4.c
 *  Program a flash cell (Intel NOR) with channel hot electron injection
 *  Erase with Fowler-Nordheim tunneling
 *  gcc -02 HEI4.c -o test1 -lm
 */

#include <stdio.h>
#include <math.h>

#define NSTEPS    100000
#define EPSOX 3.453133e-11    // F/m
#define EPSSI 1.03594e-10     // F/m
#define Qe 1.6021918e-19

main(int argc, char *argv[])
{
    int i, j, m;
    double TOX, TUNOX, FGarea, VTO, Vth, Vgs;
    double Nfg, Qfg0, Qfg, Ifn, Afn, Bfn, Cox;
    double Qmm1, Qm, Qmp1, Qbar, Im, Imp1, Qerror;
    double t, deltat, deltatold, tout, dtout, tend;
    double twrite, terase;
    double tox, tunox;

    double x, y, lambda, lambdaEm, LambdaT, Leff;
    double Vs, Vg, Vd, Vsat, Vfg, P1;
    double Isub, Ids, Ig, Esat, Em, Eox, Eox1, Eox2, Phib, L;
    double Ai=2.0e+6, Bi=1.7e+6, Xj=3.25e-7;

// Intel device (NOR)
    goto ERASE;

    PROGRAM:
    // hot electron injection, dist. in cm
    Vg = 12;
    Vd = 5;
    Ids = 0.35e-3;   // amps
    TOX = 8e-9;      // 8 nm
    TUNOX = 8e-9;    // 8 nm
    tox = 100*TOX;      // in cm
    tunox = 100*TUNOX;  // in cm
    Leff = 3e-4;     // 3 micron
    VTO = 2.6;
    FGarea = 0.5e-14;   // sq-m
    twrite = 15e-6;

    L = 0.22*pow((tox + tunox),0.33)*sqrt(Xj);
    LambdaT = 6.16e-6;    // 61.6 nm
    lambda = 2e-7;        // 2 nm
    Esat = 2e+4;
    x = fabs(Vg - VTO);
    Vsat = x*Esat*Leff/(x + Esat*Leff);
```

```
   y = (Vd - Vsat)/L;
   Em = sqrt(y*y + Esat*Esat);
   lambdaEm = lambda*Em;
   Isub = Ids*(Ai/Bi)*Em*L*exp(-Bi/Em);   // units of Ids
   Cox = EPSOX/(TOX);   // F/sq-m
   printf(" PROGRAM\n");
   printf(" Vg = %.1f, Vd = %.1f, Vsat =  %.3e, VTO = %.1f,
            Cox = %.3e\n", Vg,Vd,Vsat,VTO,Cox);
   printf(" Em = %.3e, lambdaEm = %.3e, L = %.3e, FGarea = %.3e\n",
           Em,lambdaEm,L,FGarea);
   printf(" Ids = %.3e, Isub = %.3e\n", Ids,Isub);
   printf("\n");

   Qm   = 0;
   Qmm1 = 0;
   tend = twrite;
//   dtout = 1e-6;
   dtout = 0.5e-6;
   deltat = 1e-7;
   deltatold = 1e-7;
   t = 0;
   tout = dtout;
   for(m=1; m<NSTEPS; m++)
   {
      // predictor
      Eox = (Vg + Qm/Cox - Vd)/(tox + tunox);   // Eox in V/cm.
      if(Eox > 0)
      {
        Phib = 3.2 - 2.6e-4*sqrt(Eox) - 4e-5*pow(Eox,0.667);
        P1 = 5.66e-6*Eox/(1+Eox/1.45e5);
        P1 *= 1/(1+(0.002/Leff)*exp(-Eox*(tox+tunox)/1.5));
        P1 += 0.025;
        P1 *= exp(-300/sqrt(Eox));
        y = lambdaEm/Phib;
      } else
      {
        Phib = 0;
        P1 = 0;
        y = 0;
      }
      Im = -0.5*Ids*(tox+tunox)*y*y*(P1/LambdaT)*exp(-Phib/lambdaEm);
      Qbar = Qmm1 + (deltat + deltatold)*Im/FGarea;  // in coul./sq-m

      // corrector
      Eox = (Vg + Qbar/Cox - Vd)/(tox + tunox);   // Eox in V/cm.
      if(Eox > 0)
      {
        Phib = 3.2 - 2.6e-4*sqrt(Eox) - 4e-5*pow(Eox,0.667);
        P1 = 5.66e-6*Eox/(1+Eox/1.45e5);
        P1 *= 1/(1+(0.002/Leff)*exp(-Eox*(tox+tunox)/1.5));
        P1 += 0.025;
        P1 *= exp(-300/sqrt(Eox));
        y = lambdaEm/Phib;
      } else
      {
        Phib = 0;
        P1 = 0;
```

```
      y = 0;
    }
    Imp1= -0.5*Ids*(tox+tunox)*y*y*(P1/LambdaT)*exp(-Phib/lambdaEm);
    Qmp1 = Qm + deltat*0.5*(Im + Imp1)/FGarea;     // in coul/sq-m

    Vfg = Qmp1/Cox;
    Vth = VTO - Vfg;
    if(Qmp1 != 0)  Qerror = fabs(Qbar - Qmp1)/Qmp1;
    else Qerror = 1;

    t += deltat;
    tout += deltat;
    if(tout >= dtout)
    {
       tout = 0;
       printf("t= %.3e, deltat = %.3e\n", t,deltat);
       printf("  Cox = %.3e, Eox = %.3e, Imp1 = %.3e\n",
                 Cox,Eox,Imp1);
       printf("  Qmp1 = %.3e, Vfg = %.3e, Vth = %.3e\n",
                 Qmp1,Vfg,Vth);
       printf("  Phib = %.3e, P1 = %.3e\n", Phib,P1);
    }
    if(t >= tend) break;

    // for the next time step
    deltatold = deltat;
    if(Qerror > 0.05) deltat *= 0.5;
    else if(Qerror < 0.001) deltat *=2.0;
    if(deltat > dtout) deltat = dtout;

    Qmm1 = Qm;
    Qm   = Qmp1;
}
printf("\n");

goto AFTER;

// erase with FN, dist. in m.
ERASE:

Vgs = -12;
VTO = 2.6;
TOX = 8e-9;
TUNOX = 8e-9;
terase = 32.0;
Cox = EPSOX/TOX;     // F/sq-m
Qfg0 = -1.29e-2;     // typical value per sq-m
Afn = 9.63e-7;       // A/(V*V)
Bfn = 2.77e+10;      // V/m

Qm   = Qfg0;
Qmm1 = Qfg0;
tend = terase;
dtout = 2.0;
deltat = 1e-6;
deltatold = 1e-6;
t = 0;
```

```
    tout = 0;
    Vth = VTO - Qm/Cox;
    printf(" ERASE\n");
    printf(" t = %.3e, Qm = %.3e, Vth = %.3e\n", t,Qm,Vth);
    for(m=1; m<NSTEPS; m++)
    {
       // predictor
       Eox1 = (Vgs + Qm/Cox)/(TOX + TUNOX);   // V/m
       Eox2 = fabs(Eox1);
       Im = -Afn*Eox1*Eox2*exp(-Bfn/Eox2);
       Qbar = Qmm1 + (deltat + deltatold)*Im;
       if(Qbar > 0) Qbar = 0;

       // corrector
       Eox1 = (Vgs + Qbar/Cox)/(TOX + TUNOX);
       Eox2 = fabs(Eox1);
       Imp1 = -Afn*Eox1*Eox2*exp(-Bfn/Eox2);
       Qmp1 = Qm + deltat*0.5*(Im + Imp1);
       if(Qmp1 > 0) Qmp1 = 0;

       Vfg = Qmp1/Cox;
       Vth = VTO - Vfg;

       if(Qmp1 != 0)  Qerror = fabs(Qbar - Qmp1)/Qmp1;
       else Qerror = 1;

       t += deltat;
       tout += deltat;
       if(tout >= dtout)
       {
          tout = 0;
          printf("t= %.3e, deltat = %.3e\n", t,deltat);
          printf("  Vgs = %.1f, Eox = %.3e, Imp1 = %.3e\n",
                    Vgs,Eox1,Imp1);
          printf("  Qmp1 = %.3e, Vfg = %.3e, Vth = %.3e\n",
                    Qmp1,Vfg,Vth);
       }
       if(t >= tend) break;

       // for the next time step
       deltatold = deltat;
       if(Qerror > 0.05) deltat *= 0.5;
       else if(Qerror < 0.001) deltat *=2.0;
       if(deltat > dtout) deltat = dtout;

       Qmm1 = Qm;
       Qm   = Qmp1;
    }

    AFTER:
    printf(" no erase \n");

}
```

APPENDIX 3: CODE FOR CALCULATING SUBTHRESHOLD LEAKAGE CURRENT IN THE FRAM

```
/*
 *   File name:  subt1.c
 *   Calculate subthreshold leakage current for FM23MLD16 FRAM
 *   gcc -O2 subt.c -o test4 -lm
 */

#include <stdio.h>
#include <math.h>

double QS(double Psis,double NA,double ND,double vtherm,double dtype);

//  EPSOX in F/cm
#define EPSOX 3.453133e-13
#define G0 8.1e+12
#define Qe 1.6021918e-19

main(int argc, char *argv[])
{
    int m, n, iter;
    double ratio, Wdep, Vbi, dtype, T, Vtherm, Efield;
    double ND, NA, Ni, beta, Psis, Vds, Vg, Vfb, Vt, Vi, tox;
    double phims, q=1.6e-19, epss=1.04e-12, epsox=3.45e-13;
    double A, W, L, mob, mob0, sign, Cox, Cs=0, k=1.380e-23;
    double Dose, Nit, Not, alpha=1.1e-11, pi=3.1415927;
    double F, dFdPsis, dQsdPsis, x, y, Qs, Qox, Psis0, PsiB;
    double Id, Igr, Idiff, Ileak, Ileak2, taug, taun, taup, Dn, Dp;
    double sigma, delx, NT, vt, phiT, phii;
    double eta, delta, gchi, Vgte, Rs, Vmax, Vl, Vgt;
    double Vgs, Eox, Y, delt1, sigma0, sigmaT, sigmaH, Nhd, Ntr;

    // for nmos dtype=1, for pmos dtype=-1
 //   dtype = 1;
    dtype = -1;
    if(dtype > 0)  // for n-channel
    {
      NA = 2.2e16;   // p substrate
      ND = 1.0e19;   // n+ drain implant
    } else
    {
      ND = 1.95e16;   // n substrate
      NA = 1.0e19;   // p+ drain implant
    }
    Ni = 1.0e10;
    W  = 7.9e-4;
    L  = 0.92e-4;
    A  = 3e-3;
    tox = 66e-7;
    Cox = epsox/tox;
    T = 300;
    Vtherm = k*T/q;  // 0.0259 @ 300 deg. K
    beta = 1/Vtherm;
```

```
    mob0 = 466;
    delta = 2;
    eta  = 2.6;
    Rs   = 0.2;
    Vmax = 7e+6;

    // total dose radiation effects
//    Dose = 0;
//     Dose = 10e+3;
//     Dose = 20e+3;
//     Dose = 50e+3;
//     Dose = 100e+3;
//     Dose = 200e+3;
     Dose = 300e+3;

    Vgs = 0;
 //   Vgs = 3.3;
    Eox = 1e-6*Vgs/tox;
    Y = 0.49*(1 + tanh(1.2*log10(Eox)));
    sigma0 = 3e-14;
    sigmaT = sigma0*pow(Eox,-0.55);
    sigmaH = 6e-14;
    if(dtype > 0)  // for n-channel
    {
      Nhd = 2.0e+10;
      Ntr = 5.5e+11;
    //  Ntr /= 2;  // for annealing
    }
    else  // for p-channel
    {
      Nhd = 2.0e+11;
      Ntr = 3.0e+11;
      // p-channel does not anneal
    }

    if(Vgs != 0)
    {
      Not = Ntr*(1 - exp(-G0*Dose*Y*sigmaT*tox));
      Nit = Nhd*(1 - exp(-G0*Dose*Y*sigmaH*tox));
    }
    else  // unbiased
    {
      delt1 = 0.5*sqrt(0.0258*EPSOX/(Qe*G0*Dose));
      Not = Ntr*(1 - exp(-G0*sigmaT*delt1*Dose));
      Nit = Nhd*(1 - exp(-G0*sigmaH*delt1*Dose));
    }
    mob = mob0/(1+alpha*Nit);

    if(dtype > 0)  // for n-channel
    {
      // metal-silicon work function difference
      phims = -0.40 -Vtherm*log(ND/Ni);
      // Bulk Fermi potential (p-doped)
      PsiB = Vtherm*log(NA/Ni);
      // trapped charge in the oxide
      Qox = (Not -Nit)*q;
    }
```

```
    else  // for p-channel
    {
      // metal-silicon work function difference
      phims = 0.465 +Vtherm*log(ND/Ni);
      // Bulk Fermi potential (n-doped)
      PsiB = -Vtherm*log(ND/Ni);
      // trapped charge in the oxide
      Qox = (0.2*Not +Nit)*q;
    }

    // for Psis=0, Vg=Vfb
    Psis = 0;
    Qs = 0;
    Vfb = phims -Qox/Cox;
    // for Psis=PsiB, Vg=Vi
    Psis = PsiB;
    Qs = QS(Psis, NA, ND, Vtherm, dtype);
    Vi = Vfb + Psis - Qs/Cox;
    // for Psis=2*PsiB, Vg=Vt
    Psis = 2*PsiB;
    Qs = QS(Psis, NA, ND, Vtherm, dtype);
    Vt = Vfb + Psis - Qs/Cox;

    if(dtype > 0)  // for n-channel
    {
//    Vg  = 3.3;
//    Vg  = 2.2;
//    Vg  = 1.0;
    Vg  = 0.5;
//    Vg  = 0.3;
//    Vg  = 0.0;
//    Vg  = -0.1;

    Vds = 2.2;
//    Vds = 0.05;
    }
    else  // for p-channel
    {
//    Vg  = -3.3;
//    Vg  = -2.2;
//    Vg  = -1.0;
    Vg  = -0.5;
//    Vg  = -0.3;
//    Vg  = 0.0;
//    Vg  = 0.1;

    Vds = -2.2;
//    Vds = -0.05;
    }

    Vbi = Vtherm*log(NA*ND/Ni/Ni);
    Wdep = sqrt(2*(epss/q)*(1/ND+1/NA)*(Vbi+dtype*Vds));
    Efield = sqrt(2*q*NA*ND*(dtype*Vds+Vbi)/(NA+ND)/epss);

    // given Vg calculate surface potential and leakage current
    Psis0 = PsiB;
    for(n=0; n<30; n++)
```

```
    {
     iter = n;
      sign = -Psis0/fabs(Psis0);
      if(dtype > 0)
      {
        x = sign*sqrt(2*epss*q*NA*Vtherm);
        y = exp(-beta*Psis0) +beta*Psis0 -1;
        Qs = x*sqrt(y);
        if(y !=0 ) dQsdPsis = 0.5*beta*Qs*(1 -exp(-beta*Psis0))/y;
        else dQsdPsis = 0;
      } else
      {
        x = sign*sqrt(2*epss*q*ND*Vtherm);
        y = exp(beta*Psis0) -beta*Psis0 -1;
        Qs = x*sqrt(y);
        if(y !=0 ) dQsdPsis = 0.5*beta*Qs*(exp(beta*Psis0) -1)/y;
        else dQsdPsis = 0;
      }
      F = Cox*(Vg -phims -Psis0) +Qox +Qs;
      dFdPsis = -Cox +dQsdPsis;
      Psis = Psis0 -F/dFdPsis;
//    printf(" Psis = %e, Pshis0 = %e\n", Psis,Psis0);
      if(fabs(Psis/Psis0-1) < 0.001) break;
      if(fabs(Qs) < 1e-12) break;
      Psis0 = Psis;
    }
//    Cs = -dQsdPsis*L*W;

    // combined drain current above and below threshold (Fjeldly)
    Vgt = (Vg -Vt)*dtype;
    Vl = Vmax*L/mob;
    gchi = (W/L)*mob*Cox*eta*Vtherm*log(1 +0.5*exp(beta*Vgt/eta));
    Vgte = Vtherm*(1 +0.5*beta*Vgt
         +sqrt( delta*delta +(0.5*beta*Vgt -1)*(0.5*beta*Vgt -1)) );
    Id = dtype*gchi*Vgte/(1 +gchi*Rs +sqrt(1 +2*gchi*Rs
+(Vgte/Vl)*(Vgte/Vl)));

    sigma = 1e-14;
    delx = 1e-6;  // width of surface traps
    // density of recombination centers including surface states
    NT   = 1e14 + Nit/delx;;
    vt   = 1e7;
    taup = 1/(sigma*vt*NT);
    taun = 1/(sigma*vt*NT);
    phiT = 1.20;
    phii = 1.0;
    taug = 0.5*(taup*exp(beta*(phiT-phii)) +taun*exp(beta*(phii-phiT)));
    Dn = 3;
    Dp = 7;

    // reverse bias diffusion current
    Idiff = q*A*(sqrt(Dp/taup)*Ni*Ni/ND +sqrt(Dn/taun)*Ni*Ni/NA)
             *(exp(-dtype*beta*Vds) -1);

    // reverse bias generation-recombination current
    Igr = q*A*Ni*(Wdep/(2*taug))*(exp(-dtype*beta*Vds) -1);
    Ileak = Ileak = Id +Igr +Idiff;
```

```
    Ileak2 = Ileak*8e+6;

    if(dtype > 0)  printf(" N channel\n");
    else  printf(" P channel\n");
    printf(" Dose = %e, Not = %e, Nit = %e\n", Dose,Not,Nit);
    printf(" ND = %e, NA = %e, tox = %e, Cox = %e\n", ND,NA,tox,Cox);
    printf(" phims = %e, PsiB = %e, Psis = %e\n", phims,PsiB,Psis);
    printf(" Vg = %e, Vfb = %e, Vi = %e, Vt = %e\n", Vg,Vfb,Vi,Vt);
    printf(" Cs = %e, Efield = %e, Wdep = %e, A = %e\n", Cs,Efield,Wdep,A);
    printf(" NT = %e, taup = %e, taug = %e\n", NT,taup,taug);
    printf(" Id = %e, Idiff = %e, Igr = %e\n", Id,Idiff,Igr);
    printf(" T = %e, Vg = %e, Ileak = %.2e, Ileak2 = %.2e\n",
T,Vg,Ileak,Ileak2);

}

// calculate induced charge in the oxide given surface potential
double QS(double Psis,double NA,double ND,double Vtherm,double dtype)
{
   double x, y, sign, beta, Qs;
   double q=1.6e-19, epss=1.04e-12;

   beta = 1/Vtherm;
   sign = -Psis/fabs(Psis);
   if(dtype > 0)
   {
     x = sign*sqrt(2*epss*q*NA*Vtherm);
     y = exp(-beta*Psis) +beta*Psis -1;
   } else
   {
     x = sign*sqrt(2*epss*q*ND*Vtherm);
     y = exp(beta*Psis) -beta*Psis -1;
   }
   Qs = x*sqrt(y);
   return Qs;
}
```

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