Microsystems
Science, Technology & Components
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Overview of ITRS Emerging Research Memory Devices

IEEE Rebooting Computing Symposium 4

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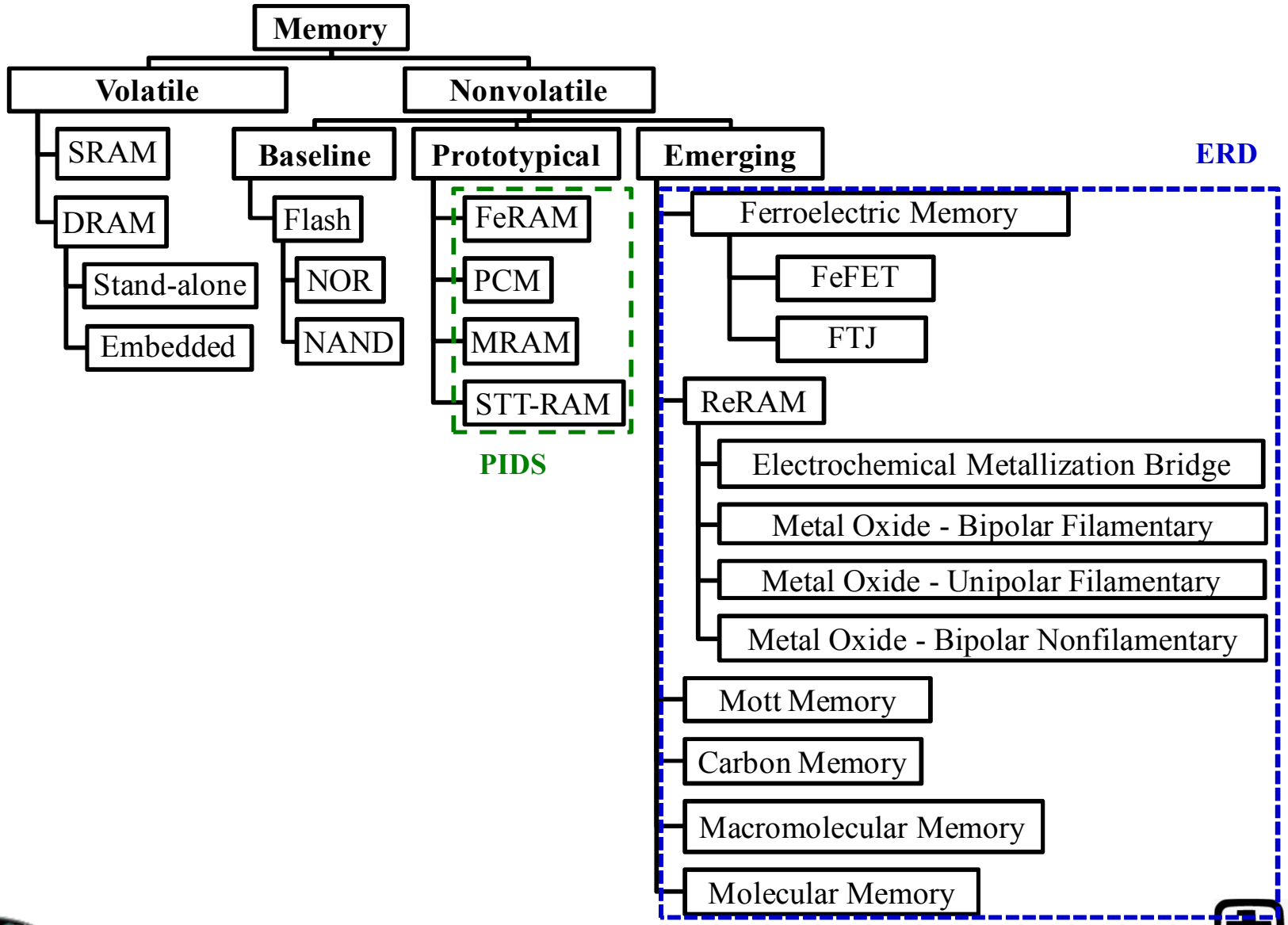
ITRS

Sandia National Laboratories

Introduction to ERD Memory

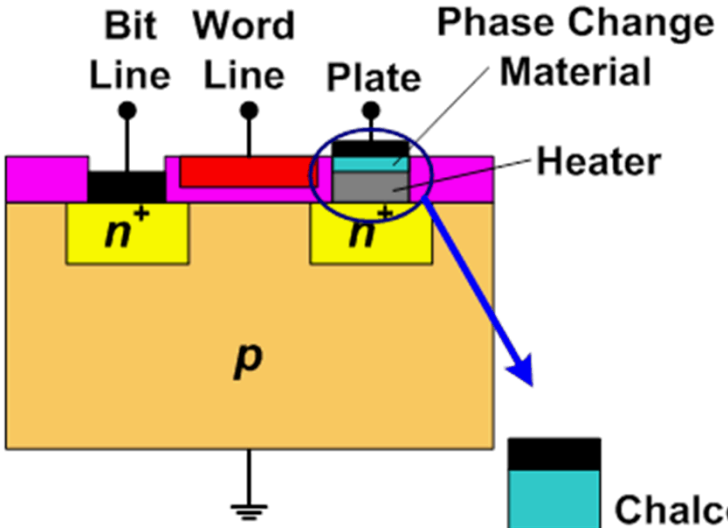
- Purpose:
  - Survey the most relevant emerging memory devices
  - Compile relevant information from the literature on device parameters, strengths, and weaknesses
- Period:
  - Every two years full update; currently finishing 2015 update
  - Workshops in off-years to collect data for next version
- Audience:
  - Foundries and Fabless Semiconductor Companies
  - Researchers from Academic Community
  - Government and Corporate Laboratories
- Target Applications:
  - Storage Class Memory: latency gap between DRAM and hard-disk drives (or NAND)
  - ITRS 2.0: Application drivers, i.e. Internet of Things

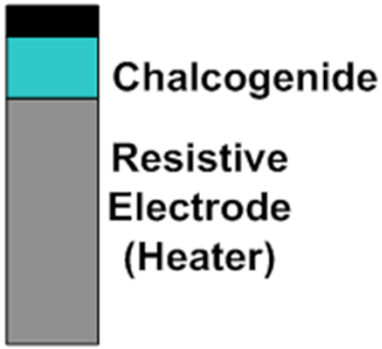
2013 ERD Memory Entries

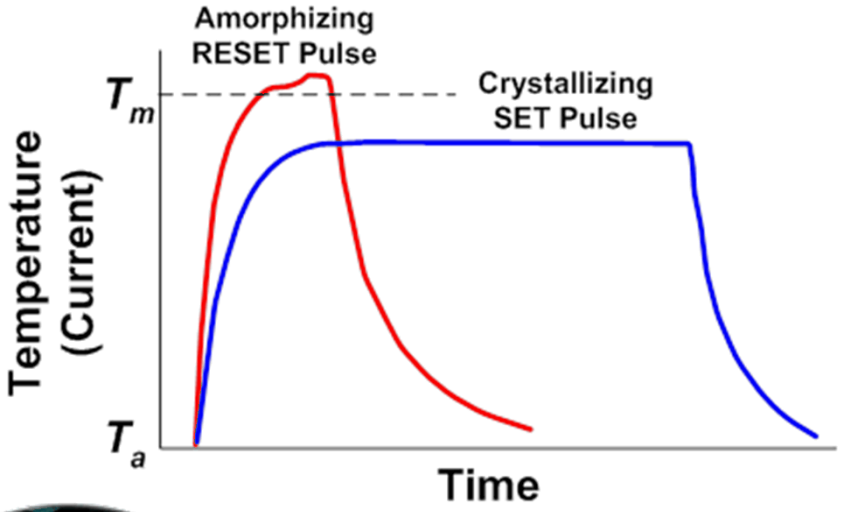


Phase Change RAM

- Type of Resistive RAM
- GST most common material
- In commercial production
  - Samsung, Micron
- Set – crystallize, long pulse
- Reset – amorphize, short high current pulse

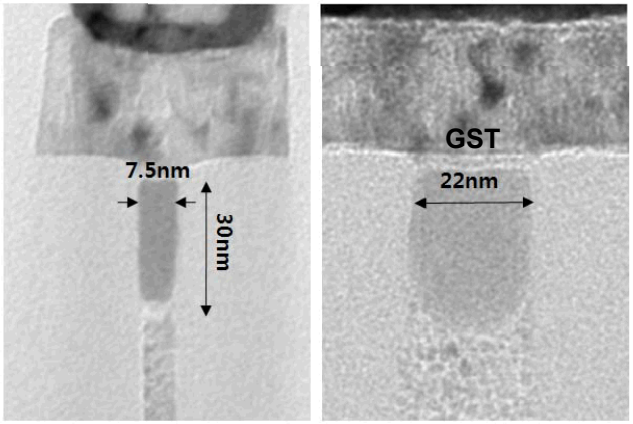






PCRAM Cell Schematic and Plot
Courtesy D.K. Schroder, ASU

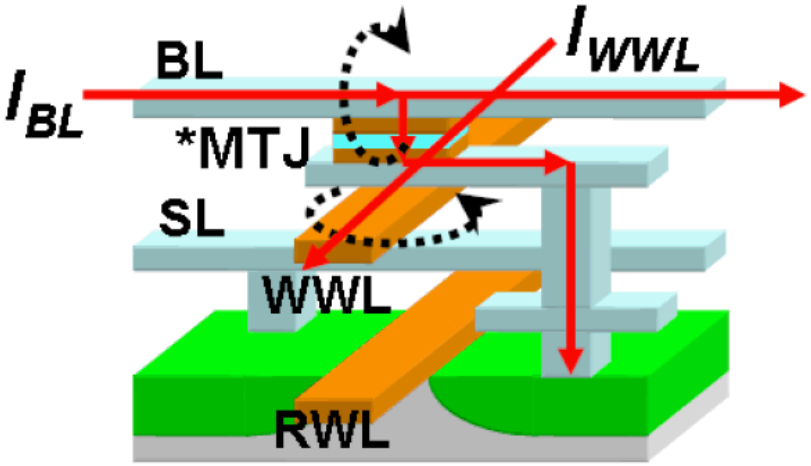
Samsung 20 nm PCRAM Cell



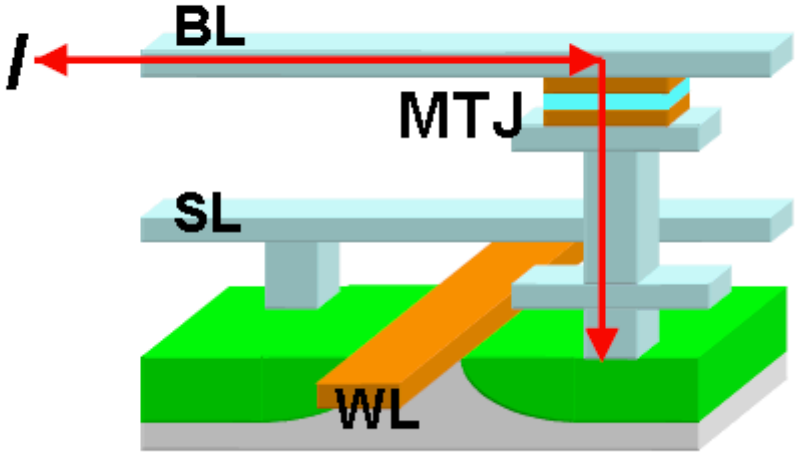
Kang et al, IEDM 2011

Prototypical Magnetic Memories

Conventional MRAM

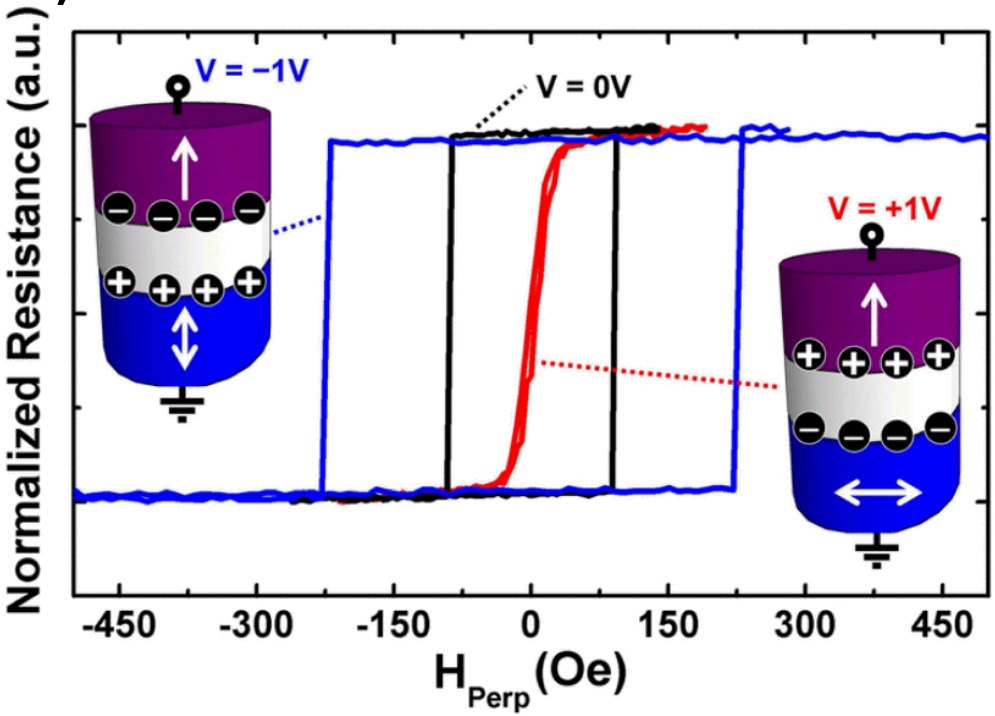


STT-RAM



Emerging Magnetic Memory

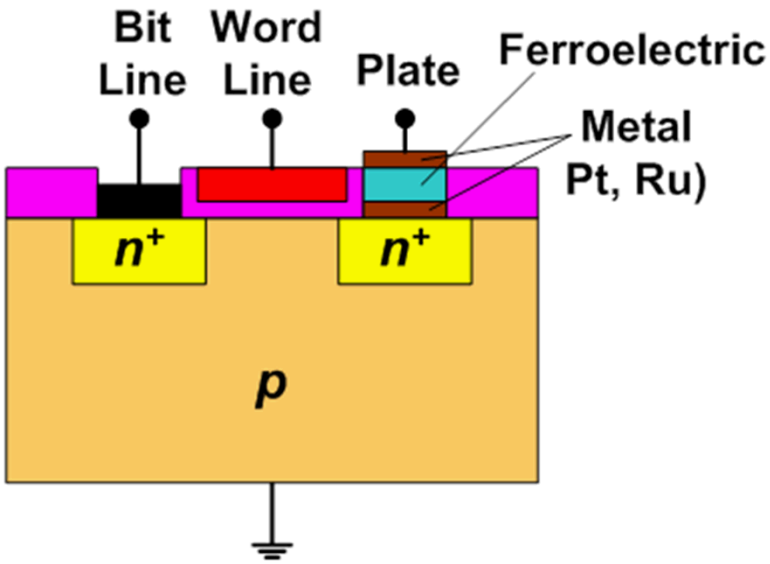
- **Magnetoelectric RAM (Me-RAM): Voltage controlled magnetic anisotropy (VCMO) effect in magnetic tunnel junction in very thin ferromagnetic film**
  - **May enable high speed, low energy switching (40 fJ/switch)**



Amiri et al (UCLA), IEEE Trans Mag 2015

Ferroelectric RAM

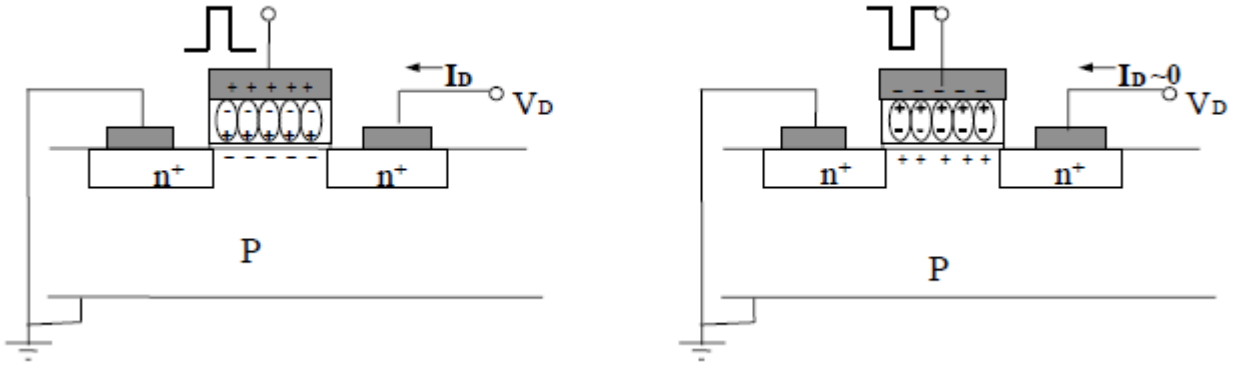
- Similar to DRAM cell
- Uses ferroelectric film capacitor
- State is stored as the polarization of the FE film
- Nearly unlimited endurance
- Moderate retention
- Process very finicky
- Commercial devices:
  - TI
  - RAMTRON (now Cypress)
  - Fujitsu



Courtesy D.K. Schroder

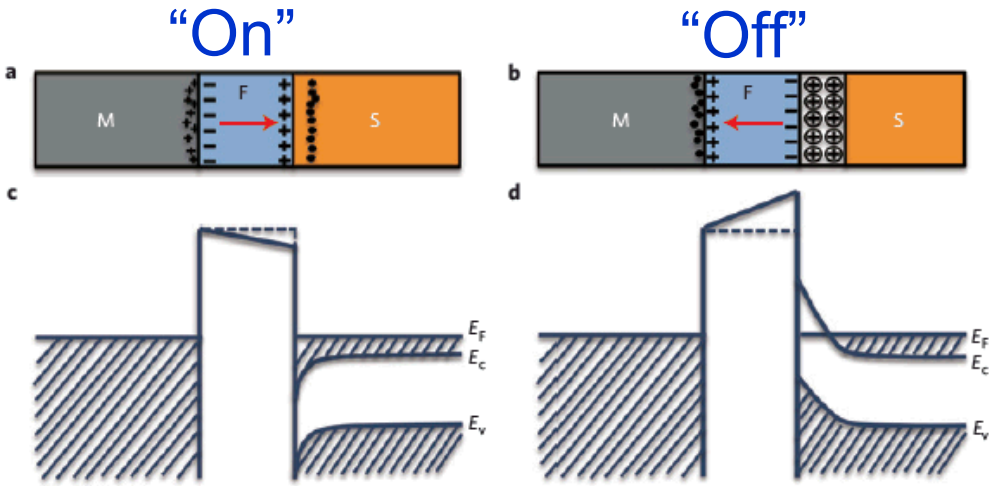
Emerging Ferroelectric Memories

Ferroelectric FET



TP Ma, ERD Memory Workshop 2014

Ferroelectric Tunnel Junction



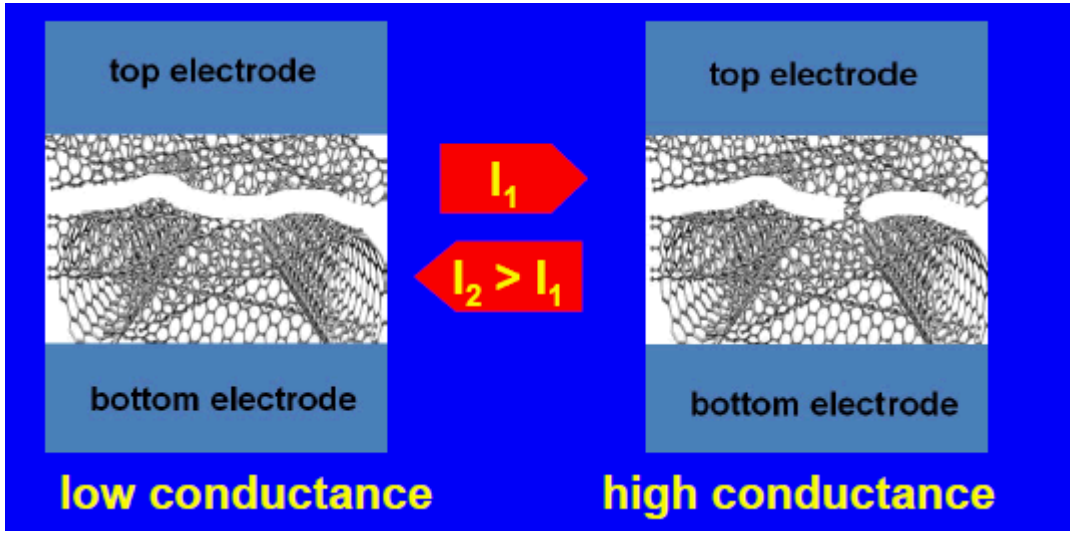
Wen et al, Nature 2013

Carbon Memory

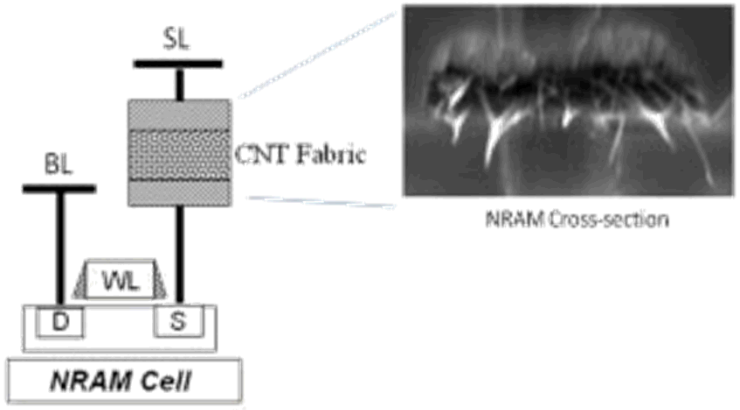
Three material systems

1. **Nanotube (single nanotube and layers)**
2. **Graphene**
3. **Amorphous carbon based resistive memory**

Many possible mechanisms!

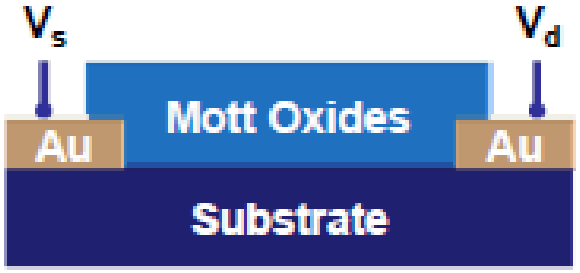


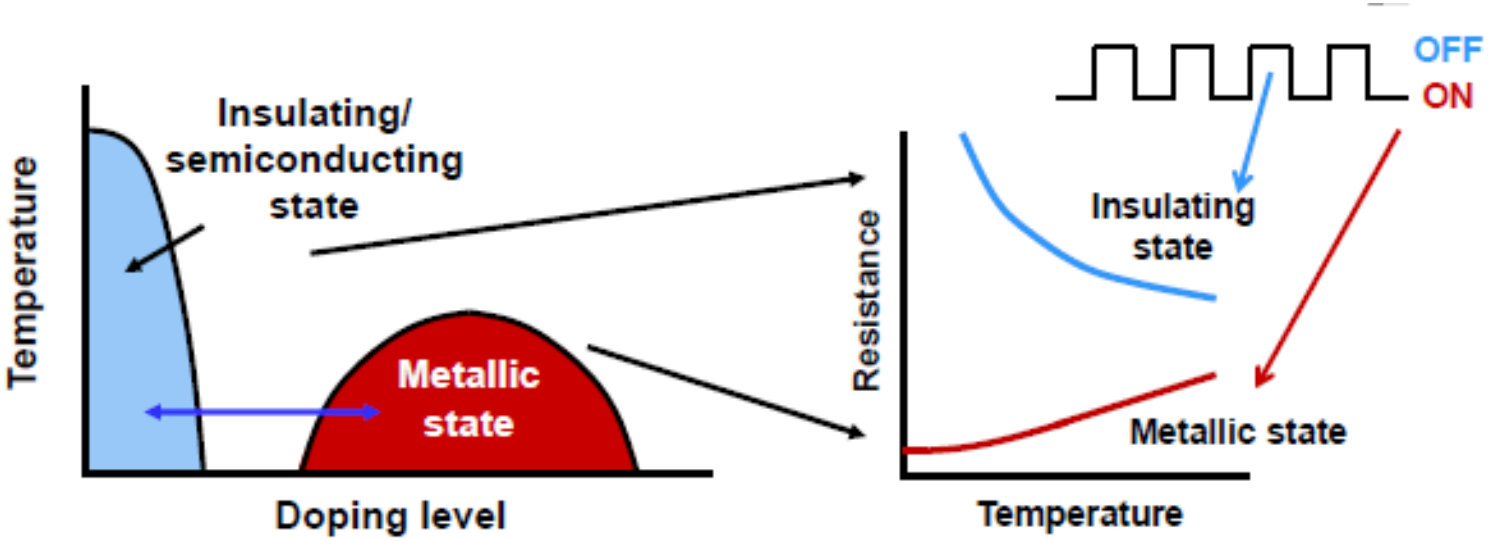
Kreupl, ERD Memory Workshop, 2014



nantero.com

Mott Memory


V_s
V_d
Mott Oxides
Au
Au
Substrate

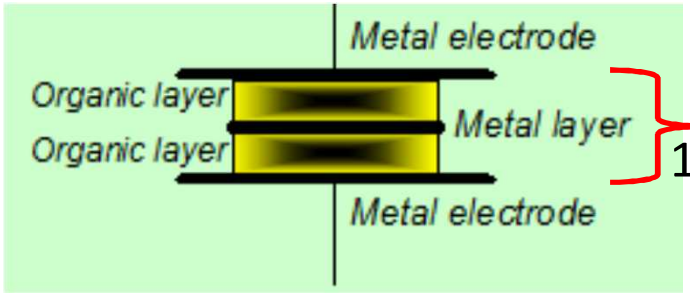

Insulating/
semiconducting
state
Temperature
Metallic
state
Doping level
Resistance
OFF
ON
Insulating
state
Metallic state
Temperature

Macromolecular vs. Molecular Memory

Macromolecular (also polymer or organic)

L. P. Ma, J. Liu, and Y. Yang
"Organic electrical bistable devices and rewritable memory cells"
APPLIED PHYSICS LETTERS VOLUME 80, NUMBER 16 22 APRIL 2002

J. OUYANG, C.-W. CHU, C. R. SZMANDA, L. P. MA and Y. YANG,
Programmable polymer thin film and non-volatile memory device,
NATURE MATERIALS, Nov. 2004



10-100nm

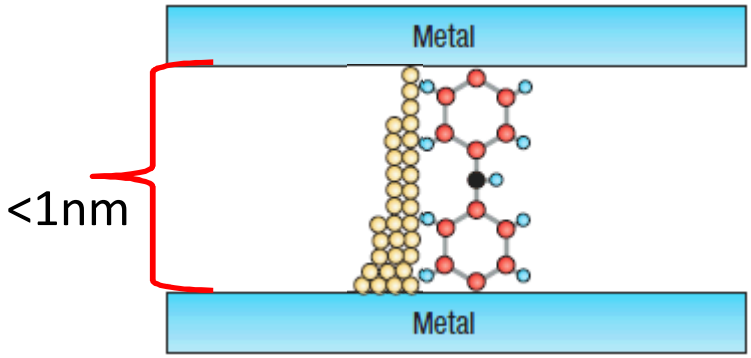
Thicker (many ML organic layer)

Emphasis: low-cost and special applications (flexible etc.)

Molecular

Read et al. "Molecular random access memory cell", APL 2001

Heath et al."A 160-kilobit molecular electronic memory", Nature 2007



<1nm

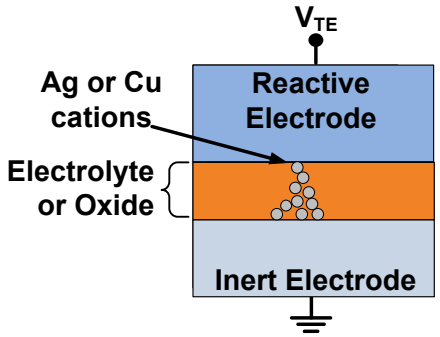
Thin (1 ML organic layer)

Emphasis: Ultimate Scaling

2013 ERD Memory Table (Part A)

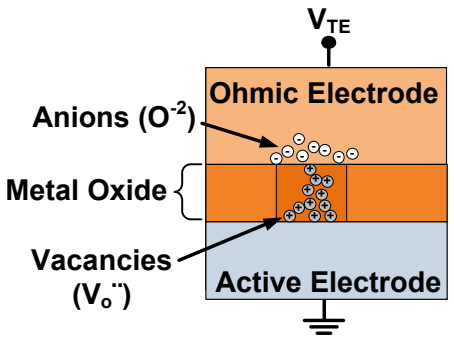
		A. Emerging Ferroelectric Memory		B. Carbon Memory	C. Mott Memory	D. Macromolecular Memory	E. Molecular Memory
Subclass		**FeFET**	**FE Tunnel Junction**	NA	NA	NA	NA
Feature size F	Best projected	Same as CMOS transistor	<10 nm	< 5 nm	5-10 nm	5 nm	5 nm
	Demonstrated	28nm	50 nm	22 nm	110nm	100 nm	30 nm
Cell Area	Best projected	$4F^2$	$4F^2$	$4F^2$	$4F^2$	$4F^2$	$4F^2$
	Demonstrated	$4F^2$	not available	not available	not available	$4F^2$	not available
Write/Erase time	Best projected	< 100pS	<1 ns	not available	<1 ns	< 10 ns	<40 ns
	Demonstrated	20ns 10 ns	10 ns	10 ns	2 ns	15 ns	10s , 0.2s
Retention Time	Best projected	10 yr	>10 y	not available	not available	> year	not available
	Demonstrated	$2.5x10^5$s (3 days)	3 days	168 h @ 250°C	not available	10^5 s	2 months
Write Cycles	Best projected	$>10^{12}$	10^{14}	not available	$>10^{16}$	not available	$>10^{16}$
	Demonstrated	10^{12}	$4x10^6$	$5x10^7$	~100	10^5	$2x10^3$
Write operating voltage (V)	Best projected	not available	1 V	not available	not available	~ 1	80 mV
	Demonstrated	+/- 5	2-3 V	5-6V	1.25/0.75	1.4	4V, ~±1.5 V
Read operating voltage (V)	Best projected	not available	0.1 V	not available	not available	< 0.1	0.3V
	Demonstrated	0.5V	0.1 V	1.5V	0.2	0.2	0.5V , 0.5V
Write energy per bit	Best projected	0.1 fJ	1 fJ	not available	not available	0.1 fJ	0.1 aJ
	Demonstrated	1 fJ	10 fJ	not available	~1 fJ	10 fJ	not available
Research activity		30	27	52	31	80	21

Electrochemical Metallization Bridge



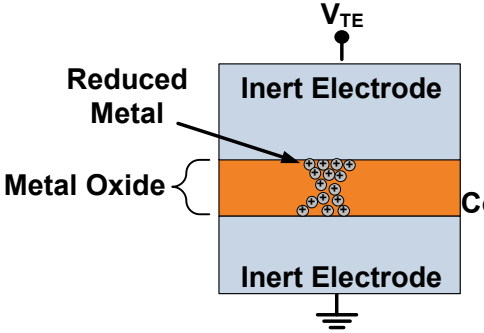
- Switching: Electrochemical formation and dissolution of Ag or Cu filament
- Cation motion (Ag or Cu)
- Chalcogenide or oxide insulating layer
- Switching depends on E-field direction
- R/W current independent of device area

Metal Oxide: Bipolar Filamentary



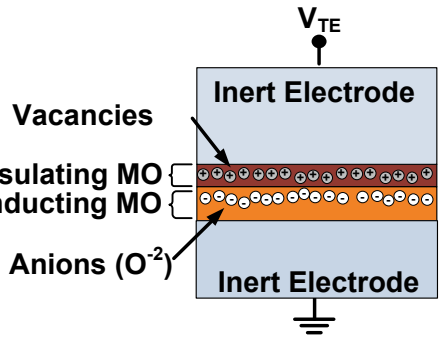
- Switching: Valence change and migration of oxygen vacancies
- Anion motion (O^{2-})
- HfO_x, TaO_x most common insulators
- Switching depends on E-field direction
- R/W current independent of device area

Metal Oxide: Unipolar Filamentary



- Switching: Thermochemical change in oxide valence state
- Anion motion (O^{2-})
- Symmetric structure
- NiO_x most common material
- Switching independent of E-field direction
- R/W current independent of device area

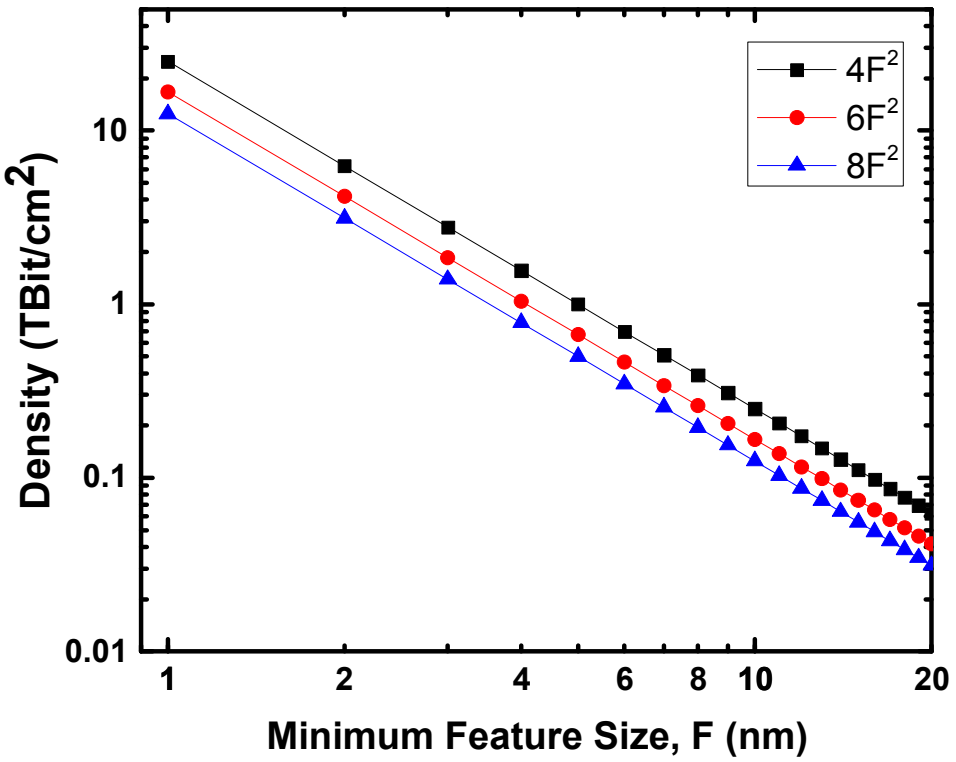
Metal Oxide: Bipolar Non-Filamentary



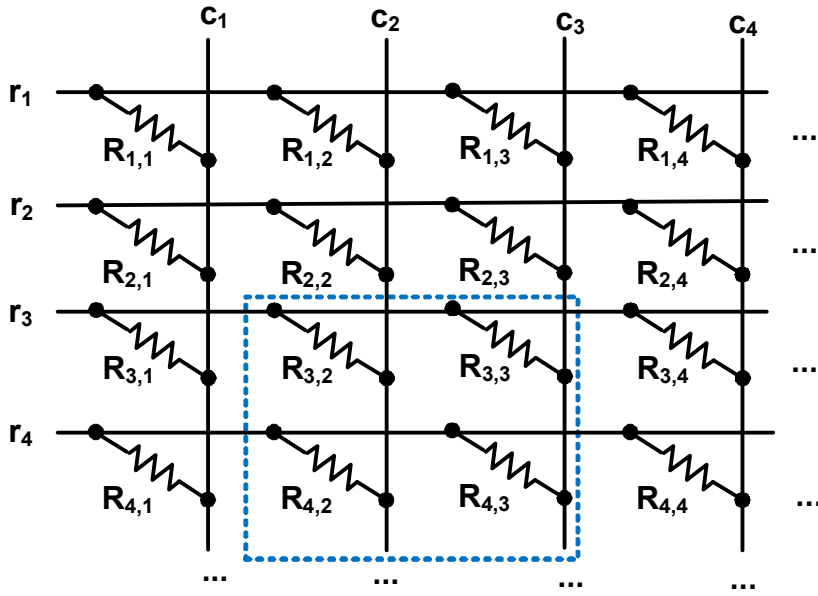
- Switching: Oxygen exchange causes Schottky barrier height change at interface
- Anion motion (O^{2-})
- Perovskite and insulating metal oxide
- Switching depends on E-field direction
- R/W currents depend on device area

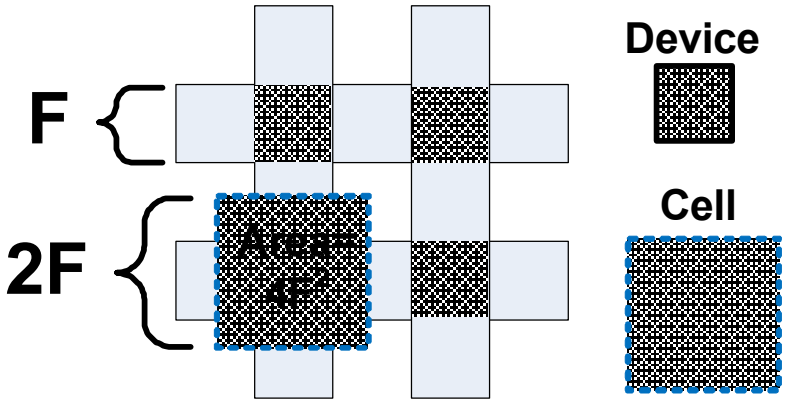
Resistive Crossbar Memories

- F=Feature size
- Max areal density possible → $4F^2$



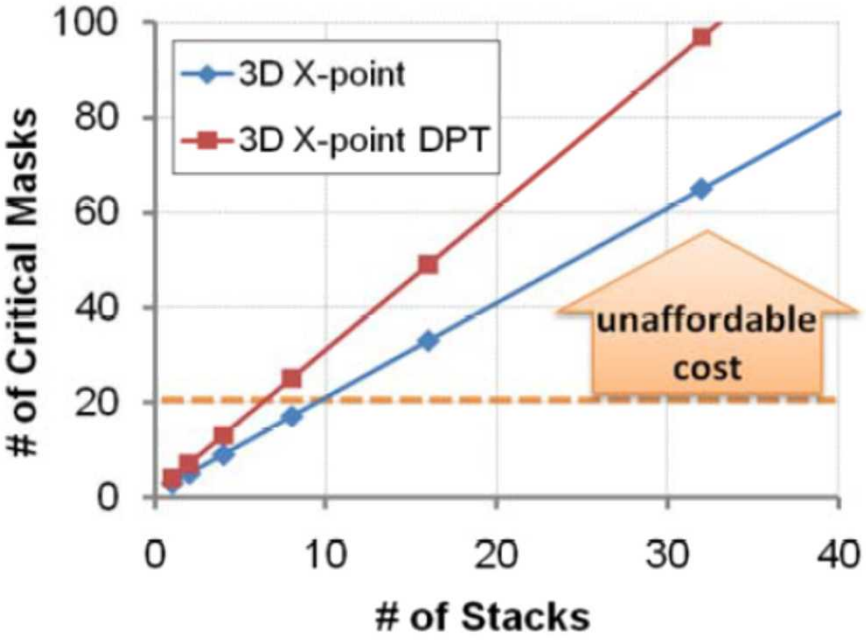
Marinella and Zhrinov, in Emerging Nanoelectronic Technologies, Wiley, 2014.





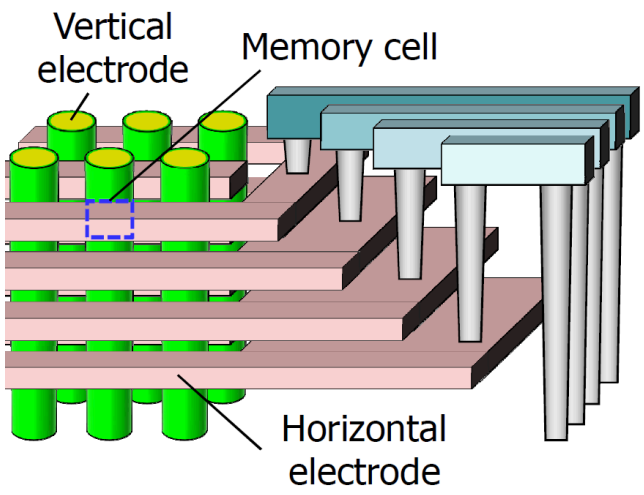
Problem with Stacking Horizontal Crosspoint Arrays

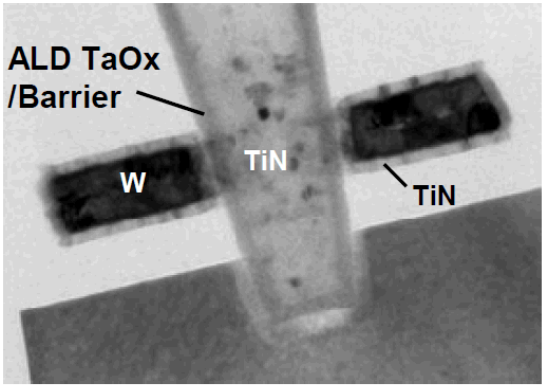
- Horizontal crosspoint stacking not cost effective past ~8 layers
  - Double patterning for HP less than ~40 nm
- No scaling path: doubling number of layers may double critical masks (and cost!)
- Need another method to continue layering…



IG Baek et al (Samsung), IEDM 2011

Samsung Vertical ReRAM Process





(a) Mold (SiO_2/Si_3N_4) Depo.

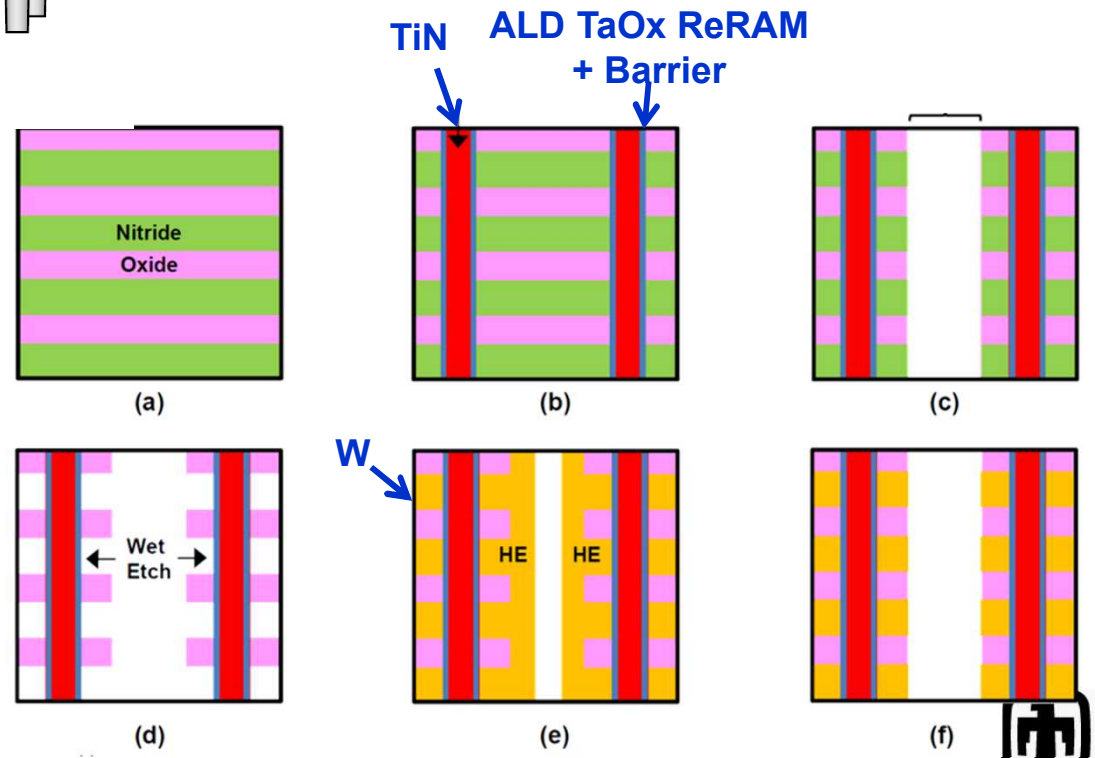
(b) Hole D/E and TMO/VE Depo.

(c) HE Cut Dry Etch

(d) Wet chemical Etch of Nitride

(e) HE Depo.

(f) Metal Node Separation

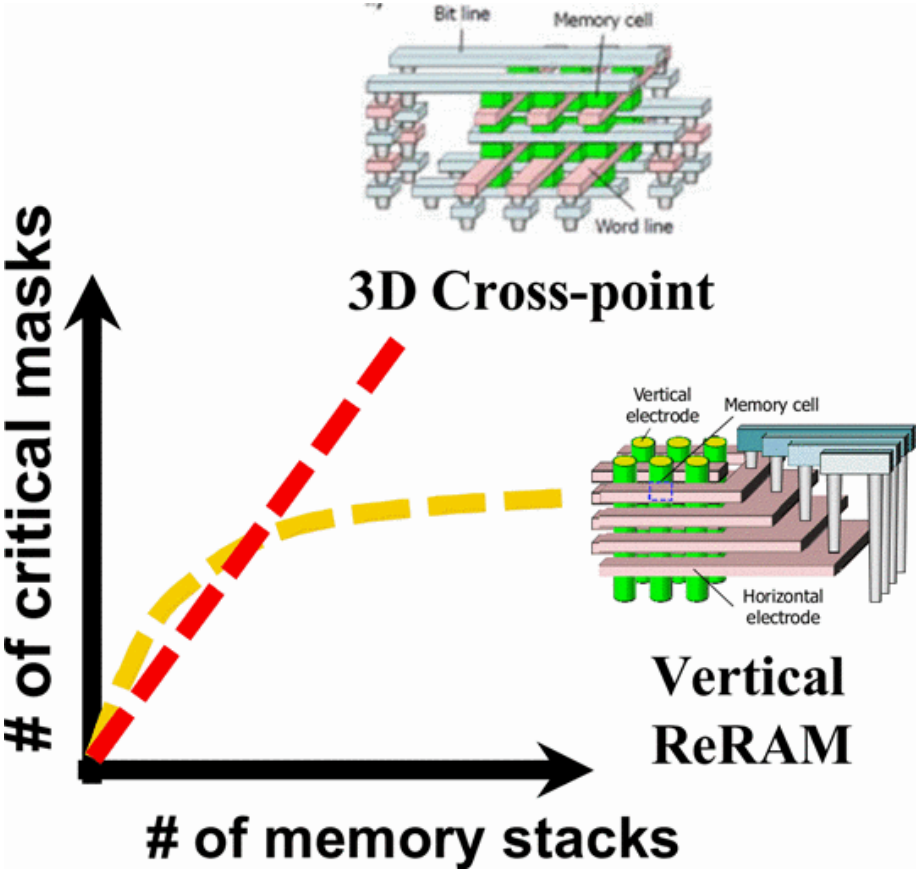


Does this process look Familiar?

IG Baek et al (Samsung), IEDM 2011

VRRAM Enables >8 Layer Stack

- Critical masks now do not scale with number of layers
- Without VRRAM, >~8 layers is cost prohibitive



SG Park et al (Samsung), IEDM 2012

2013 ERD Memory Table (Part B – ReRAM)

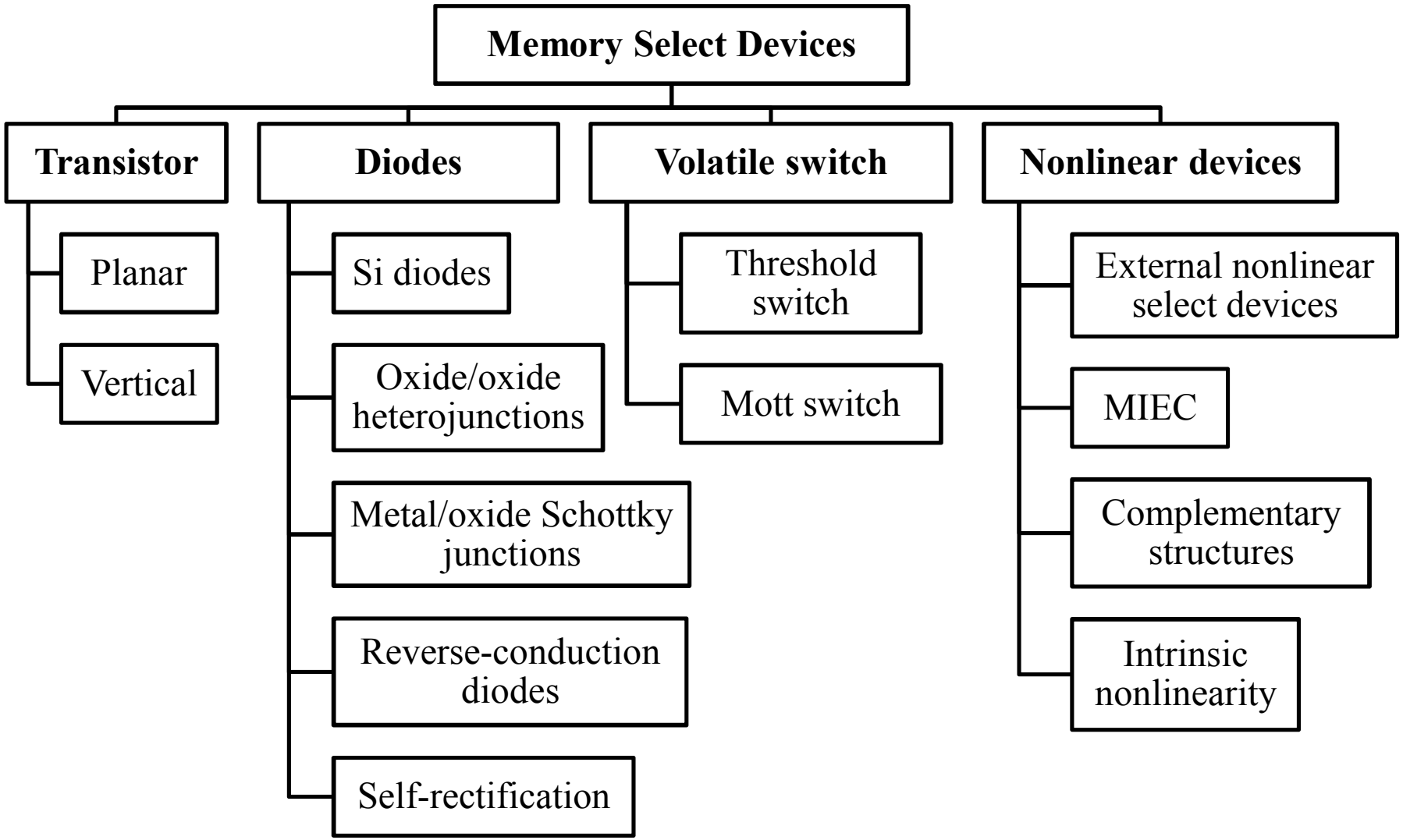
		A. Electrochemical Metallization Bridge	B. Metal Oxide: Bipolar Filamentary	C. Metal Oxide: Unipolar Filamentary	D. Metal Oxide: Bipolar Non-filamentary
Storage Mechanism		Electrochemical filament formation	Valence change filament formation	Thermochemical effect filament formation	Change in tunneling characteristics near interface
Feature size F	Best projected	<5nm	<5nm	not available	<10nm
	Demonstrated	20 nm (GeSe) 30 nm (CuS)	5 nm (AlOx)	35 nm	40 nm
Cell Area (2D)	Best projected	$4F^2$	$4F^2$	$4F^2$	$4F^2$
	Demonstrated	$4F^2$	$4F^2$	$4F^2$	$4F^2$
Write/Erase time	Best projected	<1ns	<1 ns	not available	10 ns
	Demonstrated	< 1ns	< 1ns	10 ns (W), 5 ns (E)	<100 ns
Retention Time	Best projected	>10yr	> 10yr	>10yr	>10 yr
	Demonstrated	1000hr 200°C	3000 hr @ 150°C	1000hr @ 150°C	4hr @ 125°C
Write Cycles	Best projected	$> 10^{11}$	$>10^{12}$	not available	$> 10^6$
	Demonstrated	10^{10}	10^{12}	10^6	10^6
Write operating voltage (V)	Best projected	<0.5V	<1V	not available	not available
	Demonstrated	0.6V	1-3V	1-3V	2V
Read operating voltage (V)	Best projected	<0.2V	0.1 V	not available	0.1 V
	Demonstrated	0.2V	0.1-0.2V	0.4 V	0.5V
Write/Erase energy (J/bit)	Best projected	not available	0.1 fJ	not available	not available
	Demonstrated	1 pJ (W), 8 pJ (E)	115fJ (W), < 1 pJ (E)	not available	1 pJ
Research activity	593 (includes all categories)				

2013 ITRS ERD Memory Survey

	Overall	Scalability	Speed	Energy Efficiency	ON/OFF "1"/"0" Ratio	Operational Reliability	Room Temperature Operation	CMOS Technological Compatibility	CMOS Architectural Compatibility
ReRAM	18.7	2.9	2.5	2.1	2.2	1.6	2.5	2.4	2.4
FeFET	17.4	2.0	2.4	2.3	2.1	1.7	2.4	2.3	2.4
FTJ	17.3	2.3	2.2	2.2	2.1	1.7	2.4	2.1	2.2
Carbon-based	17.0	2.2	2.2	2.0	2.3	1.7	2.4	2.0	2.2
Mott	16.6	2.1	2.4	2.1	2.2	1.7	1.9	2.0	2.2
Macromolecular	13.9	1.8	1.7	1.7	1.6	1.3	2.2	1.7	1.8
Molecular	13.9	2.6	1.7	2.0	1.3	1.1	2.0	1.6	1.8

www.itrs.net

Select Device



Application Space

	Embedded NVM Replacement[1]	NAND Flash Replacement (e.g. SSD)[2]	S-Type Storage Class Memory[3]	M-Type Storage Class Memory[3]	Stand-Alone DRAM (DIMM) Replacement[4]	CMOS Integrated DRAM/Storage/Main Memory[5]
Time to Implementation	**Now**	**5 years**	**5 years**	**5-10 years**	**5-10 years**	**> 10 years**
Quantitative Requirements						
Min Bit Level Endurance	10^3-10^6	10^3	10^6	10^9	10^{16}	10^{16}
Min Bit Level Retention	10 y	6-12 months	10 y	5 days	64 ms	10 y
Max System Level Read/Write Latency	100 µs	100 µs	5 µs	200 ns	100 ns	10 ns
Max System Level Write Energy	10^4 pJ	100 pJ	25 pJ	100 pJ	100 pJ	1 pJ
Max Feature Size	180 nm	12 nm	20 nm	20 nm	20 nm	10 nm
Min 2D Layer Density	10^9 bit/cm	10^{11} bit/cm	10^{10} bit/cm	10^{10} bit/cm	10^9 bit/cm	10^{11} bit/cm
Max Cost	30 $/GB[6]	2 $/GB	4 $/GB	10 $/GB	10 $/GB	10 $/GB
Qualatative Requirements						
Performance	Low	Low	Moderate	High	High	High
Reliability	High	Low/Moderate	Moderate	Moderate	Moderate	High
CMOS Compatibility	Required	Useful/Not Req	Useful/Not Req	Useful/Not Req	Useful/Not Req	Required
BEOL Process	Required	Not Required	Not Required	Not Required	Not Required	Required
Layering Capability	Not Required	Required	Required	Useful/Not Req	Required	Required

1: Based on common embedded microcontrollers with flash based program/data memory

2: Based on modern NAND flash characteristics, considering a stand-alone module.

3: Based on SCM info from 2013 ITRS ERD Tables

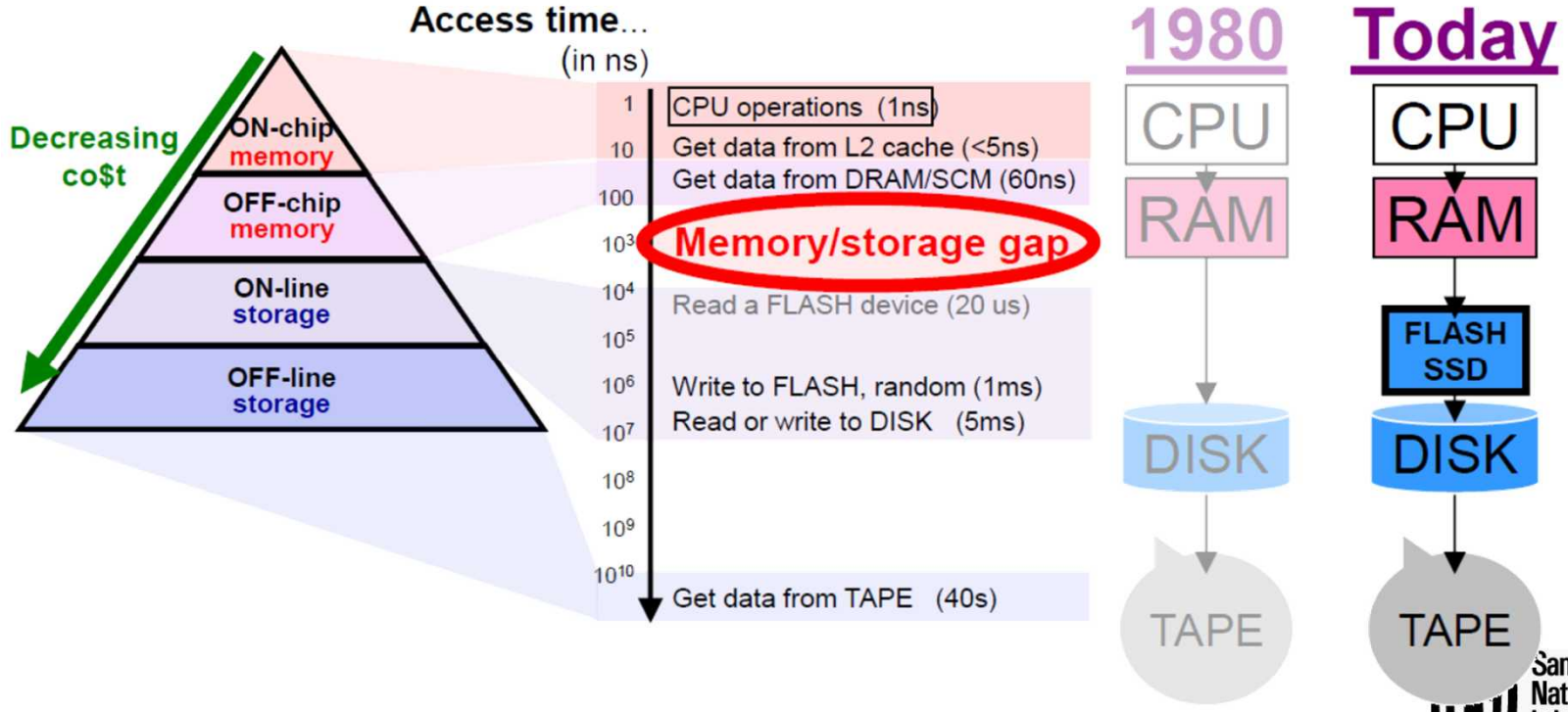
4: Based on modern DRAM characteristics.

5: High performance logic CMOS integration based on estimated requirements for data-center level processor (e.g. a "nanostore" [6]). This could also be thought of as a "univeral memory" which does not require tradeoffs in performance or reliability.

6: Based on the cost of a standalone external microcontroller memory; information on the cost per bit of flash integrated in a microcontroller is not available.

Storage Class Memory

- Major target application for emerging memory technologies
- Addresses major latency discrepancy between memory and storage DRAM to HDD (or flash)
- Workshop in 2012 to address suitability of ERD devices to SCM



Target Device/System Specs for SCM (ERD8)

Parameter	*Benchmark* [A]			*Target*	
	HDD [B]	**NAND flash** [B]	**DRAM**	**Memory-type SCM**	**Storage-type SCM**
Read/Write latency	3-10 ms	~100µs (block erase ~1 ms)	<100 ns	<200 ns	1-5µs
Endurance **(cycles)**	unlimited	10^3-10^5	unlimited	$>10^9$	$>10^6$
Retention	>10 years	~10 years	64 ms	>5 days	~10 years
ON power **(W/GB)**	0.003-0.05	~0.01-0.04	0.4	<0.4	<0.10
Standby power	~52%-69% of ON power[C]	<10% ON power	~25% ON power	<5% ON power	<5% ON power
Areal density	~ 10^{11} bit/cm^2	~ 10^{11} bit/cm^2	~ 10^9 bit/cm^2	$>10^{10}$ bit/cm^2	$>10^{10}$ bit/cm^2
Cost **($/GB)**	~0.1-1.0 [D]	2	10	<10	<3-4

Assessment for Storage Class Memory

	Prototypical (Table ERD3)			*Emerging (Table ERD5)*					
					Redox RRAM				Others
Parameter	FeRAM	STT-MRAM	PCRAM	Emerging ferroelectric memory	Conducting bridge	Metal Oxide: Bipolar Filament	Metal Oxide: Unipolar Filament	Metal Oxide: Bipolar Interface Effects	Carbon-based Memory, Mott Memory, Macro-molecular Memory, Molecular Memory
Scalability	☹	😐	🙂	😐	🙂	🙂	🙂	🙂	?
MLC	☹	☹	🙂	☹	🙂	😐	😐	😐	?
3D integration	☹	😐	🙂	☹	😐	🙂	🙂	🙂	?
Fabrication cost	😐	😐	😐	😐	😐	🙂	😐	😐	?
Retention	😐	😐	😐	😐	😐	🙂	😐	☹	?
Latency	🙂	🙂	😐	🙂	😐	😐	😐	😐	?
Power	🙂	😐	☹	🙂	🙂	😐	☹	😐	?
Endurance	🙂	🙂	😐	😐	😐	😐	☹	😐	?
Variability	🙂	☹	😐	😐	😐	☹	☹	🙂	?

Summary

- Significant ongoing research in emerging memory technologies
- ERD held several successful workshops on emerging memory, logic, and architectures in 2014-2015
- ERD Memory Workshop in August 2014; some results:
- Most promising: (has remained constant for many years)
  - PCRAM
  - STT-MRAM
  - Oxide ReRAM
- "In need of resources" gave new results:
  - Oxide ReRAM (also most promising)
  - Emerging Ferrorelectric Memories
  - Carbon Memories
- Does memory need the equivalent of Nikonov and Young?
- Will be sending out ERD 2015 chapter for review soon!

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Questions?

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Key Updates to 2013

- Updated all tables with current values from the literature
- Split ReRAM into four individual categories
  - Electrochemical Metallization
  - Metal-oxide Bipolar Filamentary
  - Metal-oxide Unipolar Filamentary
  - Metal-oxide Bipolar Nonfilamentary
- Split Ferroelectric Memory into two categories
- Removed nanoelectrical-mechanical systems (NEMS) based memory due to lack of research progress
- Added carbon memory
- Added write-energy