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Thermal Management via Carbon Nanotubes for Power Electronics

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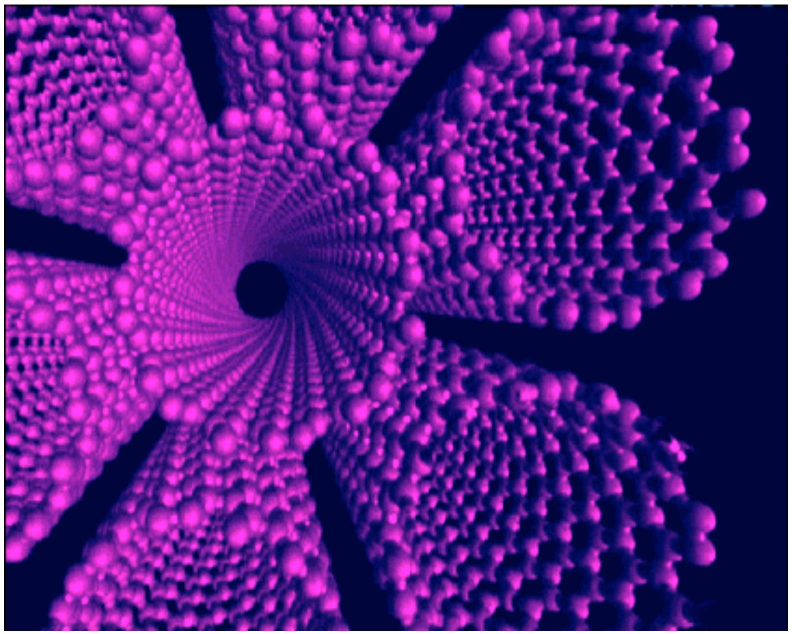

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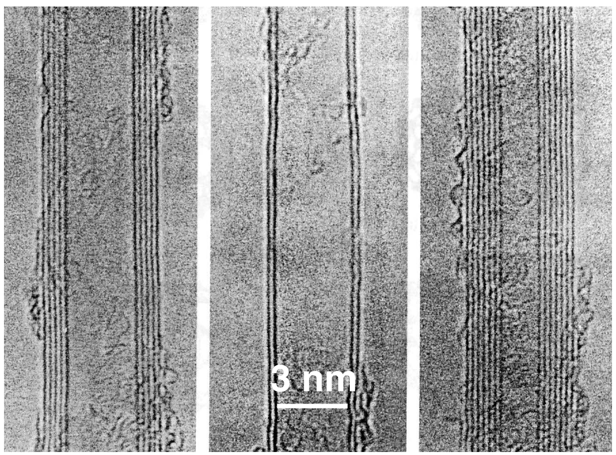
Outline

1. Introduction on carbon nanotubes
2. Introduction for thermal interface materials
3. CNT requirements for TIMs
4. CNT array fabrication methods
    - Thermal CVD growth of CNT arrays
    - Nanopore template formation on substrate-of-choice
    - EC deposition of Co catalyst nanowires
5. Critical issues for optimizing thermal properties of a CNT array
    - Crystalline quality of individual CNTs
    - Optimizing density of CNTs in array
    - Planarizing CNT array tips for optimal contact density
6. Summary

Helical Microtubules of Graphitic Carbon

Sumio Iijima, NEC Corporation
Nature, Dec. 7, 1991

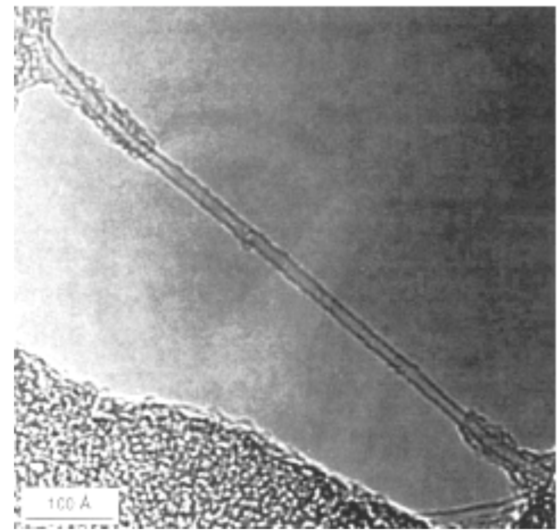
5 layers	2 layers	7 layers
6.7 nm	5.5 nm	6.5 nm



- produced using arc discharge, similar to fullerene synthesis.
- coaxial tubes of graphitic sheets, ranging from 2 to 50.
- helical pitch varies from tube-to-tube
- lengths up to 1 micron

Bethune et al, IBM Almaden
Nature, June 17, 1993

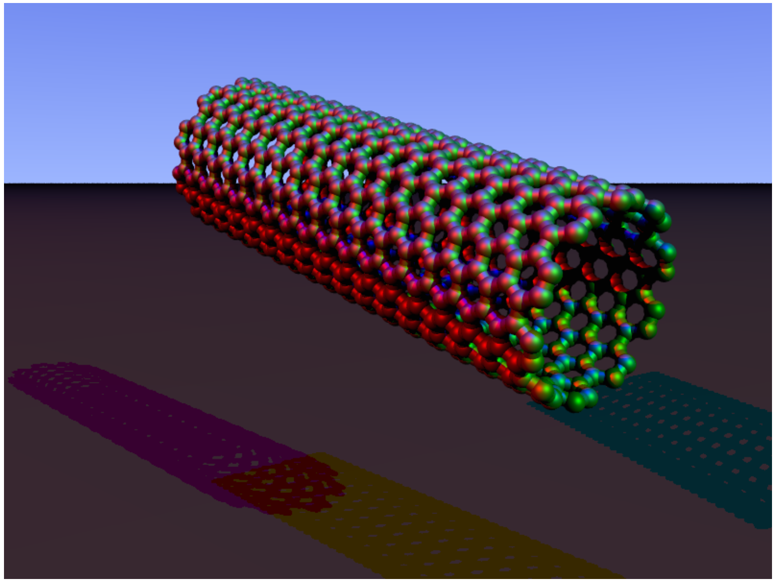
1st Report of Single Atomic Layer Wall Carbon Nanotube, or SWNT



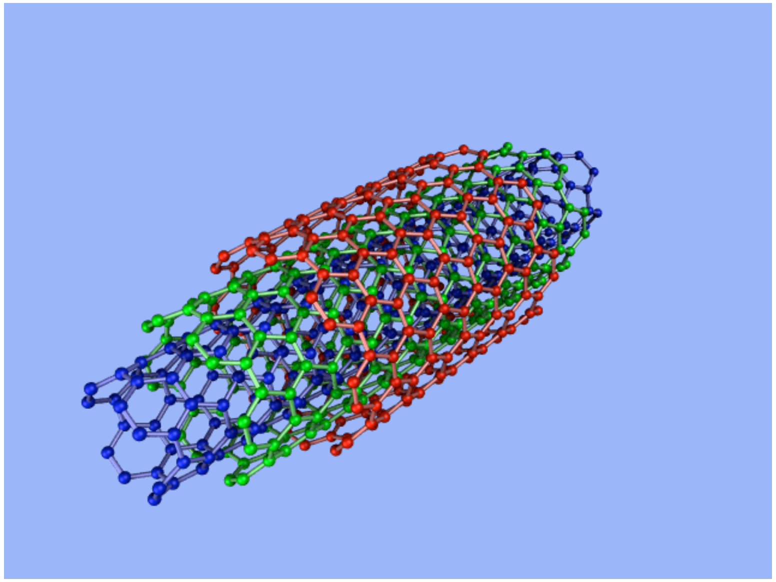
- produced using arc discharge, with Co catalyst present.
- diameters = 1.2 ± 0.1 nm
- lengths of several microns

Carbon Nanotubes (CNTs)

Single-Walled CNTs (SWNTs)
high thermal conductivity
semiconducting or metallic



Multi-Walled CNTs (MWNTs)
high thermal conductivity
metallic conduction



The Holy Grail for SWNTs

enabling nanoelectronics

Electronics, Volume 38, Number 8, April 19, 1965

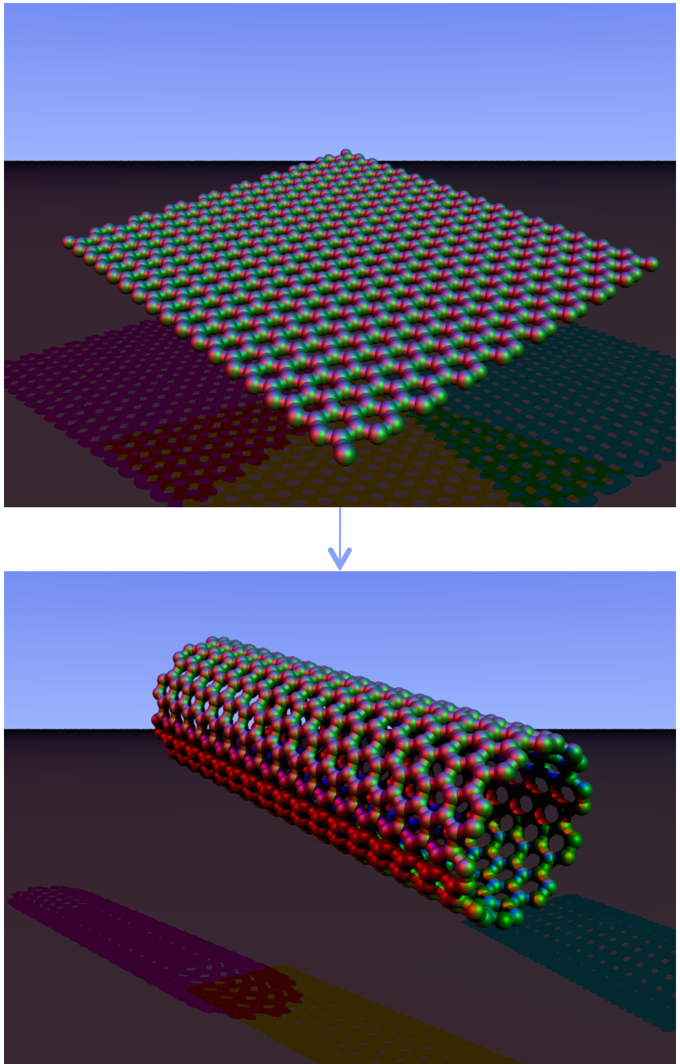
Cramming more components onto integrated circuits

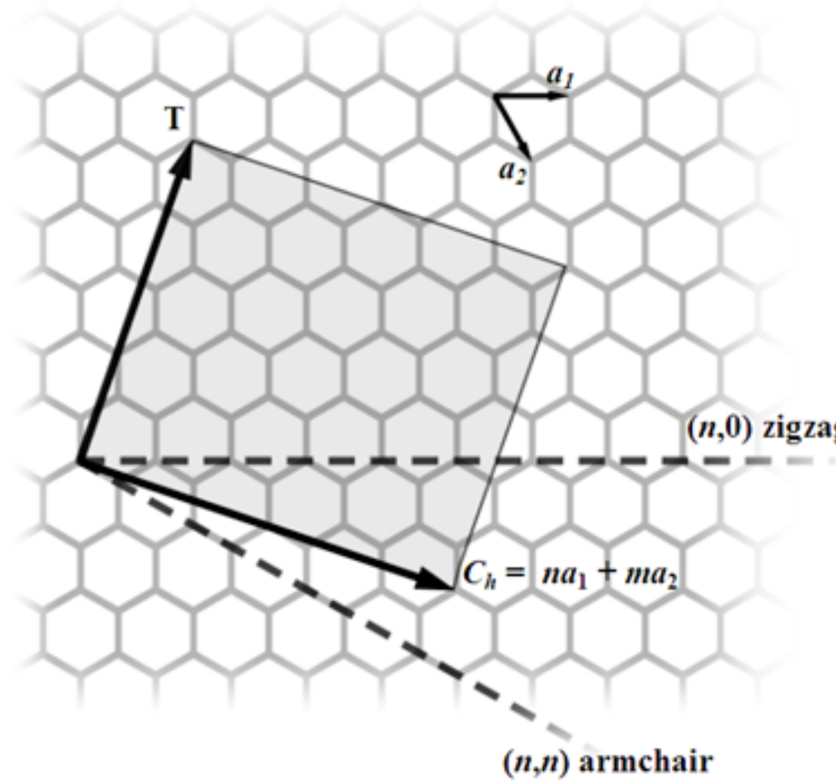
With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

SWNT Chirality

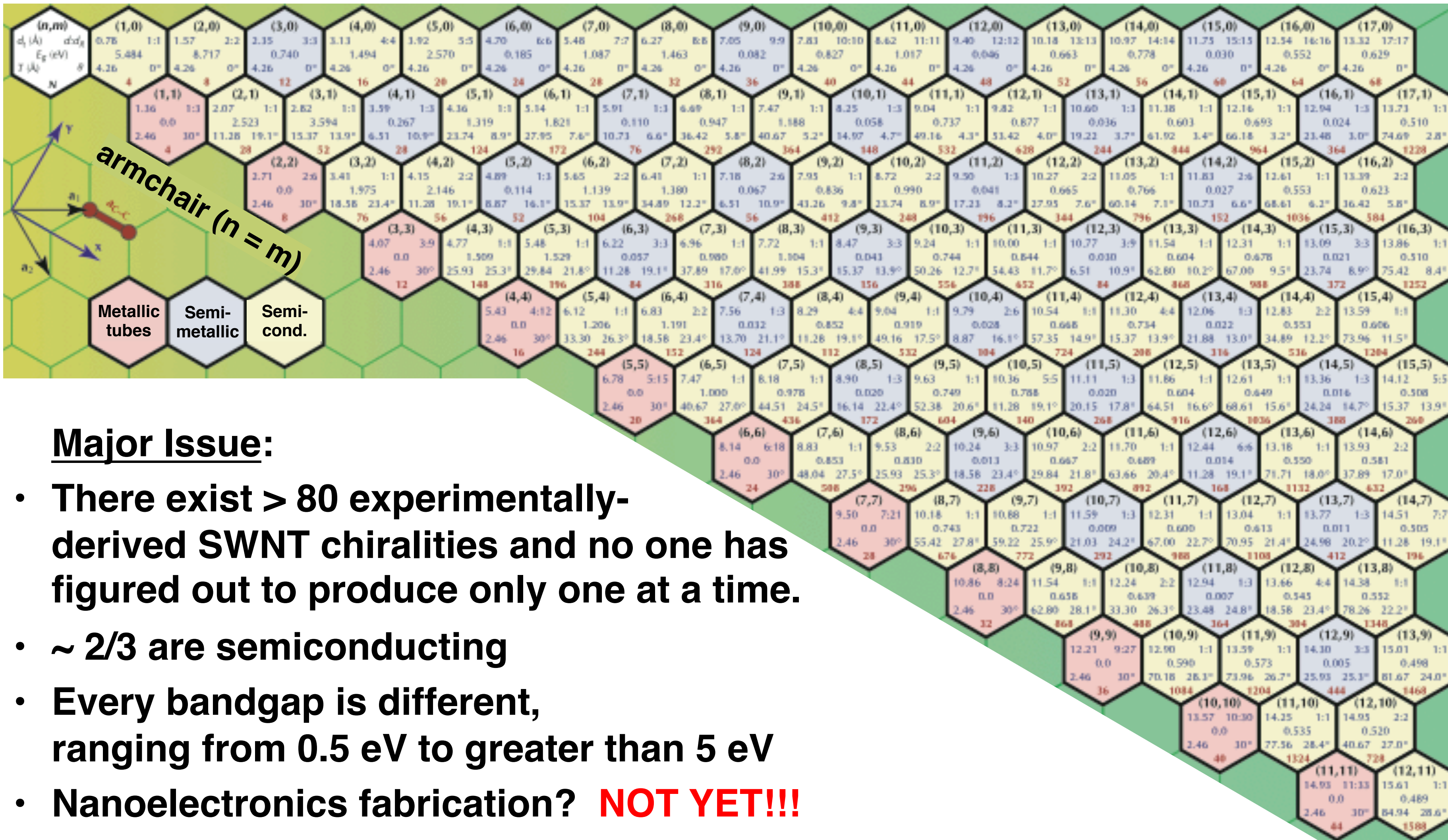




if n = m, then metallic (armchair)
if n – m = 3, then semimetallic
all other chiralities are semiconducting

Chirality Map

zigzag(m = 0) increasing diameter



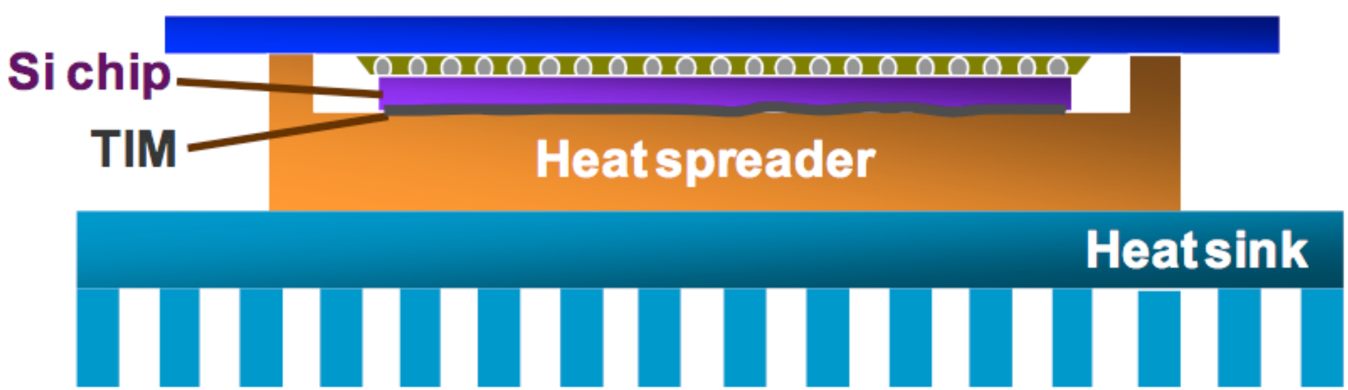
Major Issue:

- **There exist > 80 experimentally-derived SWNT chiralities and no one has figured out to produce only one at a time.**
- **~ 2/3 are semiconducting**
- **Every bandgap is different, ranging from 0.5 eV to greater than 5 eV**
- **Nanoelectronics fabrication? NOT YET!!!**

Electronic Applications

That Do Not Depend on Chirality (or Wall Number)

- ballistic transport (nano-connections between device components)
- cold-cathode field emission (room-temperature electron guns)
  - flat panel displays
  - sensors
  - nano e-beam lithography
- **thermal interface material (TIM) – *passive cooling***
  - ***think high-tech Ag-paste for high-power applications***



Removing heat generated by high-power electronics devices is often a limiting factor in system performance.

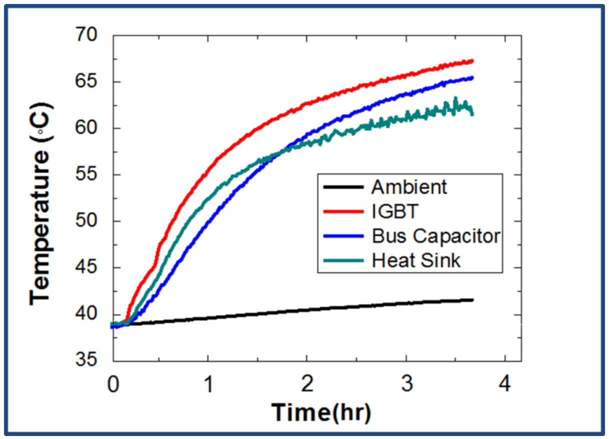
Requirements for High-Quality TIMs

1. **High thermal conductivity**
2. **Excellent adhesion and thermal bond to both heat source and heat sink**
3. **Thermal stability at operating temperatures (does not degrade with temperature cycling)**
4. **Negligible thermal stresses (does not delaminate)**

all are necessary for high-performance TIMs

The Problem: Heat Removal from Existing TIMs Is Not Good Enough

Example: Temperature Rise of IGBT in Typical PV Inverter

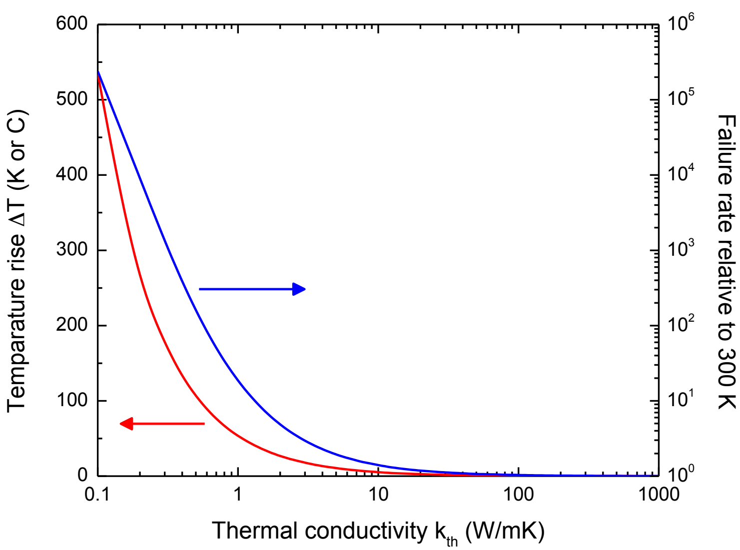


The insulated gate bipolar transistor, IGBT (i.e. power electronics) is a hot element in a typical photovoltaic inverter system.

Most failure mechanisms follow an Arrhenius relationship for the failure rate acceleration factor:

$AF = \exp(-E_A/kT)$

E.g. ~ 8 KW IGBT dissipates 535 W of heat.



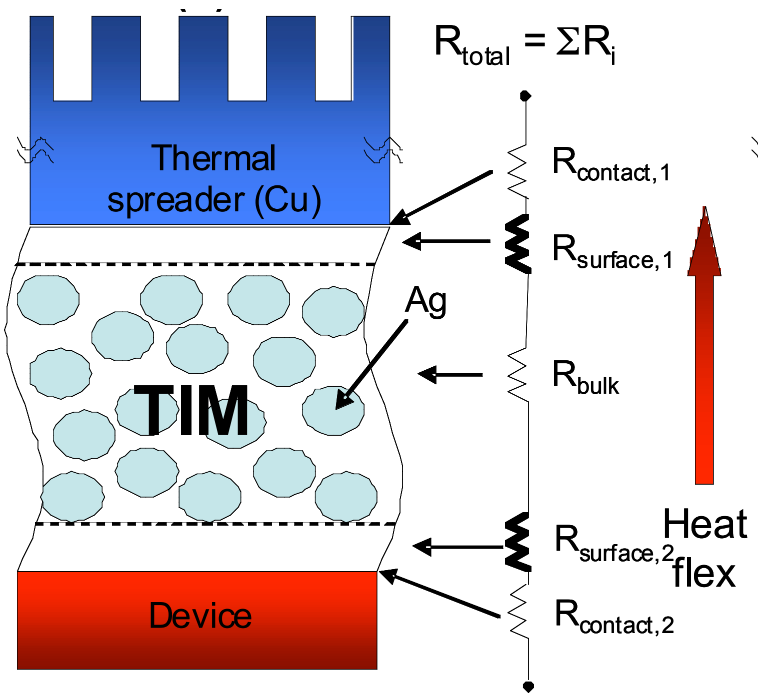
- Both temperature rise and device failure rate increase with the use of low thermal conductivity TIM materials.
- Device failure rates are a problem when TIM $\kappa < 20$ W/m•K, and are a serious problem with TIM $\kappa \sim 1$ W/m•K.

Courtesy of Bob Kaplar

Problems with Commercial TIMs

Metal/epoxy composites (e.g. Ag paste)

Excellent thermal contact
Poor thermal conductivity
Thermal cycling degradation
Poor adhesion quality



TIMs can only be as good as their thermal conductivity!

Thermal conductivity	
Ag	420 W/m•K
Cu	401 W/m•K
Al	237 W/m•K
Au	317 W/m•K
Si	148 W/m•K
In	82 W/m•K
Epoxy	0.23 W/m•K

Unfortunately, the thermal conductivity of metal-filled epoxies are dominated by percolation through the epoxy, resulting in values typically < 1 W/m•K.

Is there a better choice?

Carbon-Filled Epoxy TIMs?

Certain forms of carbon have very high thermal conductivity!

Material	Thermal Conductivity
Diamond	90 – 2320 W/m•K
Carbon Nanotubes (CNTs)	10 – 3000 W/m•K
Unsupported Graphene	4840 – 5300 W/m•K

Epoxy/carbon composites of these materials run into similar issues:

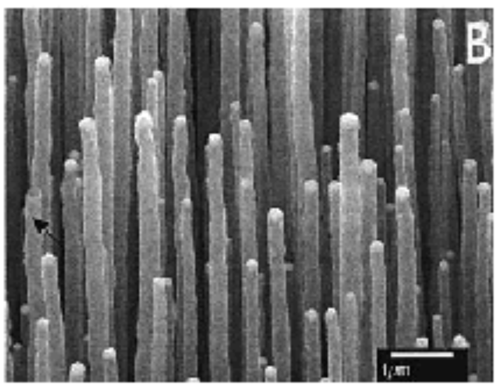
1. phonon percolation between carbon particles through epoxy
2. stress-induced phase separation due to mechanical squeezing to make the thermal contacts

Question: Can we take advantage of high-thermal conductivity carbon materials for TIMs w/out using epoxies?

Taking Advantage of CNT Array Geometry

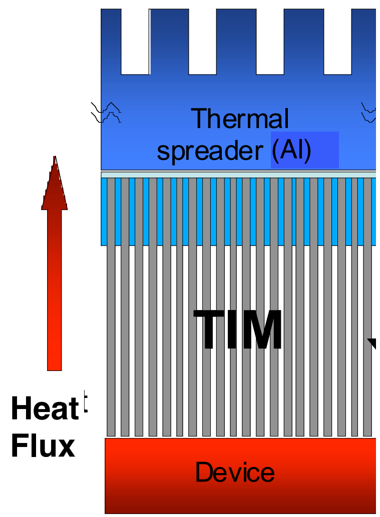
Advantages of aligned CNT TIM vs. conventional metal-filled epoxies

First report of well-aligned CNTs using plasma-enhanced hot-filament CVD.

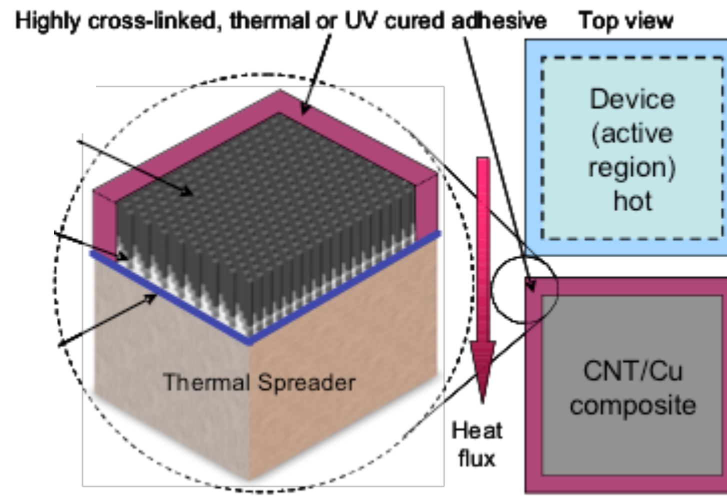


Ren, Huang, Xu, Wang, Bush, Siegal and Provencio, *Science* (1998).

CNT-based TIM concept with no epoxy in thermal pathway.



Conceptual design of CNT-based TIM application



Siegal and Yang

Thermal conductivity of CNTs spans > two orders-of-magnitude!

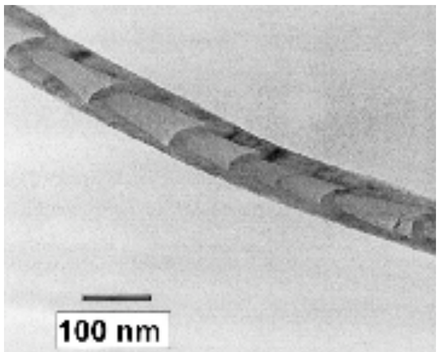
• Yi et al, PRB (1999)	25 W/m K
• Hone et al, APL (2000)	200 W/m K
• McEuen et al, PRL (2001)	3000 W/m K

} ***Due to crystalline quality of CNTs!***

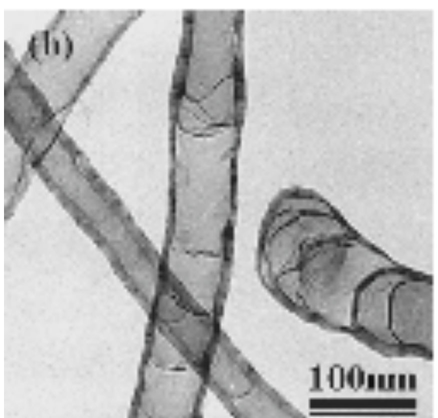
Various CNT Defects Observed by TEM in the Literature

all grown using high-rate plasma CVD processes

Bamboo Structures

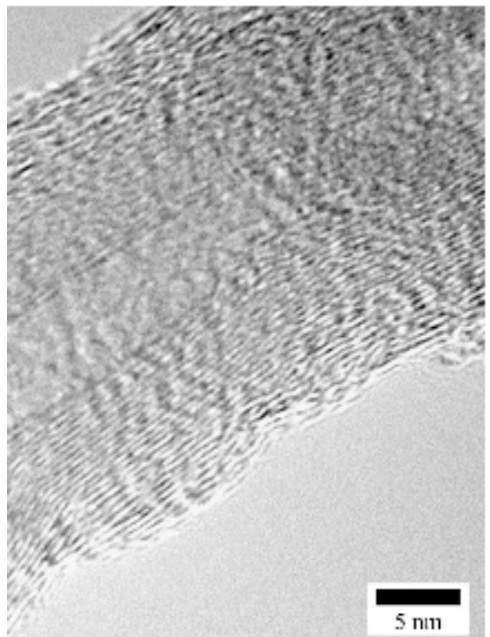


Lee et al, Chem Phys Lett (2000)



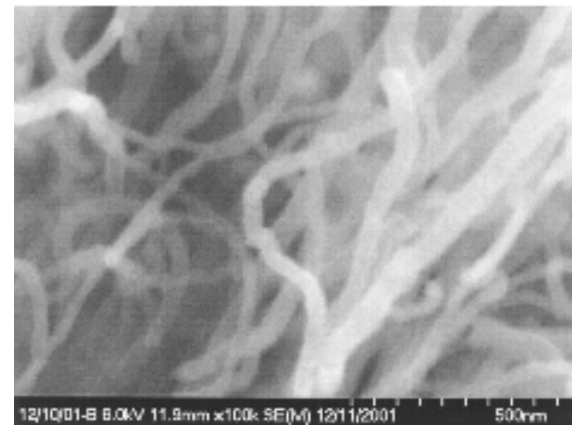
Park et al, Thin Sol Films (2002)

Changes in Wall Structure



Okuyama et al, JMR (2006)

Kinks & Bends

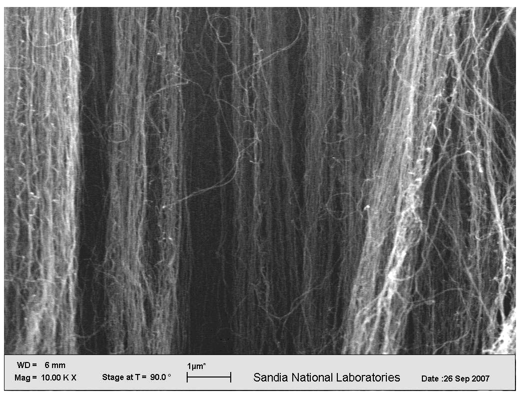


Luo et al, EC & SS Lett (2003)

Breaks in CNT Wall Structures

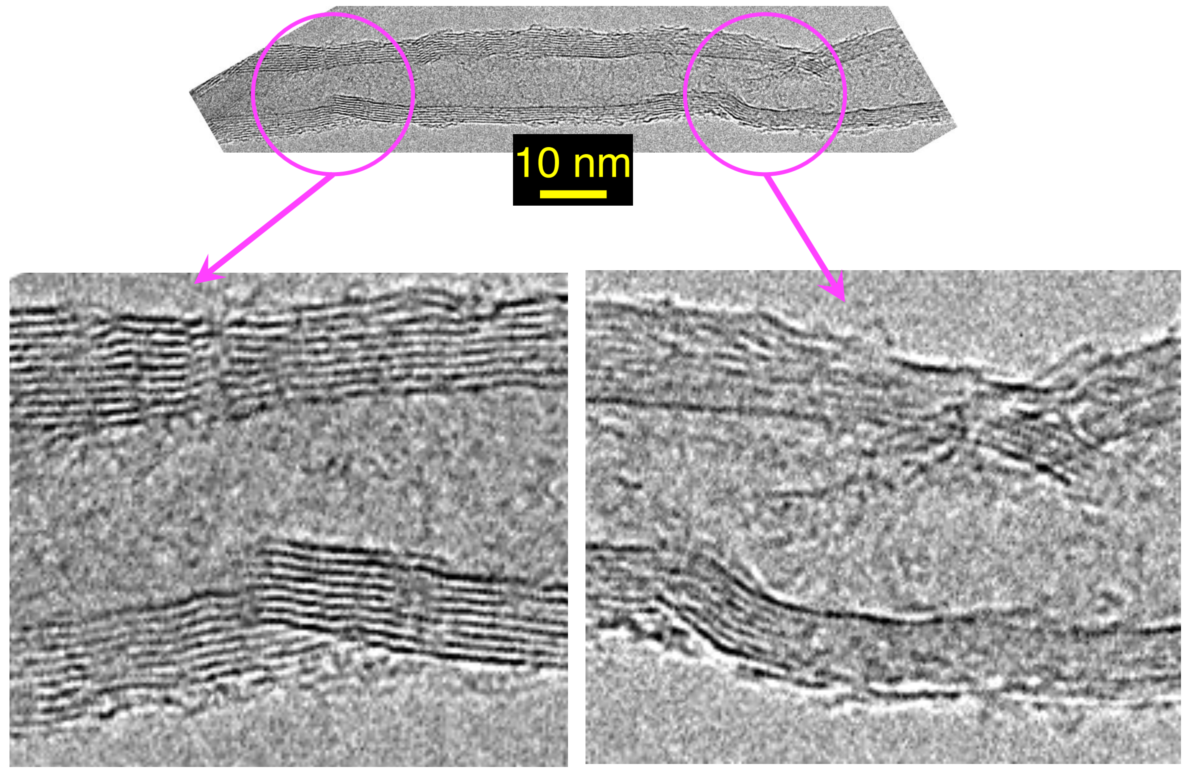
CNT forest grown by high growth rate plasma CVD process

Siegal and Huang (unpublished)



SEM cross-section image of typical CNT forest grown using plasma-enhanced CVD.

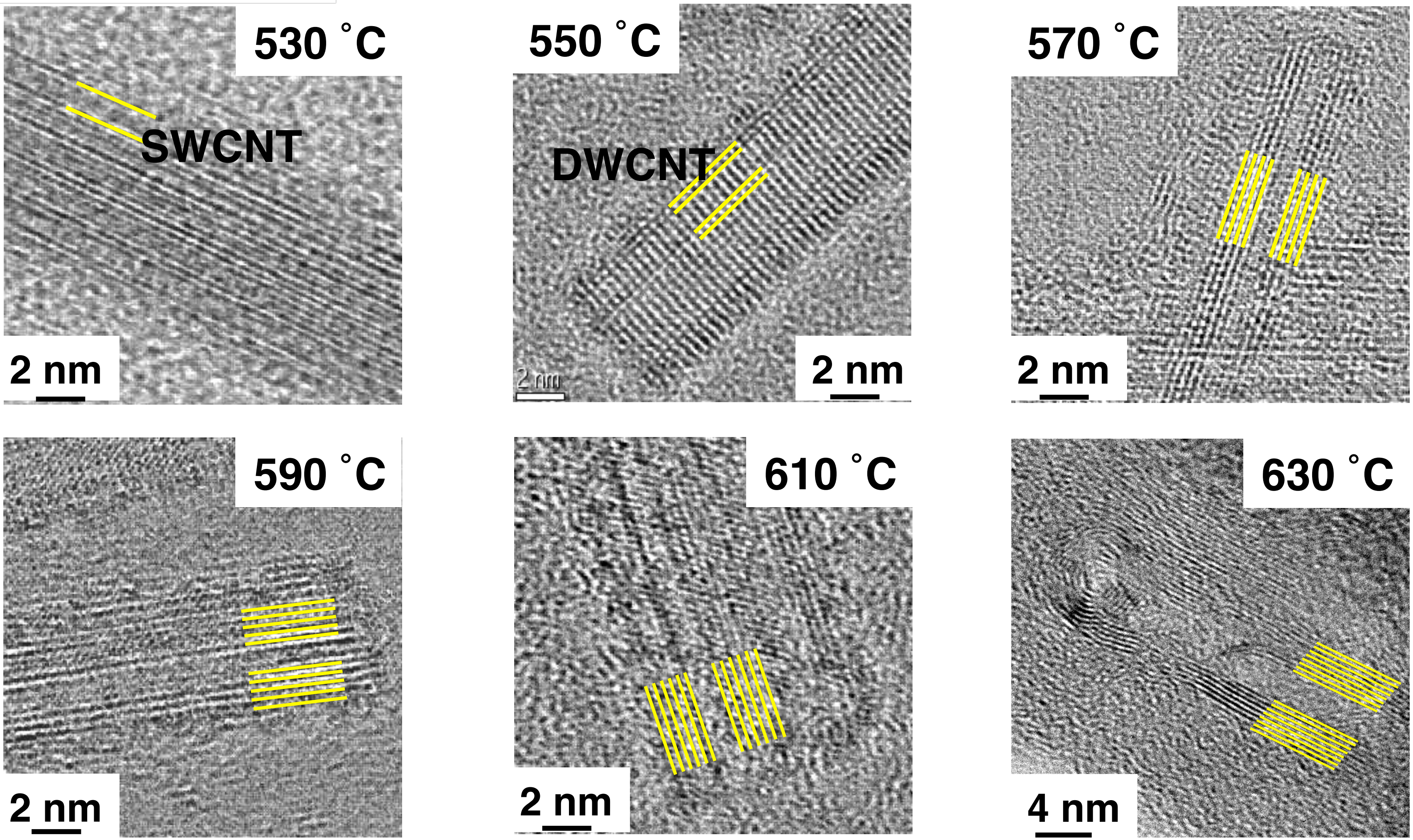
Note: CNT entanglement leads to only 5 – 10% filling of volumetric space!



Inner and outer diameters, wall numbers all vary both CNT-to-CNT and within a single CNT.

Such breaks in wall structures will play havoc with transport properties!

Thermal CVD (slower growth rate) for Higher Crystalline Quality CNTs

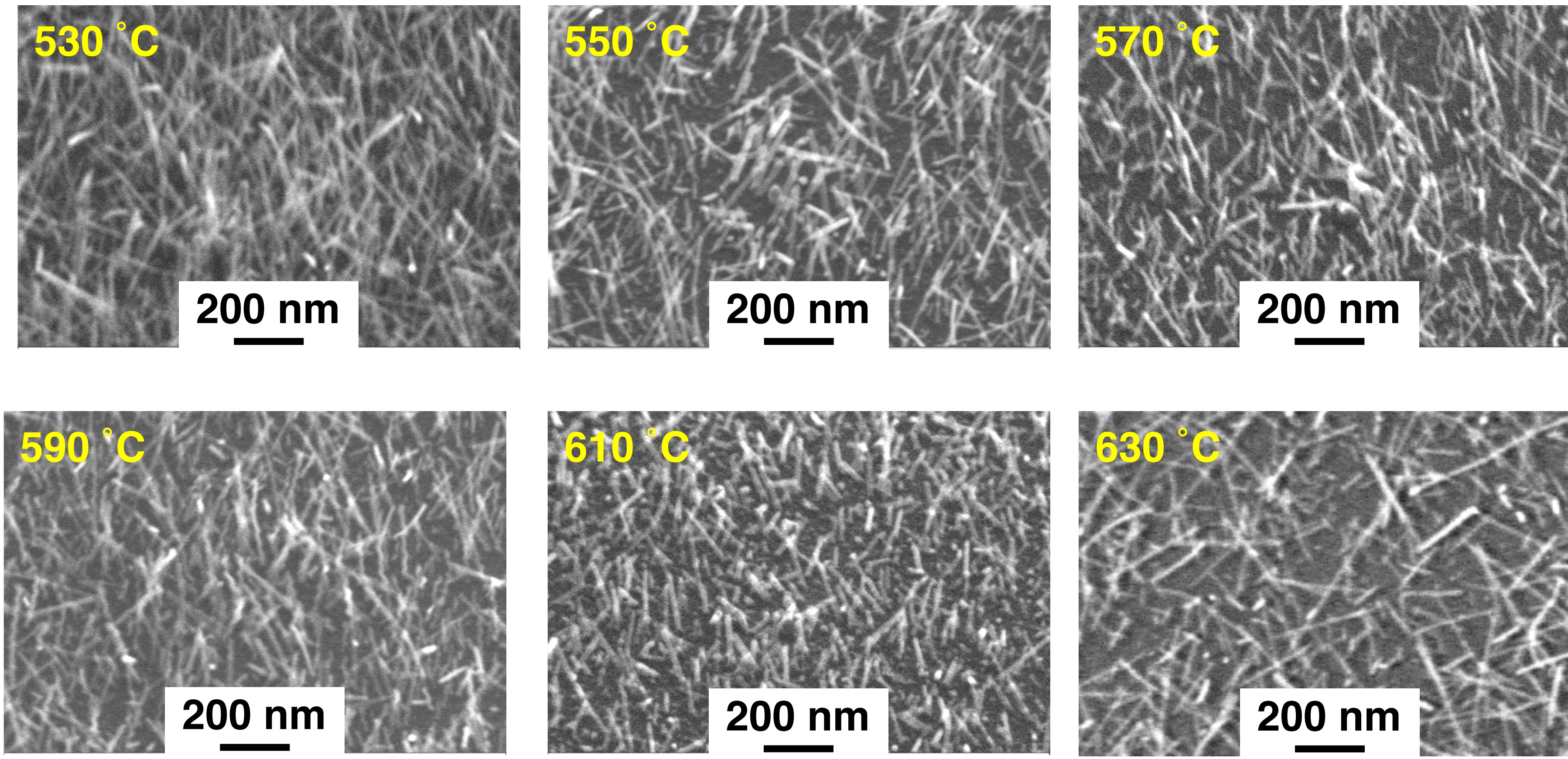


Slowing the CNT growth rate improves their crystalline quality!

Siegal et al, *J. Phys. Chem.* (2010).

Thermal CVD Arrays

SEM images show abundant CNT growth at every temperature.
However, no preferred alignment. ***Need to use a nanopore template.***

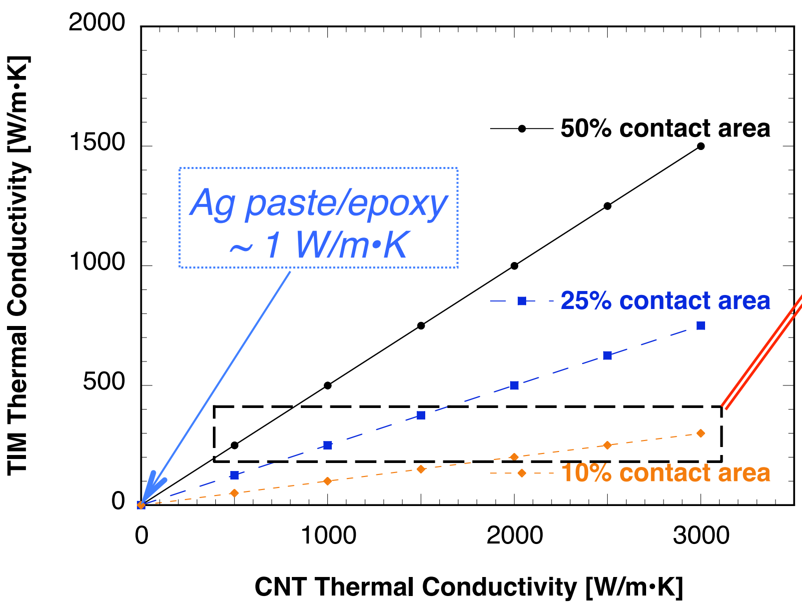


(resolution limit of SEM makes all diameters look similar)

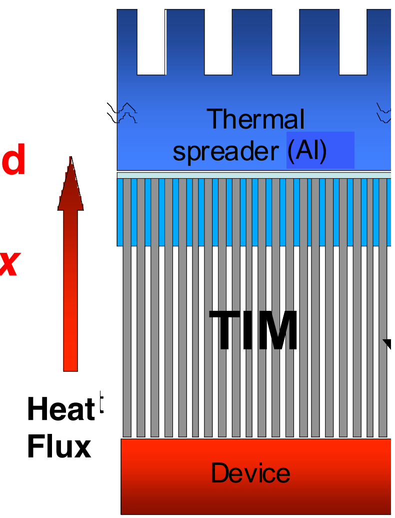
Siegal et al, *J. Phys. Chem.* (2010).

Sandia National Laboratories

Required Properties for CNT TIMs

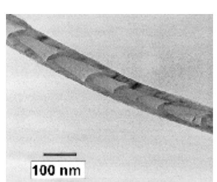


Goal: **eliminate TIM thermal bottleneck and improve performance *by factors of 10 – 500x without even full optimization!***

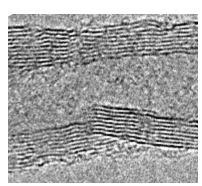


CNT Quality ⟶

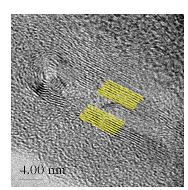
Plasma-Enhanced CVD | Thermal CVD



Lee et al, Chem Phys Lett (2000)



Siegal, Huang (unpublished)



Siegal et al. J. Phys. Chem. (2010)

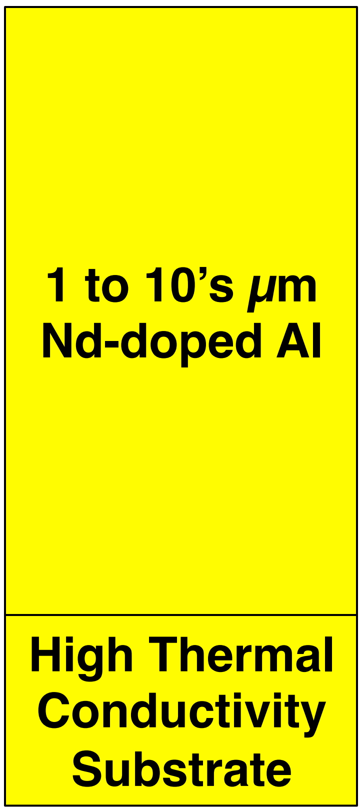
Properties for optimal CNT-TIM performance

- **no adhesives in thermal path.**
- **high CNT site density to increase number of thermal pathways, i.e. no entanglement!**
- **planarized array tips to maximize thermal contacts to hot device surfaces.**
- **high-crystalline quality CNTs for high thermal conductivity.**

Anodized Al-Oxide Nanopore Templates

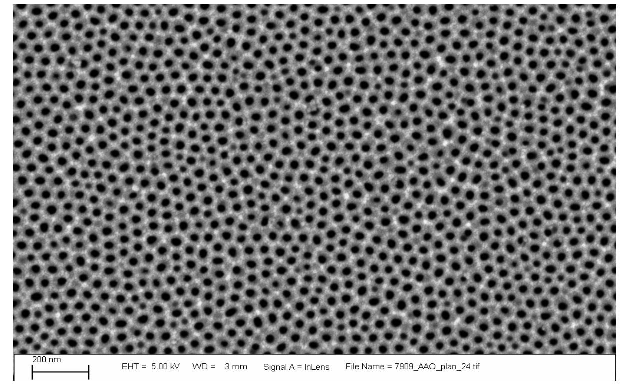
Anodized Aluminum Oxide (AAO) Nanopore Templates on Substrates

Sputter low-stress, mirror-smooth Nd-doped Al films onto thermal sink substrate.

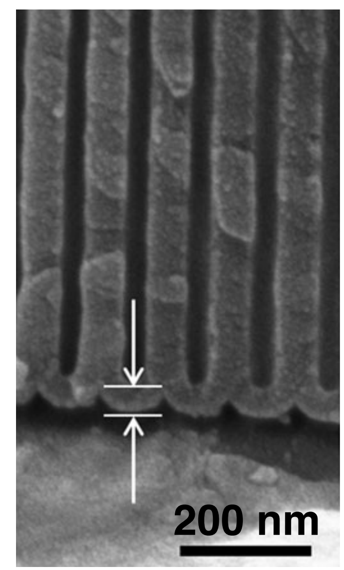


forms nanopore template following anodization

Al, Al-alloy, Si, sapphire (depends on application)



oxide barrier at well bottoms prevents the ECD of metal catalysts for CNT growth



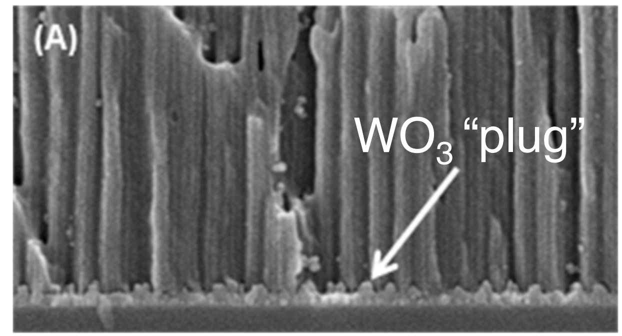
Limmer et al, *JES*, **159**, D235 (2012)

Anodized Al-Oxide Nanopore Templates

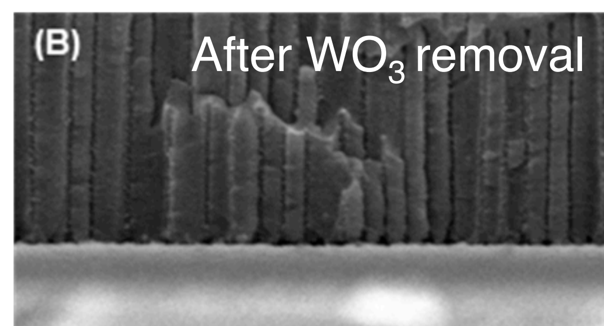
Anodized Aluminum Oxide (AAO) Nanopore Templates on Substrates

Sputter low-stress, mirror-smooth Nd-doped Al films onto thermal sink substrate.

1 to 10's μm Nd-doped Al	**forms nanopore template following anodization**
100 nm W	**sacrificial W layer that prevents Al-oxide 'crud' at pore bottoms**
High Thermal Conductivity Substrate	**Al, Al-alloy, Si, sapphire (depends on application)**



Chemically-selective etching of sacrificial W-oxide "valve" layer leaves a conductive W layer at pore bottoms, *critical for electro-chemical deposition of Co-metal catalysts for CNT growth.*



Rochford et al, *JMR*, **30**, 316 (2015)

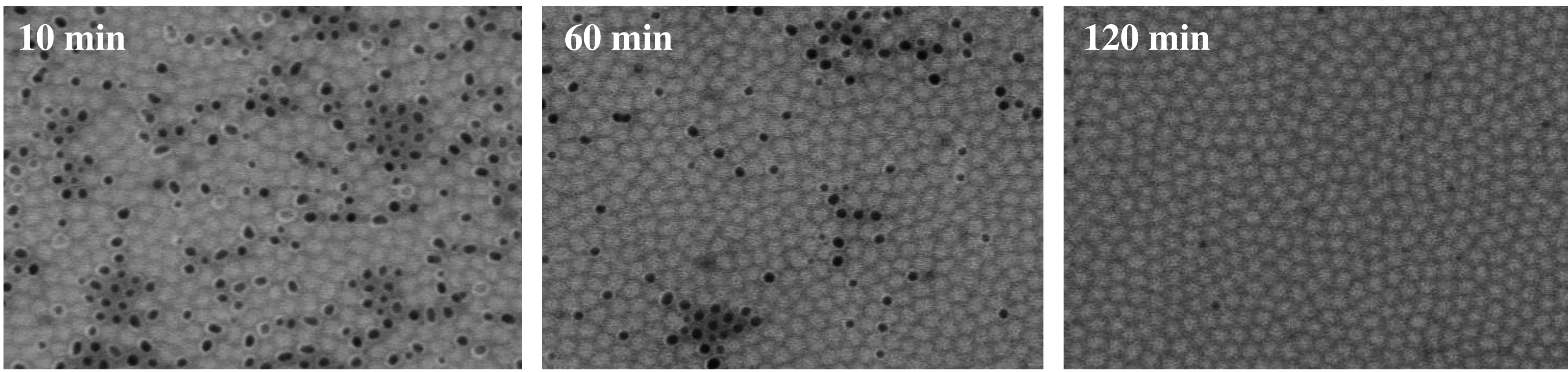
Catalyst Deposition Inside Nanopores

Electrochemical deposition of Co nanowires inside AAO pores

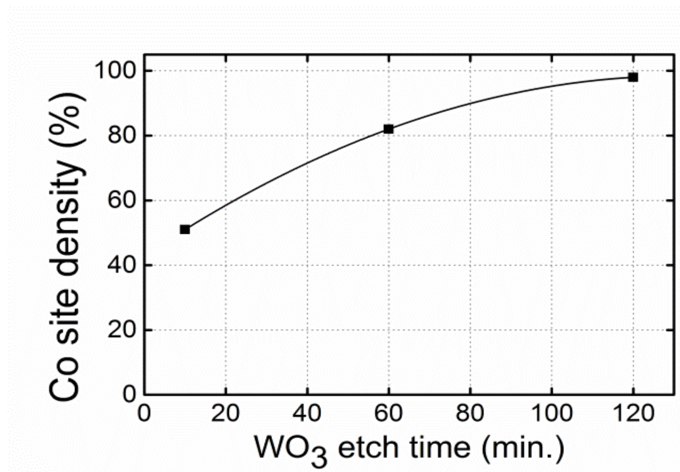
(Nanotubes will only grow from catalyst-filled pores)

Controlling the duration of the WO_3 etch step controls the catalyst site density!

(0.2 M, pH 7 phosphate buffer solution)



To study catalyst site density, samples are ion-milled to expose catalyst wires inside pores. Dark pores are empty, light-colored pores are full of Co.

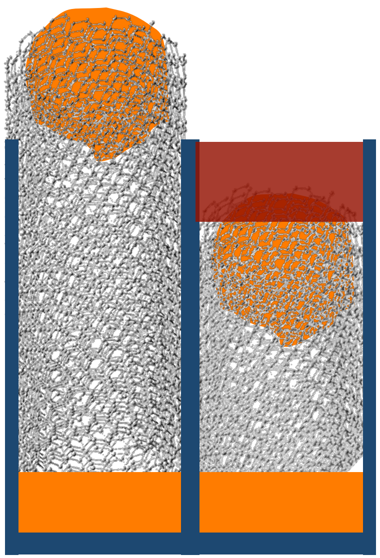


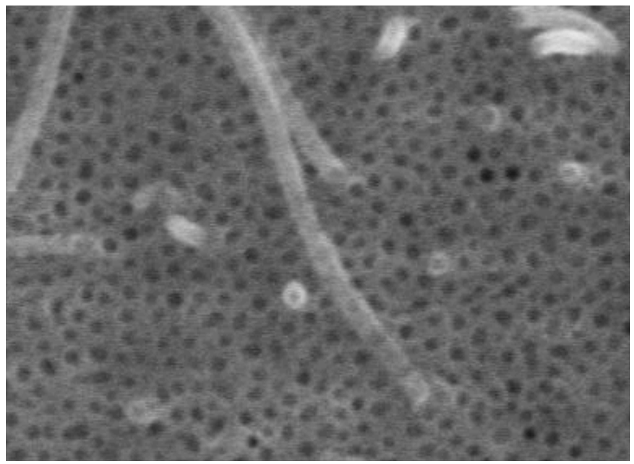
10^{10} nanopores/cm^2 and 75 nm diameters yields > 44% surface coverage!

Rochford et al, *JMR*, **30**, 316 (2015)

CNT Growth in AAO Nanopores

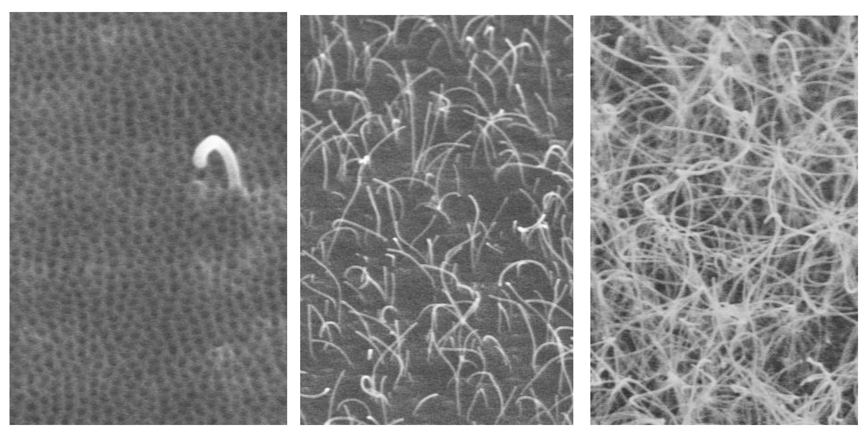
AAO catalyzes C_2H_2 decomposition and can plug the pore openings with amorphous-carbon, preventing the emergence of CNTs.





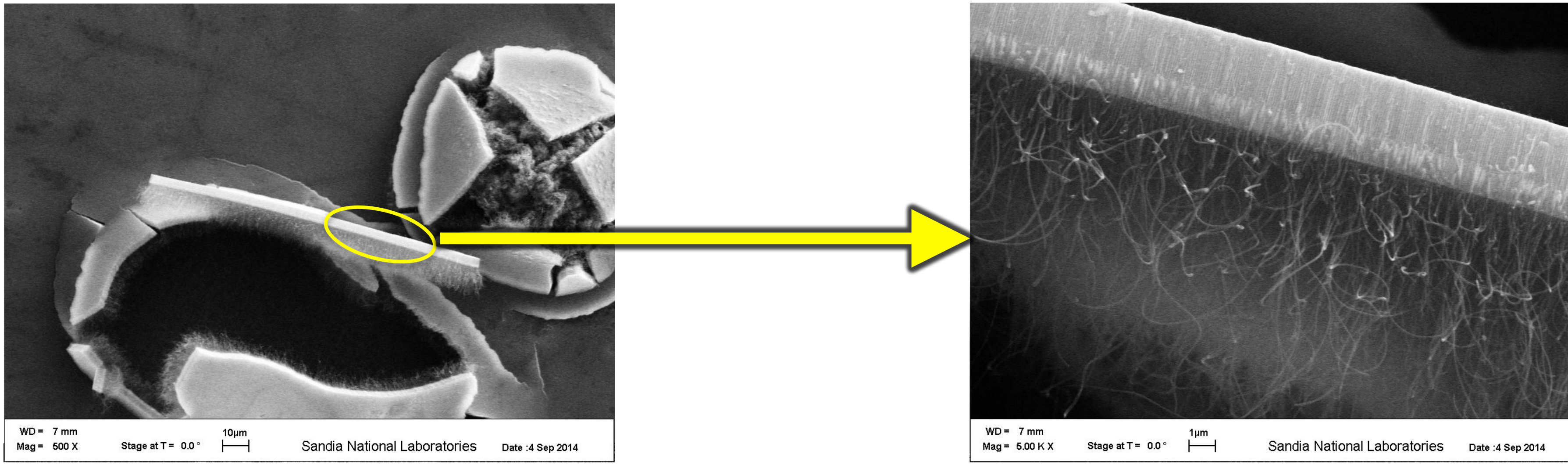
Most nanopores are dull gray, **while a few appear much darker.** The gray pores are filled with a-C that preventing CNTs from growing 'up and out'.

Competition exists between CNT and a-C growth. Need short distance between top of catalyst and template surface, *i.e. small aspect ratios.*



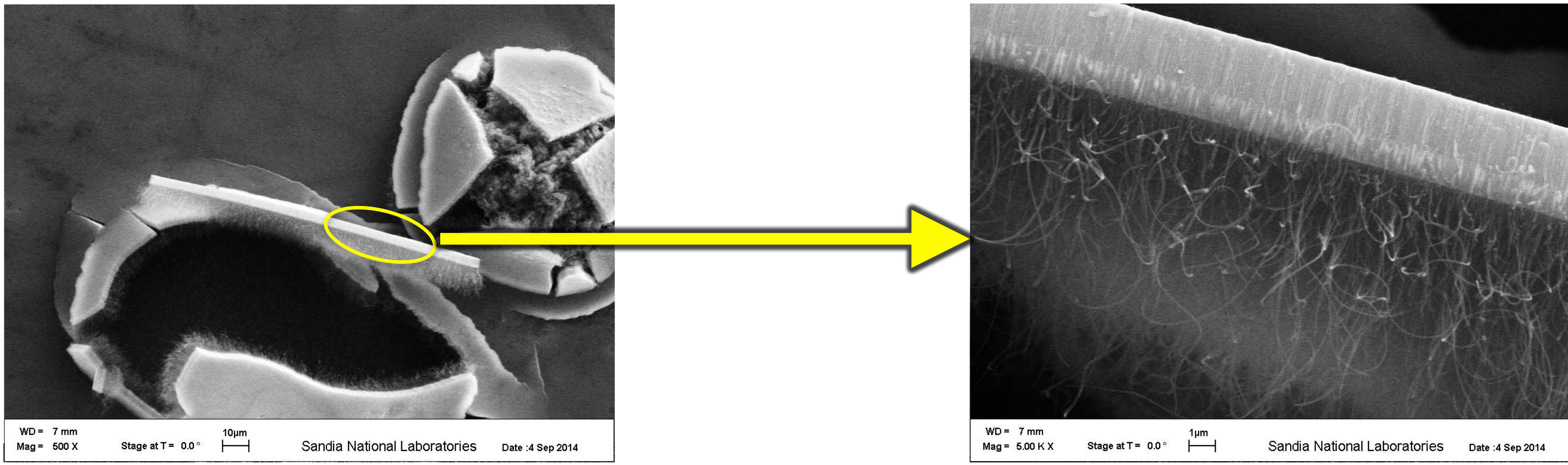
Rochford et al, *JMR*, **30**, 316 (2015)

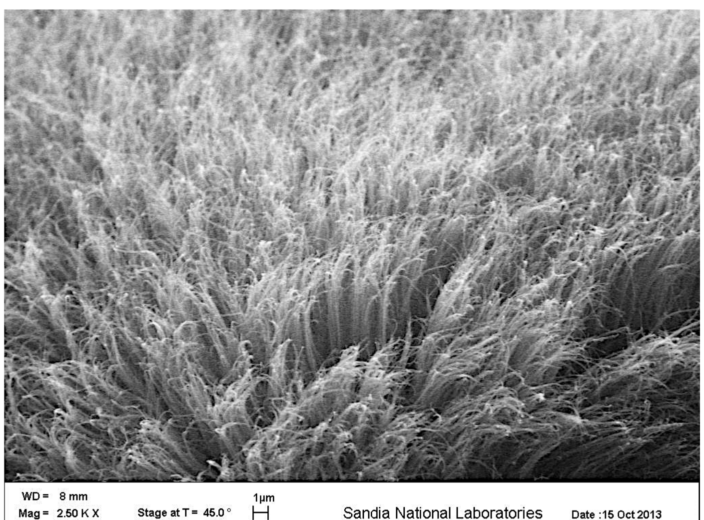
Controlling the Co Catalyst Position



- *Occasionally,* we experience a film stress situation where the AAO template cracks and somewhat detaches from the substrate.
- Note that Co filled ~ 30% of the AAO pore depth. No CNTs grew from the AAO surface, however…
- **Note the very high CNT density from the underside of the template where the Co-catalyst is flush with the template, *perhaps 1 CNT per nanopore…***
- ***Can we control this catalyst geometry on the top surface?***

Controlling the Co Catalyst Position





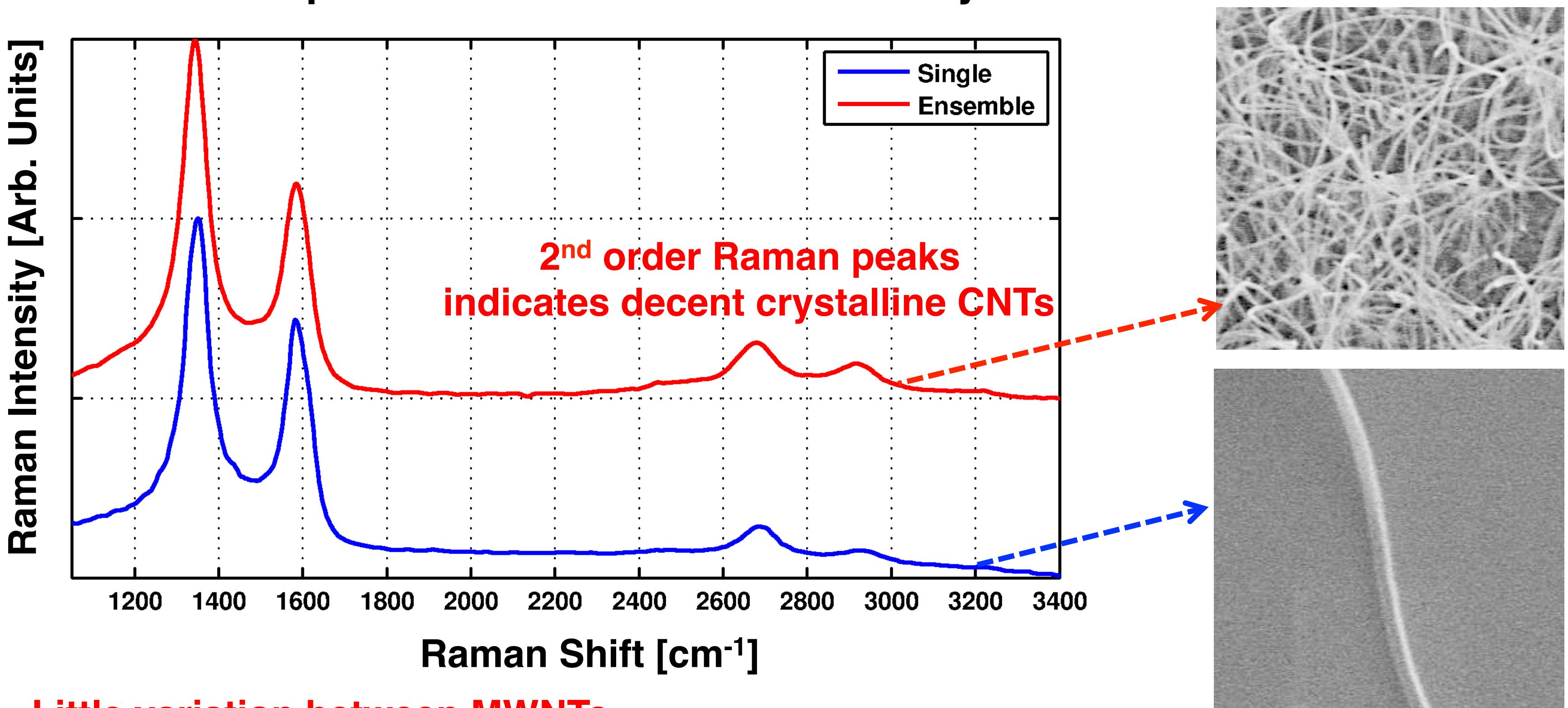
- Now we embrace the inability to precisely control ECD height of catalyst, and allow it to slightly over-coat the template surface.
- Use ion beam milling to polish the surface so that the catalyst is flush with the AAO surface.
- CNTs may be growing from every pore! 44%?
- ***This needs further study. E.g. how far can we etch the Co back into the pores?***

CNT Microstructural Quality

individual CNTs vs. full arrays

Raman spectroscopy confirms growth of uniform MWNTs

Individual spectrum is the same as the array!



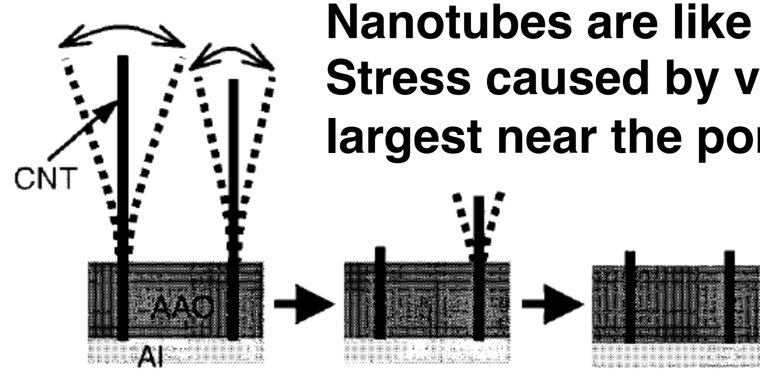
- Little variation between MWNTs
- I(D)/I(G) of 1.9 implies moderate disorder
- Consistent with non-graphitized CVD-grown MWNTs

Rochford et al, *JMR*, **30**, 316 (2015)

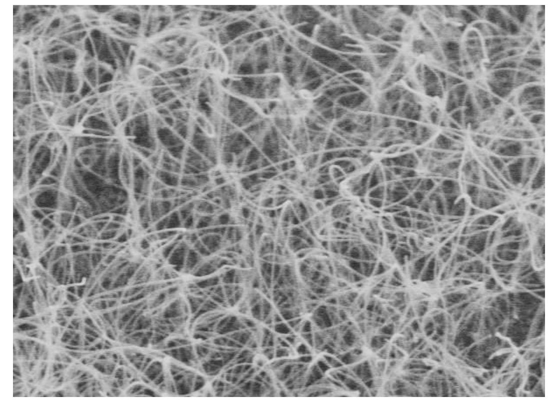
Planarization of CNT Arrays

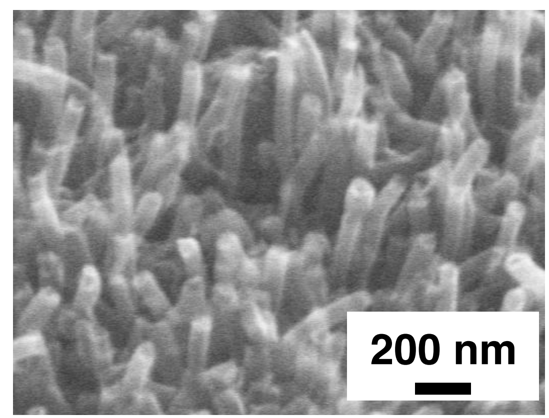
40 kHz ultrasonication for 1 minute in acetone bath

Nanotubes are like cantilevers. Stress caused by vibration is largest near the pore mouth.



Jeong et al. *Chem. Mater.* (2002)



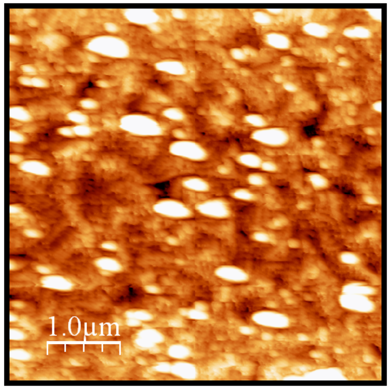


- CNTs uniformly cut to ~ few tenths of a μm above the AAO.
- CNT site density remains high after cutting, suggests that the CNTs are not being pulled out of pores or cut below the AAO surface.
- *Will need to etch catalyst somewhat below the template surface to prevent CNTs from detaching.*

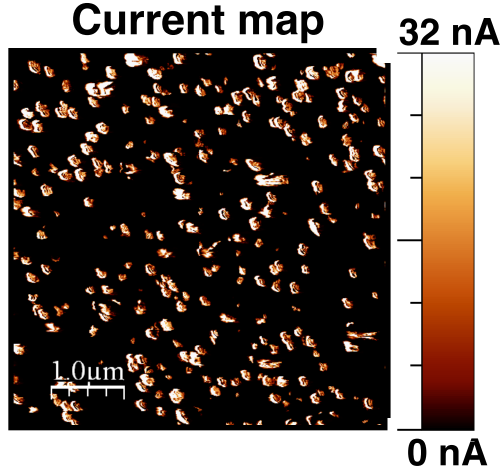
Rochford et al, *JMR*, **30**, 316 (2015)

CNT-Substrate Ohmic Contacts

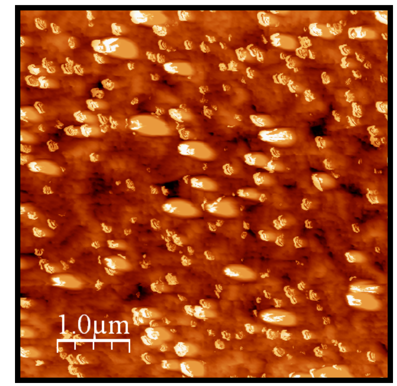
AFM map



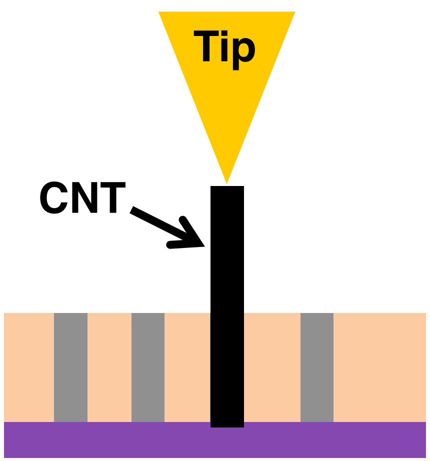
Current map



Merged map

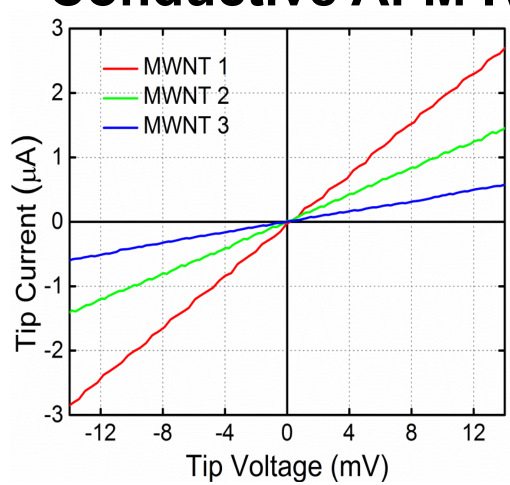


AFM provided evidence that cleaved CNTs remain highly conductive



Loading Force ~ 1.6 μN

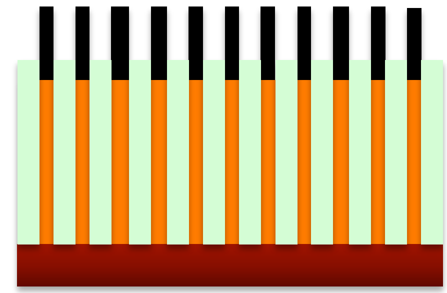
Conductive AFM IV



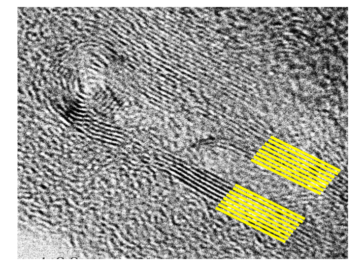
Conductive AFM confirms that electrical continuity to the substrate *is preserved after ultrasonic cutting!*

Rochford et al, *JMR*, **30**, 316 (2015)

CNT TIM Summary

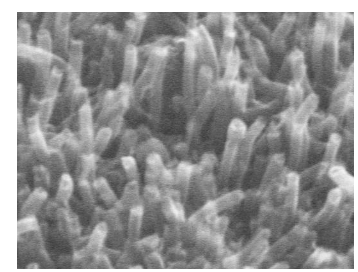


- Removing heat generated by high-power electronics is often the limiting factor in system performance.
- CNT-TIMs could eliminate epoxy from the thermal path and improve TIM performance by orders-of-magnitude.



- Thermal CVD grows higher crystalline quality CNTs than plasma-enhanced CVD.
- Thermal CVD requires the use of a nanopore template to provide vertical orientation.

- The aspect ratio of the nanopore above the Co catalyst is critical to achieve a high CNT site density.
- Ultrasonication can planarize an array without damaging the CNTs to provide a uniform surface for making thermal contacts to a heat source.



- ***Next steps: (a) optimize ion beam milling to control template aspect ratio, (b) study CNT crystalline quality vs. CVD growth temperature, and (c) measure thermal properties!***