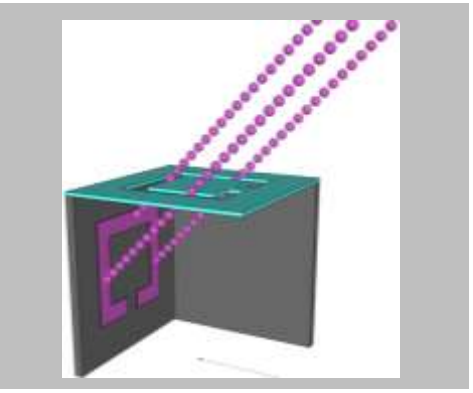
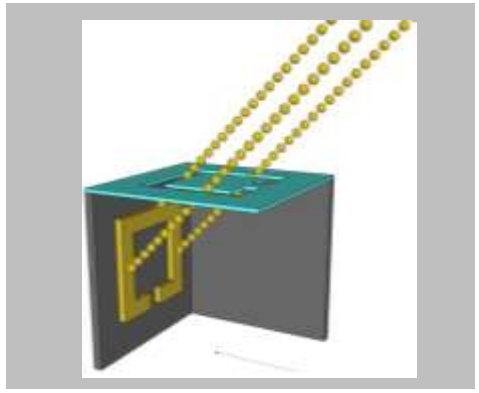
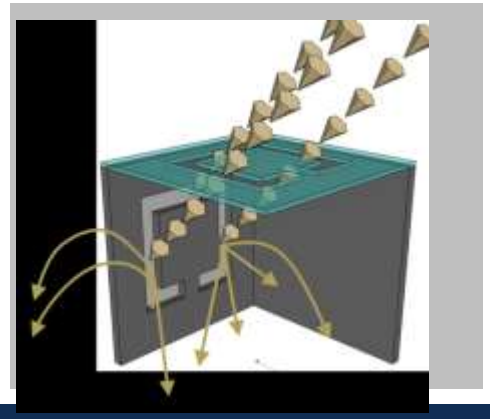
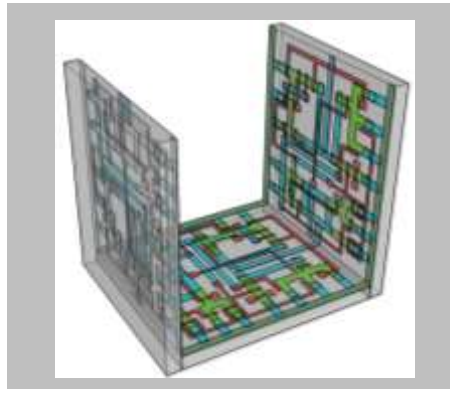
Exceptional service in the national interest

SAND2016-3416C

3D-ICs Created Using Oblique Processing

D. Bruce Burckel

dbburck@sandia.gov

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SAND NO. 2011-XXXXP

Outline

1.) Background

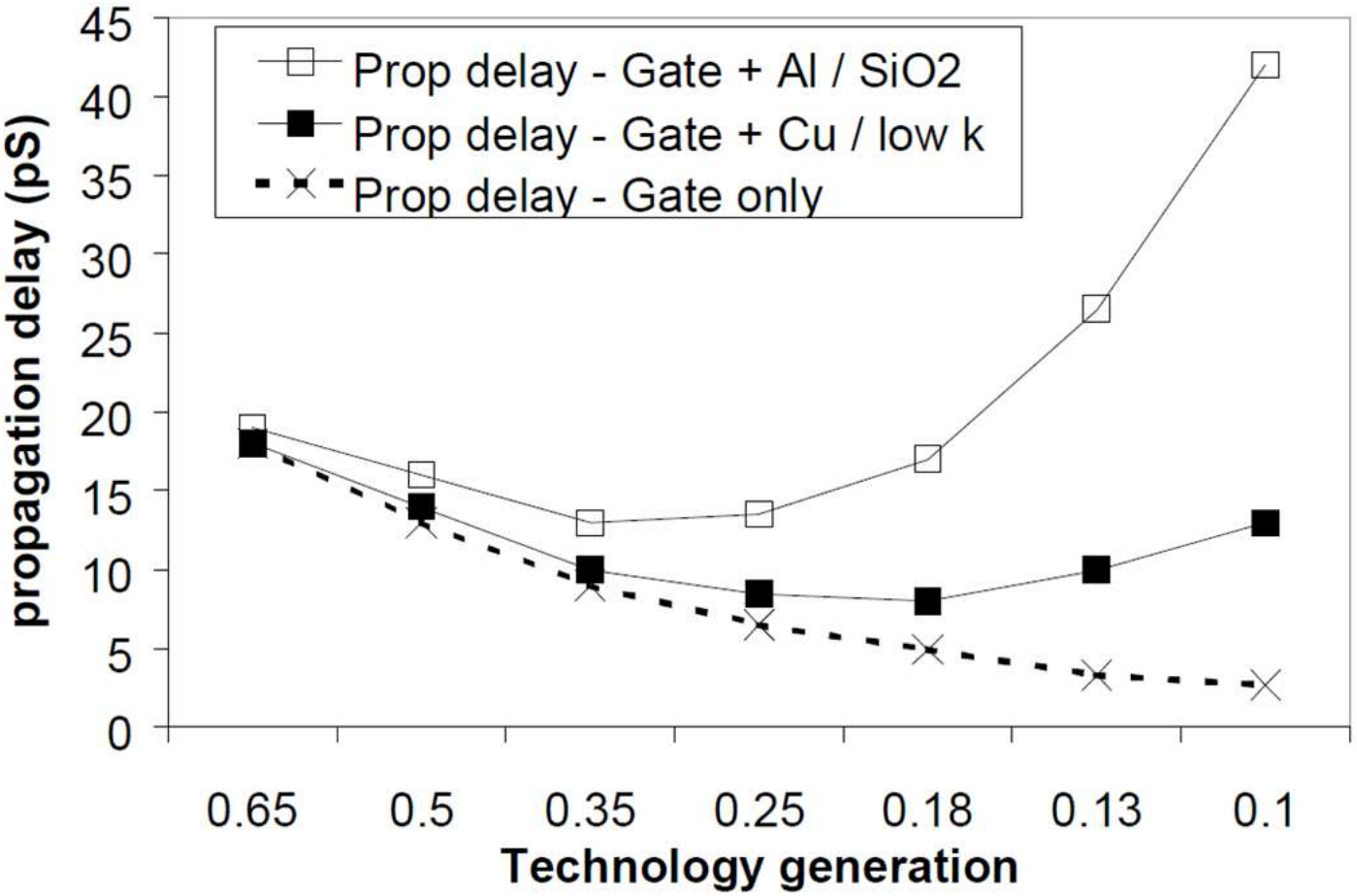
2.) Device Level 3D-ICs vs.
TSV-centric and Monolithic 3D-ICs

3.) Device Level 3D IC Fabrication

4.) Prospects

Background

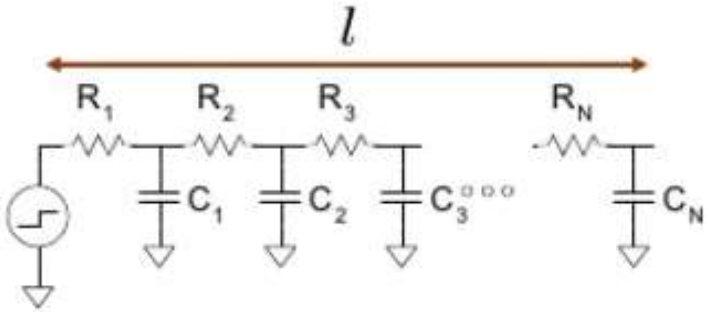
Interconnect Delays Dominate Modern Transistors



Keith Buchanan, "The evolution of interconnect technology for silicon integrated circuitry," GaAs MANTECH Conference, (2002)

3D ICs Reduce Interconnect Length

Treating Interconnects as distributed circuit elements :



R_i = resistance per unit length
C_i = capacitance per unit length

$$\text{RC delay} \propto L^2$$

$$\text{Joule Heating} \propto L$$

Rent's rule and wire length estimation

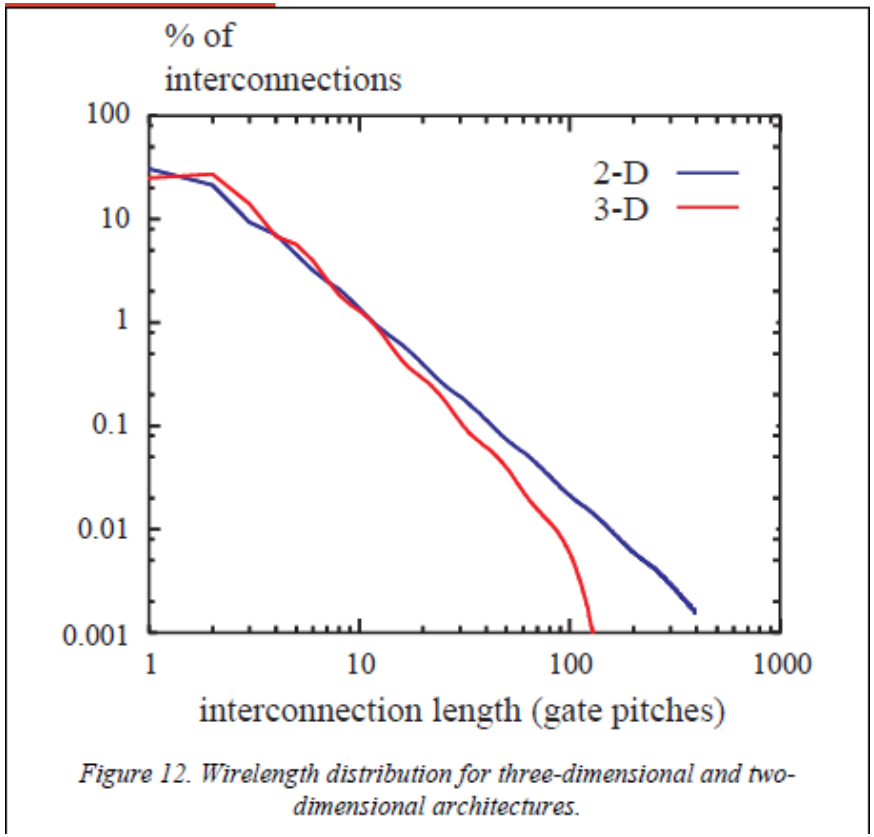
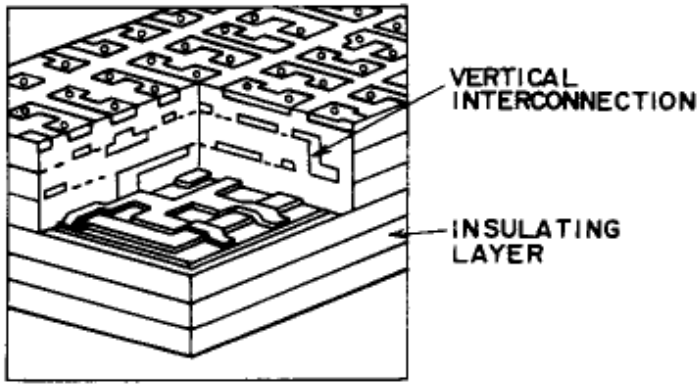


Figure 12. Wirelength distribution for three-dimensional and two-dimensional architectures.

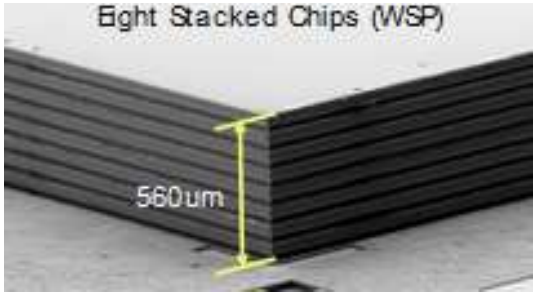
D. Stroobandt, "Recent advances in system-level interconnect prediction," *IEEE Circuits and Systems*, **11**, pp3-20, (2000).

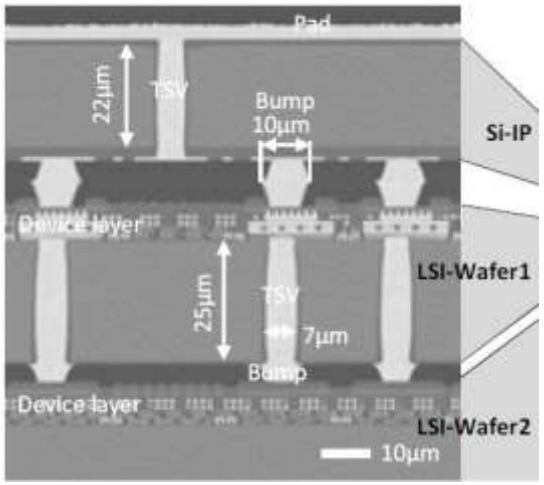
Predominately “3DIC” = TSVs



Y. Akasaka, “Three-Dimensional IC Trends,” Proc. IEEE, 74, pp1703-1714, (1986)

DARPA MTO
3D-ICs Portfolio

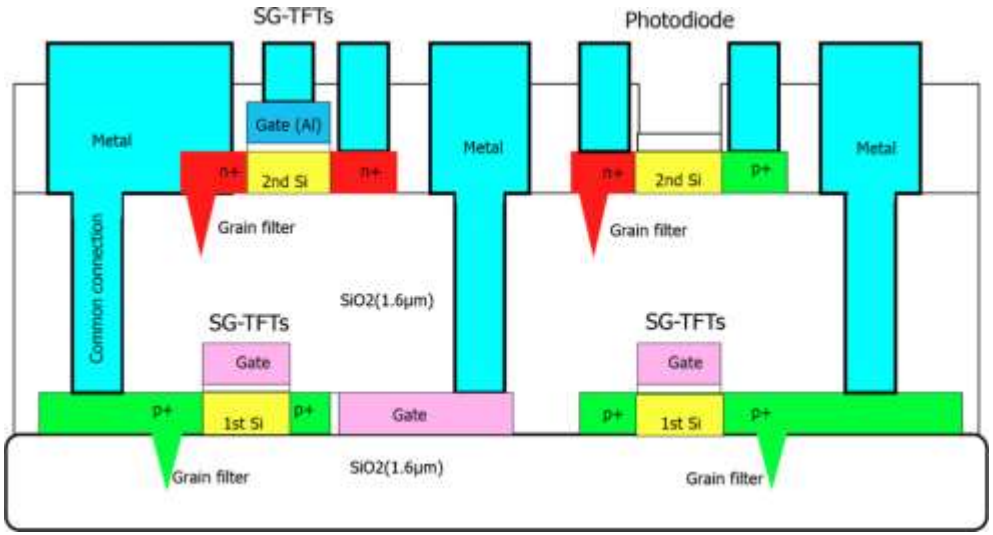


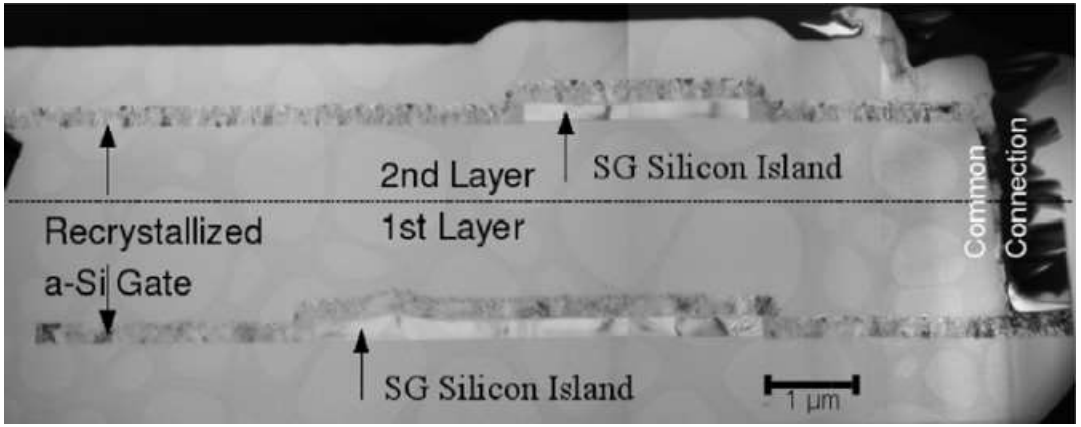


Solid State Technology

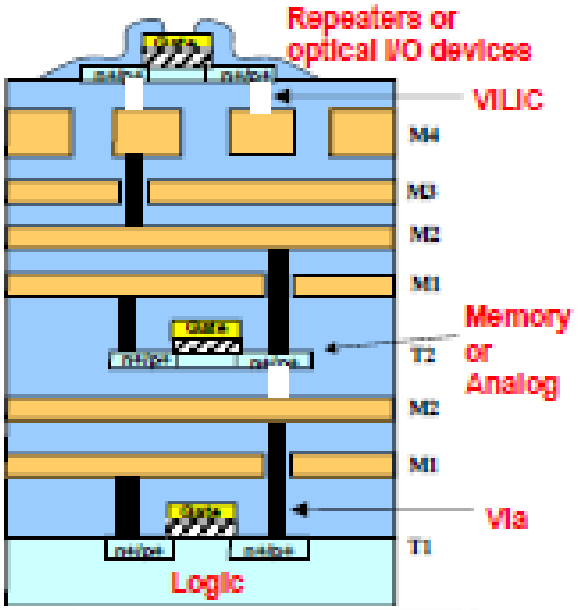
IFTLE 176 2013 IEDM; Micron, TSMC, Tohoku Univ., NC State, ASET

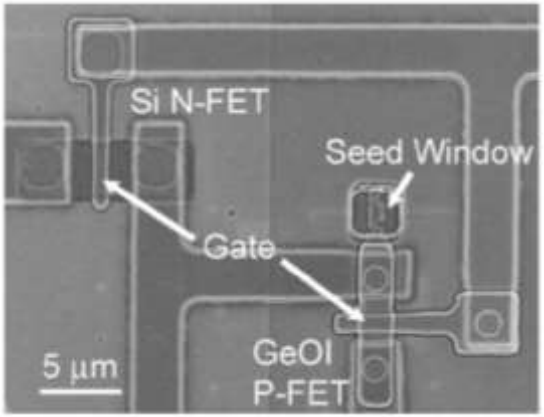
Monolithic 3D-ICs





Ishihara et. al., "Monolithic 3D-ICs with single grain Si thin film transistors," Solid State Electronics, 71, pp. 80-87, (2012).

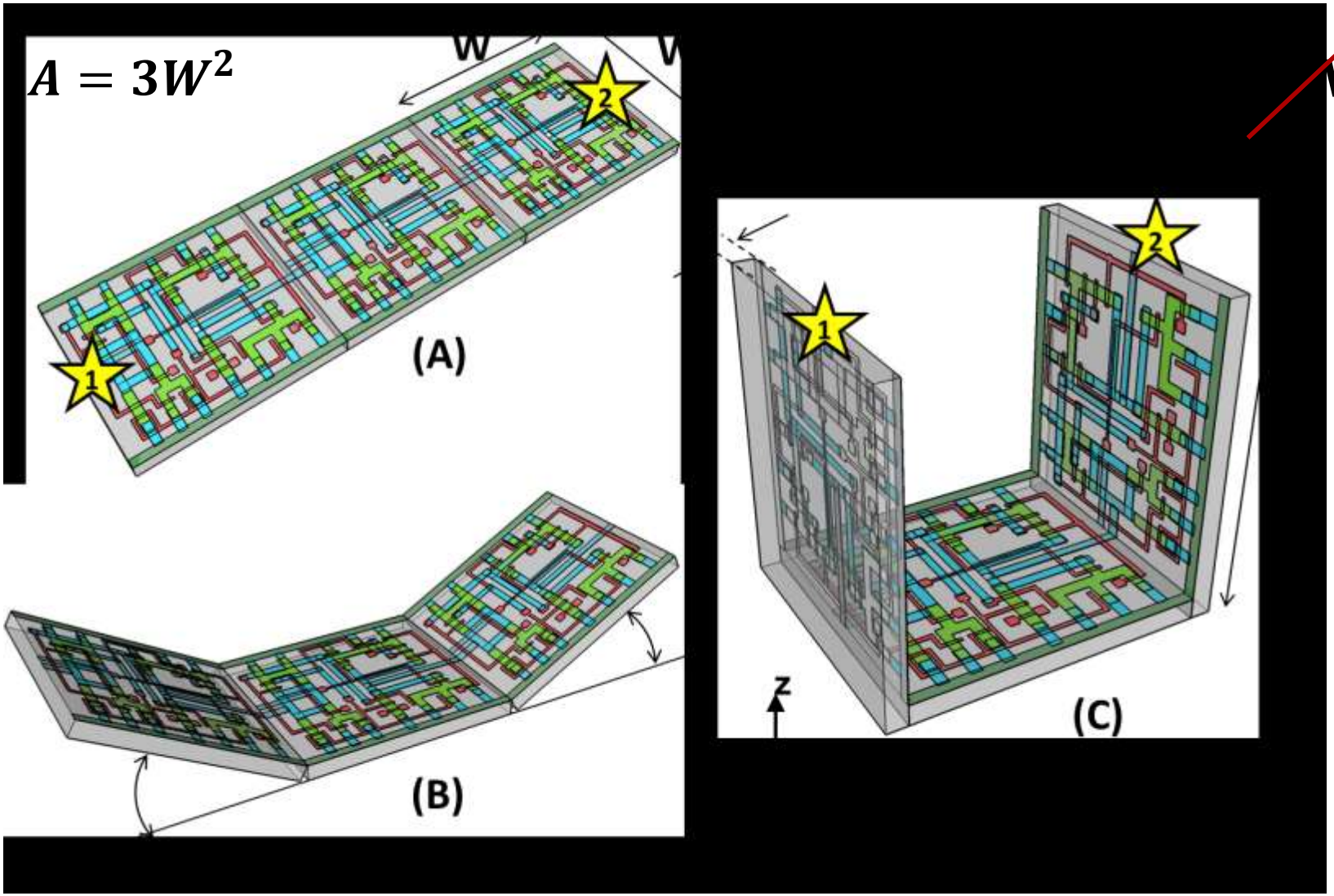




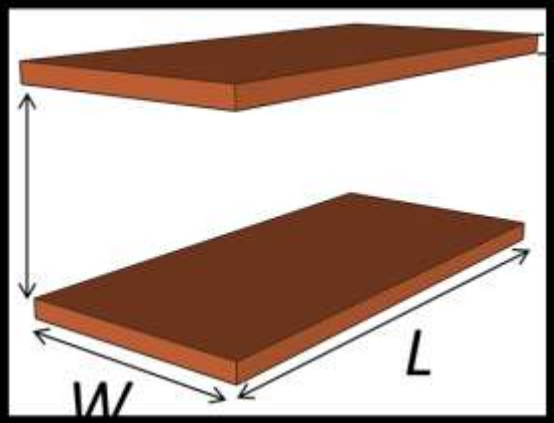
Wong et. al., "Monolithic 3D Integrated Circuits," IEEE VLSI TSA, 1-4244-0585-8/07, (2012).

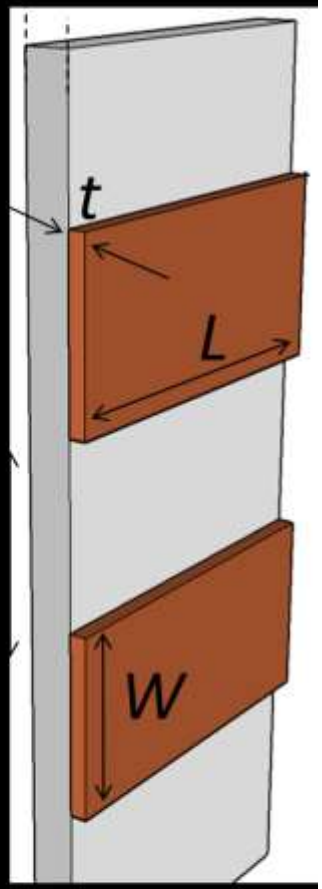
Device Level 3D-ICs

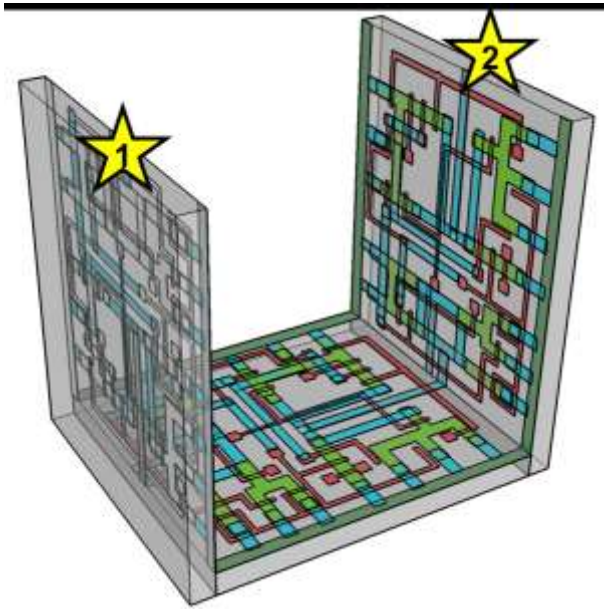
3D-ICs by Folding Space



Spatial DOF Routes to Reduced Capacitance

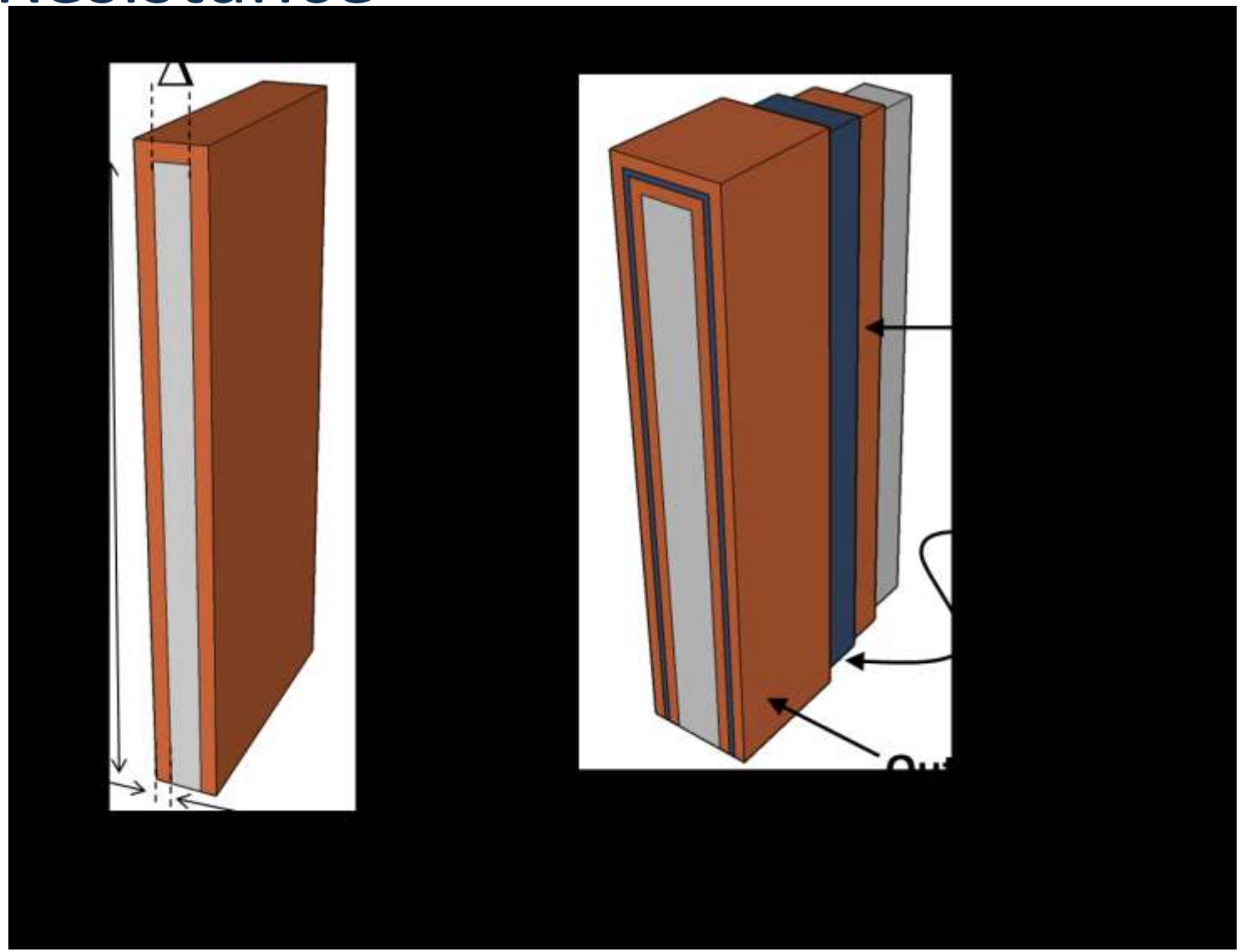




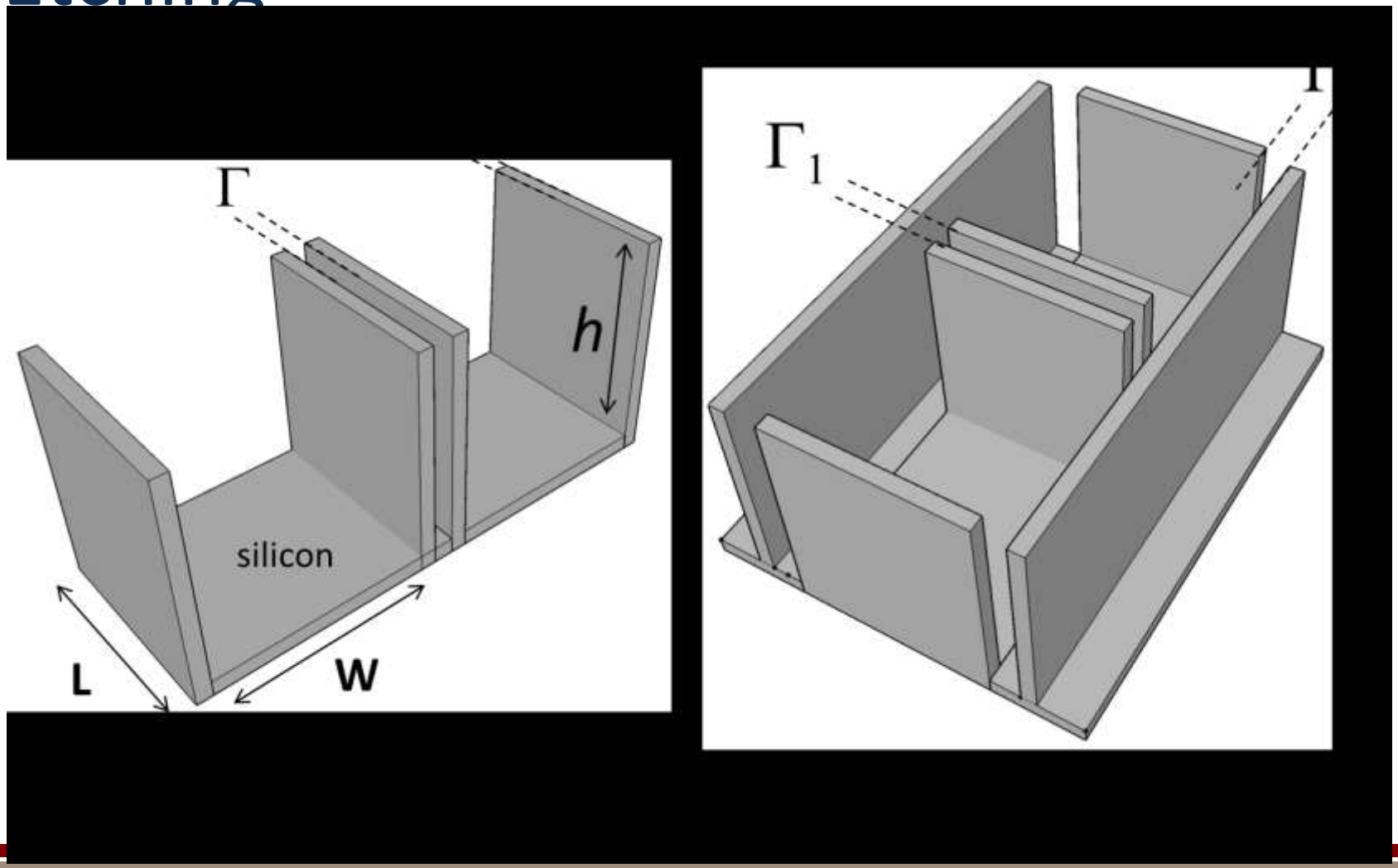


An interconnect connecting 1-2 is *W* away from the traces on the floor and has negligible overlap with traces on the side wall.

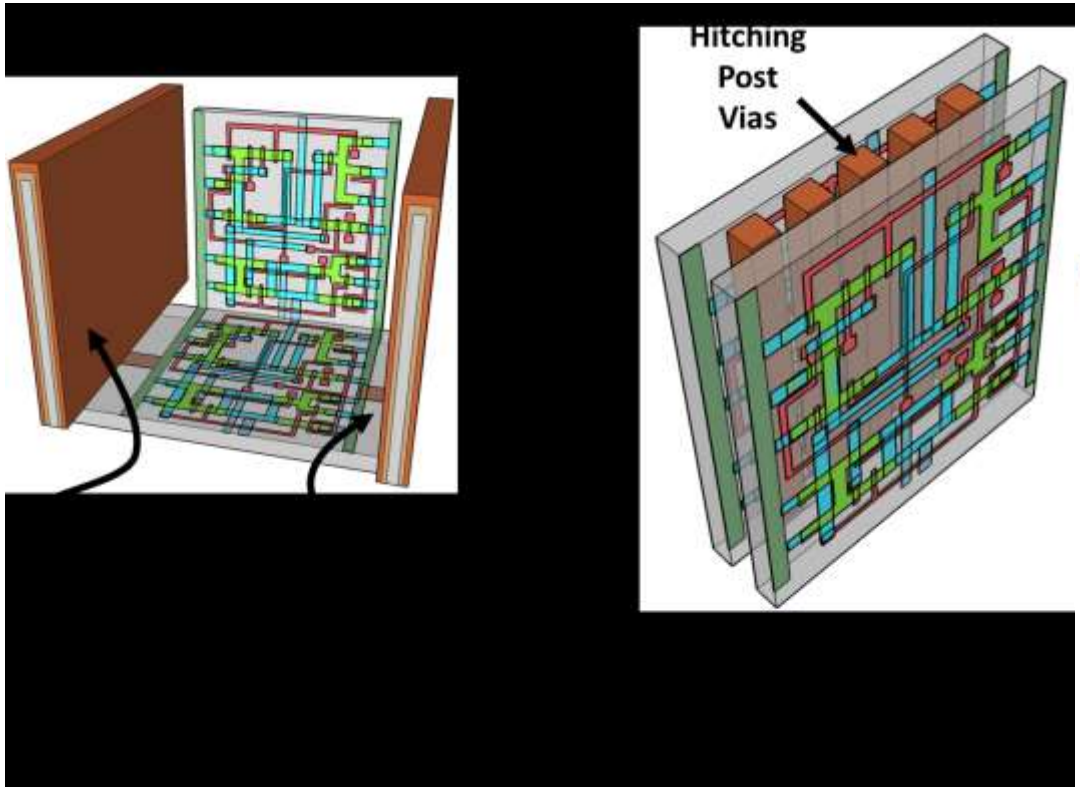
Spatial DOF Routes to Reduced Resistance

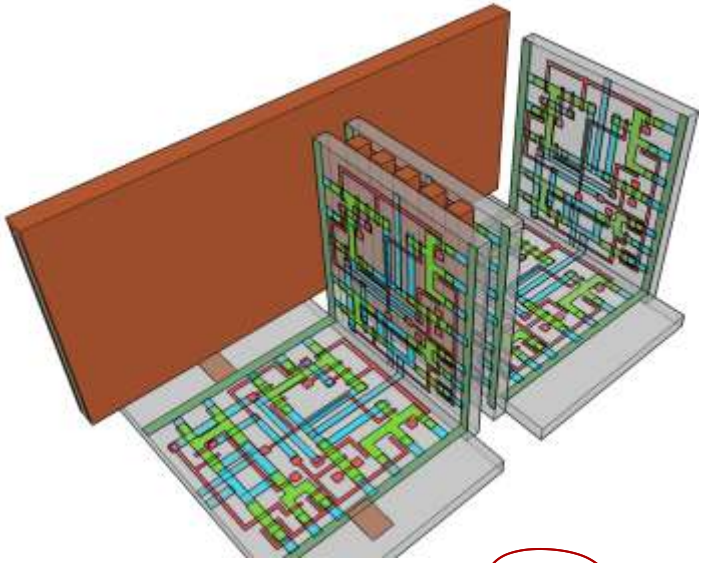


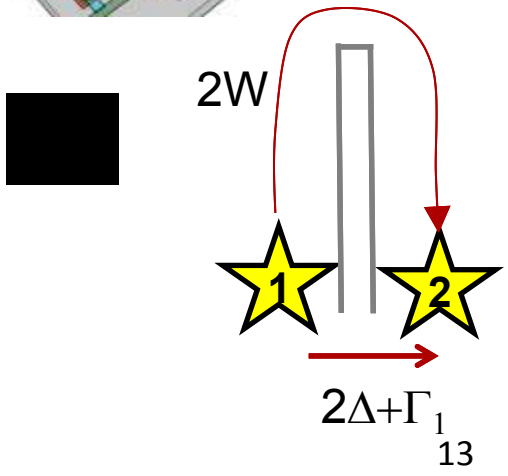
Manufacturable Route to 3D-ICs in a Folded Space: High Aspect Ratio Si Etching



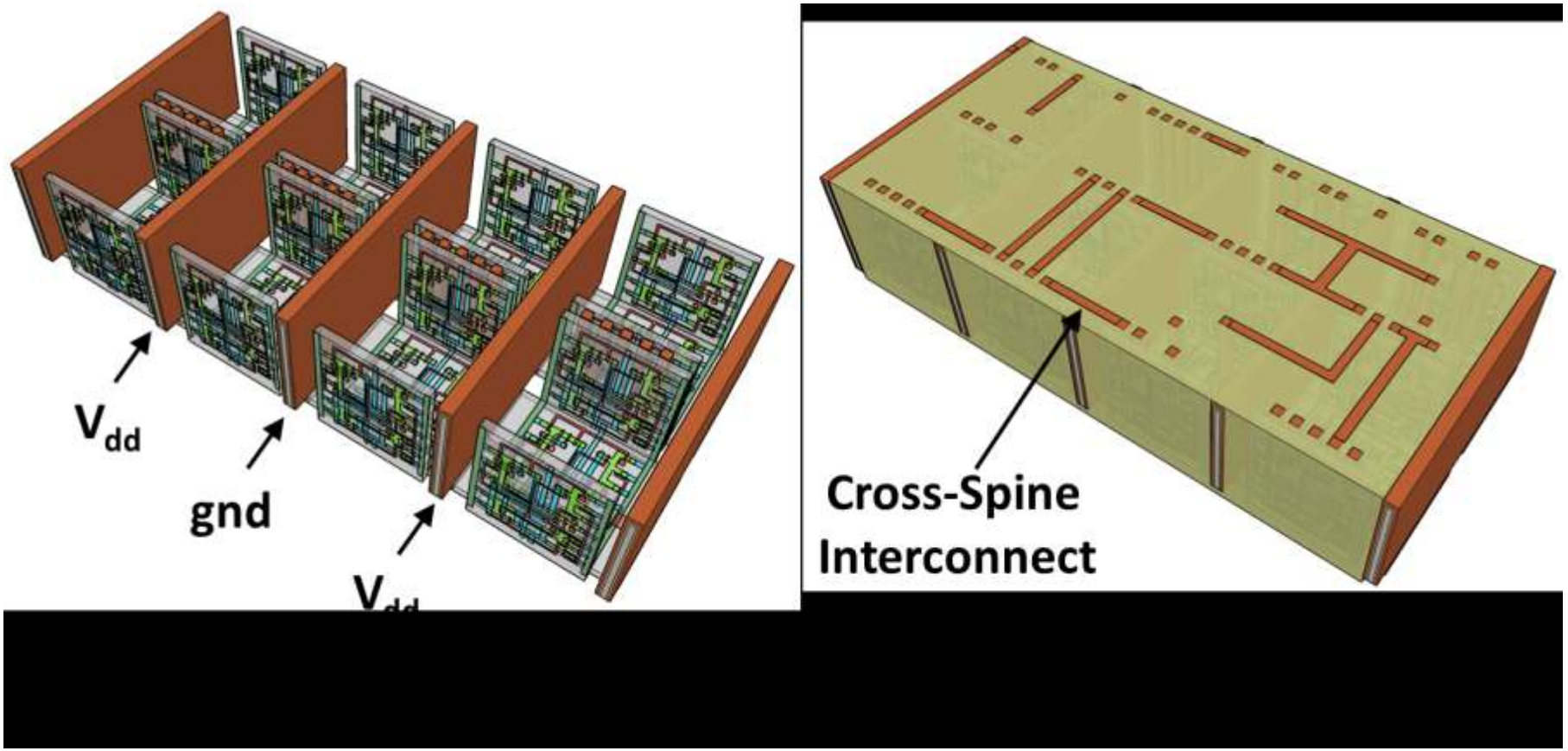
Device Level 3D-ICs with Local Interconnects







Device Level 3D-ICs with Regional Interconnects



After device level patterning – standard BEOL planarization and interconnects are possible

Device Level 3D-IC Fabrication

Required Processing Steps

Blanket Processes

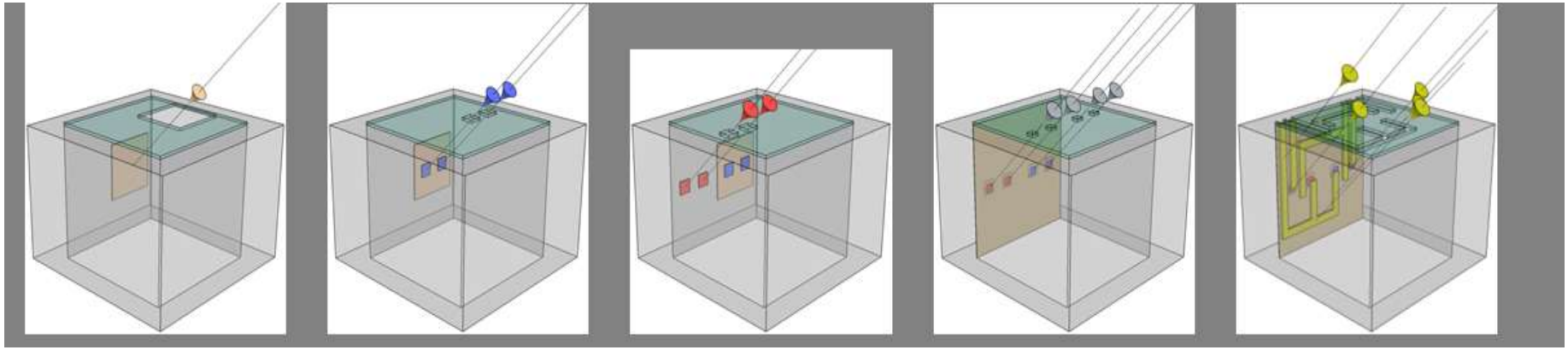
Oxidation, CVD, ALD, anneal

+

Directional Processes

Implantation, Deposition, Plasma Etch

Long Channel Metal Gate CMOS



Well Implant

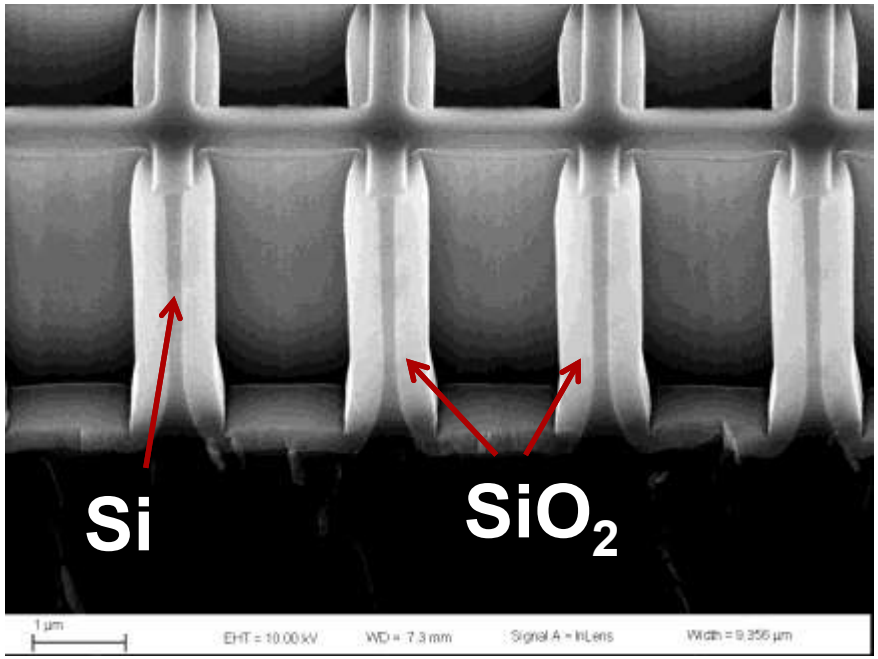
PMOS Source/Drain Implant

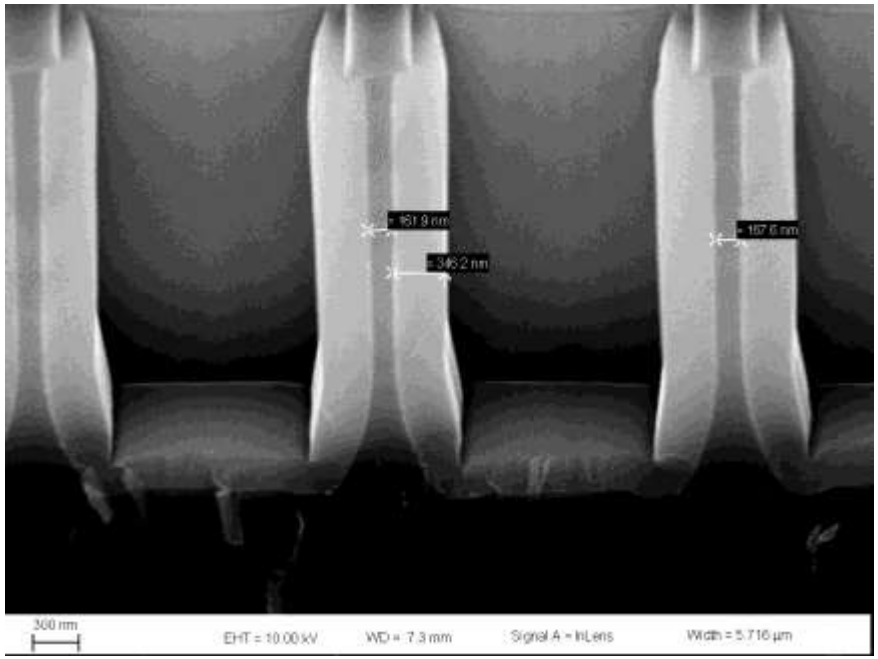
NMOS Source/Drain Implant

Contact Cuts

Metal 1 Deposition

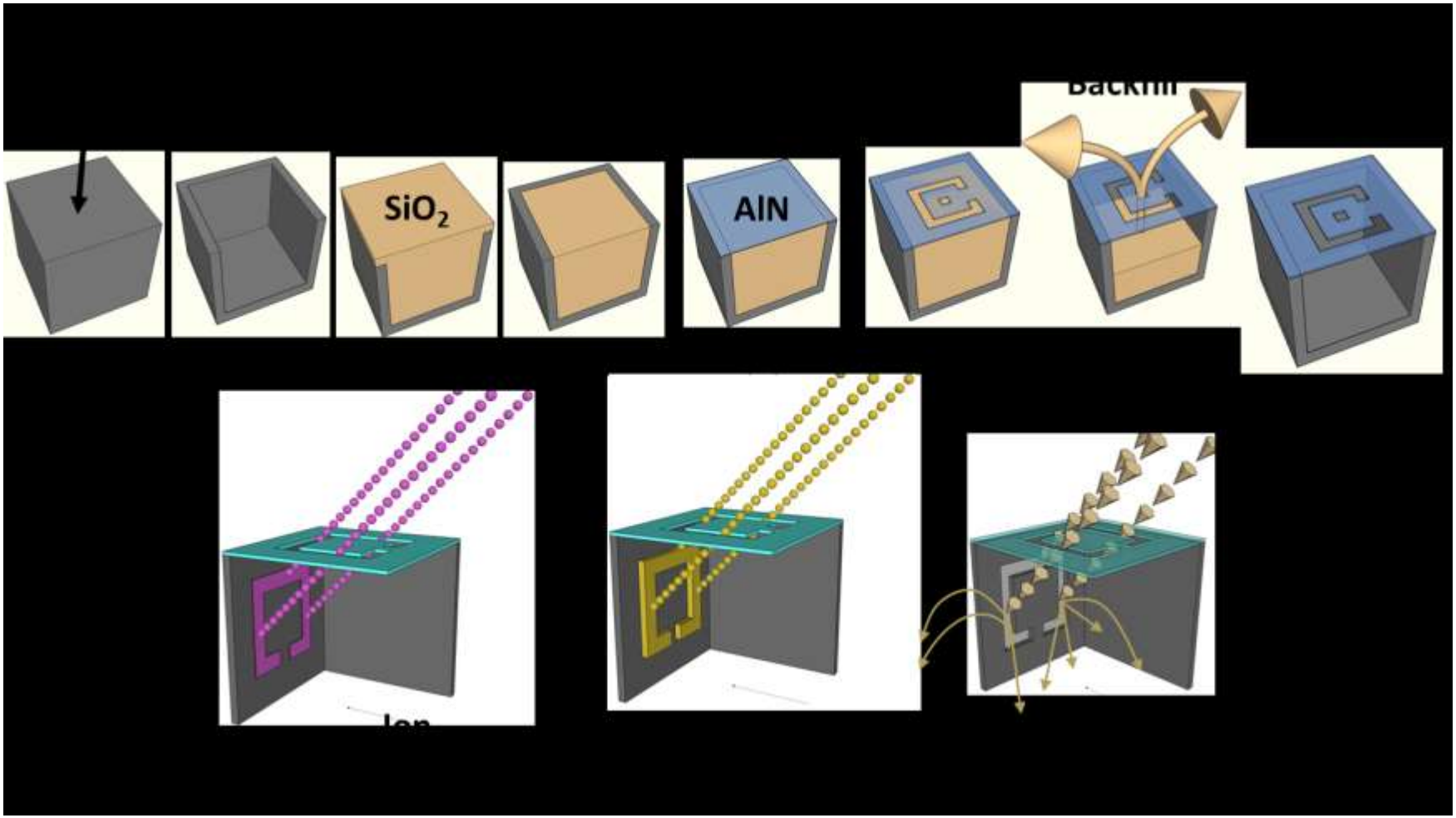
Blanket Processes - Oxidation





Prospects for HVM: Conformal oxidation, CVD deposition and ALD deposition have all been demonstrated and present no issues for HVM processing.

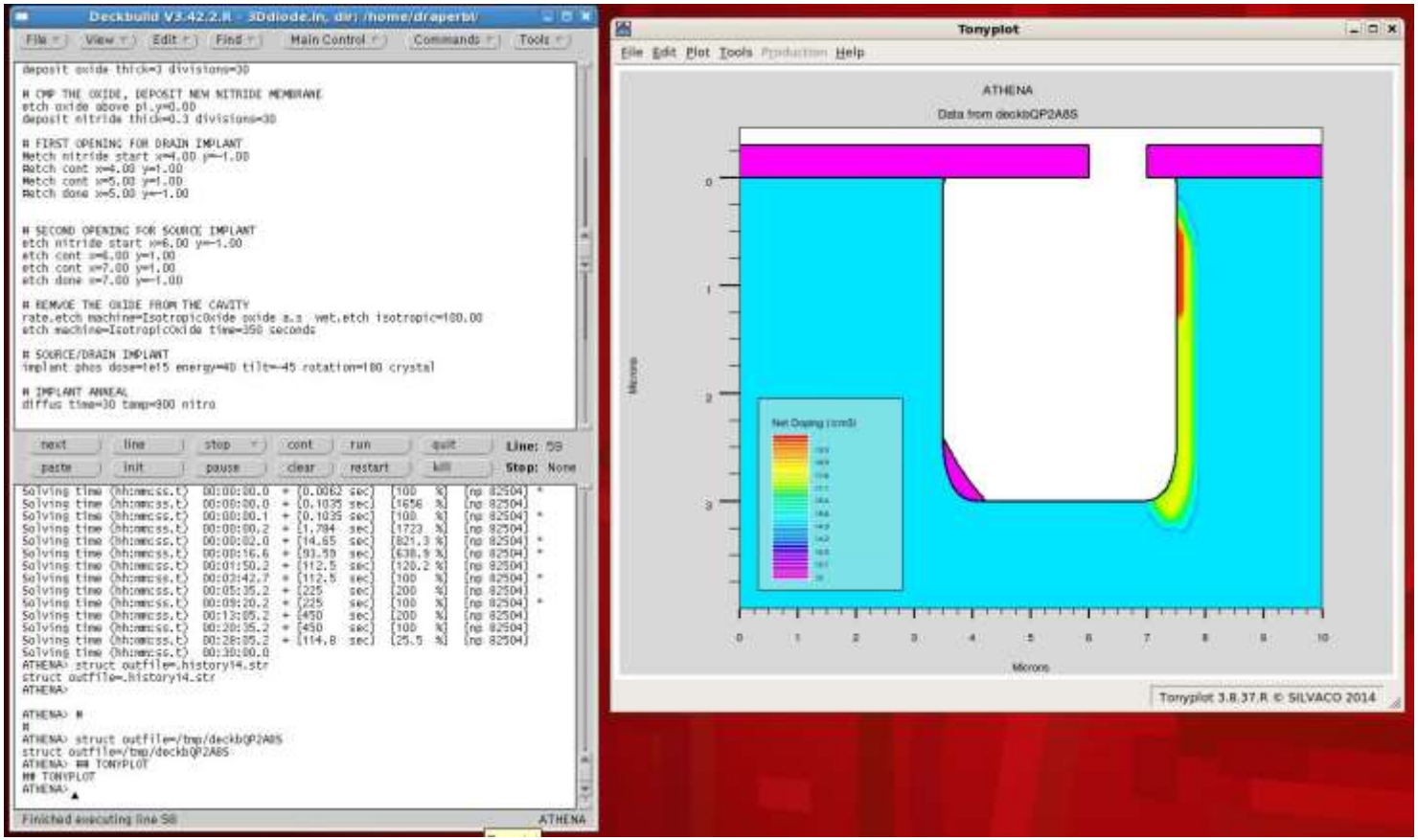
Oblique Processing Flow



Prospects for HVM:

1.) All lithography occurs on a CMP-flat surface, so this approach is compatible with high NA immersion lithography
2.) Steps (C)-(G) required for each patterning step (but SAQP is no picnic either)

Oblique Implantation

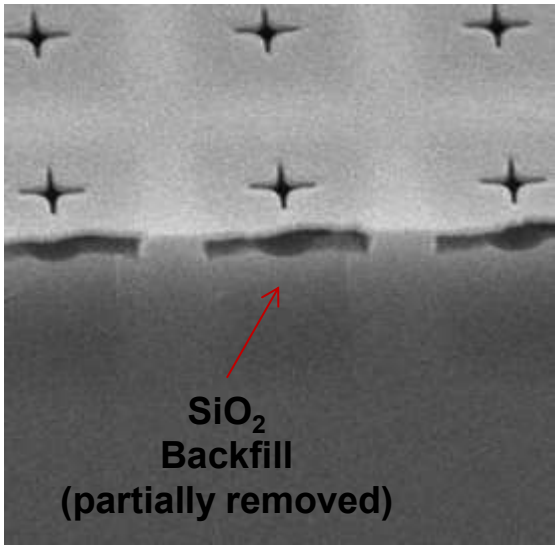


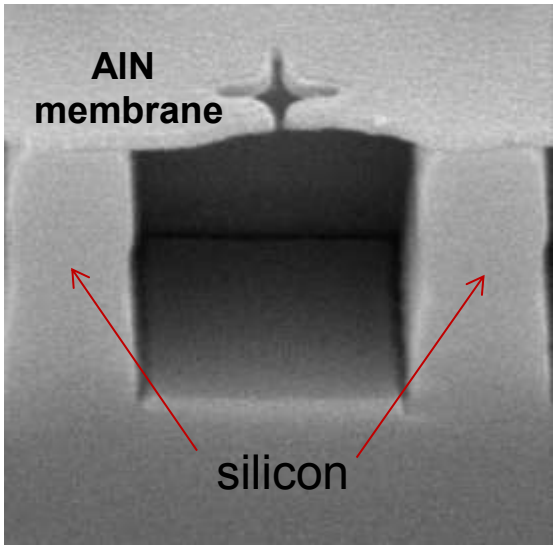
Prospects for HVM:

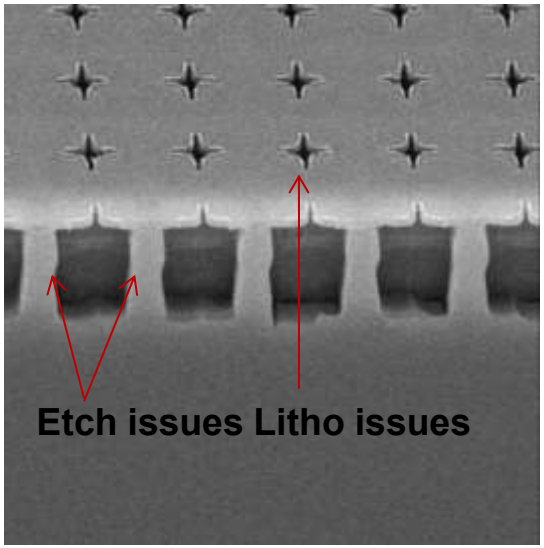
1.) Modern ion implant tools already perform angled halo implants in HVM.

2.) Selection of proper membrane can provide improved stopping power.

Backfill and Evacuation

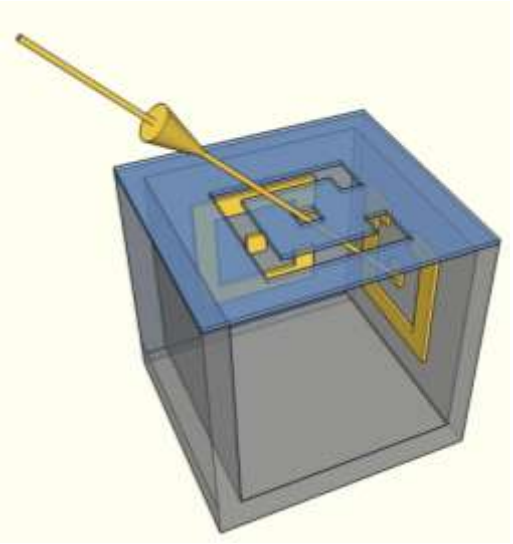


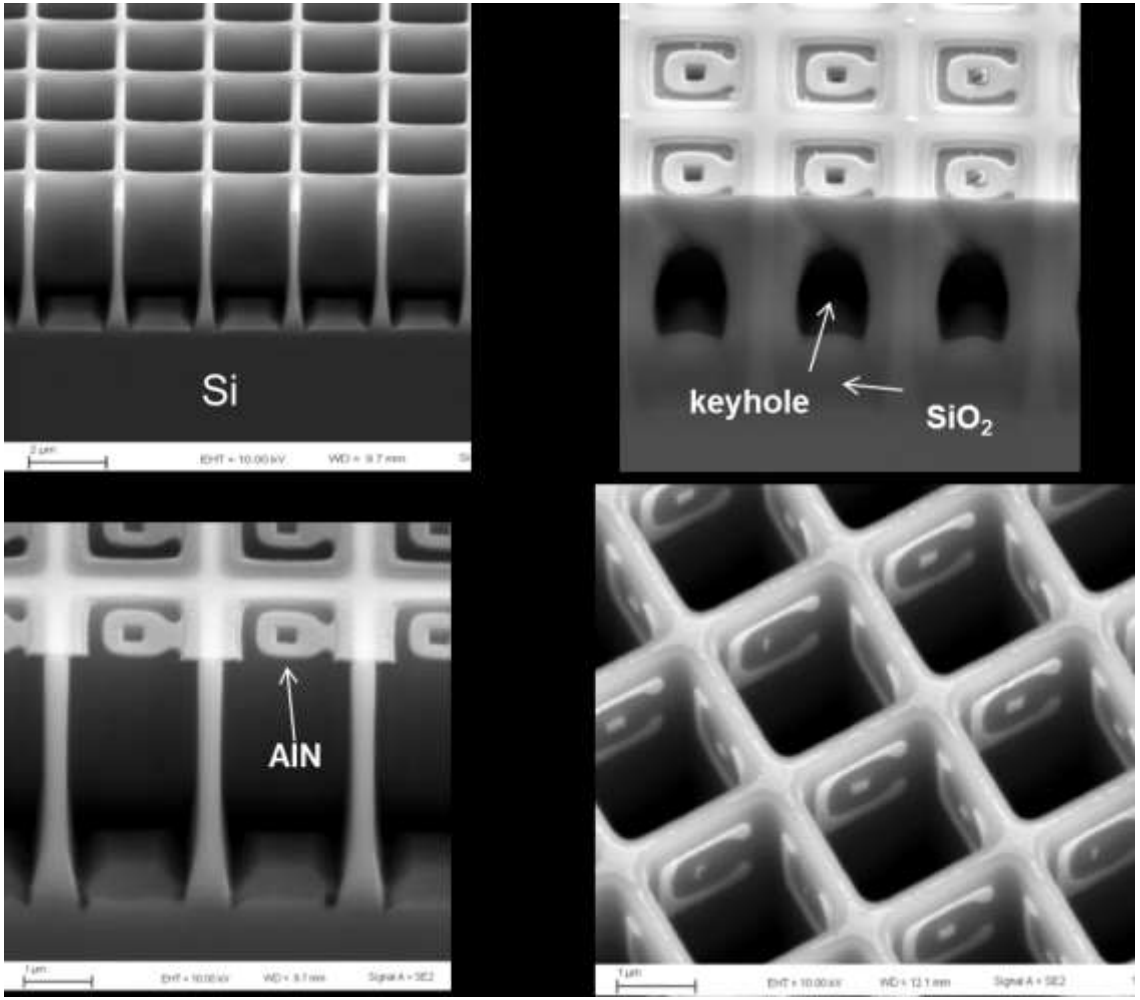




Backfill Material	Membrane Material
SiO_2 (CVD - inorganic)	AlN
Polysilicon (CVD – inorganic)	Si_3N_4
Polyimide (spin applied - organic)	Photoresist
	W, Al

Oblique Deposition

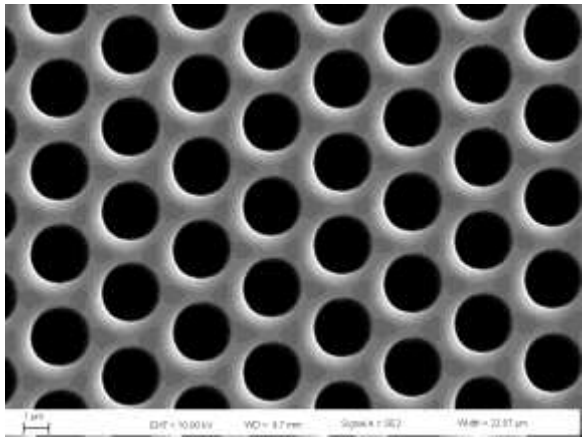


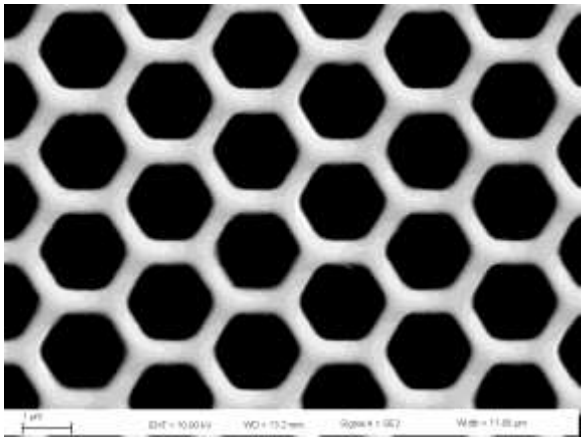


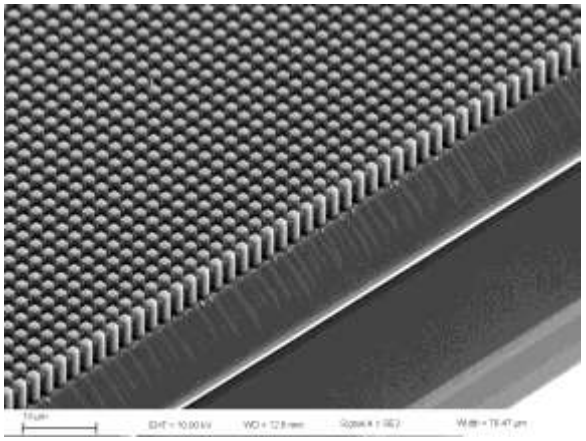
Prospects for HVM:

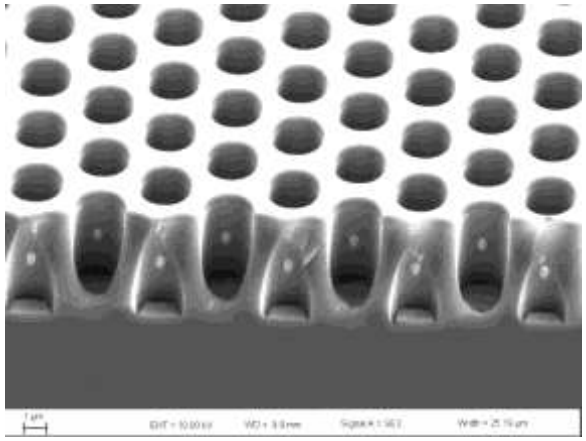
1.) Only an angled fixture required
2.) Inherently a liftoff process
3.) Flux homogenization may be necessary (no rotation)

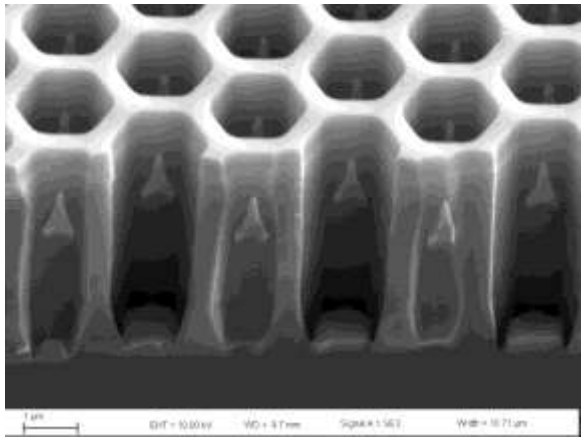
Oblique Deposition

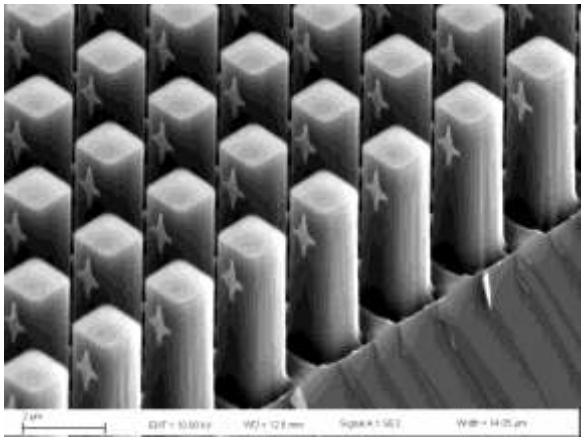




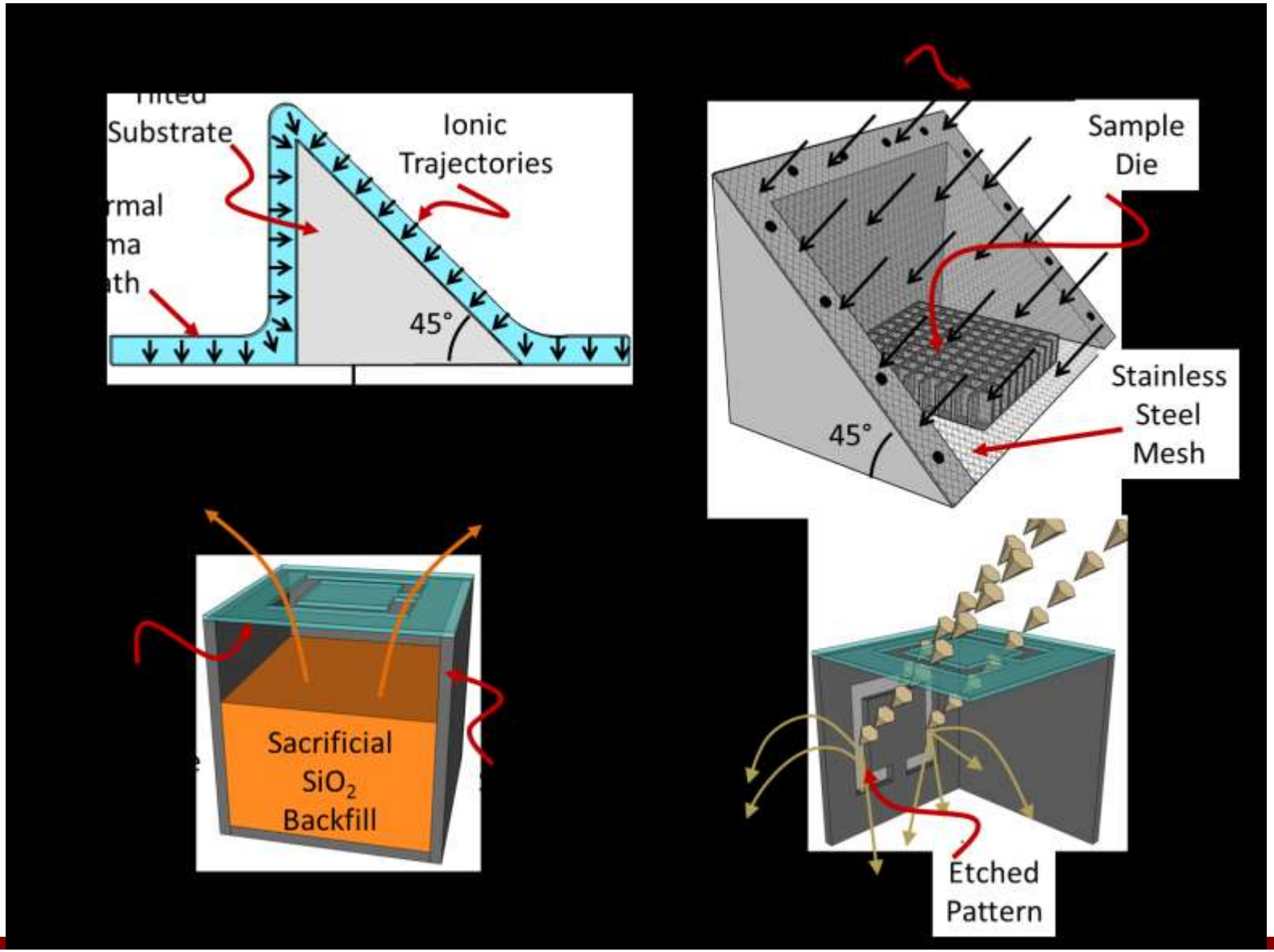




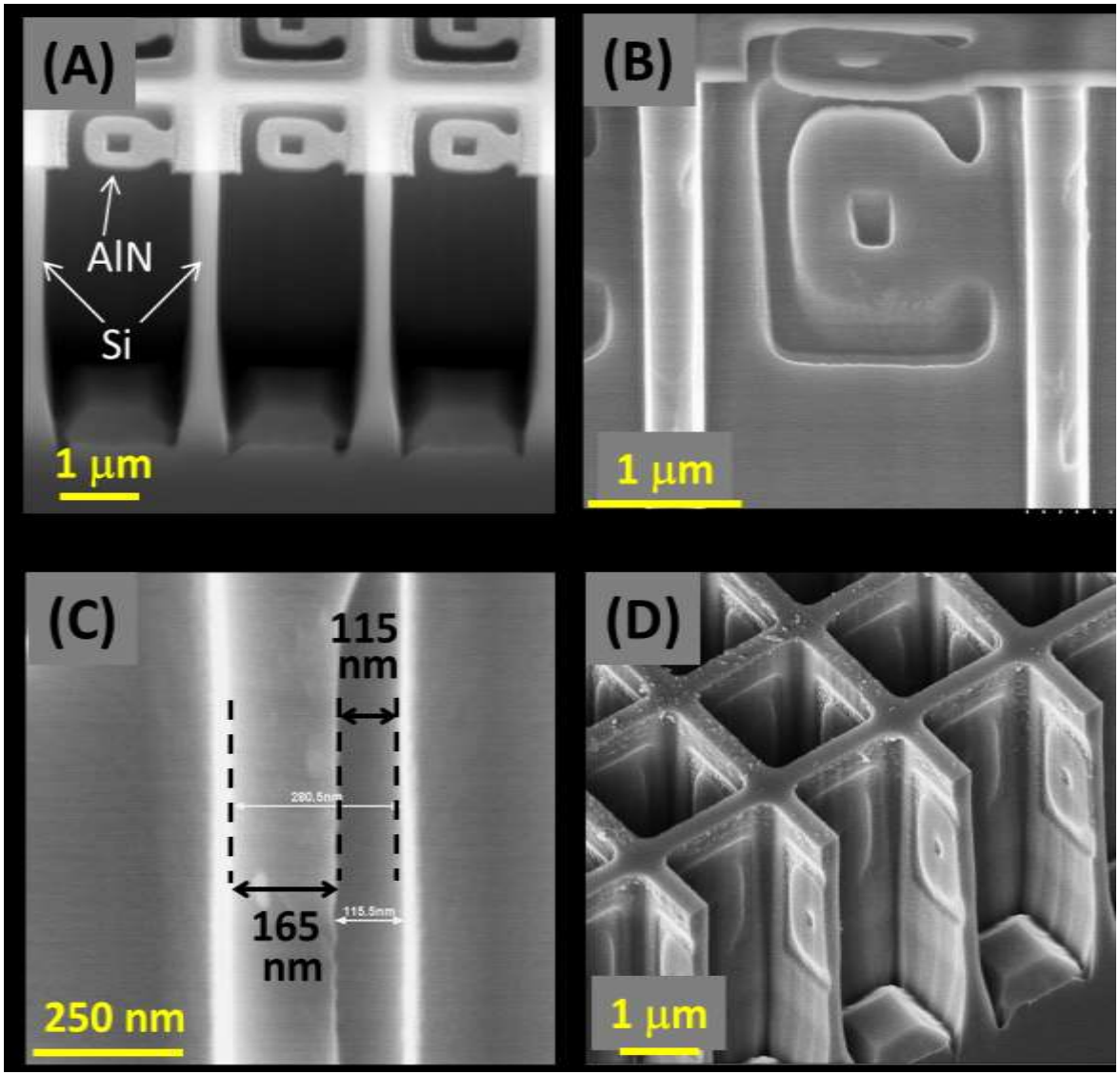




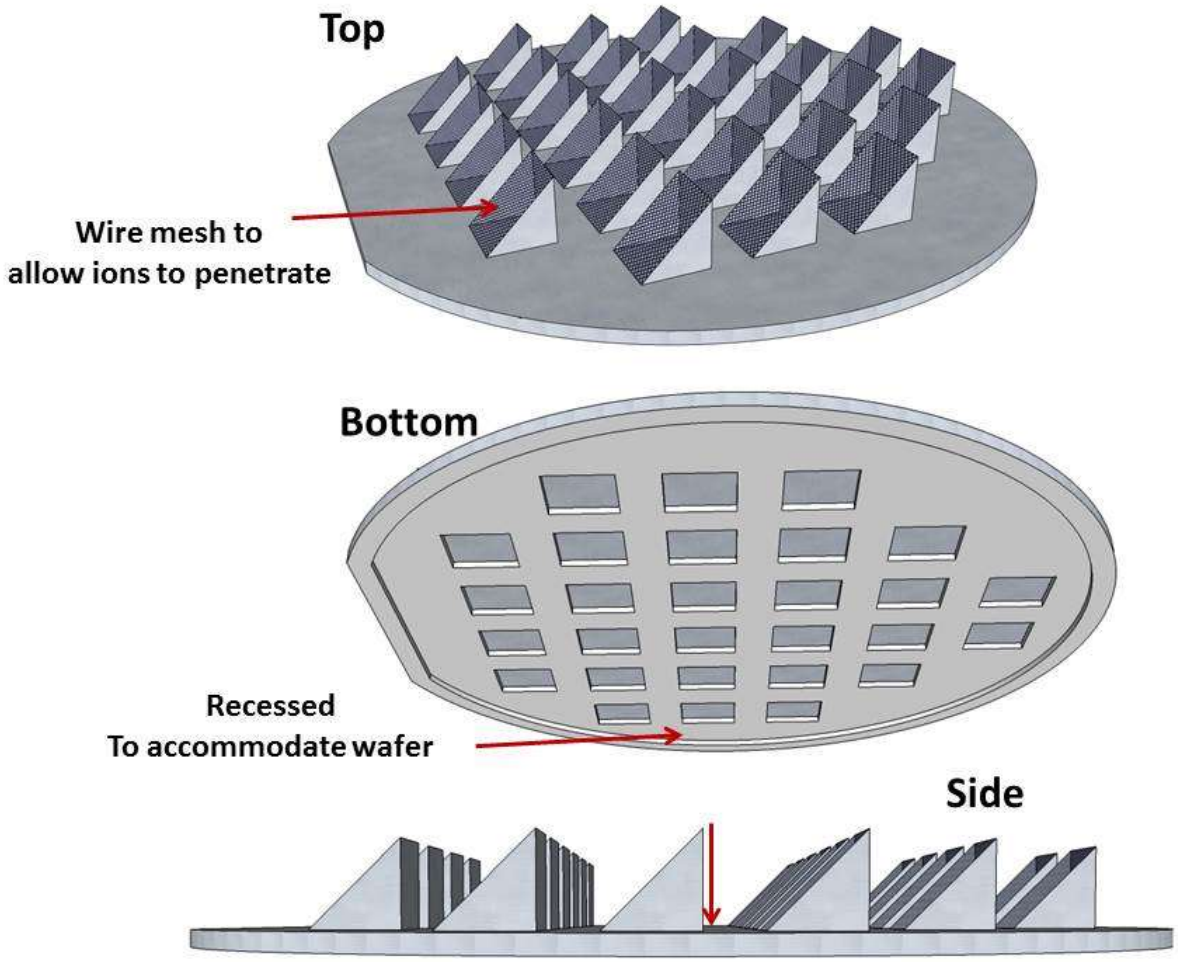
Oblique Plasma Etching



Oblique Plasma Etching



Die-Level Faraday Cage Clamp Ring



Prospects for HVM: **1.) Die-level Faraday cage clamp ring converts current ICP to oblique processing equipment.**

Prospects

- This approach is crazy – but so is considering graphene, CNTs, non- Von Neumann computing, etc.
- Quantitative measurement of resolution for dep, implant and etch is still required.
- Impact of non-<100> silicon surfaces.
- Strategies are required for layout, placement and routing, alignment, isolation, strain, planarization, in-line testing etc.
- Use of familiar materials, current toolsets and 60+ years of insight are un-matched for alternative approaches.
- This approach does not preclude engagement of either TSV-centric or monolithic 3D IC approaches.

Acknowledgements

Paul Davids, Paul Resnick, Bruce Draper,
Patrick Finnegan, Robert Jarecki, David Henry

Questions?

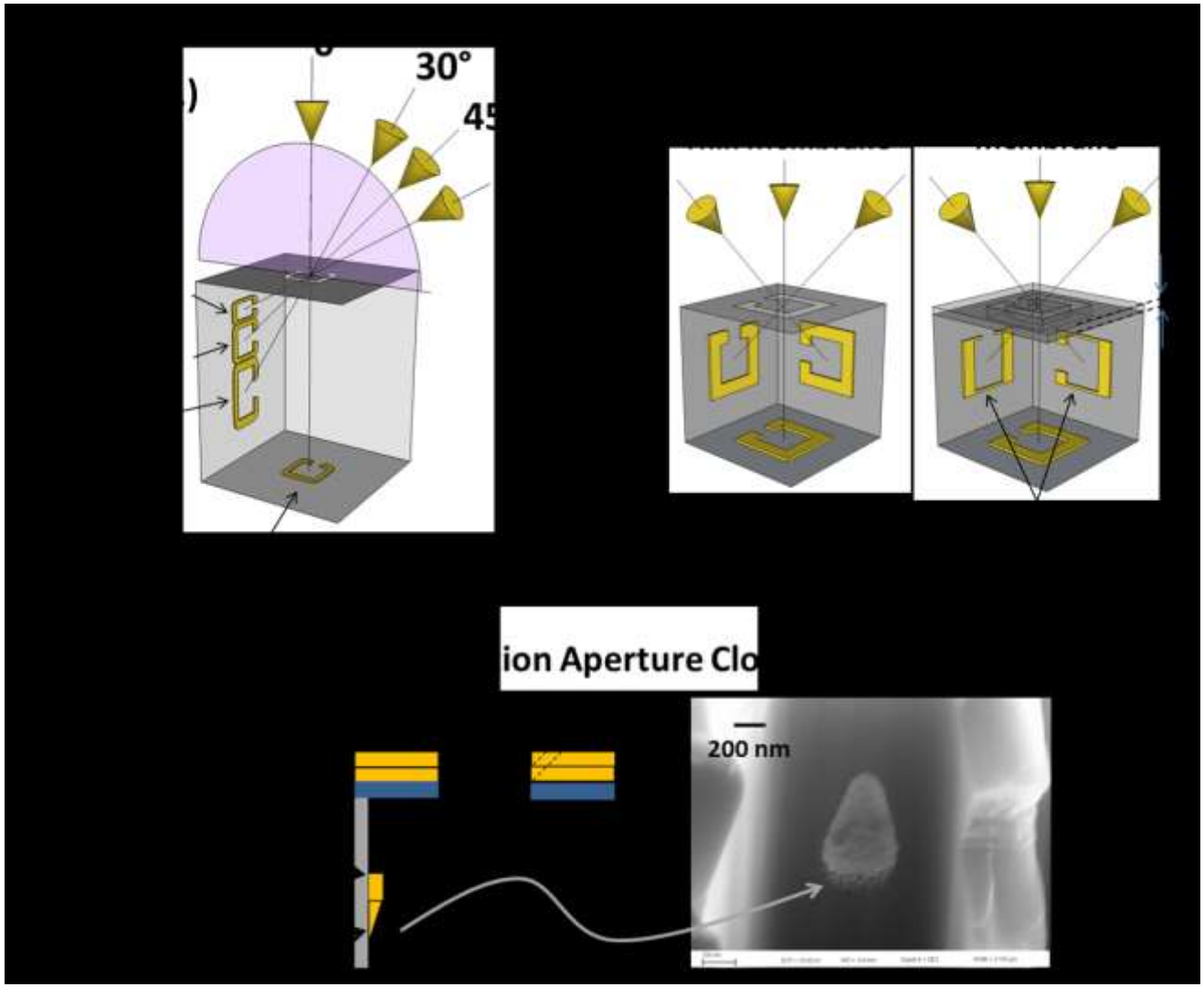
dbburck@sandia.gov

Notes from a Plenary

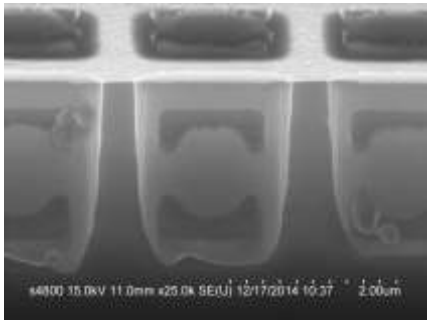
Greg Yeric "Moore's Law at 50: Are we planning for retirement?" – IEDM 2015

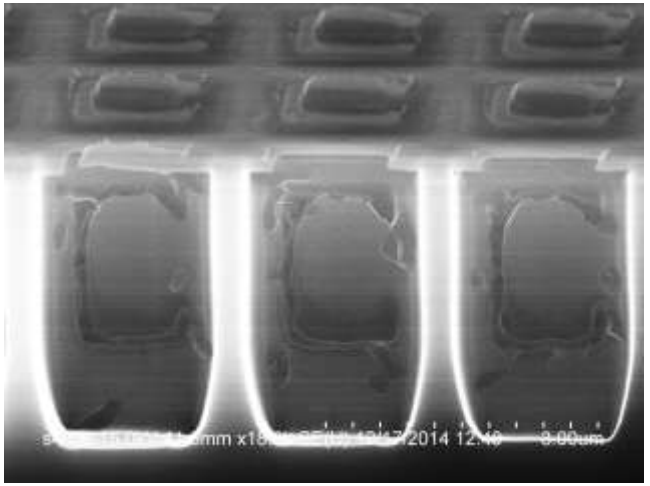
- "The scaling roadmap for the next 10 years is truly complex, and it is possible to foresee significant sacrifices in density for the sake of scheduling"
- "the achievable transistor density has eroded, even as we have added significant wafer cost with new Middle of Line (MOL) layers."
- "Breakthroughs in wire parasitics would be some of the most impactful to Power/Performance/Area scaling."
- "This level of circuit impact increases the need for investment in the metal stack aimed not just at pitch scaling but also at improving RC."
- "From at least the 45 nm node, we can create smaller logic blocks using gate pitches larger than nominal, owing to the combined effects of parasitics, strain, and lithography limitations."

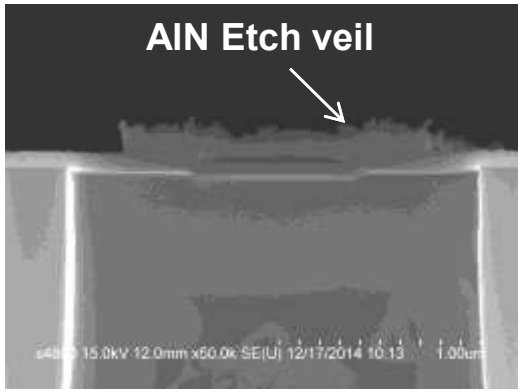
Sources of MPL Distortion

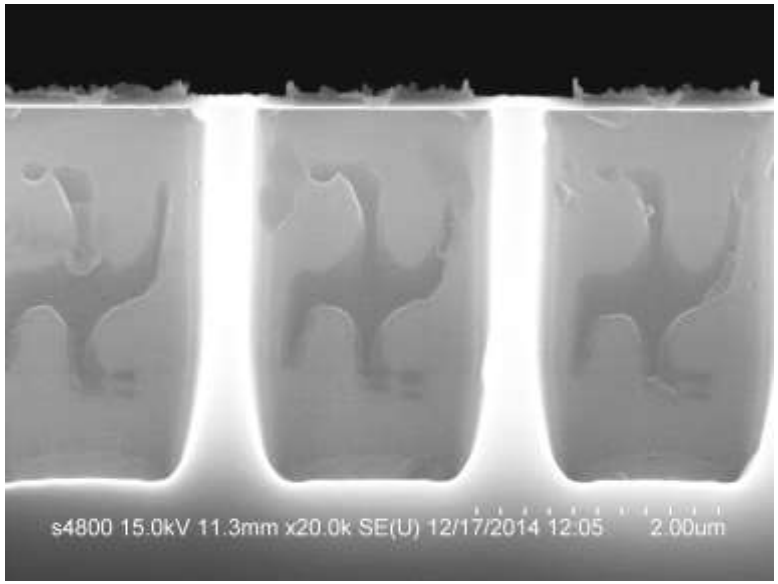


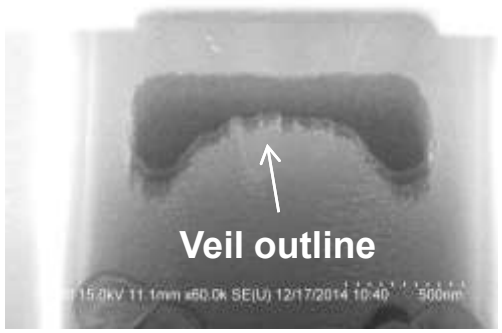
Example SEMs of vertical patterned etches











Wafer-level Faraday Cage Clamp Ring