Final Report for DOE/EERE

DE-FOA-0001018: Solar Manufacturing Technology 2 (SOLARMAT 2)

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12/6/2016

Signature Date

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EXECUTIVE SUMMARY

For photovoltaic (PV) manufacturing to thrive in the U.S., there must be an innovative core to the technology. Project Automate builds on 1366's proprietary Direct Wafer® kerfless wafer technology and aims to unlock the cost and efficiency advantages of thin kerfless wafers. Direct Wafer is an innovative, U.S.-friendly (efficient, low-labor content) manufacturing process that addresses the main cost barrier limiting silicon PV cost-reductions – the 35-year-old grand challenge of manufacturing quality wafers (40% of the cost of modules) without the cost and waste of sawing. This simple, scalable process will allow 1366 to manufacture "drop-in" replacement wafers for the $10 billion silicon PV wafer market at 50% of the cost, 60% of the capital, and 30% of the electricity of conventional casting and sawing manufacturing processes.

This SolarMat project developed the Direct Wafer processes' unique capability to tailor the shape of wafers to simultaneously make thinner AND stronger wafers (with lower silicon usage) that enable high-efficiency cell architectures. By producing wafers with a unique target geometry including a thick border (which determines handling characteristics) and thin interior regions (which control light capture and electron transport and therefore determine efficiency), 1366 can simultaneously improve quality and lower cost (using less silicon).

As a result of this SolarMat project, 1366 achieved the following:

- Successfully developed methods of controlling local thickness of Direct Wafer, enabling framed wafers with strong edges and thin interior regions.
- Developed measurement methods for verifying target geometry was met.
- Demonstrated the benefits of thin, framed wafers for improved handling through cell processing.
- Fabricated cells using thin Direct Wafer product with framed borders to demonstrate efficiency potential.
- Incorporated thin, framed wafers into mini-modules to validate performance of target geometries through soldering, lamination, and accelerated testing including thermal cycling.

COMPARISON OF PROPOSED VERSUS ACTUAL PROJECT GOALS

The following table summarizes the project's proposed goals versus actual progress for each task. There were no deviations between initial negotiated deliverables / milestones and actual milestones achieved.

Task #	Task and Milestone Description	Actual Deliverable / Milestone	Completed
1.1	*Modeling Mechanical: FEM Report simulating stresses for uniform thickness compared to thin wafer with thick frame*	*Report submitted to DOE demonstrating projected benefits*	Q2-2015
2.1	*Measurement Method 1: Quantify edge thickness of thin wafer with thick border*	*Vision system with cameras and custom lighting tested and implemented on furnace.*	Q2-2015
2.2	*Measurement Method 2: Measure thickness step changes with spatial resolution <0.5mm*	*Laser based displacement sensors adapted for use on shiny as-grown wafer surfaces.*	Q2-2015
2.3	*Grow framed wafers and demonstrate total average thickness <80% of average edge thickness*	*First achieved in August with average thickness by mass of 160um compared to 240um edge thickness*	Q3-2015
2.4	*Improve thickness control in thin region with TTV less than half average total thickness*	*Demonstrated target TTV on wafers with <140um average thickness in wafer interior region*	Q1-2016
3.1	*Modeling Electrical: quantify how efficiency will depend on wafer thickness based on thickness, doping, bulk lifetime and cell architecture*	*PC2D model used to model BSF, PERC and IBC cell structures summarized in Q3 report.*	Q3-2015
3.2	*Wafer handling: Process thin wafers with frames through cell processing and demonstrate breakage rate <5%*	*Thin wafers with frames processed through BSF cell line at 1366 with breakage rate below target.*	Q1-2016
3.3	*Modeling validation: Electrical performance tested to match predictions from 3.1 for select architectures*	*Efficiency with industrial PERC processing validated within 5% of prediction down to thickness of 130 um.*	Q2-2016
4.1	*Single cell modules: Test tabbing and lamination of thin wafers with frames to determine if busbar thickening is necessary, check by EL for cracks*	*10 cells encapsulated into mini-modules without cracks*	Q4-2015
4.2	*Stringing cells: Test with mini-modules of 9+cells including thermal cycling*	*3 mini-modules produced and tested. 90-125um central thickness showed no cracking after TC50.*	Q1-2016
4.3	*Hot spot analysis: Testing for partial module shading by measuring temp <150C for 60sec at -12V or 8A*	*50 cells measured for hot spots at -12V. Typical max temps below 60°C.*	Q2-2016

PROJECT OBJECTIVE

Task 1.0: Define Target Geometry

The ability to locally control wafer thickness introduced many possibilities for target geometry, and this task studied the impact of different options on mechanical strength and subsequent yield through standard manufacturing processes via the use of Finite Element Modeling to simulate the stresses imposed on a wafer at various process steps. Three different stress conditions were evaluated to represent various stresses imposed on wafers during manufacturing processes and for each condition, three different geometries were considered to determine the potential impact of the locally varying thickness.

Edge Stress

The first stress condition looked at a fixed edge load, as may be encountered during automated wafer handling. Figure 1 shows the impact of such a load on a standard uniformly thick wafer of 180 µm thickness (top) and 80 µm thickness (middle), which would likely result in breakage given a common critical breakage stress for silicon wafers of ~100 MPa. Using the concept of locally controlled thickness, a model of a wafer which is 80 µm thick for the bulk of the area, but increases to 180 µm thick at the perimeter was constructed (bottom image). This shows the frame of uniform 180 µm thickness from the wafer perimeter inward 1.5mm. This configuration allows for a maximum stress of only 57 MPa, comparing favorably with the uniform 180 µm thick case having maximum stress of 55 MPa. This is possible because the stress field dissipates before reaching the thin region of the wafer. Here we have a wafer which uses only 58% of the silicon used in the 180 µm wafer and whose thickness is 80 µm for approximately 95% of its normal area.

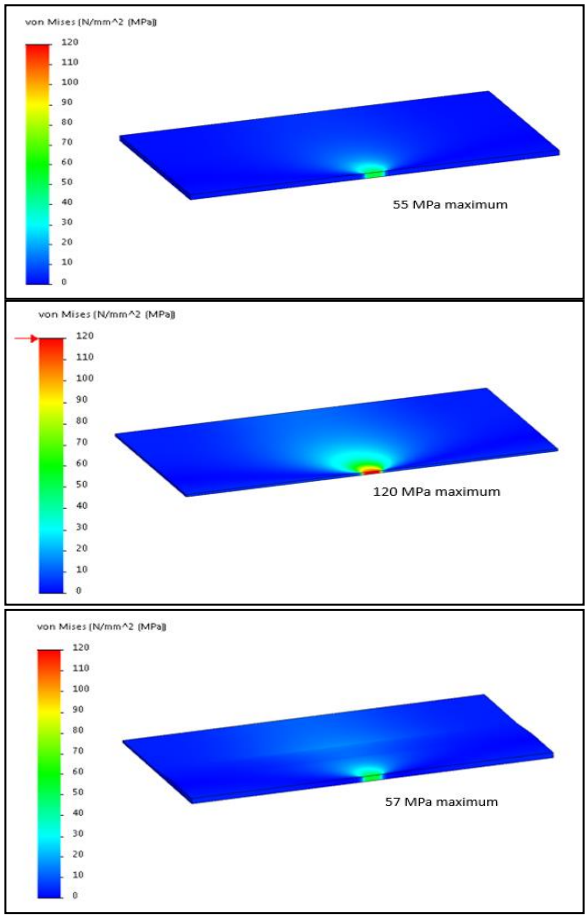


Figure 1: Edge load on 180 µm wafer (top) 80 µm wafer (middle) and 80 µm thick wafer with locally controlled 180 µm thick frame (bottom)

Soldering Stress

A second case of soldering stress is treated in greater detail in the technical report submitted to DOE entitled, “COMPARATIVE ANALYSIS OF PHOTOVOLTAIC WAFERS WITH LOCALLY CONTROLLED THICKNESS”. This accounts for the CTE mismatch between the silicon wafer and the copper ribbon and then considers the

addition of a locally thick region of the wafer directly underneath where the ribbon is soldered to the wafer.

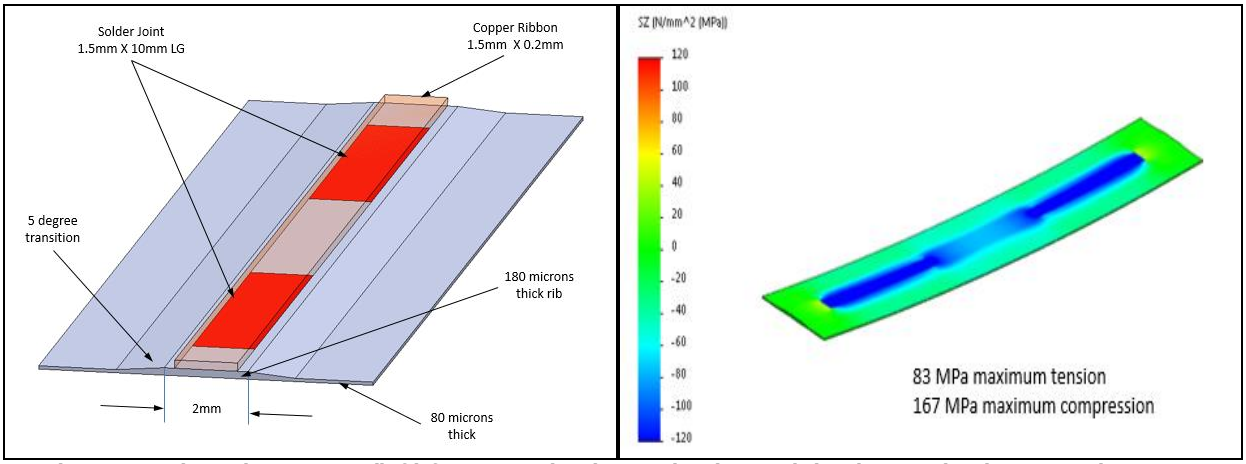


Figure 2: Selected geometry (left) for strengthening region beneath busbar, and subsequent impact on resulting stress field (right).

Stringing Stress

The last stress state considered was the local force imposed from the interconnect ribbon folding over at the edge of a wafer and then forces are exerted during the lamination process. Figure 3 below displays modeling results indicating that when wafer thickness is uniformly reduced to only 80 µm, stress values increase significantly and exceed the critical strength limit. Using the same locally controlled thick frame configuration as was used in the edge-load scenario, breakage problems can be alleviated. Figure 4 shows that the wafer of 80 µm thickness with 180 µm thick frame 1.5 mm wide and a 5º transition angle allows for maximum tensile stress less than half of the value for a uniformly thin wafer.

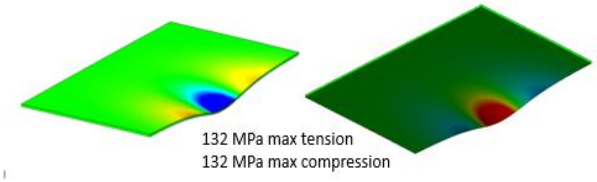


FIGURE 3: STRINGING STRESS ON 80 MICRON WAFER

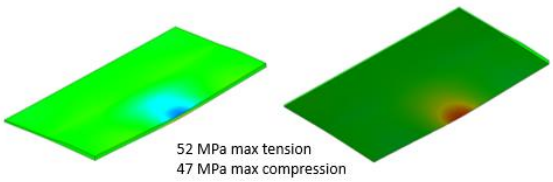


FIGURE 4: STRINGING STRESSON 80 MICRON WAFER LOCALLY CONTROLLED THICKNESS

Additional details can be found in the full report submitted to DOE in fulfillment of this deliverable, entitled “COMPARATIVE ANALYSIS OF PHOTOVOLTAIC WAFERS WITH LOCALLY CONTROLLED THICKNESS”.

Task 2.0 Develop Methods for Obtaining Desired Profile

Subtask 2.1 Measurement Method 1 - Edge thickness:

The current industry-standard method of measuring wafer thickness uses capacitive displacement sensors with a spot size of ~5mm, which are used by 1366 for measuring thickness for interior regions of Direct Wafer product. But these sensors prohibit accurate measurement of thickness of a narrow border because of their large spot size. To achieve this goal, a camera inspection system was developed by 1366, enabling visual inspection of the wafer edges when viewed from the side along with appropriate lighting. Several challenges presented themselves while developing this method. The lighting of the laser cut edge was challenging and several options were evaluated before a custom panel light was developed both for adequate lighting as well as minimizing cost because these will be integrated into each furnace and two systems per furnace are envisioned. In addition to the lighting conditions, appropriate selection of optical lens and aperture was required to match the camera resolution to the field of view to achieve the desired precision and depth of field (to accommodate some variability in the wafer position).

A test stand was developed first, and the image analysis algorithm was developed to confirm the measurements were repeatable and accurately represented the geometry of interest (thickness along the edge). Next, a system with 2 cameras and lighting conditions was mounted to the integrated inspection station of each furnace. A top view is shown in Figure 5, with the wafer visible at the top edge of the image, and it will be transported on the belt down through the image, with the two camera and lighting systems to the left and right sides.

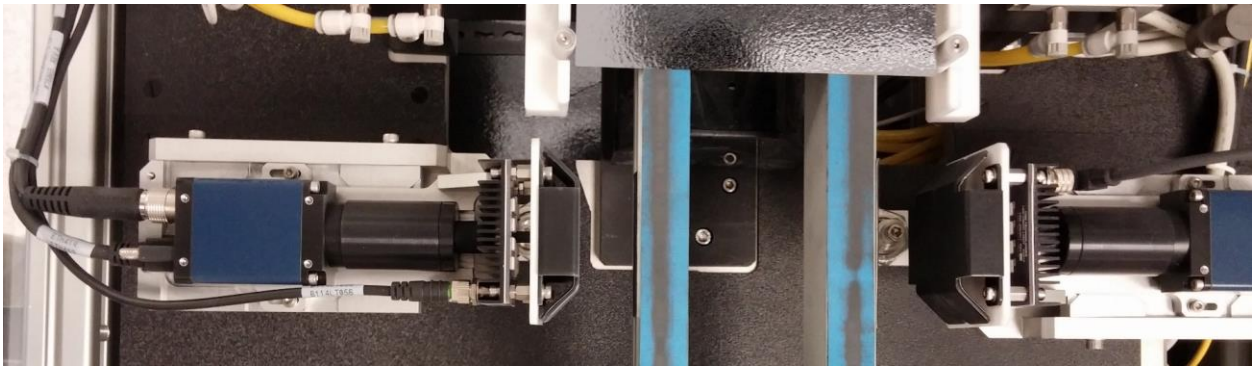


Figure 5: Measurement system developed to measure thickness looking at the edges of a wafer.

The subsequent images are shown in Figure 6, where the wafer edge is illuminated white on a black background. The software uses a rake function to detect the threshold at the edge of the wafer and converts the pixels to microns. The three pairs of red lines are the points of measurement along the image and are 1mm apart, with a field of view

of ~2.5mm. Images are captured at a wafer translation speed of 180mm/s and the 60Hz acquisition rate of the cameras enables a 3mm step size between images.

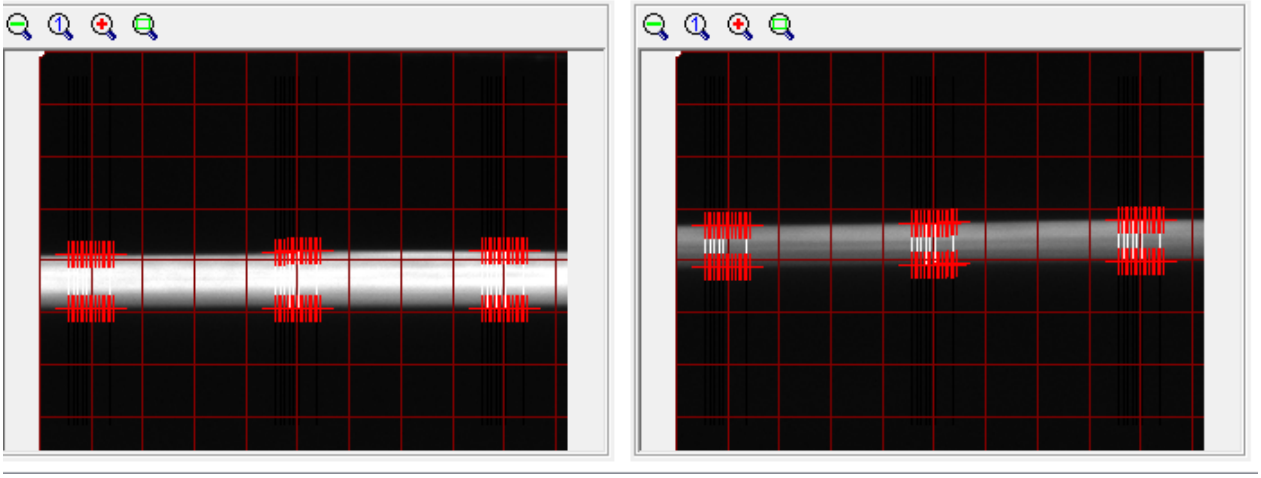


Figure 6: Images from edge vision camera system for measurement of wafer thickness at the edges.

This was then automated with image processing algorithms to generate plots of thickness for each wafer edge. The motion sequence is automated on the furnace inspection station to pass the wafer through the cameras for a first set of images from left and right, then the belt retracts the wafer, a pedestal lifts the wafer off the belt to rotate it 90 degrees, and then the wafer passes through the cameras a second time to measure the other two edges. This is all done within ~7 seconds. (imaging takes < 1 second per pass, but motion sequence takes extra time)

Subtask 2.2 Measurement Method 2 – Measure thickness step changes

The accuracy of placement of the local thickness control is important to maintaining the frame in the correct location on the wafer. If the alignment is not correct, the width of the border may not be sufficient. The measurement method is important to verify that the thick region is grown in the correct location with respect to the laser trimming process that subsequently defines the wafer edges. Again, the capacitive sensors have too large of a spot size to achieve this, so 1366 investigated the use of laser displacement sensors. The specularly reflective surface of the Direct Wafer product immediately after growth posed a challenge. The initial laser sensors tested either had too small of a spot, and resulted in having difficulty at grain boundaries due to light scattering, or with larger spot sizes, the working distances were too long and the imaging sensors would not accurately determine the distance within the desired tolerance. The results were very noisy and not repeatable. Some internal efforts were pursued using a laser combined with a position sensitive detector that would feed back where on the sensor the reflected light hit, which could be used to calculate the relative height and angle of the surface the laser was incident upon. In the midst of this testing, we were able to identify a similar commercially available sensor that operated under similar principals with the laser incident on a shiny surface at 45 degrees, set up for looking at specular surfaces. This also required an appropriate spot size to avoid too

much noise at grain boundaries. The selected sensor has a rectangular spot size of 30 µm x 0.5mm wide. The sensor was used with a wafer travelling at 180 mm/s for a horizontal resolution of 36 µm. Sample scans are shown in Figure 7, showing the width of a thick frame approximately 4mm wide. Figure 8 shows the sensor mounted above the surface of the as-grown wafer.

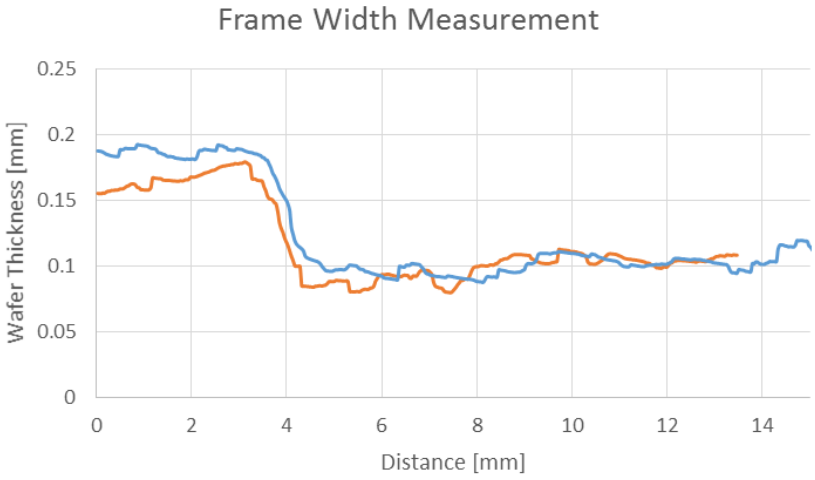


Figure 7 (left): Plot of wafer thickness highlighting step change in thickness near the edge of wafer.

Figure 8 (right): Laser displacement sensor designed for use with reflective surfaces.

Subtask 2.3 Grow Framed wafers and demonstrate average thickness < 80% of edge thickness.

Having developed appropriate measurement methods in the previous quarter to monitor edge thickness independently from average wafer thickness (either by mass or by interior data points of the thickness map), 1366 investigated a number of different methods of implementing local control over wafer thickness. Several different options were explored, all of which control the local extraction of heat from the melt during solidification. As each method was tested on the furnace, the measurement methods were used to determine if the method was successful.

A set of 200+ wafers grown in Aug 2015 were produced under conditions for thin wafers with thick borders. The three relevant metrics compared for the milestone were:

- **ThicknessFromMass** is a simple conversion of the measured total mass of the wafer from a load cell after laser trimming, divided by area and density of 2.3g/cc.
- **EdgeThicknessMedian** is a measured value using the new camera-based system 1366 developed in Subtask 2.1.
- **ThicknessInnerAve** is calculated using the inner 14x14 (196 points) measurements of a thickness map. The full map is a 16x16 array measured

using capacitive displacement sensors to determine thickness, but the outer points can be impacted by the frame, so are excluded.

The average thickness for the special wafers was reduced to 160um as measured by mass or 140 in the interior region only as measured by the capacitive sensors. The ratio of ThicknessFromMass to EdgeThicknessMedian demonstrated the real edge thickness achieved a ratio of 67% and satisfied the Subtask 2.3 milestone target (<80%).

Subtask 2.4 Improve thickness control in thin region to TTV less than half average thickness

Additional improvements to thermal uniformity were implemented throughout January and February and the target milestone for this task was demonstrated in a production furnace on March 10th, 2016 during the production of material to be subsequently used for subtasks 3.3, 4.2 and 4.3. The ThicknessFromMass shifted from an average thickness of 198 microns to 155 microns, while the EdgeThicknessMedian, which used the method developed by Subtask 2.1, showed that the border of the wafers did not change significantly (actually increased by ~15 microns. Meanwhile, the average thickness of the interior region of the wafer (ThicknessInnerAve) was reduced from 190 microns to 138 microns. The target metric for this milestone was to maintain a TTV for the inner region of less than half the average thickness. In this case, less than 77.5 microns. The demonstrated average TTV while growing thin wafers with frames was 65 microns.

Task 3.0 Efficiency potential and wafer handling

Subtask 3.1 Modeling Electrical

This task modelled the electrical performance of thin Direct Wafer products for industrially relevant cell architectures. Specifically, today's industry-standard for multicrystalline wafers is full-area aluminum BSF, which serves as the baseline. Many Tier 1 manufacturers are introducing PERC processes into high volume production, which was analyzed along with an IBC structure that is less common and not currently applied to multi-crystalline wafers due to the high cell processing cost. PC2D modeling software (www.pc2d.info) was used to analyze the impact of wafer thickness for the different architectures and the other two main variables were wafer bulk lifetime and wafer bulk resistivity.

Back surface field (BSF) solar cell architecture
Approach

The default BSF model provided on the PC-2D web site was used but the following simulation parameters were adjusted for Direct Wafer:

- Front finger spacing: 1.42 mm
- Doping concentration (N): variation 1 – $2 \cdot 10^{-16}$ cm^{-3}
- Bulk electron lifetime (tau): variation 20 – 80 μs
- P emitter sheet resistance (sheet rho): 90 Ohms/sq
- Front reflectance (Wavelength multiplier Trans Top): measured values for RIE texture
- Emitter recombination current (Jo1 Top): 10^{-13} A/cm^2
- Back side recombination current (Jo1 Bottom): $4 \cdot 10^{-13}$ A/cm^2
- p-n junction recombination current (Jo2 Top): $3 \cdot 10^{-8}$ A/cm^2

Results

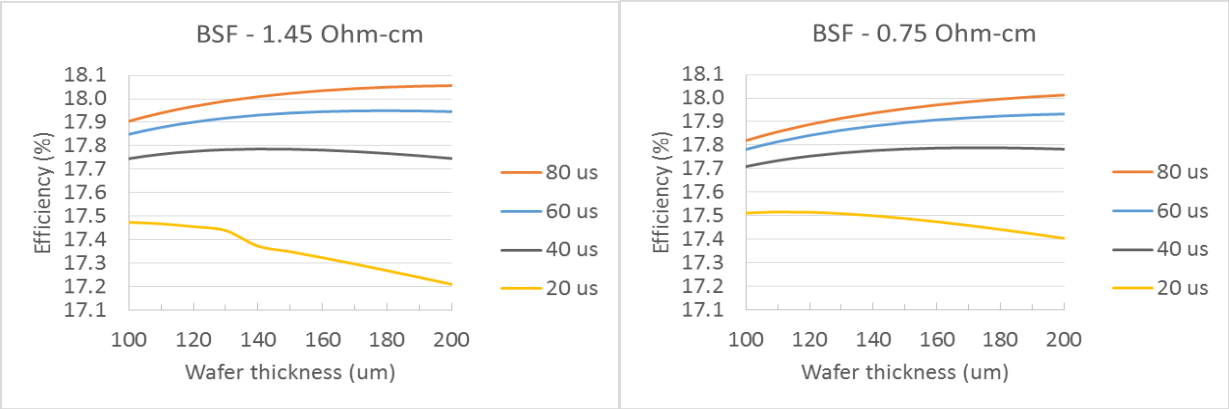


Figure 9: Efficiency as a function of wafer thickness for different bulk electron lifetimes in a P-type BSF solar cell for two different bulk resistivities.

- For 20 μs bulk lifetime, strong efficiency increase with decreasing wafer thickness. About 0.15% absolute efficiency gain when going from 200 to 150 microns in a cell with 1.45 Ohm-cm bulk resistivity.
- Efficiency gain with thickness reduction decreases with increasing bulk lifetime. For 40μs bulk lifetime, only about 0.05% gain when going from 200 to 150 microns in a cell with 1.45 Ohm-cm bulk resistivity. Efficiency loss when going even thinner.
- For bulk lifetime >60 μs, highest efficiencies are achieved for 200 micron thick wafer, and an efficiency loss is observed for decreasing wafer thickness
- Similar trends for higher-doping/lower-resistivity substrates but with a tightened efficiency distribution: overall lower efficiency for the highest bulk lifetimes (60 & 80 μs) and overall higher efficiency for lowest bulk lifetime (20 μs)

Passivated Emitter and Rear Cell (PERC) architecture

Approach

The default PERC model provided on the PC-2D web site was used but the following simulation parameters were adjusted for Direct Wafer:

- Front finger spacing: 1.42 mm
- Back finger spacing: 0.71 mm
- Doping concentration (N): variation 1 – $2 \cdot 10^{-16}$ cm^{-3}
- Bulk electron lifetime (tau): variation 20 – 80 μs
- P emitter sheet resistance (sheet rho): 90 Ohms/sq
- Front reflectance (Wavelength multiplier Trans Top): measured values for RIE texture
- Emitter recombination current (Jo1 Top): 10^{-13} A/cm^2
- Back side recombination current (Jo1 Bottom): $2 \cdot 10^{-14}$ A/cm^2
- p-n junction recombination current (Jo2 Top): $3 \cdot 10^{-8}$ A/cm^2

Results

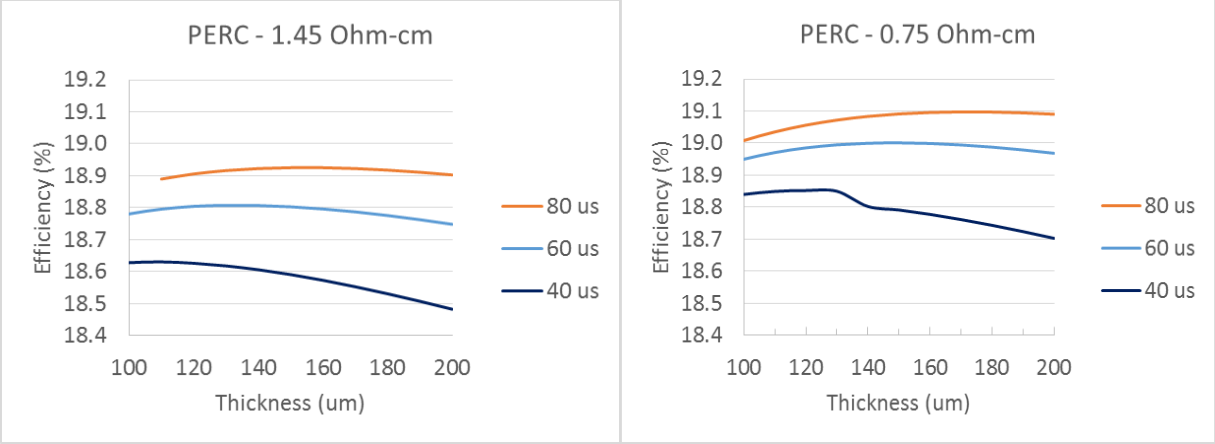


Figure 10: Efficiency as a function of wafer thickness for different bulk electron lifetimes in a P-type PERC solar cell for two different bulk resistivities.

- For 40 μs bulk lifetime, considerable efficiency increase with decreasing wafer thickness. About 0.1% absolute efficiency gain when going from 200 to 150 μm in a PERC cell with 1.45 Ohm-cm bulk resistivity.
- Efficiency gain with thickness reduction decreases with increasing bulk lifetime. For 60 μs bulk lifetime, only about 0.05% gain when going from 200 to 150 μm in a PERC cell with 1.45 Ohm-cm bulk resistivity.
- For bulk lifetime >60μs, fairly constant efficiency for all simulated wafer thicknesses but still with a slight maximum around 150 – 160 μm
- Similar trends for higher-doping/lower-resistivity substrates (see Fig. 3) but overall with 0.2% absolute higher efficiency for all bulk lifetimes considered

Interdigitated Back-surface Cell (IBC) architecture

Approach

The default IBC model provided on the PC-2D web site was used but the following simulation parameters were adjusted for Direct Wafer:

- Doping concentration (N): variation $1 \cdot 10^{-16}$ cm^{-3}
- Bulk electron lifetime (tau): variation 100 – 400 µs
- Front reflectance (Wavelength multiplier Trans Top): measured values for RIE texture

Results

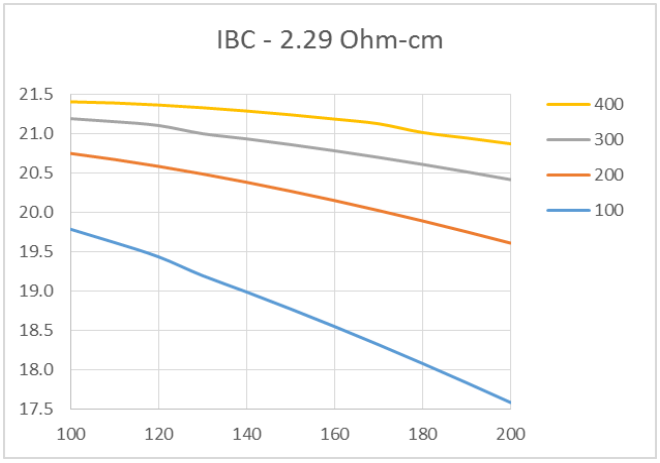


Figure 11: Efficiency as a function of wafer thickness for different bulk electron lifetimes in an n-type IBC solar cell with 1.45 ohm-cm bulk resistivity.

- Considerable efficiency increase with decreasing wafer thickness for all bulk lifetimes under considerations
- Largest efficiency gains for lowest bulk hole lifetime

The potential efficiency gain as a function of wafer thickness and bulk diffusion length was modeled for different architectures. Most advanced back cell architectures rely on local back contact, so there is significant impact of both wafer thickness and also bulk doping level on the lateral conductivity between the local contacts. The goal of this task is both to optimize the wafer properties to take best advantage of customers' cell architectures.

Discussion

Bulk lifetimes between 10 and 30 µs were usually obtained in previous generations of Direct Wafer® (e.g. at the time when the DOE project was applied for) so that significant efficiency gains were to be expected from decreasing the wafer thickness. Since then, Direct Wafer electrical quality has significantly improved so that the latest generations of Direct Wafer usually show considerably higher bulk lifetimes between 40 and 80 µs (measured at $1 \cdot 10^{-14}$ cm^{-3} excess carrier density close to the operating point of the solar cell). Therefore, for reduced wafer thickness in a BSF cell structure, only marginal efficiency gains can be expected for wafers at today's lower end of the lifetime spectrum, while no efficiency gain at all can be expected for the best performing wafers (Fig. 9).

However, simulations suggest that, for the current lifetime range, a decreased wafer thickness should help decrease the efficiency variation across a batch of BSF solar cells with varying bulk lifetime. For two different bulk lifetimes of 40 and 80 µs, an efficiency delta of 0.3% absolute is expected at 200 microns wafer thickness. For a decreased wafer thickness of 150 microns, the efficiency spread should decrease and an efficiency delta of about 0.2 % absolute observed.
A tighter efficiency distribution helps to reduce cell-to-module losses and therefore, leads to increased module efficiencies, in particular when the most poorly performing cells are improved, which is the case when using thinner substrates.

In PERC-type solar cells, the positive effect of decreased wafer thickness on efficiency remains stronger even for the increased bulk lifetimes obtained in the latest generations of Direct Wafer (Fig. 10). A 0.1% absolute efficiency gain is expected for wafers with 40 µs bulk lifetime when decreasing the wafer thickness from 200 to 150 µm. At the same time, no considerable efficiency losses are observed for highest-lifetime wafers when decreasing the wafer thickness, likely due to improved photon absorption through improved internal reflectance in PERC structures. For 80 µs bulk lifetime, an efficiency maximum is still expected to lie around 150 – 160 µm.
In addition to improved absolute efficiencies for thinner PERC cells, the efficiency distribution is expected to tighten by 0.1 % absolute when reducing the wafer thickness from 200 to 150 µm.
Finally, simulations at lower base doping suggest that - if bulk lifetimes can be kept at similar levels - higher efficiencies can be achieved in PERC structures for lower bulk resistivity <1.45 Ohm-cm.

An IBC structure is one of the most advanced cell architectures that is currently being produced industrially on n-type, mono-crystalline silicon wafers, and has therefore been simulated as well. No data for bulk lifetime or surface recombination currents in n-type Direct Wafer is available to date, but in principle, it is straight forward to grow thin, n-type silicon wafers of any desired thickness and doping concentration with the Direct Wafer technology. N-type silicon is much less sensitive to common metal impurities and therefore, several times higher minority carrier lifetimes are usually obtained in n- over p-type silicon wafers of equal material quality. Figure 11 shows a clear trend of increasing efficiency with decreasing wafer thickness is observed for all simulated bulk hole lifetimes between 100 and 400 µs. The lifetime and efficiency potential with thin, n-type Direct Wafer may therefore be worth exploring.

Subtask 3.2 Wafer Handling: Process through cell processing with <5% breakage.

The wafers used for cell processing at 1366 for this task were produced in December (see Q4-2015 report). The wafers used for this test had an average wafer thickness at the perimeter of 180-200 microns, and an average interior thickness of 110-130 microns. The process flow at 1366 consists of standard Al BSF cell process with the following steps:

1. RIE texture
2. Pre-POCl clean
3. POCl diffusion

4. Glass removal etch
5. PECVD SiNx deposition
6. Screen print Ag solder pads on back and oven dry
7. Screen print Al full area back and oven dry
8. Screen print Al front and oven dry
9. Belt furnace firing
10. Laser JI
11. IV Testing

For the screen printing steps, the mechanical yield for the 100 wafer lot was 96%. One wafer was broken when printing Ag pads on back, 2 wafers broke when printing full Al back, and 1 wafer broke when printing front Ag. This was quite encouraging for a first attempt without making any process adjustments and successfully demonstrated the target breakage rate for Subtask 3.2 of <5%.

The additional concerns to be addressed regarding metallization are to determine if the thickness transitions between thick and thin areas affect line width either by local increases (which would affect shaded area) or local decreases (which would cause greater line resistance).

Figure 12: shows an image of the printed gridlines of a Direct Wafer with thick frame in comparison to a standard sawn multicrystalline wafer printed under similar conditions (right side). In both cases, the laser cut lines from junction isolation are visible near the perimeter. The area of thickness transition for these wafers was ~5mm in from the edge.

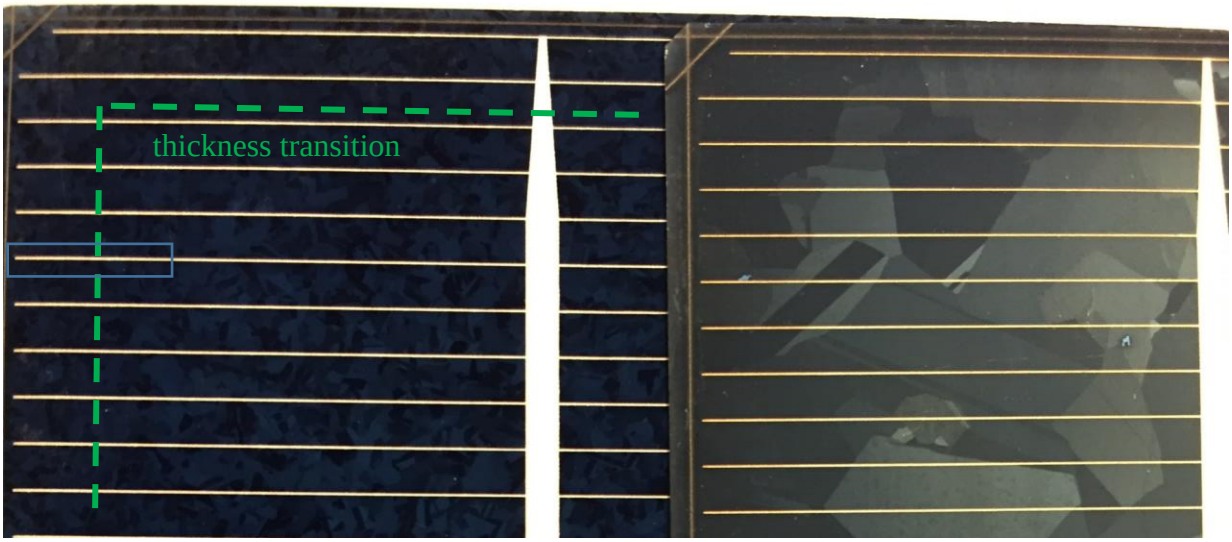


Figure 12: Screen printing gridlines across the thickness transition

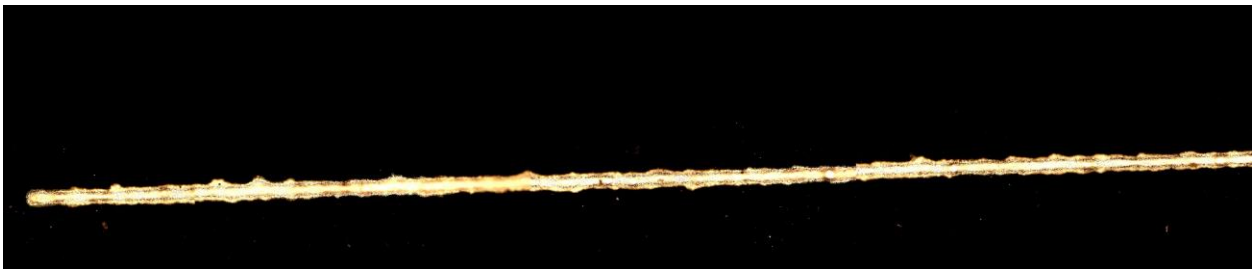


Figure 13: Stitched microscope image of the blue rectangular inlay region from Figure 15, showing the outer 10mm of one gridline.

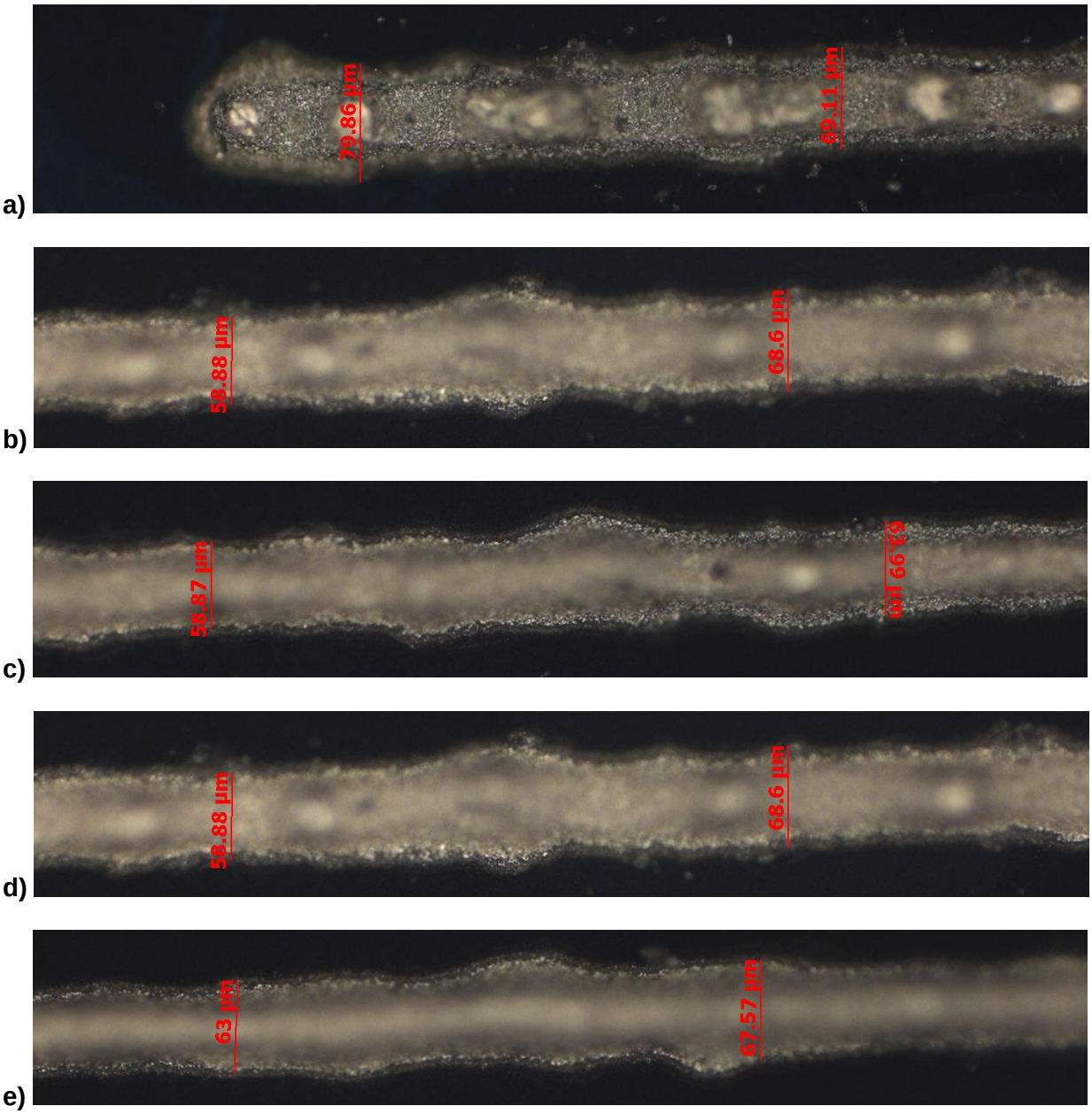


Figure 14: Individual microscope images making up Figure 13, which measurements of finger line width. Each image is progressively farther from the edge starting with a) 0mm b) 2.5mm c) 5mm d) 7.5mm and e) 10mm. The thickness transition occurs somewhere in image c) and is within the typical variation.

The initial set of wafers produced in December and processed into cells in February did not have raised busbars, so the proposed Rbb measurement does not actually measure the region of the wafer that includes the thickness transition. However, the measurements were taken and are summarized in Figure 15, along with some subsequent measurements of Rbb on wafers that included raised busbars (grown on March 10th with data shown in Figure 18). In both cases, the measured Rbb values were well within the specified target of 20%.

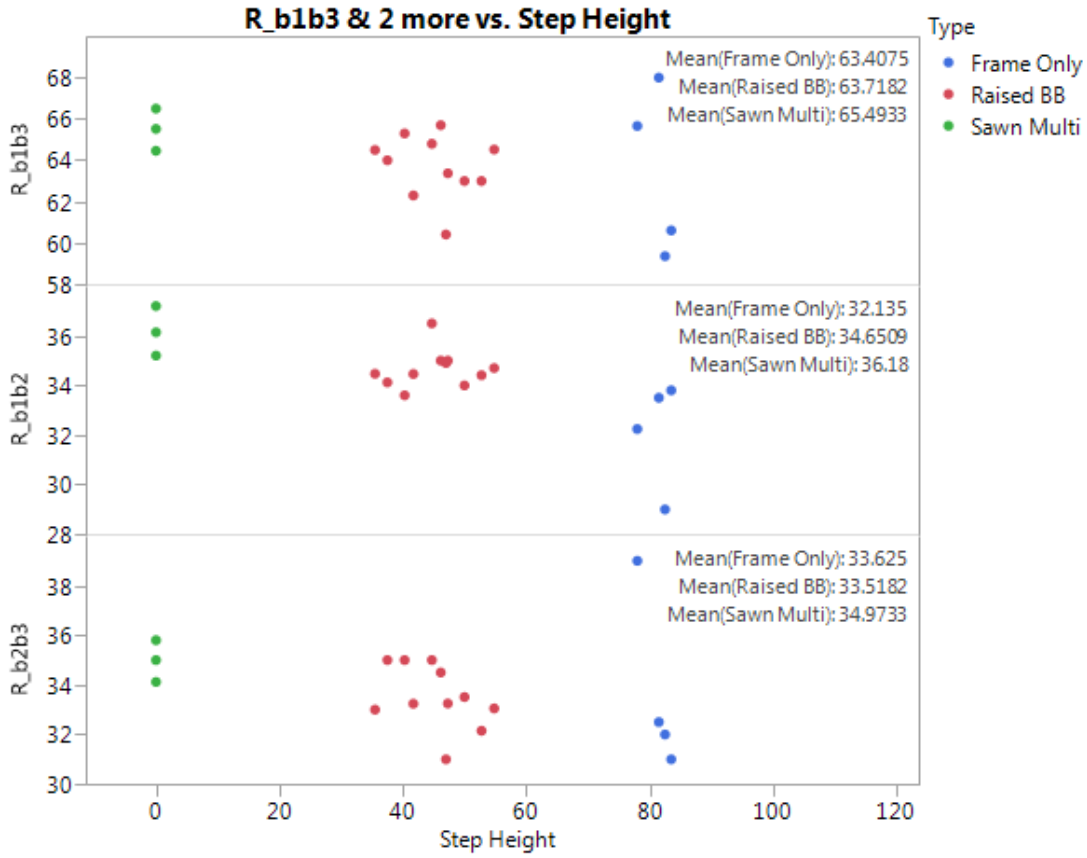


Figure 15: Resistance between busbars measured across thickness step. R_b1b2 is measured between left and center, R_b2b3 is measured between center and right busbars, and R_b1b3 is from left to right (similar to sum of previous 2).

While not specified as part of Milestone 3.2, The EL images Figure 16 further illustrate the line continuity achieved with screen printing across the wafer regions with thickness transitions near the busbars. These EL images would show dark regions if there were any line discontinuity.

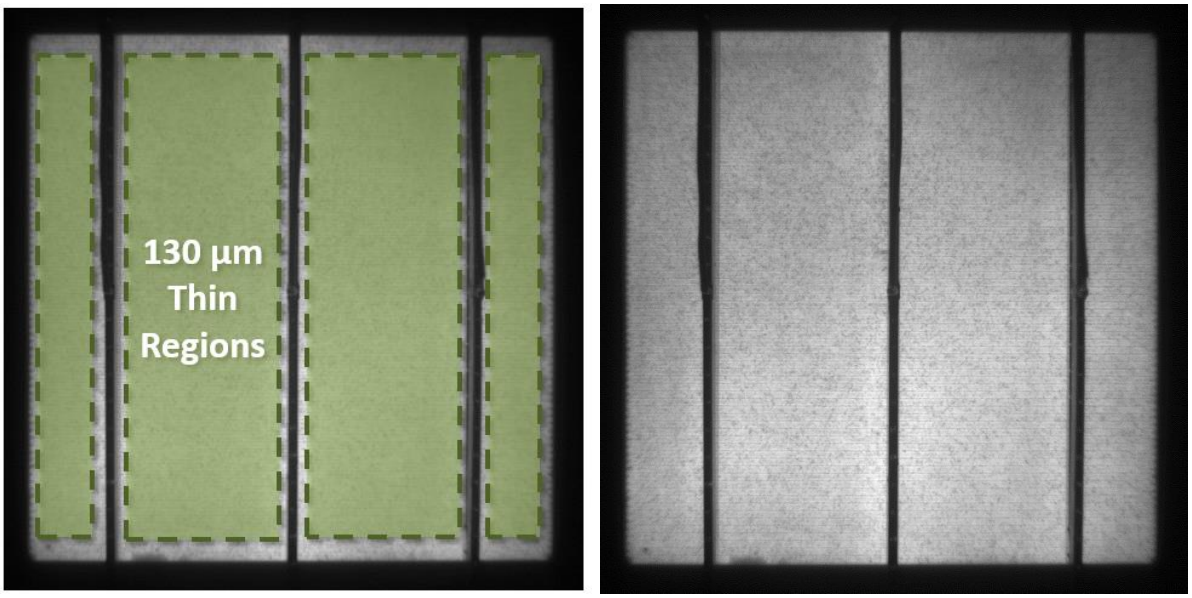


Figure 16: EL images of a Direct Wafer sample with 180+ micron wafer thickness around the perimeter and underneath the 3 busbars, but thin wafer area in the interior region. Left image simply has the mask added to explain where the wafer is thinner. Right image shows the unmasked results without line breaks.

Subtask 3.3 Modeling validation: Electrical performance tested to match predictions.

Direct Wafer samples grown on March 10th and described previously in subtask 2.3 were textured and provided to an industrial partner for PERC cell processing. The samples of thin wafers w/ thick frames ranged in thickness from 120 to 150 microns and

were compared against standard thickness Direct Wafer product. The cell results are summarize in Figure 17.

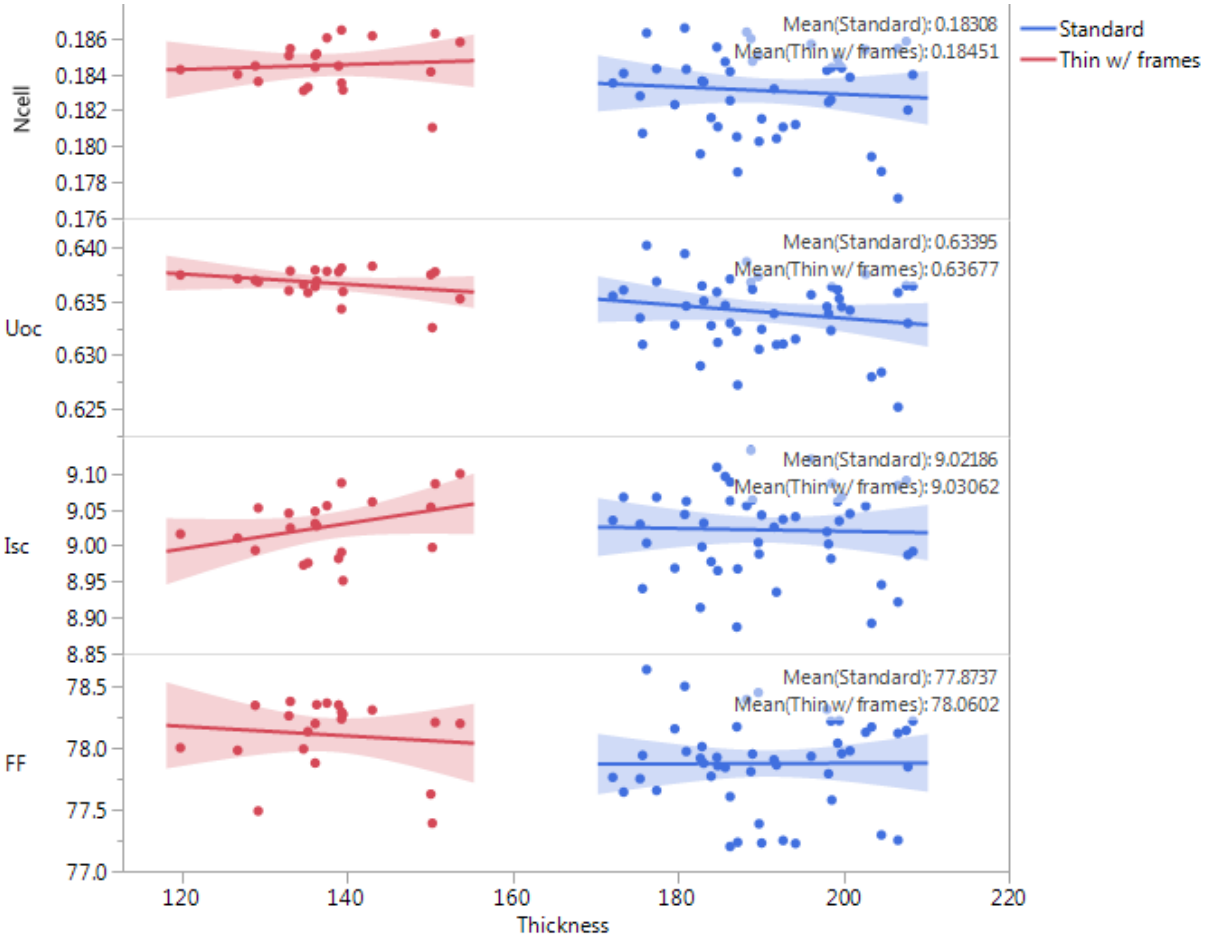


Figure 17: PERC cell efficiency achieved by a customer on an industrial cell line.

The electrical modeling provided previously in Subtask 3.1 predicted that for PERC cells, there would be a small increase in efficiency with decreasing thickness based on factors including the bulk resistivity and bulk lifetime of the wafers.

The predicted average for the standard thickness of 180 microns was slightly above 18.5%. The actual measured efficiency values for the standard thickness was 18.3%. Model parameters were adjusted to better match the observed performance for standard material. One difference is the average bulk resistivity of these wafers was higher, at 1.6 ohm-cm, and the expected bulk lifetime may be slightly lower than 40 µs.

An overlay of the experimental results and the adjusted model is shown in Figure 18.

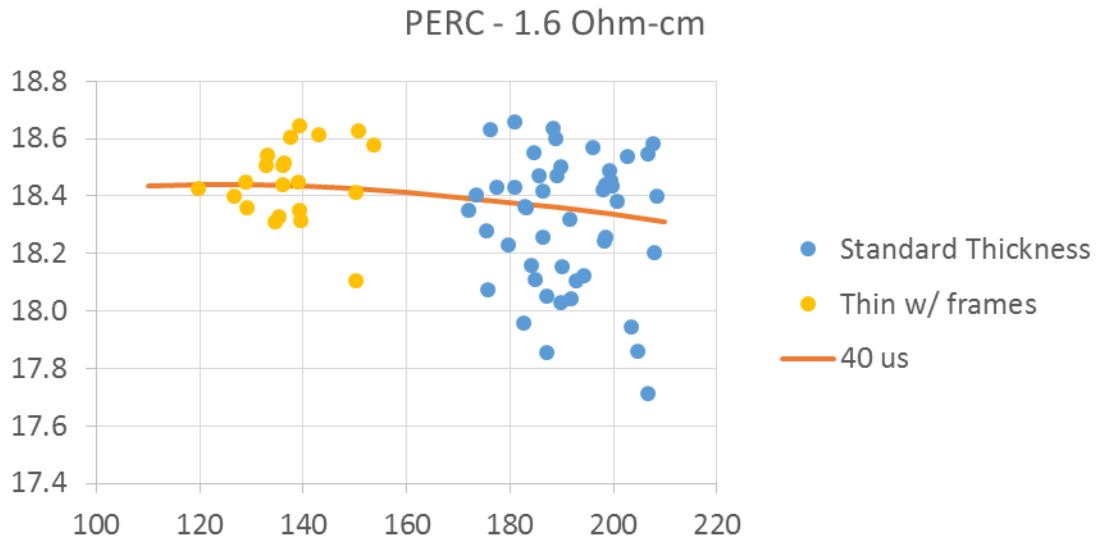


Figure 18: Comparison of experimental results with model predictions for PERC cell process.

The predicted efficiency for a wafer thickness of 140 µm is slightly above 18.4%. The milestone target was to demonstrate accuracy within 5%, which corresponds to within 0.9% absolute efficiency. The average efficiency measured for the ~140µm thick cells was 18.45%, well within the target value.

Task 4.0 Strength testing of thin, framed Direct Wafer

Subtask 4.1 Single cell modules:

The thermal and mechanical stresses imposed on a finished cell during the soldering or interconnect ribbon and subsequent lamination process represents a significant challenge for thin silicon wafers.

Wafers produced from Subtask 2.3 were processed into solar cells at 1366 using our pilot cell line with BSF processing and a traditional 3 busbar metallization pattern. Soldering of interconnect ribbon was done manually, first on the front side, then on the rear, with a 1.5mm wide soft copper ribbon. Then the cell with busbars was assembled into a stack as designated in Figure 19, and followed a lamination thermal and vacuum cycle.

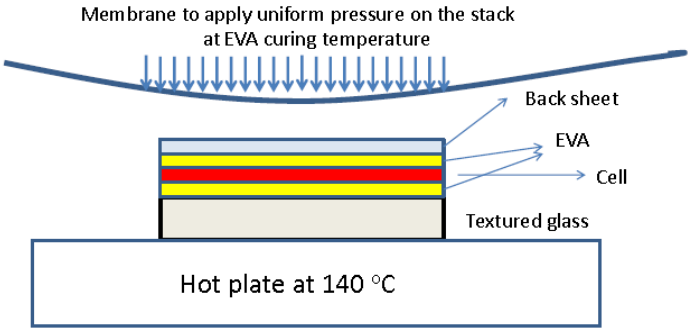


Figure 19: Schematic of single cell laminator developed by 1366 to make single cell coupons.

There was a learning period to develop the method, and some early test samples initiated cracks. We subsequently made a few adjustments to the procedure for manual soldering of busbars. Some improvements were simply by the practice of more uniform application of the solder to not overload in any area and use of a wider 2.5mm tipped soldering iron. Another improvement was to preheat the cell on a heated vacuum chuck to 140degC prior to soldering to minimize thermal stress. We also purchased a ribbon puller to straighten the ribbon prior to application. The tip was applied to the wafer using a smooth motion at constant speed, and then process was repeated for the back side. These changes more closely mimic the conditions present in a production tabber/stringer.

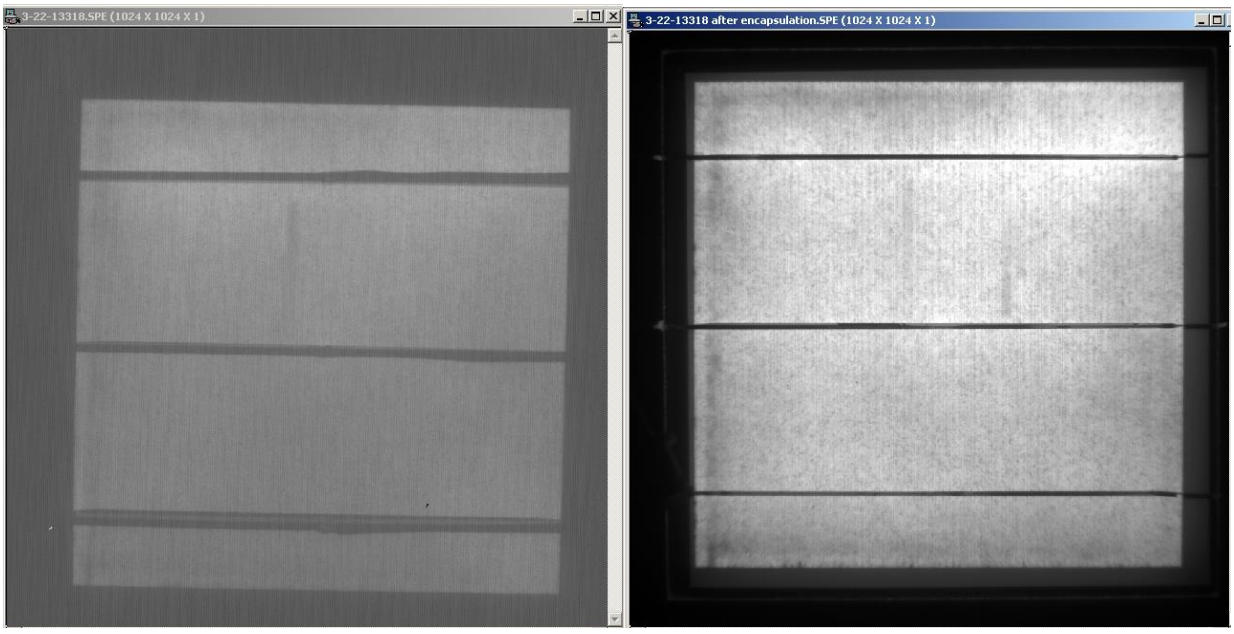


Figure 20: Electroluminescence images of thin wafer with frames before (left) and after (right) lamination with EVA and glass.

An excel file showing the EL images for 10 wafers before and after lamination, showing no crack formation was provided to demonstrate completion of the milestone for Subtask 4.1, with an example shown in Figure 20. The left image is a bit hazy because the EVA is not yet cured. You can see in the right image (post-lamination) that there is the glass frame visible if you look closely. Some dark lines are visible pre-lamination, which are due to line breaks of the silver front gridlines, not cracks. Samples were shown to DOE representatives during a visit to DC on December 10th.

Subtask 4.2 Stringing cells: Test with mini-modules of 9+ cells including thermal cycling:

1366 does not have stringing and tabbing or encapsulation capabilities for larger than single cells. To demonstrate the objective of this subtask, the cells produced from the February internal cell processing run of Subtask 3.2 were provided to Jabil Solar and Environmental Test Center in St. Petersburg, Florida. Here, they used a manual soldering process to fabricate strings and encapsulated 9-cell minimodules from the cells provided.

The wafer ID's and corresponding wafer thickness used for the mini-module production are summarized in the table below.

3-034-007984 114 µm	3-034-008065 85 µm	3-034-007955 98 µm
3-034-008499 101 µm	3-034-007793 110 µm	3-034-008197 95 µm
3-034-008262 96 µm	3-034-008059 95 µm	3-034-008686 98 µm

EL images were taken after tabbing and stringing of the cells into a mini-module in order to record the initial appearance of each cell. Then an additional EL image is taken after lamination is completed, to confirm the lamination process itself did not induce any microcracks.

After lamination, the mini-module was conditioned in Jabil's environmental chamber for 50 thermal cycles between -40°C to +85°C. This accelerated testing subjects the wafer to stresses due to the mismatch of CTE between silicon and the copper buswire. A final EL image is taken after the environmental testing to confirm there was no initiation of cell cracks during the thermal cycling.

Subtask 4.3 Hot spot analysis: Testing for partial module shading by measuring temp < 150C for 60 sec at -12V or 8A.

The IV test results for the cells produced in Milestone 3.3 were provided as part of that milestone description. The cell manufacturer additionally provided the reverse bias breakdown current values recorded at -10V (Irev1) and -13V (Irev2) as shown in Figure 21.

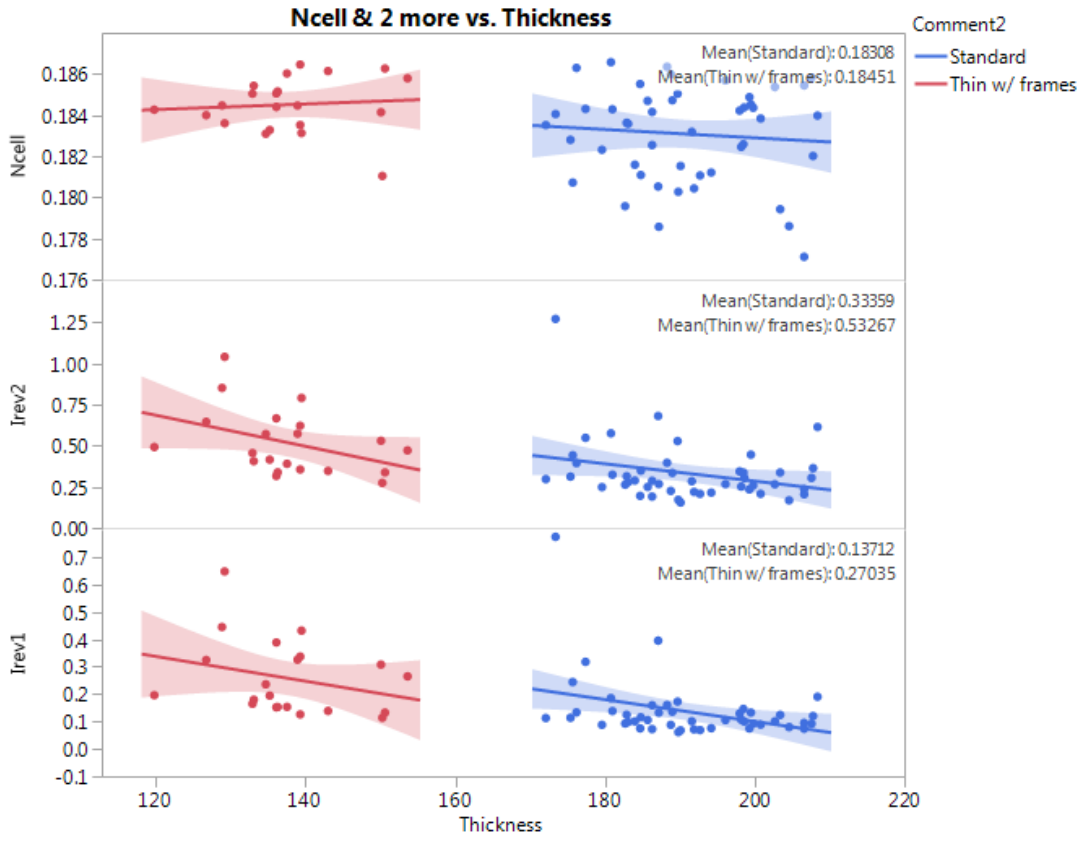


Figure 21: Measurements of reverse bias breakdown current for thin cells fabricated by customer on an industrial cell line.

These cells were shipped back to 1366 for additional measurements of hot spot by infra-red imaging. A screen shot of the camera software interface is provided in Figure 22.

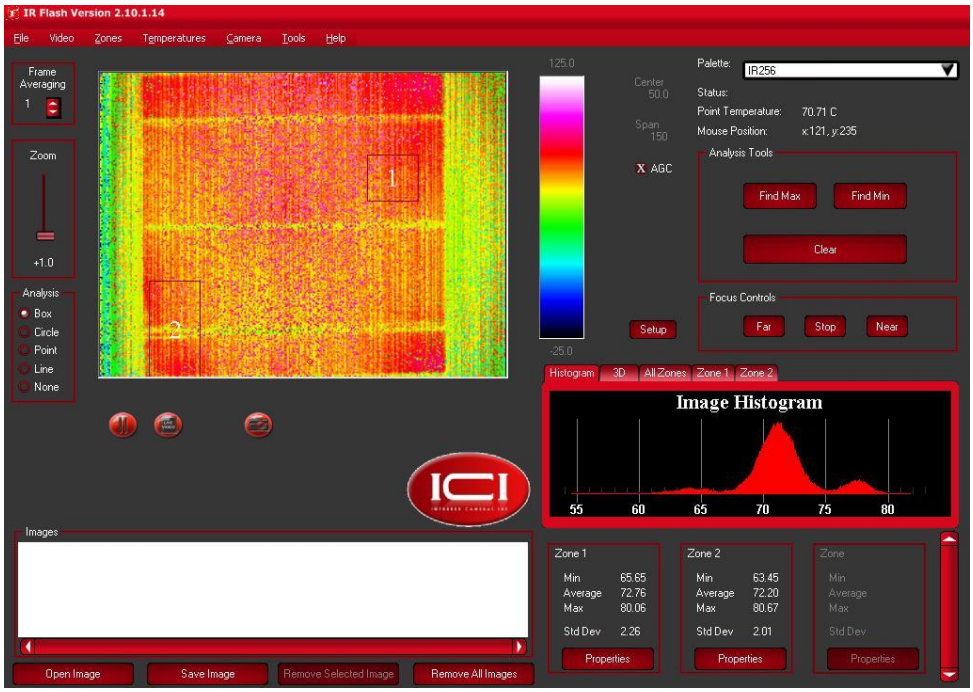


Figure 22: IR camera imaging software with an example of mapping and max temperature recording.

The IR camera system was calibrated using a solar cell on a hot plate with a thermocouple attached, then max temperature values were recorded by holding a cell in a probe fixture to apply -12V bias voltage for 30 seconds (values reached steady state in <5 sec) and both leakage current and maximum temperature were recorded, with the results tabulated in Table 1. These hot spot analysis results satisfied the criteria set for Milestone 4.3.

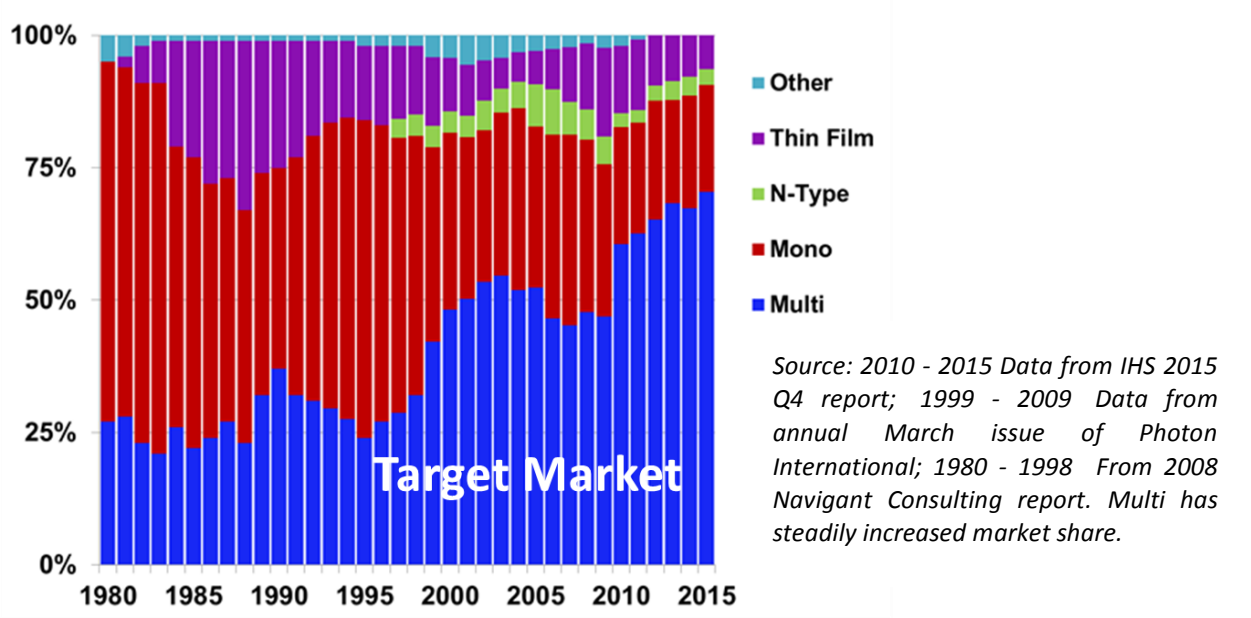
WaferID	Thickness	Irev (A)	Tmax (degC)		WaferID	Thickness	Irev (A)	Tmax (degC)
5-019-004657	139	0.29	41		**5-019-005230**	151	0.2	35
5-019-004667	151	0.31	39		**5-019-005281**	155	0.3	42
5-019-004695	134	0.3	43		**5-019-005291**	152	0.3	46
5-019-004797	137	0.59	104		**5-019-005293**	155	0.2	42
5-019-004887	145	0.55	54		**B13-09**	130	0.3	46
5-019-004906	144	0.35	43		**B13-19**	135	0.3	43
5-019-004918	142	0.3	40		**B13-21**	148	0.3	51
5-019-004933	142	0.36	45		**B13-22**	145	0.4	44
5-019-004964	145	0.3	41		**B13-23**	131	0.2	41
5-019-004996	134	0.2	42		**B13-24**	145	0.2	40
5-019-004701	128	0.2	44		**B13-26**	138	0.2	43
5-019-004829	124	0.6	48		**B13-27**	128	0.3	44
5-019-004845	134	0.6	49		**B14-06**	110	0.8	63
5-019-004882	132	0.2	41		**B14-09**	121	0.4	41
5-019-004928	131	0.5	127		**B14-18**	123	0.5	48
5-019-004934	131	0.2	44		**B14-20**	109	0.3	56
5-019-004947	129	0.3	42		**B14-28**	102	0.6	45
5-019-004989	145	0.2	41		**B14-34**	111	0.5	44
5-019-005142	155	0.3	45		**B14-40**	119	0.4	74
5-019-005152	149	0.2	42		**B14-41**	112	0.4	41
5-019-005160	159	0.4	45		**B14-43**	122	0.5	53
5-019-005204	150	0.1	38		**B14-46**	112	0.5	43
5-019-005206	153	0.2	42		**B14-47**	118	0.3	46
5-019-005216	149	0.3	40		**B14-48**	117	0.5	44
5-019-005222	151	0.3	43		**B14-50**	110	0.4	40

Table 1: Measured Irev and Max temperature from IR camera imaging of hot spots for cells produced from thin Direct Wafer product with thick frames.

The Tier 1 cell and module manufacturer that processed the cells for Subtask 3.3 was pleasantly surprised by the handling of the wafers provided and has requested larger sample quantities for follow on tests.

COMPETITIVENESS IN THE MARKETPLACE

Our disruptive technology addresses a $10 billion market at 50% of the cost, 60% of the capital, and 30% of the energy use compared to conventional casting and sawing manufacturing. Some prevailing opinions from industry observers state that the market is moving towards advanced thin film structures and high efficiency mono-crystalline wafers. Although it is difficult to predict the future, looking at historical trends – that includes data from both the start and end of the award period – suggest this forecast may not hold true. In fact, multicrystalline continues to gain market share as seen below. Multi has steadily increased market share against competing monocrystalline (higher efficiency but also higher cost) and thin film (cadmium telluride and CIGS) technologies over the last thirty years due to a superior efficiency versus cost profile. Multicrystalline technology continues to deliver the lowest LCOE in the market.



Source: 2010 - 2015 Data from IHS 2015 Q4 report; 1999 - 2009 Data from annual March issue of Photon International; 1980 - 1998 From 2008 Navigant Consulting report. Multi has steadily increased market share.

Figure 23: Historical PV market share by technology

The multi segment is 1366's target market. The total installed capacity for conventional crystalline silicon in 2016 is estimated by IHS to be 67 GW_p. The strength of the Direct Wafer technology is its compatibility with this installed base.

The strength of this dominant value chain is demonstrated in the resulting cost reductions summarized in Figure 24, with current module prices <$0.40/W. The wafer remains nearly 40% of this total cost and represents one of the largest opportunities for further cost reduction.

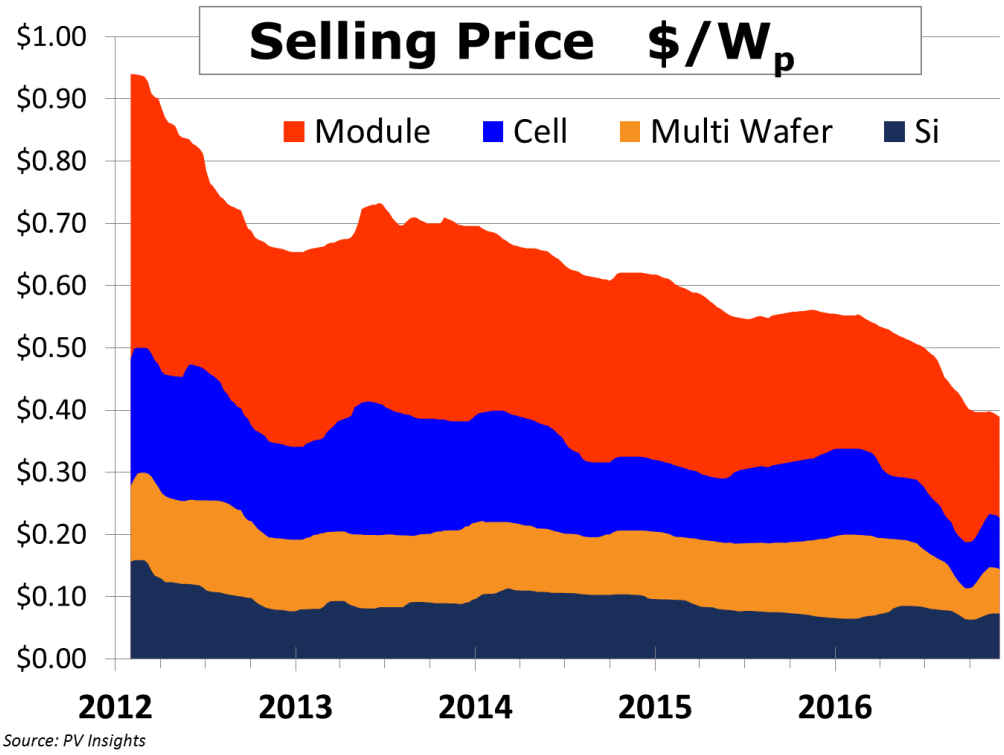


Figure 24 – Selling price of crystalline Silicon PV modules and components.

1366's technology will further strengthen these trends with a disruptive solution that allows downstream customers to both realize 5% to 10% improvements in their margins and build a long-term, differentiated product roadmap that leverages their existing billion dollar cell and module investments built around the industry standard 156 mm wafer.

Competitive Technologies

There are several different methods for producing "kerfless" silicon wafers without casting and sawing: solidifying melt either against a substrate (includes Direct Wafer) or as a vertical ribbon, ion implantation and cleaving, exfoliation, and epitaxial growth. Growth of vertical ribbon was commercialized but unable to stay competitive due to a combination of very low throughput, non-standard geometry, and high dislocations resulting from curvature in thermal gradients. The ultra-thin kerfless wafer technologies that produce 20µm to 50µm-thick wafers (ion implantation and cleaving, epitaxial growth, and metal bonding and exfoliation) have the potential for high efficiency modules and <1g/W Si usage but face serious adoption and technical challenges. Thin wafers can be both a feature and a limitation, since it lowers silicon cost, but forces the companies to find simultaneous solutions to several challenges imposed by ultra-thin wafers, such as downstream cell and module handling without breakage, rear surface passivation, and integration into cell and module production lines.

A key advantage of the Direct Solidification approach, such as Direct Wafer, a top target technology because of the potential value impact as well as short time to market as it

delivers “standard” 156mm, 200µm-thick wafers that can “drop-in” to the existing cell and module supply chain and therefore can be adopted rapidly.

SUBJECT INVENTIONS, PUBLICATIONS, AND PRESS RELEASES

Publications/Presentations

- TEDx, November 2015: How to Power the World for Just 2 Cents, Frank van Mierlo
- SiliconPV, March 2016: Low-Cost Kerfless Wafers with Gradient Doping Exceeding 19pct in PERC Production Line
- SNEC, May 2016: Low Cost, High Performance Kerfless Direct Wafer® Technology Incorporating a Drift Field
- EUPVSEC, June 2016: 3 Dimensional Direct Wafer® Product with Locally-Controlled Thickness

Press Releases

- 4-8-15: 1366 Technologies Extends Series C with $5M Investment from Haiyan Capital
- 4-9-15: IHI to Deploy 1366 Technologies’ Direct Wafers® in New Solar Installations
- 10-7-2015: 1366 Technologies to Construct New Direct Wafer® Manufacturing Facility in New York
- 10-25-15: 1366 Technologies Achieves New Performance Records at Hanwha Q CELLS Customer Trials
- 4-12-2016: Hanwha Q CELLS and 1366 Technologies Enter Into 5-Year Supply Agreement
- 5-5-16: 1366 Technologies Receives $10M Investment from Hanwha Investment Corporation
- 6-28-16: 1366 Technologies and Wacker Chemie AG Announce Strategic Agreement

Media Articles

- **PV-tech**: Major Polysilicon Producer Invests in 1366 http://bit.ly/293eoEJ
- **PV Magazine**: Wacker Chemie partners with 1366 Technologies http://bit.ly/296gwMK
- **Solar Industry Magazine**: 1366 Secures Investment, Supply Deal From Leading Polysilicon Maker http://bit.ly/292JJch
- **Recharge:** Germany's Wacker Chemie links with wafer maker 1366 Technologies http://bit.ly/29bQNAe
- **SeeNews Renewables**: 1366 agrees equity investment, supply contract with Wacker http://bit.ly/290OrpS
- **The Boston Globe**: Bedford solar cell company makes silicon deal http://bit.ly/290Iipq
- **BostonInno:** This MIT Solar Spinoff Just Landed a Huge Deal with a Multinational Co.http://bit.ly/29dk6VL

- **Chemical Week**: Wacker, 1366 Technologies form partnership, including equity investment by Wacker http://bit.ly/29534Xo
- Solar Server: 1366 Technologies, Wacker Chemie announce strategic partnership including USD 15 million investment by Wacker http://bit.ly/296wG82
- **Chemical Engineering**: Wacker Chemie and 1366 Technologies Form Strategic Partnership For Solar Energy http://bit.ly/29fXSjf
- **The Boston Globe:** Silicon Solar Company Gets $10M to Help Build New Factory https://www.bostonglobe.com/business/2016/05/05/embargoed-may-solar-silicon-company-gets-help-build-new-factory/0dNsGX6kQOlXsfBPu5HGkN/story.html
- **PV-Tech**: 1366 Technologies Secures Major Direct Wafer Supply Deal http://www.pv-tech.org/news/1366-technologies-secures-major-direct-wafer-supply-deal
- **FORBES**: 1366 Technologies Aims To Slash Solar Wafer Costs 50% And Make Solar Cheaper Than Coal http://www.forbes.com/sites/peterdetwiler/2015/11/23/1366-technologies-aims-to-slash-solar-wafer-costs-50-and-make-solar-cheaper-than-coal/#2f92d56748c8
- **Cleantechnica**: 1366 Technologies Direct Wafer Hits Performance Record http://cleantechnica.com/2015/11/18/1366-technologies-direct-wafer-product-hits-performance-record/
- **PV Magazine**: Hanwha Q CELLS Steps Forward as 1366 Direct Wafer PERC Collaborator http://www.pv-magazine.com/news/details/beitrag/hanwha-q-cells-steps-forward-as-1366-direct-wafer-perc-collaborator_100021850/#axzz4C7sZTfuh
- **FORTUNE**: Solar Start Up to Build Big Factory in Upstate New York http://fortune.com/2015/10/07/solar-factory-upstate-new-york/
- **Bloomberg: New York Draws Another Solar Manufacturers as it Shapes New Hub** http://www.bloomberg.com/news/articles/2015-10-07/new-york-draws-another-solar-manufacturer-as-it-shapes-new-hub
- **The Wall Street Journal**: 1366 Extends Series C Again with $5M from Haiyin Capital
- **PV-tech:** China and Japan Get Interested in 1366 Technologies' Direct Wafer® Technology http://www.pv-tech.org/news/china_and_japan_get_interested_in_1366_technologies_direct_wafer_technology