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Digital Regulation of a Phase Controlled Power Converter[1]

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Abstract

The Relativistic Heavy Ion Collider, now in construction at Brookhaven National Laboratory, will use phase controlled power converters for the main dipole and quadrupole magnet strings. The rectifiers in these power supplies will be controlled by a digital regulator based on the TI 320C30 Digital Signal Processor (DSP). The DSP implements the current loop, the voltage loop, and a system to actively reduce the sub-harmonic ripple components.

Digital firing circuits consisting of a phase-locked loop and counters are used to fire the SCRs. Corrections for the sub-harmonic reduction are calculated by the DSP and stored in registers in the firing circuit. These corrections are added, in hardware, to the over-all firing count provided by the DSP. The resultant count is compared to a reference counter to fire the SCRs.

This combination of a digital control system and the digital firing circuits allows the correction of the sub-harmonics in a real-time sense. A prototype of the regulator has been constructed, and the preliminary testing indicates a sub-harmonic reduction of 60 dB.

DIGITAL FIRING CIRCUIT

The timing for the system is derived from a PLL that is locked to the power line frequency on the secondary side of the rectifier transformers. This PLL develops a 2.949120 MHz clock that is used in counters in the digital firing circuit. This clock drives a reference counter and a command counter and provides a firing resolution of 7.324219 millidegrees. The reference counter is modulo 49152 and therefore wraps around once for every power line cycle. The command counter is modulo 4096 and wraps around once every 30 degrees of the power line cycle. The reference counter is loaded with an offset count in such a way that the zero of the counter occurs at the full rectify point of one of the 12 phases. The command counter is loaded with an offset once every power line cycle and its 0 coincides with full rectify of a phase every 30 degrees.

The 4 MSBs of the reference counter are decoded to provide 12 time intervals called "slots". For each slot there are four pairs of SCRs that may be fired. The first pair in each slot is active from 60 to 90 degrees, the next from 90 degrees to 120 degrees, the next from 120 degrees to 150 degrees, and the last from 150 degrees to 180 degrees. Each slot is divided into 4096 discrete firing times by the command counter.

The DSP develops a 14 bit command word, this command word

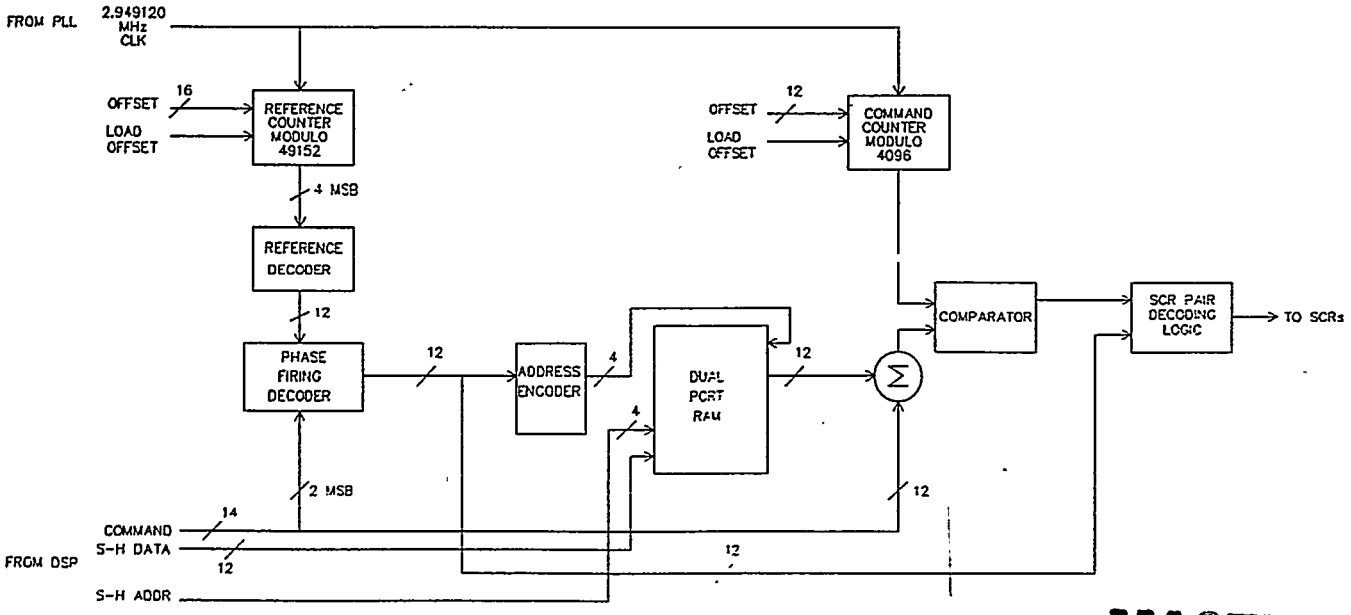

Figure 1 Digital Firing Circuit Block Diagram

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DISCLAIMER

is based on 16384 firing times in 120 degrees of angle. The 4 MSBs from the reference counter select which slot will be fired next, while the 2 MSBs of the command word are decoded to select which of the four pairs of SCRs in that slot will fire. The selected slot is also encoded to provide the address for the proper sub harmonic correction stored in the dual-port ram. The 12 LSBs of the command word are compared with the command counter to fire the selected SCR pair. This method frees the DSP from keeping track of what SCR pair should fire.

THE CONTROL LOOP

The control loop consists of an inner voltage loop and an outer current loop. The two loops are similar and the discussion of the voltage loop applies to the current loop as well.

The voltage is sampled at the input to the ripple filter to provide maximum bandwidth. After an anti-aliasing filter the voltage is digitized at 11520 Hz. This provides 16 samples during each phase. The blocks of 16 samples are aligned so that each block straddles two phases. Each block of 16 samples is integrated with a digital integrator. This provides rejection of the 720 Hz ripple frequency and its' multiples. The voltage data is filtered using a 20 pole elliptic filter and then downsampled by a factor of 16 to match the sample rate of the power converter. The feedback is then compensated with a digital Proportional-Integral (PI) section. The output from the PI section is used to compute a count for the digital firing circuit. This count is proportional to the desired firing angle, and during this calculation the power converter's transfer function is linearized. This allows the power converter to be modeled as a Digital to Analog Converter (DAC) with a sample rate of 720 Hz.

The current loop differs only in its' front end. The current command is sent to the regulator via a serial bus from the control system at a 720 Hz rate. This command is in 24 bit unipolar format. The regulator converts this to an analog voltage. The feedback for the current is derived from a Direct Current Current Transducer (DCCT). The DCCT's output is in the form of an analog voltage, this voltage is subtracted from the command DAC's voltage. The resulting error signal is amplified by a factor of 16 and then digitized by a 16 bit A/D at 11520 Hz. The rest of the current loop is identical to the voltage loop except for the PI coefficients.

SUB-HARMONIC CORRECTION

The sub-harmonic correction algorithm is based on this equation:

$$\Delta f_k = \sum_{n=0}^{11} c_n \Delta_n \frac{1}{2\pi} e^{jkn30^\circ}$$

where f is the complex frequency component of the waveform, c is the step height vector, and Δ is the perturbation vector. This relation shows the corrections to the firing time can be found by using the Inverse Discrete Fourier Transform (IDFT) where the twiddle factors are replaced by

$$W = e^{j30^\circ}$$

The output is sampled after the ripple filter in order to correct the harmonics least filtered. The regulator samples the phases for one power line cycle and 16 samples per phase are taken resulting in 192 points in the Discrete Fourier Transform. This results in 30 Hz of frequency resolution in each frequency bin. The Goertzel Algorithm is used to implement both the DFT and the IDFT. This method avoids storage of the twiddle factors and allows calculation of only the subharmonic frequencies. The subharmonic corrections are sent to the dual port ram in the digital firing circuit and correct the overall firing time calculated by the DSP. Testing indicates the 360 Hz subharmonic can be reduced by 60 dB using this type of system.

ACKNOWLEDGMENTS

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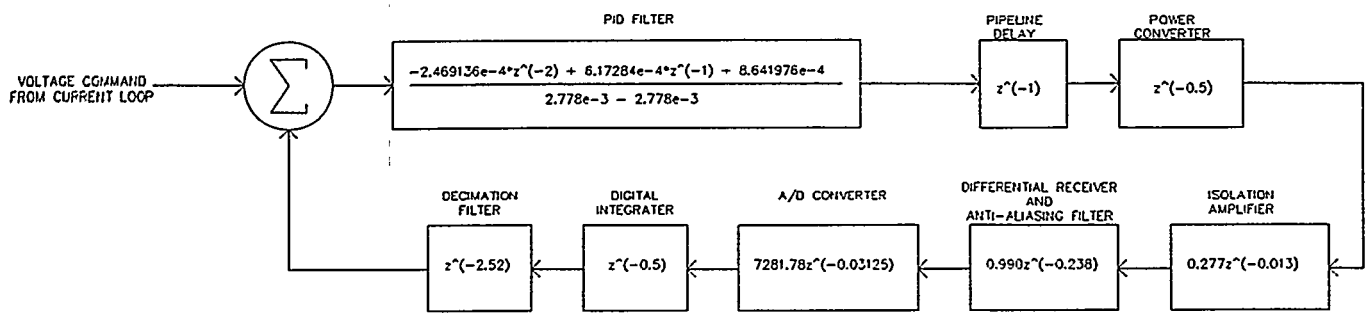

Figure 2 Voltage Loop Block Diagram