

Large arrays of dual-polarized multichroic TES detectors for CMB measurements with the SPT-3G receiver

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ABSTRACT

Detectors for cosmic microwave background (CMB) experiments are now essentially background limited, so a straightforward alternative to improve sensitivity is to increase the number of detectors. Large arrays of multichroic pixels constitute an economical approach to increasing the number of detectors within a given focal plane area. Here, we present the fabrication of large arrays of dual-polarized multichroic transition-edge-sensor (TES) bolometers for the South Pole Telescope third-generation CMB receiver (SPT-3G). The complete SPT-3G receiver will have 2690 pixels, each with six detectors, allowing for individual measurement of three spectral bands (centered at 95 GHz, 150 GHz and 220 GHz) in two orthogonal polarizations. In total, the SPT-3G focal plane will have 16140 detectors. Each pixel is comprised of a broad-band sinuous antenna coupled to a niobium microstrip transmission line. In-line filters are used to define the different band-passes before the millimeter-wavelength signal is fed to the respective Ti/Au TES sensors. Detectors are read out using a 64x frequency domain multiplexing (fMux) scheme. The microfabrication of the SPT-3G detector arrays involves a total of 18 processes, including 13 lithography steps. Together with the fabrication process, the effect of processing on the Ti/Au TES's T_c is discussed. In addition, detectors fabricated with Ti/Au TES films with T_c between 400 mK 560 mK are presented and their thermal characteristics are evaluated. Optical characterization of the arrays is presented as well, indicating that the response of the detectors is in good agreement with the design values for all three spectral bands (95 GHz, 150 GHz, and 220 GHz). The measured optical efficiency of the detectors is between 0.3 and 0.8. Results discussed here are extracted from a batch of research of development wafers used to develop the baseline process for the fabrication of the arrays of detectors to be deployed with the SPT-3G receiver. Results from these research and development wafers have been incorporated into the fabrication process to get the baseline fabrication process presented here. SPT-3G is scheduled to deploy to the South Pole Telescope in late 2016.

Keywords: CMB, SPT-3G, Bolometers, Transition Edge Sensors, Microfabrication, Superconducting Detectors, South Pole Telescope.

1. INTRODUCTION

The cosmic microwave background (CMB) is remnant radiation from the early universe that provides a unique window for exploring fundamental physics. The discovery of the CMB in 1965^{1,2} validated the Hot Big Bang model of cosmology³, its homogeneity led to the theory of inflation, and its anisotropy⁴ showed the geometry of the universe is flat and gave a complete census of the matter-energy content of the universe⁵⁻⁸. Current and upcoming CMB experiments focus on characterizing the extremely faint CMB polarization, particularly the B-mode component. Measurement of the CMB B-mode polarization signal has the potential to detect primordial gravitational waves generated during an epoch of inflation. The CMB can also constrain the sum of neutrino masses as well as the energy scale of inflation. Current CMB detectors have evolved to the point where they are limited by the intrinsic variation in the incident photon flux. Reaching the sensitivity required to characterize the CMB B-mode polarization signal requires the fabrication of focal planes with orders of magnitude more detectors than current instruments. Developing multichroic pixels constitutes an economical approach to increasing the number of detectors within a given focal plane area. This paper presents the fabrication and characterization of arrays of multichroic pixels of antenna-coupled transition-edge-sensor (TES) bolometers⁹⁻¹¹ with bands centered in the atmospheric windows at 95 GHz, 150 GHz and 220 GHz. The detector arrays will be used in the third generation CMB receiver of the South Pole Telescope, SPT-3G¹², which will be deployed in December 2016.

Section 2 of this paper provides an introduction on the SPT-3G focal plane and multichroic pixel architecture, Section 3 gives an overview of the monolithic fabrication process of the detector arrays, Section 4 describes cryogenic testing of the fabricated arrays, including results of optical and thermal characterization of multiple detector arrays, and Section 5 contains conclusions.

2. SPT-3G FOCAL PLANE AND MULTICHROIC PIXEL ARCHITECTURE

2.1 SPT-3G focal plane

The SPT-3G focal plane is comprised of ten hexagonal arrays of detectors fabricated on 150 mm (100) Si wafers. Each array of detectors contains 269 multichroic pixels plus two pixels used to pattern the alignment marks required for lithography. Each pixel contains six TES detectors, sensitive to three frequency bands and two linear polarizations, for a

total of 16,140 detectors in the focal plane. This is over an order of magnitude increase in the number of detectors fielded in the previous experiment on the SPT, SPTpol¹³.

To read out the detectors, pairs of 5 μm wide Nb traces, with a 5 μm pitch, are routed from each detector to bond pads located the edges of the hexagonal arrays. Deep-access automatic wire bonding is used to connect the bond pads on the wafer to the readout system. To individually read out the 16,140 detectors while reducing the total cryogenic thermal loading, cold component complexity, and cost of the system, a digital frequency domain multiplexing (fMUX) system has been developed^{21,22}. The fMUX system reads out 64 TESs using a single pair of wires.

2.2 Multichroic pixel architecture

The SPT-3G multichroic pixel design builds upon prior development of multichroic, dual-polarization bolometers at UC Berkeley^{10,11,14,15} and TES detectors at Argonne National Laboratory^{16–18}. An overview of one of the multichroic pixels and its components is shown in Fig. 1. As shown in Fig. 1 (a), each pixel contains a self-complementary, log-periodic, broadband, sinuous antenna that is sensitive to linear polarizations^{19,20}. The mm-wave signal received by the sinuous antenna is capacitively coupled to a Nb microstrip transmission line that runs along the metallic arms of the antenna (Fig. 1 (b)). Three-pole quasi-lumped-element filters split the signal into three spectral bands centered around 95 GHz, 150 GHz and 220 GHz. To route the signal between the antenna and their respective bolometers, Nb/SiO_x/Nb cross-over structures, as shown in Fig. 1 (c), are required. After the spectral bands are defined by the lumped-element filters, each of the individual signals running in the microstrip transmission line (three bands and two linear polarizations) is routed to its respective bolometer island, where it is thermalized using a 20 Ohm Ti/Au load resistor. The change in temperature of the island is then sensed by a Ti/Au (200/20 nm) TES. The 20 nm Au layer in the TES acts as a protection layer to prevent oxidation of the Ti. A 750 nm thick layer of Pd is deposited on the bolometer island to increase the heat capacity to stabilize the detector. The bolometer islands are released by removing the Si substrate underneath. This provides thermal isolation between the island and the main Si substrate. A thermal weak link between the island and the thermal sink is defined by four long, narrow legs, as shown in Fig. 1 (d). A detailed view of the components in the bolometer island is shown in Fig. 1 (e).

3. FABRICATION PROCEDURE

Each of the ten detector arrays that will populate the SPT-3G focal plane is fabricated on a 675 μm thick, 150 mm diameter, silicon (100) wafer coated with a 1 μm layer of Low Stress Nitride (LSN) deposited by low-pressure chemical vapor deposition (LPCVD). All layers are patterned using stepper-based lithography, except for the array-level wiring layout, which is patterned by optical lithography using a contact mask aligner. The fabrication of the SPT-3G detector arrays is carried out at the Materials Science Division and the Center for Nanoscale Materials at Argonne National Laboratory. The step-by-step fabrication process flow of the detectors is presented in Fig. 2.

We start the fabrication by etching two stepper alignment marks in the LSN. These marks are required for processing the wafers during the 13 lithography steps involved in the fabrication process. An overlay between layers better than 150 nm is obtained. After defining the alignment marks, a 300 nm Nb ground layer is deposited and etched to define the antenna, filters, and slots for each of the six bolometers in a pixel. This is followed by the deposition of a 500 nm layer of SiO_x by reactive sputtering at 250 C. The SiO_x layer is the dielectric for the microstrip transmission lines and filter capacitors. In a previously reported version of our fabrication process¹⁸, the deposition of the SiO_x layer was immediately followed by deposition of the Nb top layer for the microstrip and the array-level wiring. Next, the Ti/Au TES and load resistor were deposited, defined by lift-off, and later connected to the Nb top layer using small (30 μm x 30 μm) Nb caps patterned together with Nb for the cross-over structures. This fabrication scheme allowed direct contact between Ti at the edges of the TES and the Nb leads. We found that the Nb-Ti contact resulted in a roughening of the TES surface, as shown in Fig. 3 (a). The nature of this Nb-Ti interaction is not well understood, and further attempts to understand the details are ongoing. Nonetheless, we found that placing a thin (30 nm) Au barrier/protection layer over the edges of both the TES and load resistor prevents the roughening, as shown in Fig. 3 (b).

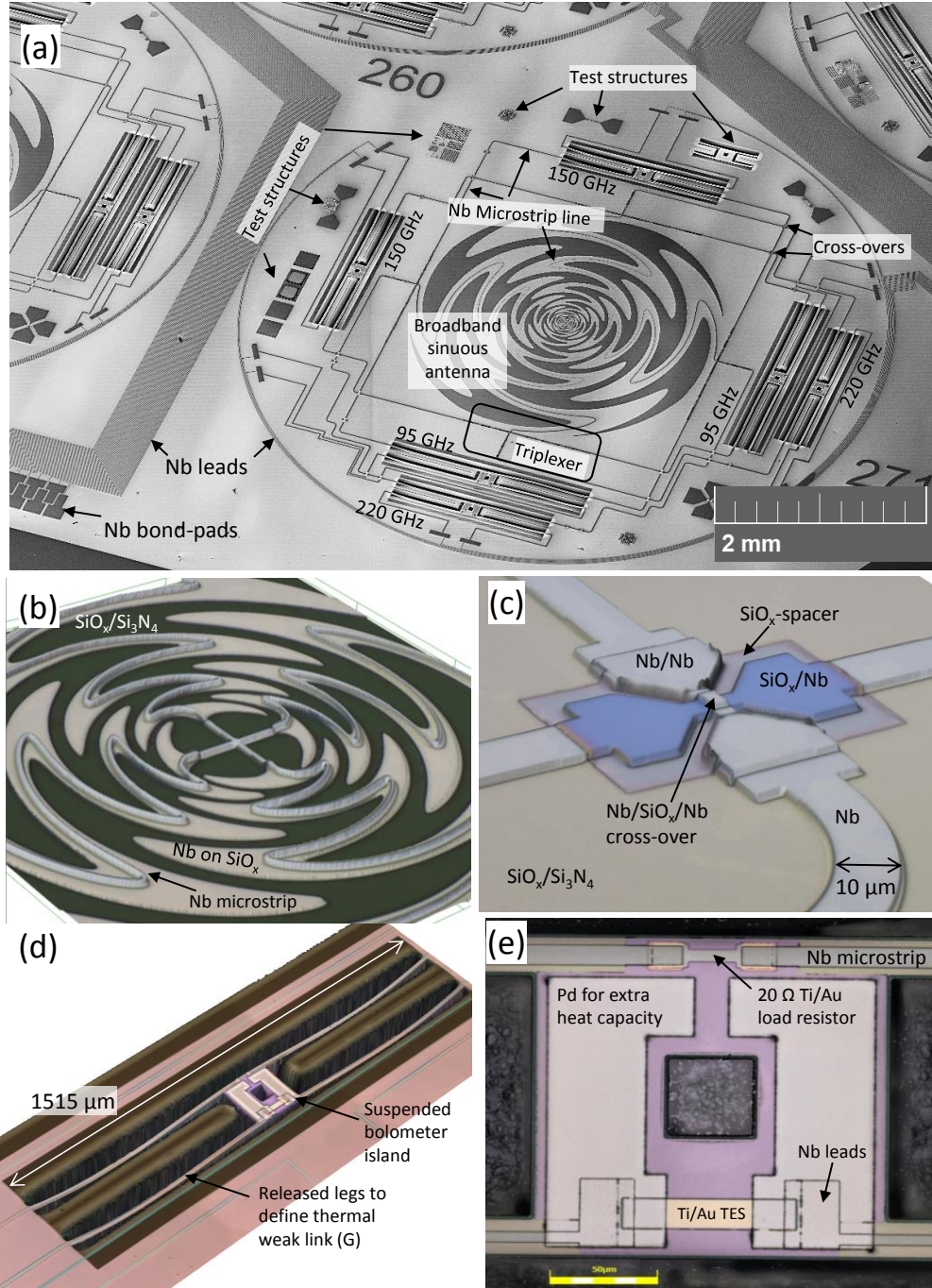


Figure 1. (a) Overview of a multichroic pixel showing the sinuous antenna coupled through a microstrip transmission line to six TES bolometers. (b) Laser micrograph of the center of the sinuous antenna. The CMB signal received by the antenna capacitively couples to the microstrip transmission line running on the metallic arms of the antenna, which serve as the ground plane of the microstrip. (c) Laser micrograph of a Nb/SiO_x/Nb cross-over structure used to route the signal from the antenna to the bolometers. (d) Laser micrograph of one of the 220 GHz detectors. The Si under the bolometer island and each of the four the legs is removed to define the weak link between the bolometer island and substrate. (e) Top view of the bolometer island. The signal brought by the microstrip from the antenna is absorbed in a 20 Ohm Ti/Au (40 nm/5 nm) load resistor. The power dissipated by the resistor is measured by the Ti/Au (200 nm/20 nm) TES which is voltage biased in the transition.

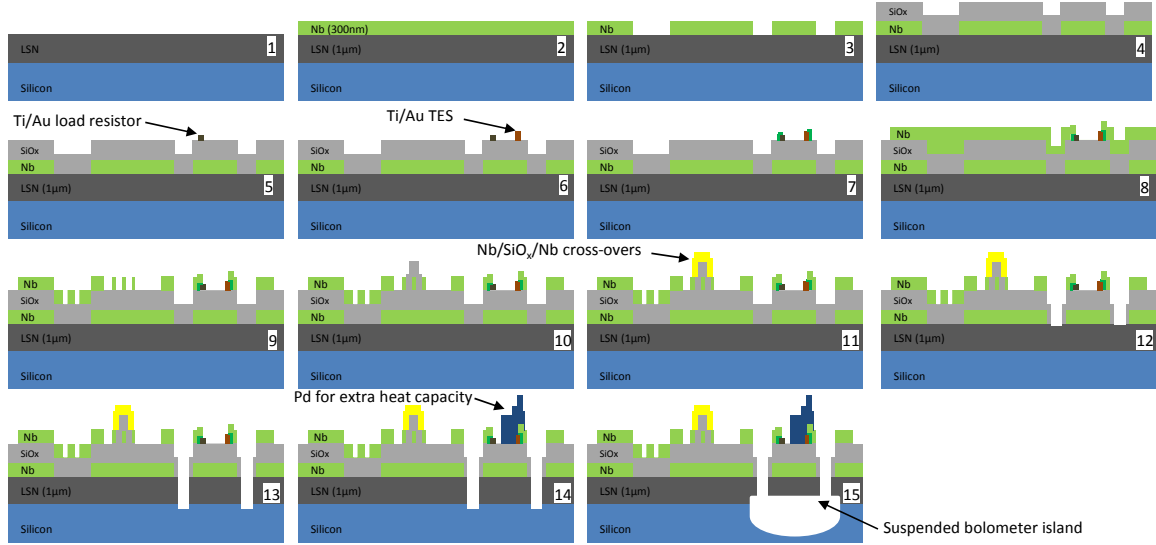


Figure 2. 1) Define alignment marks on LSN substrate. 2) DC sputtering of Nb ground plane. 3) Etching of Nb ground plane to define antenna, three-pole filters and detector slots. 4) Deposition SiO_x by reactive sputtering; 500nm dielectric layer for the microstrip. 5) Lift-off of 20 Ohm Ti/Au load resistor. 6) Lift-off of Ti/Au TES. 7) Lift-off Au caps to protect the edges of the resistor and the TES. 8) Deposition of Nb top layer. The contacts of the Nb to the resistor and TES are defined by lift-off, while the microstrip and leads are defined by an etching process. 9) Etching of Nb to define the microstrip top layer, as well as the array level wires and the bond-pads at the edges of each wafer. 10) Room-temperature RF sputtering and lift-off of SiO_x spacers for cross-over structures. 11) Lift-off of Nb for top layer of cross-over structures. 12) Etch trenches in the SiO_x to define the legs of the bolometers. 13) Etch SiNx from the trenches to define the legs of the bolometers and expose the Si surface. 14) DC sputtering and lift-off of Pd to add heat capacity to the bolometer island. 15) Dice wafers into their final hexagonal shape, XeF_2 etch of the Si under the island and legs and final O_2 cleaning step to remove left-over photoresist from the surface of the wafers.

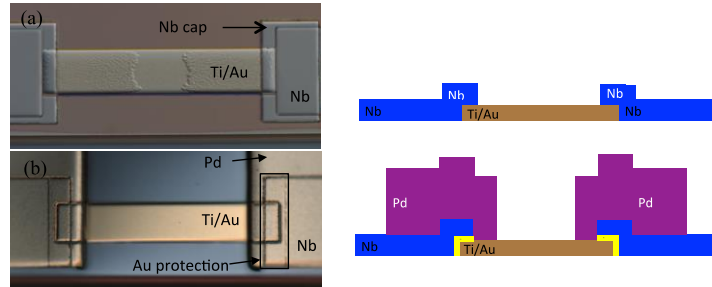


Figure 3. Top and cross-sectional views of the Ti/Au TES to Nb leads connection with (a) and without (b) Nb caps. (a) The TES and Nb leads are connected using Nb caps, allowing for direct Ti-Nb contact at the edges of the TES. A roughening of the TES is observed. (b) Au caps are deposited to protect the edges of the TES, preventing any direct Ti-Nb contact. The Nb leads are then deposited as part of the top Nb layer used for the microstrip and array level wiring, removing the need for Nb caps. No roughening of the TES surface is observed for this configuration.

Figure 4 (a) shows $R(T)$ curves obtained for the cases in which the TES and Nb leads were contacted using Nb caps without using any protection layer. In general, these TES devices showed broad transitions (~ 50 mK) with step-like features. As shown in Fig. 4 (b), the broadening of the transition and the step-like features are greatly reduced when Au caps are used to prevent any direct contact between the Ti in the TES and the Nb leads. In our current process, the Ti/Au TES and load resistor films are deposited after the SiO_x layer, then the contact areas are covered with Au protection caps.

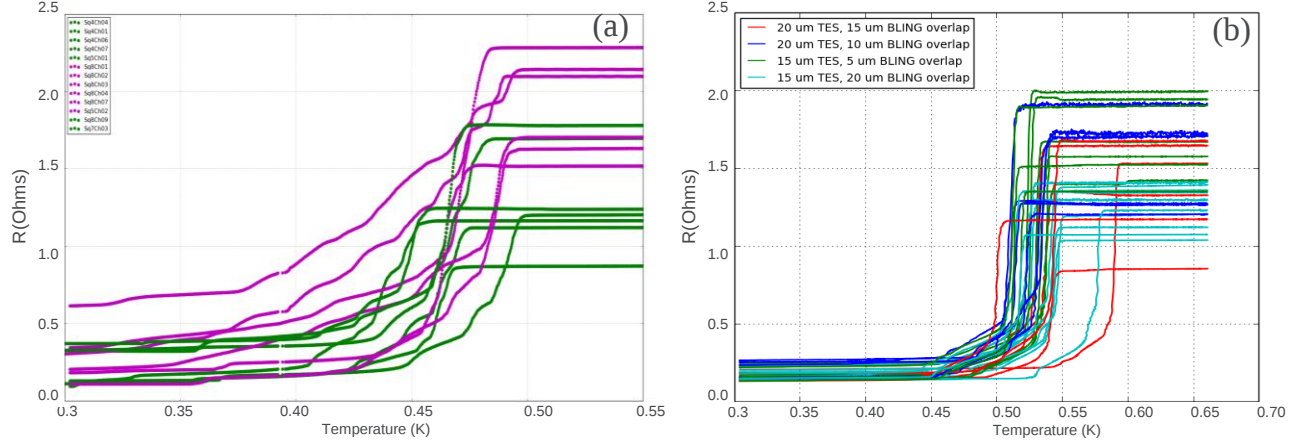


Figure 4. Comparison of the $R(T)$ curves for detectors prepared with and without allowing Ti-Nb contact. (a) The TES is connected to the leads using a layer of small ($30\ \mu\text{m} \times 30\ \mu\text{m}$) Nb caps, direct Ti-Nb contact is allowed. (b) Au caps are deposited to protect the edges of the TES. The Nb leads are then deposited such that direct Ti-Nb contact is avoided.

Following the deposition of the protection caps, the Nb top layer is deposited and patterned using two lithography steps. First, the connection to the TES and resistor is defined by lift-off. Next, the microstrip and array-level wiring are defined by a CHF_3/SF_6 RIE etching process. The cross-over structures shown in Fig. 1 (c) are fabricated by two successive lift-off processes. First, a $350\ \text{nm}$ SiO_x dielectric spacer (deposited at room temperature) provides insulation where one Nb top wire must cross over another. Next, a $400\ \text{nm}$ Nb jumper completes the cross-over connection. To guarantee good Nb-Nb contact, the deposition of the final Nb layer of the cross-overs is preceded by a 30 minute back-sputtering process using a $25\ \text{W}$ Ar plasma. This process removes any Nb oxide from the surface of the bottom Nb layers of the cross-overs. Following the fabrication of the cross-overs, trenches are opened to the Si substrate to define the four legs that will hold the island after release. These trenches are opened by two RIE CHF_3/Ar based etches, in which $500\ \text{nm}$ of SiO_x and $1\ \mu\text{m}$ of LSN are removed to expose the Si layer around the legs and island. Next, a $750\ \text{nm}$ thick layer of Pd is deposited on the island to add heat capacity. At this point, an additional lithography step is performed to clean the trenches around the legs and prepare the bolometer island for releasing. Before releasing the islands, the wafer is diced into the final hexagonal shape using a diamond saw. Next, the bolometer islands and their legs are released by removing the Si underneath using XeF_2 isotropic chemical etching. This step is followed by a final O_2 RIE process to remove resist from the surface of the wafer. At this point, the bolometer island looks like a membrane suspended by 4 legs, each approximately $20\ \mu\text{m}$ wide and $600\ \mu\text{m}$ long. Fig. 1 (d) shows one of the released detectors after fabrication is completed. Additional details in the fabrication process, as well as the components of the SPT-3G multichroic pixels, have been presented elsewhere¹⁸.

4. FULL ARRAY TESTING RESULTS

The laboratory cryogenic characterization of the SPT-3G detector arrays is carried out in multiple test beds by institutions involved in the SPT-3G collaboration, including Fermilab, Argonne National Laboratory, the University of Chicago, UC Berkeley, University of Toronto, Case Western Reserve University and University of Colorado Boulder. In this section we present results of the thermal and optical characterization of three selected SPT-3G detector arrays (arrays are labeled as W followed by a two-digit number). The arrays presented here are part of a set of nearly 30 research and development wafers that have gone through the full fabrication process. Through several iterations, we have incorporated the testing results obtained from these research and development arrays to get to the baseline fabrication process presented in Fig. 2. The arrays whose results are presented here sample the general performance of this batch of research and development wafers. We chose to incorporate them in this manuscript either because they were characterized in greater detail (W69), or because they represent the efforts we have undergone to get our detectors operating according to design (e.g., by testing Ti/Au TES films with different expected values of T_c).

4.1 Thermal characterization

To characterize the thermal properties of our detectors, the saturation power is measured at stage temperatures (T) ranging between the bath temperature ($T_b \sim 280$ mK) and the TES T_c (~ 550 mK). The saturation power at a given stage/wafer temperature is

$$P_{tot} = K * (T_c^n - T^n) \quad (1),$$

where K is a constant that depends on the geometry and material properties of the legs supporting the island to the substrate, and the value of the exponent n indicates the thermal carrier in the weak link (legs); $n=1$ if electrons are the main thermal carriers and $n=3$ if phonons dominate. Fitting P_{tot} vs T to Eqn. (1) yields K , n , and T_c ($P_{tot}=0$). The thermal conductance of the legs is

$$G(T_c) = \frac{dP_{tot}}{dT} = nKT_c^{n-1} \quad (2)$$

and the phonon noise equivalent power (NEP) in the TES is

$$NEP = \sqrt{\gamma 4k_B T_c^2 G} \quad (3),$$

where k_B is Boltzmann's constant and γ is a number between 0.5 and 1 that accounts for the temperature gradient along the legs supporting the TES island. We assume $\gamma = 0.5$. Fig. 5 shows $I(V)$, $R(T)$ and $P_{tot}(T)$ curves for one of our detectors. This device has $NEP = 3.3 \times 10^{-17} \text{ W}/\sqrt{\text{Hz}}$.

Figure 6 shows a summary of the thermal performance of several detector wafers. Our target T_c is 510 mK. We have found that T_c for Ti/Au TESs is affected by the normal processing occurring during fabrication. In general, we see a decrease in T_c when wafers are heated after the TES films are deposited. A decrease in T_c between 50 mK and 100 mK has been observed for heating of the TES at 185 C for 5 to 30 min. Intermetallic diffusion of Ti into Au is a possible mechanism for the change in T_c with heating.

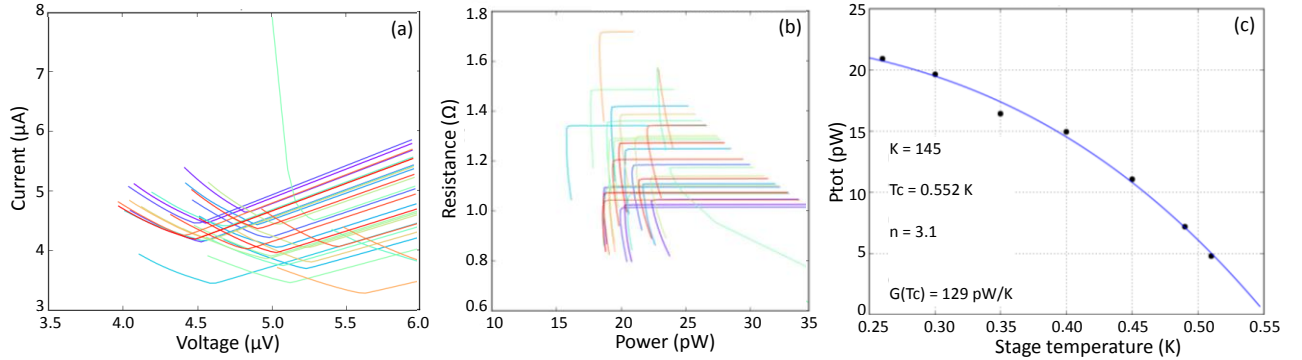


Figure 5. Measurement of the bias power as a function of the stage temperature for one of our detectors. (a) I - V curves, (b) TES resistance as a function of bias power. (c) Values of P_{tot} obtained from the I - V curves as a function of stage temperature. The blue line in (c) is the fit obtained using Eqn. (1). The fitted values of K , n , and T_c are shown in the legend. $G(T_c)$ in the legend is calculated using Eqn. (2). The colors of the lines in (a) and (b) correspond to different detectors in the array.

For W64 and W69, we avoided any heating above 110 C to the wafer after the TES was deposited. In consequence, T_c for W64 and W69 is higher than our target T_c . Considering that heating the TES lowers T_c , we are currently investigating the possibility of using a controlled heating process to tune T_c after the TES films are deposited. W77 has Ti/Au (50/30 nm) TESs, instead of the Ti/Au (200/20 nm) TESs in W64 and W69, resulting in a much lower T_c . W77 also shows a large scatter in T_c , indicating that thinner Ti/Au TESs can be easily affected by non-uniformities in the deposition and lift-off of the bilayer.

As shown in Fig. 6 (b), the thermal conductivity factor (K) of our detectors is centered on $150 \text{ pW}/K^n$. These results are in good agreement with the design values for K , which are based on the 95 GHz detectors fabricated at ANL for the SPTpol receiver¹⁶. The extracted values of n are around 2.7, indicating that phonons are the main thermal carrier in the legs of the bolometers. Fig. 6 (c) presents the distribution of the saturation power (P_{tot}) measured for our detectors. The target saturation powers for the three different spectral bands are: 10.6 pW (95 GHz), 16.0 pW (150 GHz) and 21.0 pW (220 GHz). These values are equal to two times the expected optical loading during normal operation, assuming an overall optical efficiency of 85%. As expected from Eqn. (1), lower values of P_{tot} are observed for detectors with lower values of T_c . P_{tot} values for W77 are about 10 pW lower than the target values, while P_{tot} values for W64 and W69 are in the order of 5 to 10 pW higher than our target values. Considering the values of T_c , K , n and G presented in Fig. 6, our current efforts are focused fabricating detectors with TES films with T_c of 510 mK to meet the P_{tot} requirements.

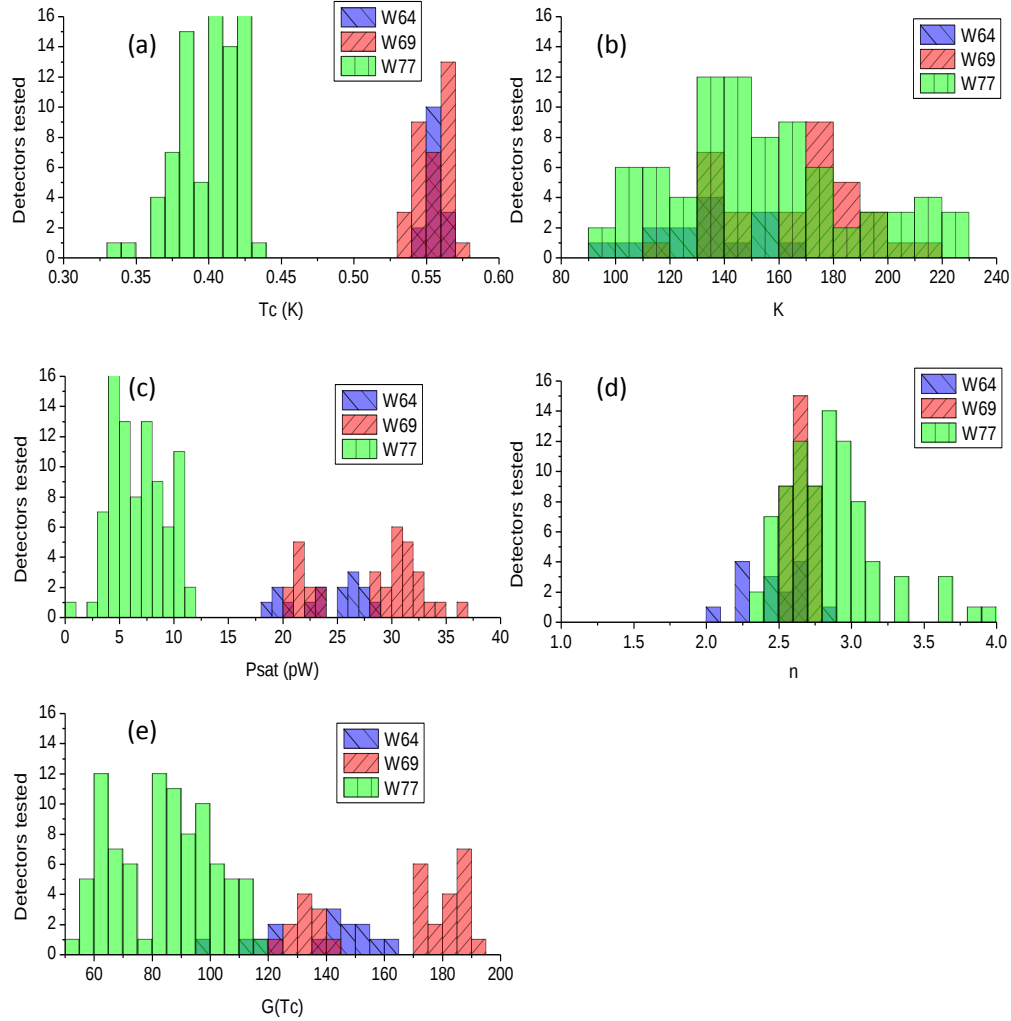


Figure 6. Summary of the thermal characteristics of array wafers W64, W69 and W77.

Figure 7 shows the spectral response for one of the SPT-3G detector arrays, measured using a Fourier Transform Spectrometer (FTS). The average spectral response is similar to Sonnet simulations for a 500 nm thick SiO_x dielectric film, which is the nominal dielectric thickness of the wafer tested. Similar results have been observed for at least four other array wafers, indicating good reproducibility in the antennas, microstrip and filters. The dips observed in the FTS response in the middle of the bands are believed to be partially due to reflections in the optical testing set-up rather than problems with the antenna coupling.

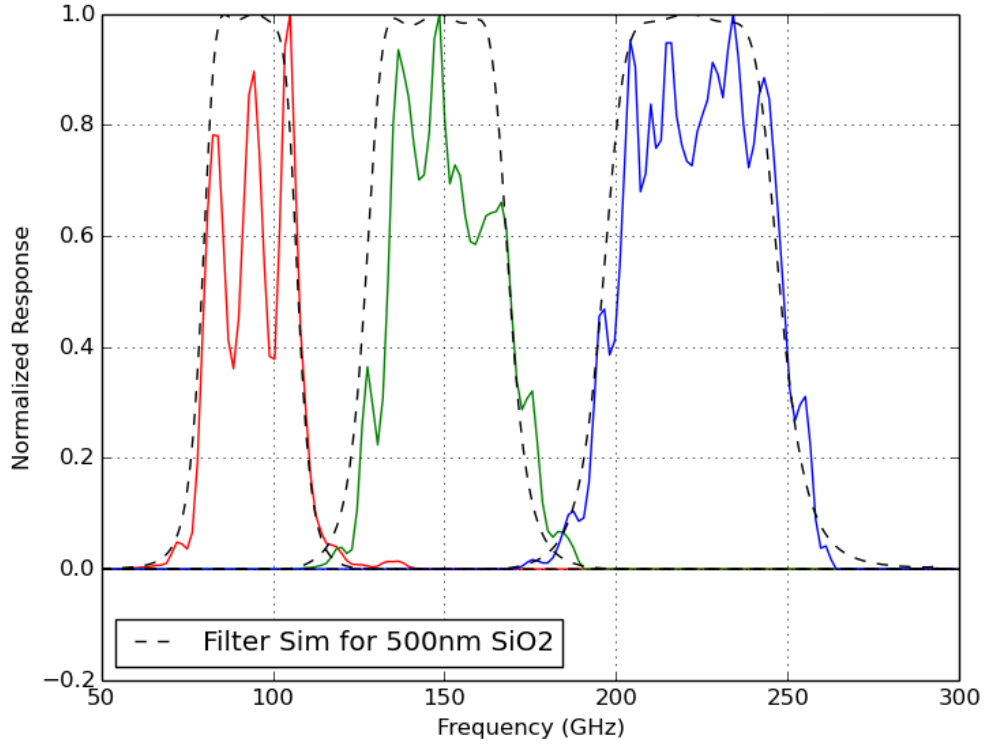


Figure 7. Average of measured bands for detectors on array wafer W69 (solid lines) and Sonnet simulations (dashed lines).

The optical efficiency (η) of the detectors was obtained by measuring the detector bias power vs. temperature of a load in front of the cryostat window and comparing with the expected incident power $P_{Load} = \eta k_B T_{Load} \int f(\nu) d\nu$. P_{load} was calculated using the average spectral response for the detectors in each band. The load was an aluminum-backed sheet of HR-10 absorber at room temperature (293 K), or soaked in liquid nitrogen (77 K) or liquid argon (87 K). Results are shown in Fig. 8.

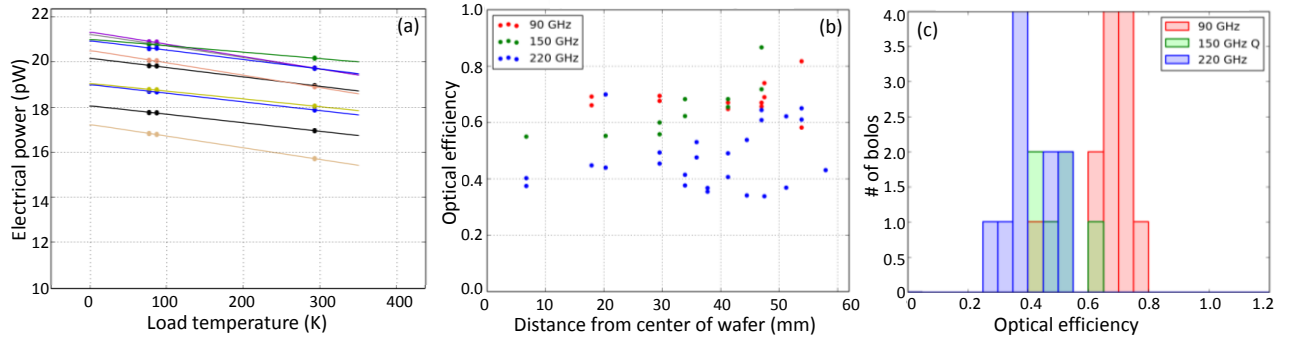


Figure 8. Optical efficiency of SPT-3G detectors. (a) P vs. T_{load} curves for 220 GHz detectors. The colors of the lines in correspond to different detectors in the array. (b) Optical efficiency as a function of the position of the detectors in the wafer for detectors in all three bands. (c) Histogram of optical efficiency.

The optical efficiency ranges from 0.3 to 0.8, and no significant trend is seen with position on the wafer.

Testing of SPT-3G detector arrays is ongoing, with results feeding back into the fabrication to tune the detector parameters.

5. CONCLUSION

We have described the fabrication and characterization of large arrays of dual-polarized, antenna-coupled, multichroic, TES bolometers for CMB measurements. These detectors will be used for the third generation receiver of the South Pole Telescope, SPT-3G. $T_c \approx 550$ mK was measured for detectors fabricated using our baseline Ti/Au (200/20 nm) TES. Detectors with a thinner Ti/Au (50/30 nm) TES showed $T_c \approx 400$ mK with a bigger scatter. By measuring I-V curves of the detectors at stage temperatures between 280 mK and 550 mK, the thermal properties K , n , and G were extracted. $n \approx 2.7$ indicates that phonons are the main thermal carriers in the legs of the bolometers. The saturation power for the detectors with Ti/Au (200/20nm) TESs is 25-30 pW, which is about 10 pW higher than the target values. Lower saturation power is measured for TESs with lower T_c , so T_c provides an effective control for tuning the saturation power. The detectors tested have values of $K \sim 150$ pW/ K^n and $G \sim 130$ pW/K, with $T_c = 550$ mK, which corresponds to $NEP \approx 3.3 \times 10^{-17} \text{ W}/\sqrt{\text{Hz}}$. The spectral response of our detectors is in good agreement with the design for all three bands, 95 GHz, 150 GHz and 220 GHz, and the optical efficiency is between 30 and 80%, with most detectors at $\sim 60\%$. Further characterization of the detectors is ongoing, and current fabrication efforts are focused on tuning the saturation power. The SPT-3G receiver will be deployed in December 2016.

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