Final Report

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Disclaimer

Executive Summary:

The “Module Embedded Micro-inverter Smart Grid Ready Residential Solar Electric System” program is focused on developing innovative concepts for residential photovoltaic (PV) systems with the following objectives:

1. An Innovative micro-inverter topology that reduces the cost from the best in class micro-inverter and provides high efficiency (>96% CEC - California Energy Commission), and 25+ year warranty, as well as reactive power support.
2. Integration of micro-inverter and PV module to reduce system price by at least $0.25/W through a) accentuating dual use of the module metal frame as a large area heat spreader reducing operating temperature, and b) eliminating redundant wiring and connectors.
3. Micro-inverter controller handles smart grid and safety functions to simplify implementation and reduce cost. A central monitoring/grid interface point of contact will be used to communicate and coordinate functions of all micro-inverters in the system and relay grid commands to the micro-inverters in smart grid setup.

The first budget period resulted in a concept design for the micro-inverter topology and a lab demonstration of the basic functionality and grid support capability

In the second budget period a modified micro-inverter topology suitable for low voltage mc-Si panels was developed, design and build of an integrated ACPV module and verification of system performance were completed. Reliability testing has been performed to assess component response to stresses and testing for IEEE1547 standards has been completed as well as preliminary tests for UL1741/1703 compliance. Further, a cost estimate for the micro-inverter has been performed.

In phase III the micro-inverter was demonstrated in the field with two different panel structures and testing of multiple micro-inverters was performed to verify grid support functions. The commercialization activity has resulted in establishing a Licensing agreement for the residential PV technologies to SPARQ Systems Inc., which will act as a commercial partner for the commercial development of technologies developed in this program.

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1. Background:

Solar electric systems based on the integration of micro-inverters and PV modules now represent ~8% of the U.S. residential market and offer many advantages related to safety, performance, and simplified installation. Deficiencies in the performance and mechanical configuration of existing micro-inverters along with functional redundancies present barriers to achieving an unsubsidized residential system cost ($3.00/W) and corresponding levelized cost of electricity (LCOE=$0.13/W) competitive with average U.S. retail electricity price.

A detailed, multi-objective study was performed to down select the topology that will be used as the foundation for the new generation micro-inverter optimized for residential PV applications. As a result of the detailed design analyses and trade-off studies, the GE team down-selected one micro-inverter topology to be used for this program. The implementation of micro-inverter prototype is finished and tested, including the hardware, control and protection software and communication interface. System reliability, compliance and cost were analyzed and the developed systems were installed in two demonstration sites with different panel types.

This work resulted in identifying a commercialization path for the micro-inverter and AC PV panel development.

2. Introduction:

The objective of this project is to develop an innovative power inverter topology that provides state-of-the art efficiency, 20+ year reliability, and support for bi-directional power flow (future reactive power) without added cost. Integration of micro-inverter and PV module that a) accentuates dual use of the module metal frame as a large area heat spreader reducing operating temperature and heat sink cost, and b) eliminates redundant wiring and connectors. Micro-inverter smart grid and safety functions internal part of the micro-inverter's control the for system cost optimization.

Phase 2 was primarily focused on the design and implementation of micro-inverter, integration of the ACPV module and performing cost, reliability and manufacturability analysis of the developed system. Furthermore, compliance with IEEE 1547 standard and preliminary evaluation of compliance with UL1741/1703 standards was performed.

Design and testing of the micro inverter is performed at GE Global research and external contractors were used for other aspects of development:

- Amphenol: for building and consultation on the micro-inverter enclosure and wiring system
- Flextronics: for cost and manufacturability analysis
- Motech: PV panel supplier
- Intertek: preliminary UL1741/1703 testing
- GE Critical power: reliability assessment through highly accelerated life testing

In Phase 3 several micro-inverter units were built for field demonstration. Two demo sites were setup: the first in Schenectady, NY where a 2.55kW system was installed

and the second in Hillsboro, OR, where a 2.8kW system was installed. The AC PV panel build was done with two different panel manufacturers, Motech and SolarWorld.

Testing of micro-inverters and building of AC PV panels were performed at GE Global Research and external contractors were used for other aspects of development and demonstration:

- Amphenol: for building and consultation on the micro-inverter enclosure and wiring system
- Innovative Test Solutions for Schenectady, NY demo site setup.
- SolarWorld: PV panel supplier and Hillsoboro, OR demo site setup.
- Motech: PV panel supplier.

Table 1: Main project tasks

Phase	SOPO Taks #	Item: Task=T Milestone=M Deliverables=D	Task Title or Milestone/Deliverable Description	Task Completion Date	% Complete	Progress Notes
1	1	T	Evaluate and down-select embedded micro-inverter topologies	3/30/2012	100%	
1	2	T	Conduct the embedded micro-inverter conceptual design and testing	11/15/2012	100%	
1	3	T	Configure photovoltaic panel and smart grid emulator	8/30/2012	100%	
1	4	T	Evaluate safety, control and grid support functions	11/15/2012	100%	
1	5	T	Conduct conceptual design of the functional circuit including Alternating Current (AC) photovoltaic module	11/15/2012	100%	
2	6	T	Design and build the embedded micro-inverter prototype	3/31/2014	100%	Build of final units transitioned to phase 3

2	**7**	**T**	Integrate and test AC photovoltaic module system	4/4/2014	100%	
2	**8**	**T**	Review system compliance, reliability, manufacturability, and cost	4/4/2014	100%	.
3	**9**	**T**	Design, Build and Install Pilot Demonstration Systems	2/28/2015	100%	
3	**10**	**T**	Operate demo and Commercialization	4/15/2015	100%	

3. Project Results and Discussion:

3.1 Significant Accomplishments by Task:

Task1: Evaluate and down select embedded micro-inverter topologies

- Conducted preliminary literature search to identify potential candidate topologies. Several topologies of interest were selected for further evaluation.
- Candidate Volt/Var control algorithms and requirements were identified and will be analyzed in detail in the later stages of Phase I.
- Extended the pool of candidate PV module technologies to include all high voltage modules (Si Sliver, thin film). Detailed analysis of the system optimization based on different modules will be performed in the next Quarter.
- Following a detailed analysis of the state-of-art and relevant standards, and based on the proposed performance parameters the team has defined a set of requirements (Cost, Efficiency, Reliability, Volt/Var support …) to guide the design process.
- Based on a thorough multi-parameter analysis of key requirements and following a detailed simulation study the GE team has selected the topology to be developed and prototyped in the next stages of the project.

Task2: Conduct the embedded μ-inverter conceptual design and testing

- Conduct conceptual design of the micro-inverter
- Benchmark micro-inverter controller
- Create BOM and estimate cost
- Build breadboard micro-inverter
- Test bi-directional power capability
- Lab demonstration for 96% efficiency and Volt/Var support

Task 3: Configure photovoltaic panel and smart grid emulator

- Grid emulator configuration for smart inverter system function testing is finished.
- Report on PV panel and grid emulator is finished and submitted to DOE

Task 4: Evaluate and design the functional circuit including ACPV with safety, control and grid support functions

- EVSE controller board was modified to work with the micro-inverter system.
- Grid support functions/algorithms of the Smart Breaker box have been developed.
- Control and communication functions were developed and tested.

Task5: Conduct conceptual design of the PV functional circuit including AC photovoltaic module

- Conceptualized the micro-inverter mechanical packaging
- 3D model constructed
- Part losses established

Task 6: Design and build the embedded micro-inverter prototype

- Finish the PCB for the Si-module version
- Tested the state machine algorithm with the trip zone protection
- Tested Zigbee communication with the new Digi Xbee chip on the new board
- Verified system functionality in closed loop operation for the Si-module version.
- Analysis of optimal operating conditions for the input resonant stage and inverter stage to minimize losses
- Performed preliminary efficiency tests.
- Performed preliminary EMI testing.
- Updated bill of materials based on various test results.

Task 7: Integrate and test AC photovoltaic module system

- Completed design and build of micro-inverter enclosure.

- Completed design and build of DC connectors and AC connectors.
- Completed design and build of AC harness
- Built and tested 7 units that were sent out to Amphenol for packaging. Two units will be potted and the rest will be placed in the enclosure.
- Defined scope of work (SOW) with Motech in order to remove the junction box and host the mountable dc connector to the micro-inverter prototype. Testing to commence upon receiving packaged units from Amphenol.
- Completed preliminary testing of UL1741/1703 testing at Intertek.

Task 8: Review system compliance, reliability, manufacturability, and cost

- Completed the build, instrumentation and testing of two units in temporary enclosures for highly accelerated life testing (HALT).
- Finalized HALT testing document and test setup with GE Critical Power
- Complete HALT testing of two units at GE Critical Power facility in Plano, TX.
- Completed reliability calculations for the redesigned micro-inverter.
- Completed cost analysis with Flextronics.

Task 9: Design, Build and Install Pilot Demonstration Systems

- Completed the build of 30 micro-inverter units
- Resolved the voltage breakdown issue identified by Intertek during testing
- Completed implementation of micro-inverter communication protocol
- Completed build of modified enclosures
- Completed micro-inverter integration with both Motech and SolarWorld panels
- Completed installation of a 2.55kW and a 2.8kW system.

Task 10: Operate Pilot Demonstration System

- Completed testing of IEEE 1547 standard compliance and reactive power support
- Collected and analyzed the data off of the two demo sites
- Completed a licensing agreement of the micro-inverter technology to SPARQ Systems Inc. and currently working with SPARQ Systems on shaping commercial opportunities

Task 11: Project Management Task:

- Identified resources for the project and established the baseline project plan, including all tasks, subtasks, milestones, deliverables, and resource allocation. Phase II is divided into 3 tasks and 14 subtasks.
- Identified tools and platforms for various subtasks. Licensed necessary software tools (MS Project, PLECS, Matlab). Identified and scheduled hardware resources within/outside of GE Global Research.
- Quarterly project review meetings have been established between DOE and GE.
- Collaboration, NDA, scope of work and legal documentation was established with different vendors Amphenol, Motech and Flextronixs.
- Principal Investigator and project team members attended several conferences and meetings and generated IP including:
    i. Sunshot forum where the poster on the work done and planned under the contract was presented at High Penetration Solar Forum 2013 at San Diego, CA.
    ii. SPI 2013 conference in Chicago, USA on October 21st.
    iii. IEEE-PES ISGT 2014 in Washington DC on Feb. 19th, 2014, and made panel presentation on project progress.
    iv. Sunshot Summit 2014, where the project progress was presented in Anaheim, CA.
    v. Paper presentations on micro-inverter system and circuit at IEEE-PVSC 2014, IEEE-ECCE 2014, IEEE-PVSC 2015.
    vi. Filed 8 patent applications on the micro-inverter circuit, control and ACPV panel mechanical aspects.

3.2 Detailed Technical Report

3.2.1 Task 1: Evaluate and down select embedded micro-inverter topologies

In this task a tradeoff study was performed to select the optimal micro-inverter topology. The work included analyzing the differences and advantages of thin film PV technologies, the trade-off between single-module and two-module micro-inverters in terms of the installation cost, annual energy yield and LCOE, A comparison of single-stage and two-stage architectures, highlighting the benefits and downfalls of both approaches. The GE team developed detailed simulation models of the selected topologies and investigated the circuits. Key metrics including efficiency and Volt/VAR support functions were also compared and analyzed. Cost and reliability were analyzed and results were also included in the tradeoff study.

As a result of the trade-off studies, the GE team down-selected one micro-inverter topology to be used for the rest of the program. The chosen topology is the LLC

resonant converter designed for two PV CIGS module connected in parallel with the partial power method followed by the Interleaved H-bridge inverter controlled with the team operation approach, referred as Topology 4 after the trade of study.

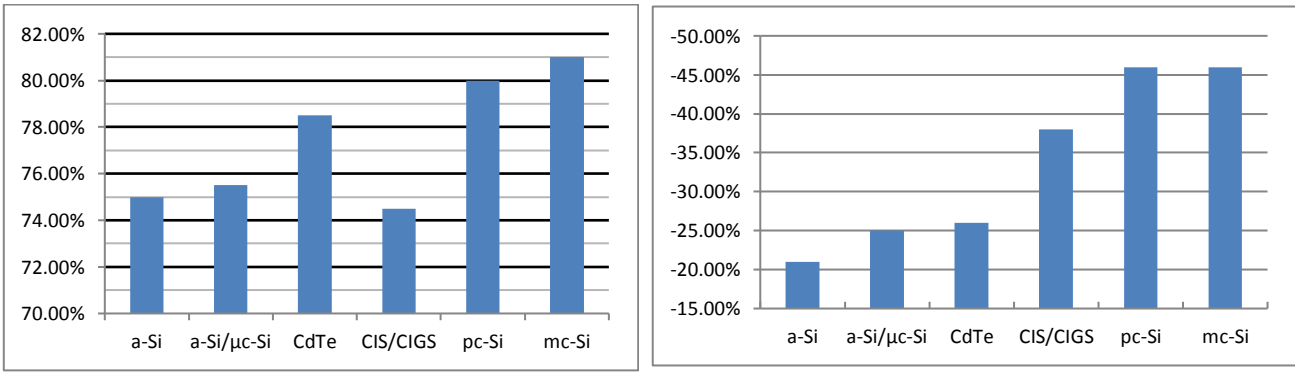
3.2.1.1 Thin Film Solar Modules

The last decade has seen a large growth of the thin-film PV industry due to the promise of significant cost savings. Thin-film technologies deploy thin layers of semiconducting materials on the order of only 2 µm thick deposited on robust substrates. The manufacturing processes used in this industry are well established and suited to mass production, which further reduces the costs. Semiconductors used to make thin-film PV cells range from silicon to tellurium and gallium. At this time, four thin-film technologies are being commercialized on a large scale:

1. amorphous silicon a-Si);
2. micromorphous silicon (a-Si/µc-Si);
3. cadmium telluride (CdTe);
4. copper indium (di) selenide (CIS) or copper indium gallium (di) selenide (CIGS).

Typical c-Si PV modules are characterized by low voltage/high current operation. In contrast, most of the thin-film modules operate at high voltages and relatively low currents, which offer advantages in string configurations. Thin-film modules typically also have lower power ratings resulting in a proportional increase in the number of modules.

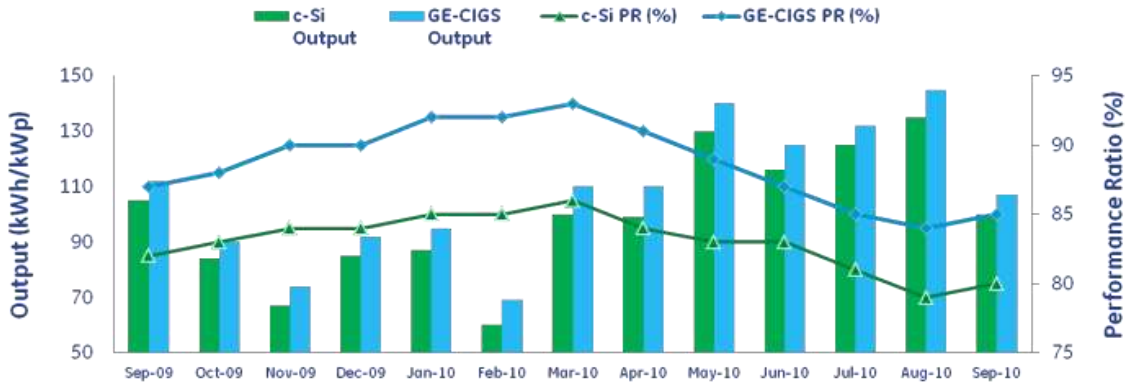
Figure 1 from [1] shows that the thin-film PV modules Vmp as a percentage of Voc ranges around 75%, whereas in the c-Si PV the average ratio is closer to 80%. This ratio is important because as it decreases, the voltage spread between Vmp and Voc increases, suggesting that array-to-inverter matching becomes more difficult.



a) V_{mp} as a percentage of V_{oc} b) Average temperature coef for P_{mp}

Figure 1: Comparative data for different cell technology

Due to the lower temperature coefficients than comparable c-Si modules (-0.44%/°C) thin-film products (-0.31%/°C) usually perform better at higher temperatures. During normal operation PV modules rarely work at constant operating conditions and the fact that the thin-film modules have a higher PTC-to-STC ratio (~94%) than standard c-Si modules (~89%) allow them to operate at higher temperatures, which in turn translates in a higher energy yield.



Site location: Japan CIGS: 2.25kW system c-Si: 4.20kW system 20° tilt

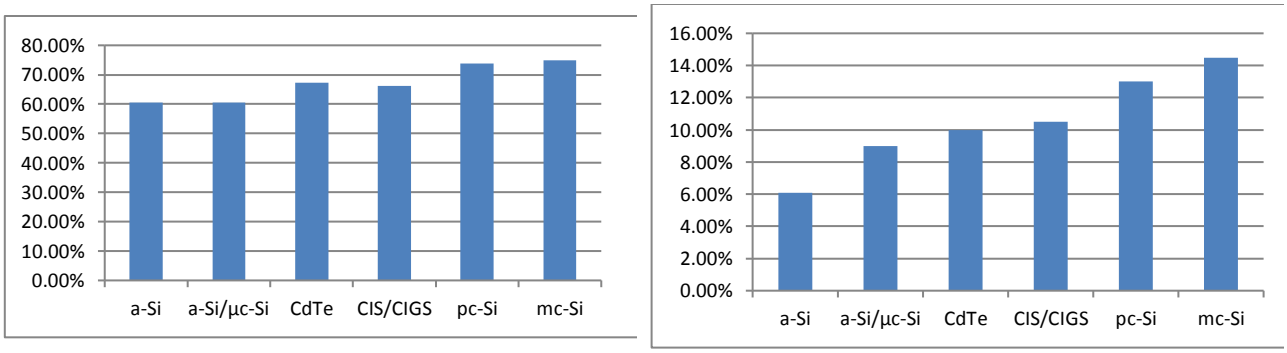
Figure 2: GE CIGS … ~10% □ energy yield vs. c-Si

After CdTe, and CIS/CIGS thin-film modules are removed from their boxes and exposed to sunlight, their output has been observed to increase by as much as 6%, which is a performance transient called dark soak, and stabilization can take up to a few weeks on large systems.

Another important performance characteristics is the fill factor (FF) which is defined as "the ratio of maximum power to the product of the open-circuit voltage and the short-circuit current."

$$FF = P_{mp}/(V_{oc}*I_{sc}) \quad (1)$$

In general, thin-film modules have higher series resistance than c-Si cells do, resulting in lower fill factors and efficiencies. Lower fill factors and rounded I-V curves mean that thin-film modules are relatively insensitive to non-optimal currents and voltages. Fill factors for different technologies are shown in Figure 3.a.



a) Fill factor b) Module efficiency

Figure 3: Fill factor and module efficiency for different cell technology

The fact that the thin-film modules are usually long and narrow helps with PV system design as it reduces the shading effects. They are typically mounted such that the long dimension of the cell is perpendicular to the ground. This kind of placement also helps to minimize the dirt deposits on the cells, thus reducing the maintenance requirements.

In terms of efficiency as shown on Figure 3.b, c-Si modules (13%-19%) still outperform the thin-film modules (6%-12%) but the gap is expected to be bridged over the next decade and both technologies should peak at approximately 20% efficiency.

Interfacing thin-film modules to the grid poses a different set of constraints when compared to traditional c-Si modules. For example, a large number of manufacturers require the use of negative-grounded inverters to prevent corrosion of transparent conducting oxide layer deposited on glass shields of most thin-film modules. This constraint prevents the use of many typical PV inverters such as bipolar, positive-ground, and transformerless architectures.

Prevalent application space for thin-film technologies has been in the utility-scale ground-mounted PV plant but lately the technology has started making inroads into the residential and commercial markets.

Some of the most mature thin-film technologies are CdTe and CIGS. Their main characteristics are listed below.

CdTe

The first technology to demonstrate lab-controlled operating efficiency higher than 15%, CdTe typically operates in the 9%-11% range [1]. As one of the first technologies to enter the market, CdTe modules represent a large portion of the installed base of thin-film modules. Some of the challenges still affecting the technology are related to lower power output, use of toxic heavy metals (Cd) in the manufacturing process, and vulnerability to moisture. Manufacturers are actively addressing these issues and next generation products are expected to minimize negative effects.

CIGS

The latest prototype modules using the CIGS technology have broken into the 20% efficiency range. However, most of the commercially available modules still operate in a much lower 9%-11% range. The first demonstration of this technology was in the mid-1980s but only recently it has garnered more attention due to the advances in the manufacturing processes that aim to reduce the high degradation rates of assembled CIGS modules. Figure 4 is showing the GE's CIGS module specifications for four different power levels.

		GE-CIGS140	GE-CIGS145	GE-CIGS150	GE-CIGS155
Maximum Power	Pmax(W)	140	145	150	155
Efficiency	%	11.4	11.8	12.2	12.6
Tolerance of Pmax		+10%/-5%			
Open circuit voltage	Voc (V)	109	110	110	108
Short circuit current	Isc (A)	2.10	2.10	2.10	2.20
Voltage at maximum power	Vmpp (V)	77	78	79	80
Current at maximum power	Impp (A)	1.82	1.86	1.90	1.95
Maximum system voltage	V DC	600V UL, 1000V IEC			
Limiting reverse current	A	7			
Maximum fuse rating	A	9			
Temperature Characteristics					
Temperature coefficient of Isc	%/°C	+0.01			
Temperature coefficient of Voc	%/°C	-0.30			
Temperature coefficient of Pmax	%/°C	-0.31			

Figure 4: GE-CIGS140 to CIGS155 Series Specification

3.2.1.2 Micro-inverter system

Cost vs. Energy Yield

The key benefit of distributed architectures results from their optimizers or micro-inverters mitigating module mismatch losses that are inherent in PV systems with the centralized inverter. Distributed MPPT at the module level effectively eliminates system losses due to the module mismatch. Distributed MPPT also minimizes shading losses. In the centralized inverter system, small amount of shading can dramatically reduce the system performance; in contrast, using the module level MPPT, any degradation in the performance of a module due to clouds, shadows or other obstructions, does not affect the performance of other modules, thus having a much smaller effect on the power harvested from the system as a whole.

Micro-inverters can deliver around 5% to 15% more power from the installation [3], and provide intrinsically safer systems. Currently, the retail price of the micro-inverter is around $1/W. By eliminating the central inverter (about $0.6/W) and high voltage DC cables, the additional cost of adding micro-inverter per module is mitigated. Combined with the higher energy yield and lower maintenance cost, micro-inverter PV systems can achieve up to 25% lower energy cost compared to the conventional central inverter system.

Nowadays dozens of companies worldwide offer or are developing distributed MPPT optimization solutions for PV systems including micro-inverters and DC-DC optimizers. Most of the micro-inverters are designed for single module use only. Recently several companies started to offer micro-inverters for dual modules, such as Enphase D380 twin-pack [4].

Compared to the single-module micro-inverter system, two-module micro-inverter system can provide a more optimized system solution by reducing the material costs, such as AC connectors, metal enclosure, and housekeeping power supplies, and reducing the installation labor cost due to the reduced inverter number. It also provides the flexibility to adapt with future higher power modules.

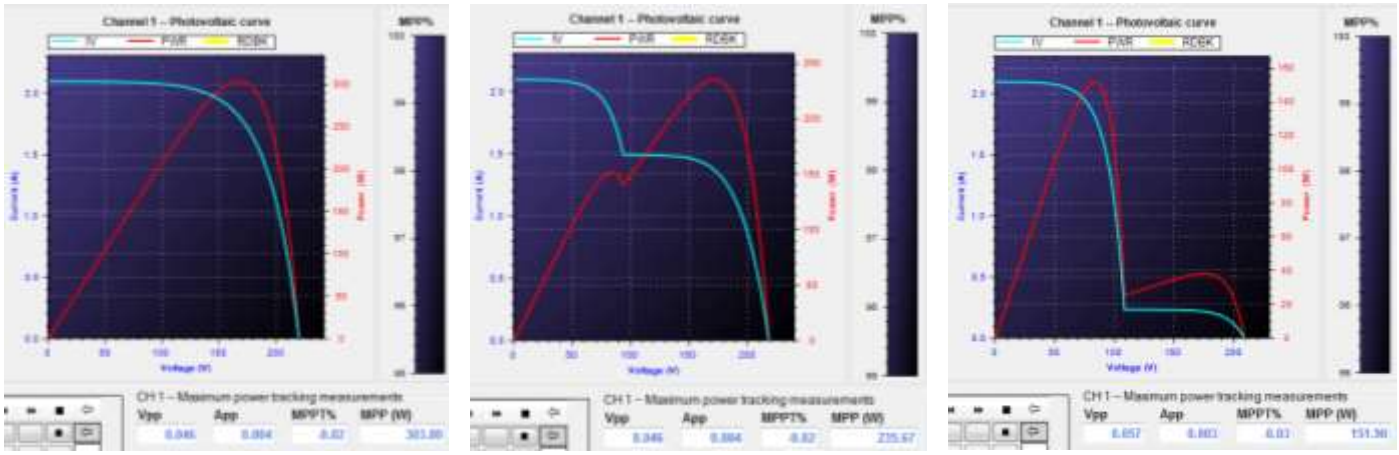
The type of connection of the two modules influences the energy yield. Some of the two-module micro-inverters contain two separate MPPT channels for each module, which maintains the single-module MPPT benefit with added cost. Using one MPPT channel for two modules either in series or in parallel results in the energy yield loss due to the module MPPT mismatch, especially during the shading condition. However, as previously discussed, thin film modules are less sensitive to shading impacts than their silicon counterparts, which gives us an opportunity to maintain both low cost and high yield in two-module micro-inverter systems.

In order to verify the above assumptions we have performed a study to identify the energy yield losses due to connecting two 150 W CIGS modules in series or parallel when compared with the independent CIGS modules.

Two CIGS modules connected in series with different irradiance distribution

First system is generated with the two CIGS module models connected in series to form a string. One module has the maximum irradiance of 1000 W/m^2 and the other module

is either operated at the same irradiance condition or shaded with irradiance of 100 W/m^2 or 700 W/m^2. Resulting string IV curves are shown in Figure 5.



a) Irradiance on both modules 1000 W/m^2

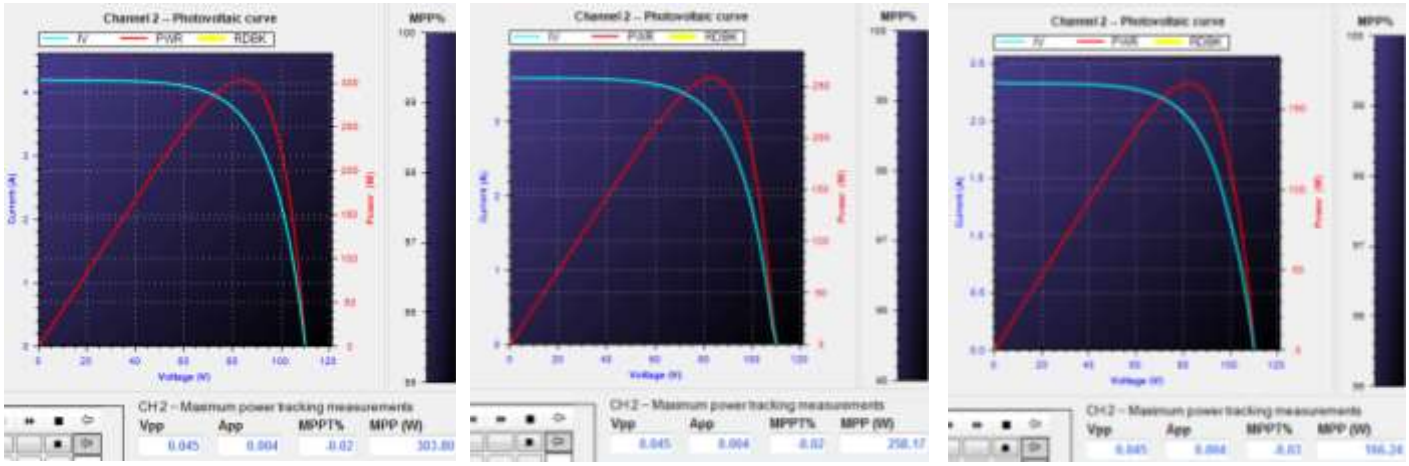
b) Irradiance on one module is 1000 W/m^2 and other is 700 W/m^2

c) Irradiance on one module is 1000 W/m^2 and other is 100 W/m^2

Figure 5: Two CIGS modules connected in series with different irradiance distribution

Two CIGS modules connected in parallel with different irradiance distribution

Second system is generated with the two CIGS module models connected in parallel. One module has the maximum irradiance of 1000 W/m^2 and the other module is either operated at the same irradiance condition or shaded with irradiance of 100 W/m^2 or 700 W/m^2. Resulting IV curves are shown in Figure 6.



a) Irradiance on both modules 1000 W/m^2

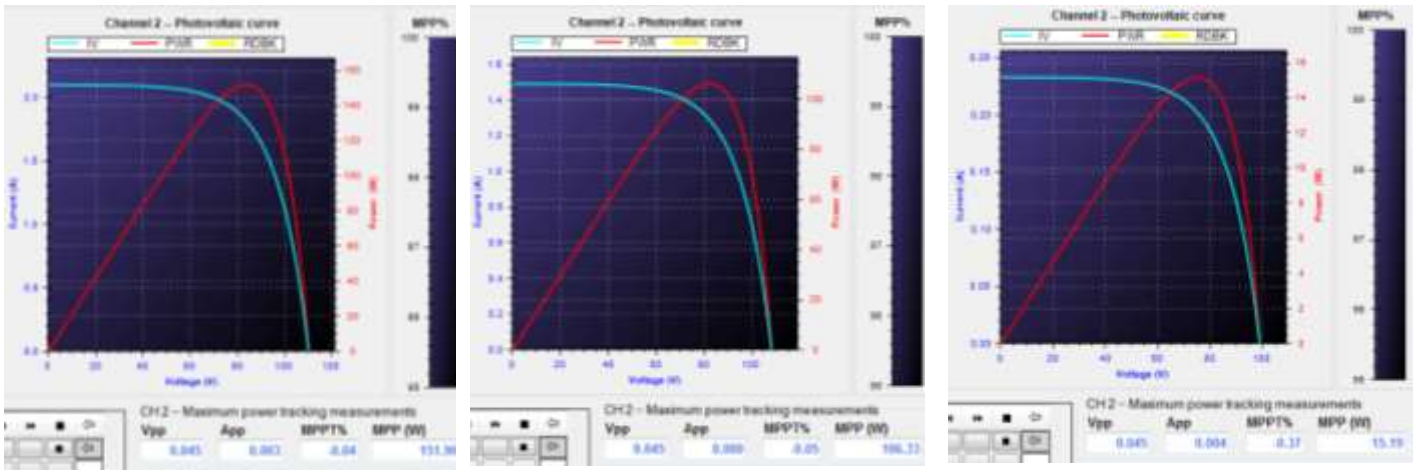
b) Irradiance on one module is 1000 W/m^2 and other is 700 W/m^2

c) Irradiance on one module is 1000 W/m^2 and other is 100 W/m^2

Figure 6: Two CIGS modules connected in parallel with different irradiance distribution

Two independent CIGS modules with different irradiance distribution

Third system is generated with the two independent CIGS module models. One module has the maximum irradiance of 1000 W/m^2 and the other module is either operated at the same irradiance condition or shaded with irradiance of 100 W/m^2 or 700 W/m^2. Resulting IV curves are shown in Figure 7.



a) Irradiance on both modules 1000 W/m^2

b) Irradiance on one module is 1000 W/m^2 and other is 700 W/m^2

c) Irradiance on one module is 1000 W/m^2 and other is 100 W/m^2

Figure 7: Two independent CIGS modules with different irradiance distribution

Table 2 shows the power losses due to the module MPPT mismatch between systems using one MPPT channel for two modules connected either in series or in parallel and two independent modules. ΔP_1 represents the power loss in the first system, while the ΔP_2 represents the power loss in the second system.

Table 2: System 1, 2 and 3 output power comparison

Irradiance	System 1	System 2	System 3	ΔP_1 [W]	ΔP_2 [W]	ΔP_1 [%]	ΔP_2 [%]
	MPPT point power [W]						
1000W/m^2 & 1000W/m^2	303.8	303.8	2*151.9=303.8	0	0	0	0
1000W/m^2 & 700W/m^2	235.67	258.17	106.33+151.9=258.23	22.56	0.06	8.74	0.02
1000W/m^2 & 100W/m^2	151.9	166.24	15.19+151.9=167.09	15.19	0.85	9.09	0.51

Table 2 shows that the power losses of the system due to the partial shading with two modules connected in parallel are negligible. In residential PV applications, the shading condition is highly variable and depends on the installation location, roof structure and surrounding environment, such as trees and chimneys. Without knowing the detailed environmental information, it is difficult to identify the exact partial shading losses. To approximately quantify the maximum power loss due to the module mismatch caused by the partial shading in two-module inverter systems, we assume the average time of partial shading condition within one year:

100% &100% STC (No shading) - 85% of time
100% &70% STC -10% of time
100% &10% STC - 5% of time

Taking the above maximum power loss data, the following equations are used to calculate the maximum power loss factor by weighing the different shading conditions:

For two CIGS module in series:

Maximum power loss factor = 0%*0.85+8.74%*0.1+9.09%*0.05=1.33% (2)

For two CIGS module in parallel:
Maximum power loss factor = 0%*0.85+0.02%*0.1+0.51%*0.05=0.03% (3)

Taking a 4.8 kW installation (32 GE 150W CIGS modules) in Phoenix, Arizona as an example, the following study using System Advisory Model (SAM), a public tool developed by NREL [5], shows the trade-off between the cost and energy yield between different micro-inverter approaches and demonstrates the benefit connecting one micro-inverter to two-modules in parallel.
The system cost information is shown in Table 3. Other than the installation costs listed in the table, operation and maintenance costs are also considered in the SAM model. Here we assume all modules are being replaced every 25 years and all inverters are being replaced every 20 years, and additional fixed maintenance cost of $50/kW-yr. The escalation rate is 3% to match the inflation rate.

Table 3: PV system installation cost breakdown

Cost ($/W)	150 W micro-inverter (single module)	300 W micro-inverter	
		2 module in parallel	2 module in series
Module (GE 150 W CIGS)	1.1	1.1	1.1
Micro-inverter	0.25	0.216*	0.216*
Racking system	0.22	0.22	0.22
Installation	0.55	0.385**	0.385**
Distribution & margin	0.88	0.88	0.88
Total installation cost	**3.00**	**2.80**	**2.80**

*Taking 150 W micro-inverter cost ($0.25/W, $37.5/unit) as the baseline, and assuming 300 W micro-inverter is using the same housekeeping supply ($1.45), metal enclosure ($7.29), and the same type of AC connector ($1.45), the two-module micro-inverter cost can be estimated as:

$37.5*2-($1.45+$7.29+$1.45) = $64.81,

resulting in $0.216/W.

**Taking the $0.55/W installation cost including mechanical and electrical labor for 150 W micro-inverter system, the inverter number of two-module micro-inverter system is reduced to half. The installation cost is estimated to be 30% lower, which is $0.385/W.

In the SAM model, system Derate factors need to be input, which account for losses in the systems that are not included in the module and inverter models, such as soiling of the module surfaces, losses in the DC wiring that connects modules, and losses in AC wiring that connects the inverter to the grid. One source of information on Derate factor is the website for NREL's PVWatts model [6]. In this study, we have selected the Derate factors based on the suggested PVwatts Derate factor with modifications for the micro-inverter system. For instance, the DC wiring and AC wiring losses will be very small due to the low current rating for the micro-inverter system. There is no step-up transformer

loss for the micro-inverter system. Table 4 shows the system Derate factors used in this study. For a single-module micro-inverter system, there will be no mismatch loss; while for a two-module micro-inverter system the mismatch loss mainly accounts for the maximum power loss due to the partial shading discussed above.

Table 4: System Derate Factors

System Derate Factor	150 W micro-inverter (single module)	300 W micro-inverter	
		2 module in parallel	2 module in series
Soiling	98%		
Mismatch	100%	99.97%*	98.67%*
Diodes and connect	99.7%		
DC wiring	99%		
Sun tracking	100%		
Nameplate	98%		
AC wiring	100%		
Step-up transformer	100%		
Overall Derate factor	**94.79%**	**94.76%**	**93.53%**

*the mismatch Derate factor represent the maximum power loss due to two-module in series or in parallel under partial shading conditions, which is calculated in equations (2) and (3).

Table 5: Cost Comparison between Single-Module and Two-Module Micro-Inverters

4.8 kW installation in Phoenix, AZ	150 W micro-inverter (single module)	300 W micro-inverter	
		2 module in parallel	2 module in series
Total installation cost ($/W)	3.00	2.80	2.80
Annual energy (kWh)	10,041	10,038	9,908
LCOE w/o ITC (¢/kWh)	14.52	13.90	14.08
LCOE with ITC (¢/kWh)*	9.95	9.59	9.72

*The residential PV systems in Arizona receives a 30% federal ITC and a 25% state ITC with a $1,000 maximum payment.

Table 5 summarizes the trade-off between single-module and two-module micro-inverters in terms of the installation cost, annual energy yield and LCOE. It shows that the micro-inverter system with two-modules in parallel has the lowest LCOE.

3.2.1.3 Topology Study

a) Power Processing Steps: Single-Stage vs. Two-Stage

Figure 8 shows two possible architectures for converting the photovoltaic panel power into utility quality power. Selection of the optimal architecture is driven mainly by efficiency, reliability, and cost. Reliability and physical size is determined largely by the size of the capacitor needed to filter the 120 Hz ripple power that must be achieved within the converter. We desire maximum DC power to be extracted from the PV panel.

Significant PV ripple power will decrease the output of the PV panel as well as cause electromagnetic interference problems. The power being delivered to the AC utility is pulsating at a 120 Hz rate. The capacitance must absorb the power difference between the DC PV power and the pulsating 120 Hz power being delivered to the utility.

In most practical cases, the capacitor shown in both approaches must perform the 120 Hz filtering. In the single stage approach, a large capacitance is needed because it not only must filter the 120 Hz power but it also must filter the resulting ripple voltage that the PV panel sees in order to draw near DC power from the panel. The single stage approach must therefore employ electrolytic capacitors if proper filtering at a reasonable physical size and cost is to be achieved. Hence, the reliability is compromised due to the significantly higher failure rate of electrolytic capacitors compared to other capacitor options [7].

In the two-stage approach a DC/DC converter extracts the maximum power (at low ripple voltage) from the PV panel and delivers it to the DC-link capacitor (labeled “small C” in Figure 8). Note in this case, however, a significant ripple voltage can be tolerated on this capacitor because the DC/AC inverter can tolerate this voltage and still deliver sinusoidal, high-quality power to the utility. Thus, a non-electrolytic, high-reliability capacitor can be used.

Note that the higher the ripple voltage the smaller the capacitor can be. However, higher ripple voltage implies a higher peak voltage stress that must be tolerated by the inverter (and also by the DC/DC converter). Figure 9 shows results from a trade-off analysis that gives the peak capacitor voltage and ripple as a function of the DC link capacitance value for the two-stage solution. Most non-isolated inverters require that the minimum DC link voltage be higher than the peak of the ac utility voltage (340 V peak for a 240 V utility). Accordingly, 380 V was selected for the minimum DC link voltage.

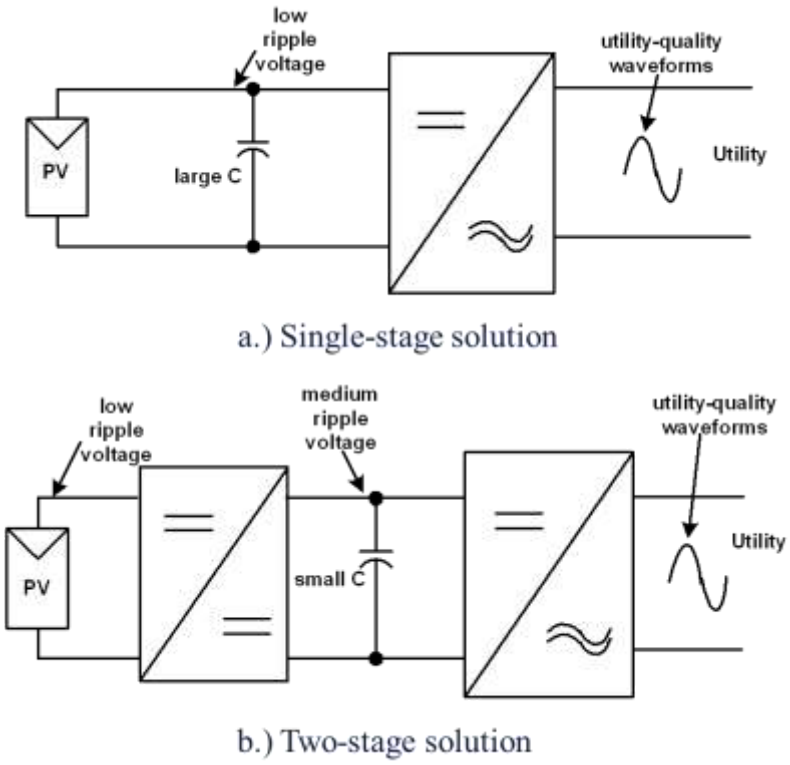


Figure 8: Power conversion architectures. a) Single-stage, b) Two-stage

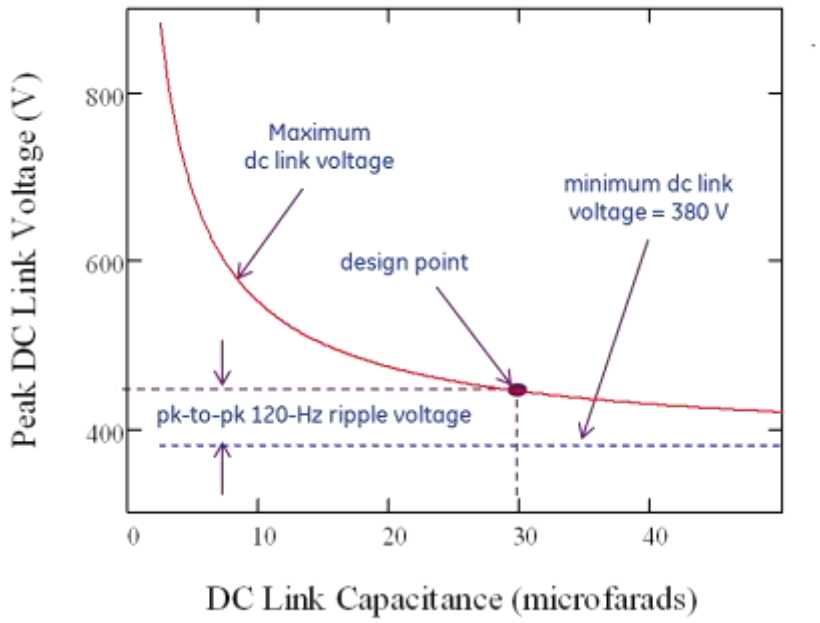


Figure 9: DC-Link Voltage Parameters vs. DC-Link Capacitance for 300 W Delivered

This curve is for 300 W being delivered to the utility. Figure 8 depicts the dependence of the peak DC-link voltage on the capacitance value as well as the dependence of the peak-to-peak ripple voltage on the DC-link capacitor (the vertical difference between the Maximum DC link voltage and the horizontal 380 V line). A reasonable design point of 30 µF has been selected (this will be discussed in later sections). For this case, a peak voltage of approximately 440 V is applied to the inverter which allows readily available, high-speed, low-loss semiconductors to be used in the inverter and DC-DC converter. As seen in the curve, lower capacitance would result in higher voltage stresses. Note that if it was desirable to reduce the ripple voltage to just a few volts as would be needed in the single stage approach, then very large capacitance values would be needed (i.e., electrolytic capacitors). Figure 10 shows simulated DC-link, 120 Hz capacitor waveforms for the design point selected above. Note that the capacitor must absorb and discharge a peak power equal to the DC power from the PV panel (300 W).

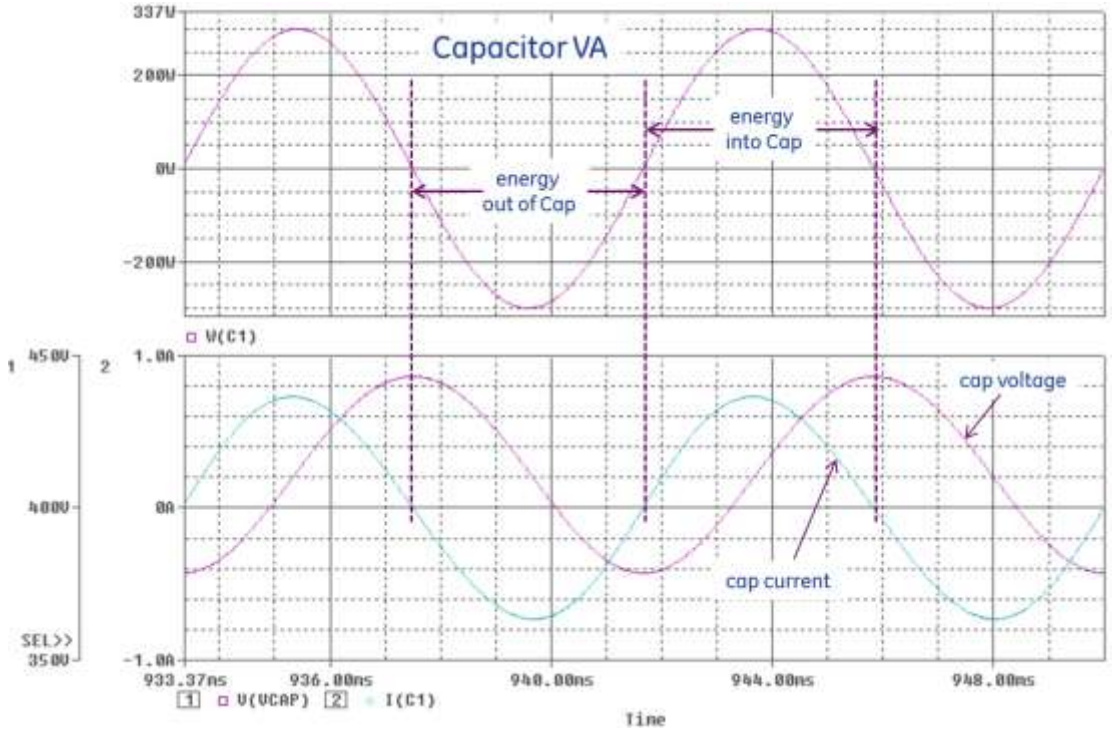


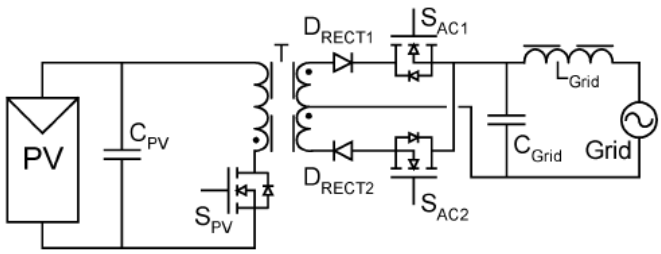
Figure 10: DC-Link Capacitor Waveforms for 300 W Delivered

Of course, the reliability gained from using a non-electrolytic capacitor is partially offset by the addition of a second stage of power conversion (the DC/DC converter). Innovative solutions for achieving very high efficiency for this input DC/DC converter that reduce the power rating of this converter and its components will be discussed in detail in the following sections.

Single-stage inverter usually requires large electrolytic capacitors, and also it is very difficult to achieve Volt/VAR control. To achieve higher reliability (without electrolytic capacitors) and to incorporate the optional Volt/VAR control, a two-stage inverter is the better choice, and further topology investigations on each stage and combination are needed for higher efficiency, lower cost, smaller size, better reliability.

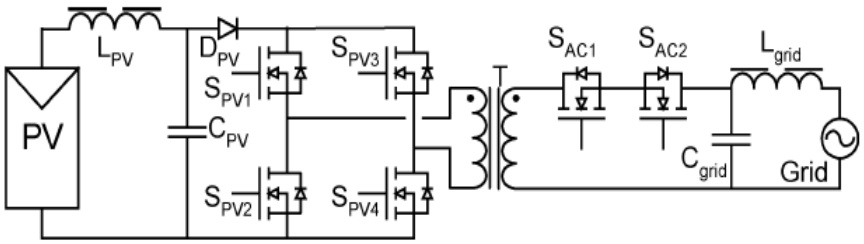
b) Selected Single-stage PV inverters

Figures 11 to 17 show several single-stage PV inverters.
Figure 11 shows a single-transistor flyback type inverter [8]. The topology consists of a single-transistor flyback converter with a center-tapped transformer. The two outputs of the flyback transformer are connected to the grid through diodes, MOSFETs, and filter, providing positive and negative output current accordingly. This topology is the simplest topology for a single-stage PV inverter. It has the inherent drawbacks of the single-stage solution, requiring large decoupling capacitance (Cpv), and the inverter must be designed to handle a peak power of the twice the nominal power. The flyback transformer provides the galvanic isolation. However, the flyback transformer needs to be well designed to minimize the leakage inductance; otherwise, additional active or passive snubber circuits are needed to deal with devices stress due to the leakage energy. The efficiency will also suffer.
Figure 12 shows a dual two-transistor flyback-type inverter [9]. Different to the previous topology, the positive and negative current is achieved by alternating the switches on the primary side and using bi-directional switches on the secondary side. This topology provides the possibility to recover the leakage energy through body diodes of primary transistors. However in this particular circuit in Figure 12, the diode D_{PV} is blocking the energy recovery, and no further information is given in [9].
Figure 13 shows a 4-switch boost inverter [10], where the DC inputs of two identical boost converters are connected in parallel to the PV source, and the load (grid) is across the two outputs. Each boost converter is modulated to produce a unipolar DC-biased sinusoidal output, 180 degrees out of phase with each other, resulting in a pure sinusoidal waveform across the load.
Similar concepts are shown in Figure 14 [11] and Figure 15 [12] by replacing the boost converter with buck-boost converter and flyback converter, respectively. Other than boost converter, buck-boost and flyback converters have both step-up and step-down functions, which provides more control flexibility. Flyback transformers also provide galvanic isolation.
Figure 16 [13] shows a non-isolated six-switch buck-boost inverter topology. The energy storage inductor L is charged from different directions in each half cycle to generate an alternating output. Two additional switches, E and F, are added to facilitate the grounding of both the PV module and the grid.
All the single-stage topologies discussed above need to have bulky decoupling capacitor because the decoupling capacitor is on the low voltage PV module side, while the topology shown in Figure 17 [14] can reduce the decoupling capacitance by adding a buck-boost stage to the flyback converter and introducing the high voltage decoupling at the intermediate DC bus.



P_{nom}=100W, η=96%(max) 91.4% (Eu)

Figure 11: Single-Transistor Flyback-Type PV Inverter [8]



P_{nom}=160W, η=92.0% (Eu)

Figure 12: Dual Two-Transistor Flyback-Type Inverter [9]

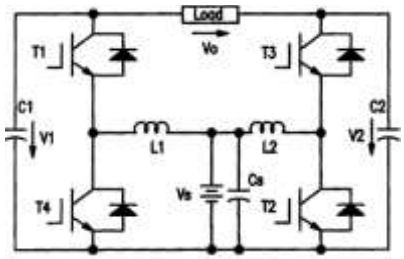


Figure 13: 4-Switch Boost Inverter [10]

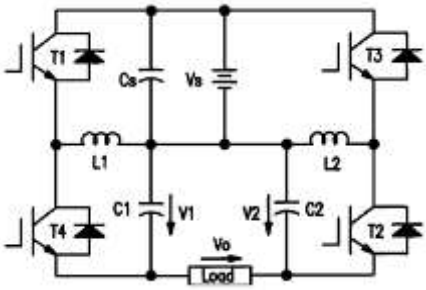


Figure 14: 4-Switch Buck-Boost Inverter [11]

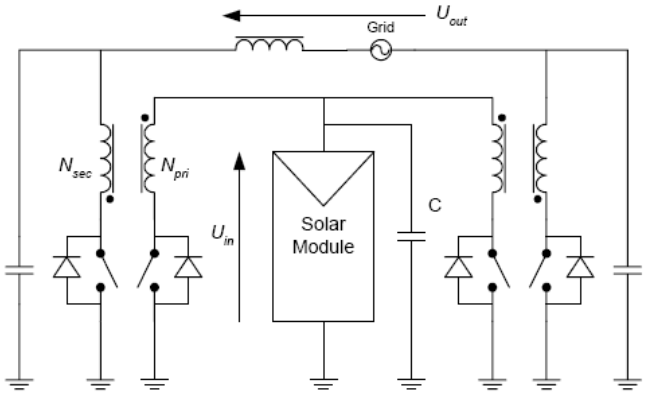


Figure 15: Bi-Directional Flyback Inverter [12]

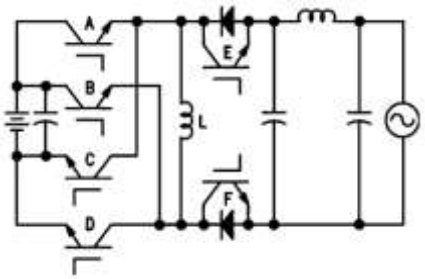
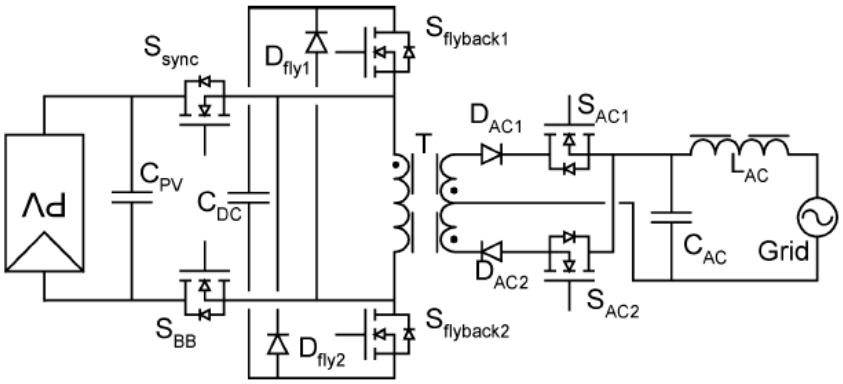


Figure 16: 6-Switch Buck-Boost Inverter [13]



P_{nom}=160W, η=87% (max), 82% (Eu)

Figure 17: Modified Shimizu Inverter (Flyback-Type Inverter With High Power Decoupling) [14]

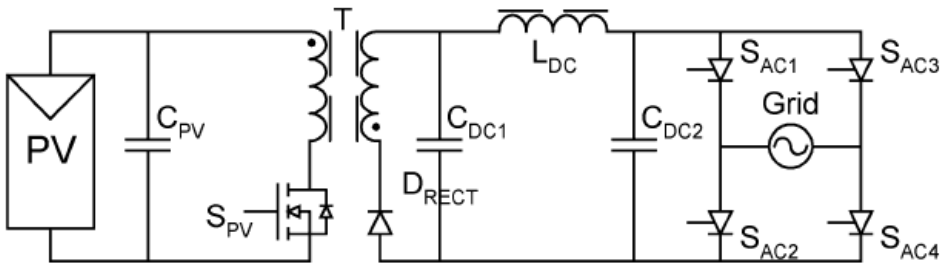
c) Selected Two-Stage PV Inverters

Figure 18 to 20 show several two-stage PV inverters.
The topology in Figure 18 [15] is a flyback converter cascaded with a line-frequency DC/AC unfolding inverter. The output of the flyback converter will be a rectified sinusoidal waveform, and the unfolding inverter simply unfolds it to the AC waveform. This topology still requires a large decoupling capacitance at PV module side. Enphase micro-inverter [23] actually is based on this topology, however many improvements are made to boost the efficiency. The flyback stage incorporates the two-phase interleaving and phase shading at light load to reduce conduction losses and switching losses as well. Quasi-

resonant operation mode is introduced to reduce the switching losses at light load. SiC diode is used to reduce diode reverse recovery losses. In the unfolding inverter stage, two MOSFETs are used to replace the thyristors to solve the possible thyristor-related current commutation issue.

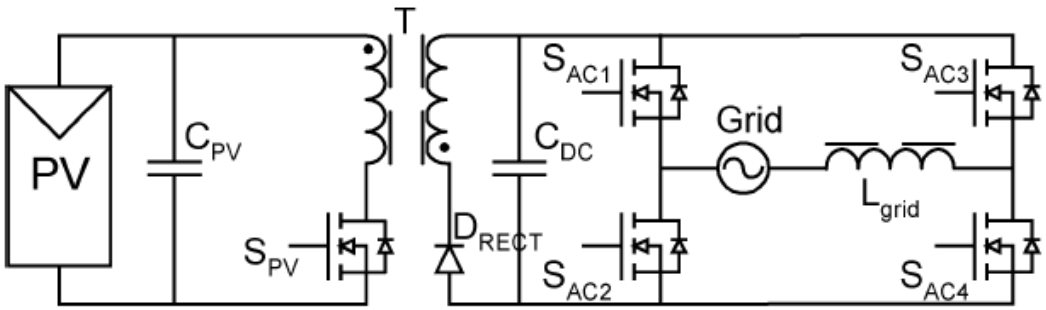
Figure 4.19 [16] shows the two-stage topology consisting of a flyback converter cascaded with a PWM DC/AC inverter. The inverter stage is now operating in the high frequency PWM mode. Since the decoupling capacitor is in the higher voltage flyback output, the capacitance value can be greatly reduced.

As discussed above, the flyback-type converter has the leakage energy issue which increases the device voltage and current stress and switching losses. Additional snubber circuit or soft-switching auxiliary circuits are usually needed to solve the issue. As an alternative, resonant DC/DC converters with soft-switching operation can be used as the DC/DC stage to achieve higher efficiency. Figure 20 [18] shows the two-stage approach consisting of a series-resonant DC/DC converter cascaded with a bang-bang inverter. The inverter is pretty similar to the PWM inverter in Figure 19, except that the two diodes D_{AC1} and D_{AC2} are added to block the rectifier function, which can prevent the in-rush current when the inverter is attached to the grid for the first time.



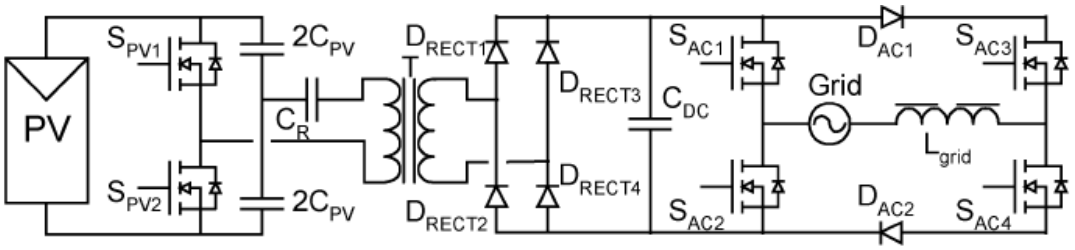
P_{nom}=150W, Vin=30V, η=92.4% nominal condition

Figure 18: Flyback Converter + Unfolding Inverter [15]



P_{nom}=100W, η=90.3% (Eu)

Figure 19: Flyback Converter + PWM Inverter [16]



P_{nom}=110W, η=90.5% (Eu)

Figure 20: SRC Converter + Bang-Bang Inverter [17] [18]

d) Summary

Both single-stage and two-stage PV inverter topologies discussed above have been evaluated in Table 6 for decoupling capacitance value, power, efficiency, and component count. Since most of the data from those papers are acquired from the academic laboratory prototypes, and also considering the continuous improvement on the semiconductor devices front, the reported nominal power and the efficiency data are given here only for reference.

Table 6: Summary of the Single-Stage and Two-Stage PV Inverter

Fig.	Topology Type	Decoupling Cap	Reported P_{nom}	Efficiency (%)	Component Count		
					L/T	C_E/C_F	S/D
11	Single-stage	2.2 mF @45 V	100 W	91.4 (Eu)	1/1	1/1	3/2
12	Single-stage	2.2 mF @45 V	160 W	92.0 (Eu)	1/2	1/1	6/1
13	Single-stage	2.2 mF @45 V	500 W		2/0	1/2	4/0
14	Single-stage	2.2 mF @45 V	215 W		2/0	1/2	4/0
15	Single-stage	2.2 mF @45 V	170 W		1/2	1/2	4/0
16	Single-stage	2.2 mF @45 V	50 W	82% (Eu)	2/0	1/2	6/0
17	Single-stage	85 uF@160 V	160 W	81.8 (Eu)	1/1	1/2	6/2
18	Two-stage	2.2 mF @45 V	150 W	92.4 (Eu)	1/1	1/2	5(1HF+4LF)/1
19	Two-stage	33 uF @400 V	100 W	90.3 (Eu)	1/1	0/2	5/1
20	Two-stage	33 uF @400 V	110 W	90.5 (Eu)	1/1	0/4	6/6

*Eu means European efficiency

In summary, single-stage inverter has single power processing handling MPPT and grid current control. It usually requires single controller, less components and result in lower costs. However single-stage inverter usually requires large electrolytic capacitors, and is also difficult to achieve Volt/VAR control. To achieve higher reliability (without electrolytic capacitors) and Volt/VAR control possibility, two-stage inverter is the better choice, and further topology investigations on each stage and combination are needed for higher efficiency, lower cost, smaller size, better reliability, etc assessment.

Table 7 shows a comparison of the single-stage and two-stage architectures. The two stage solution eliminates the most unreliable component (the electrolytic capacitor) while still maintaining high efficiency and reliability (albeit with increased parts count). The two stage approach also has more flexibility since several DC/DC converters can feed one inverter. Separate PV panels can each feed a separate, maximum power tracking DC/DC converter which can then feed a single inverter. Also, several different PV panel types with different voltages can be accommodated due to the DC/DC converter's ability to boost (or buck) the PV voltage to that required by the inverter's DC link.

Table 7: Comparison of Single-Stage and Two-Stage Approach

	Single Stage	Two Stage
DC Link Capacitor Type	Electrolytic	Film
Capacitor Reliability	Low	High
Parts Count	Lower	Higher
Efficiency	Highest	High
Overall Reliability†	Lower	Higher
Cost*	Medium-	Medium+
Flexibility	Lower	Higher

†see section 3.2.1.6

*see section 3.2.1.5

3.2.1.4 GE micro-inverter converters

In order to achieve the high efficiency and low cost two-stage PV inverter, different DC/DC converter topologies and DC/AC inverter topologies and combinations are going to be investigated in this section. Additional approaches to improve efficiency will also be investigated, such as soft switching techniques, partial power processing, and multi-phase interleaving and phase shading techniques.

a) DC/AC Stage Converters

Full Bridge Converter with Unfolding Leg

The Full Bridge DC/AC inverter with an unfolding phase leg (DC/AC-UPL) is one of the topologies that GE investigated. The schematic for this circuit is shown in **Error! R eference source not found.**.

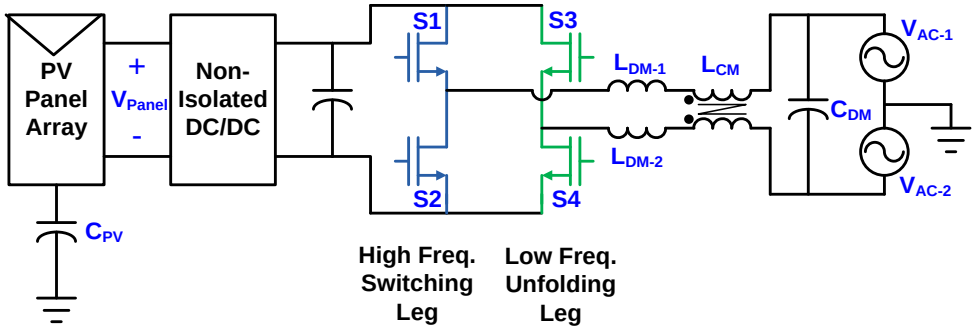


Figure 21: Full-bridge DC/AC Inverter with Unfolding Phase Leg

The circuit consists of four MOSFET switches, S1-S4. Switches S1 and S2 operate at a very high switching frequency, for example 20 kHz, while the other phase leg consisting of S3 and S4 switches at the utility line frequency, 60 Hz.

The circuit of **Error! Reference source not found.** also includes a non-isolated DC/DC f ront end power converter. The purpose of this front end converter is to boost the voltage from the PV panel. Since this DC/DC front end converter does not provide transformer isolation, any unintentional common-mode currents can flow from the PV panel, through the DC/DC converter, to the DC/AC-UPL circuit. A filter circuit consisting of two differential mode inductors (L_{DM-1}, L_{DM-2}), a common-mode inductor (L_{CM}), and a differential mode capacitor (C_{DM}) are shown to smooth out the current switching waveform from the inverter to be a nearly sinusoidal current flowing into the utility grid (V_{AC-1}, V_{AC-2}).

Error! Reference source not found. also includes an unintentional parasitic capacitance f rom the photovoltaic array to the ground. This capacitance can be many 10's of nano Farads (nF), due to the large surface area of the PV panels, and the nearby grounded mechanical structure used to hold the PV panels in place. This capacitance can change over time due to the environmental conditions such as rain, and other effects. It is this parasitic capacitance that provides a problematic path for common-mode currents to flow through, and there are rigid limits to the amount of common-mode current that can flow through this path. The common-mode current limitations are governed by the Electromagnetic Interference (EMI) regulatory standards, such as FCC15 in the United States.

The reference signals used to control the gate drive circuits of S1-S4 are shown in **Error! R eference source not found.**. There are two distinct gate commands, one for the phase leg consisting of S1 and S2, the other is the gate command used for the phase leg of S3 and S4.

The specific gate drive signals are generated, as shown in **Error! Reference source not f ound.**23, where S1 and S2 are operated in a complementary manner. The AC reference is the commanded current to flow into the AC utility grid, as shown by the top (red) waveform in **Error! Reference source not found.**.

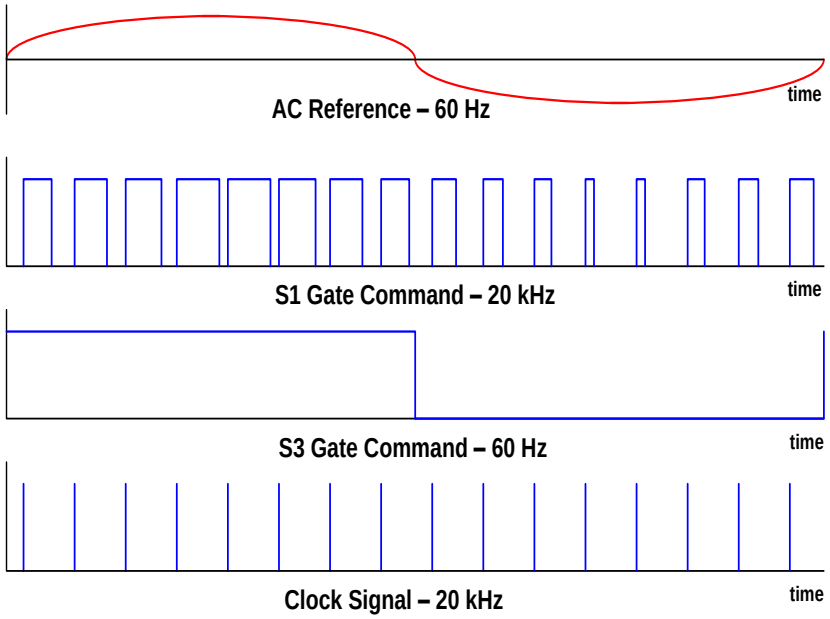


Figure 22: Gate Drive Command Signal Generation

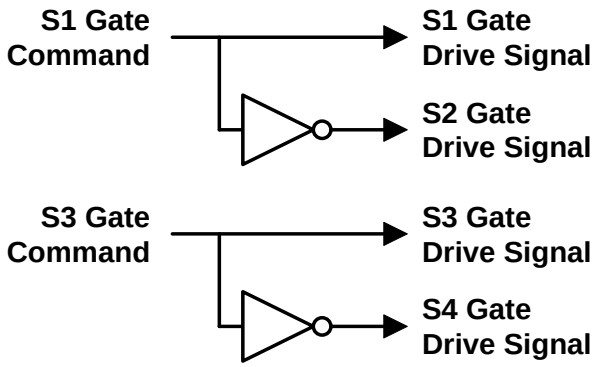


Figure 23: Gate Drive Signal Generation

The current flowing in L_{DM-1} is due to the switching of the high frequency phase leg. This current has a di/dt associated with the switching of devices S1 and S2. The low frequency phase leg (S3, S4) is not switching during an AC half cycle. Thus, there is no corresponding forced current in L_{DM-2} to be equal and opposite to the current in L_{DM-1}, which would minimize the common-mode currents. Instead, the current flowing in L_{DM-1} has two possible return paths, L_{DM-2} or the photovoltaic panel parasitic capacitance, C_{PV}. As stated earlier, the value of C_{PV} can be quite large, thus a significant current would want to flow into this common-mode path, which is in violation of safety and regulatory requirements. A very large, complex common-mode filter is necessary to redirect the currents away from C_{PV}. This filter would also require electrical damping, and would contribute to the significant power loss for the overall system.

The advantages of the DC/AC-UPL inverter are:

- High efficiency – One phase leg is switching at high frequency, while the other phase leg switches at line frequency. The low frequency phase leg could consist of very low conduction loss devices, such as the low resistance MOSFETs, or thyristors. There are

only two switches operating at high switching frequency, thus minimizing switching losses.

- Simple control – standard PWM control methods are used for the high frequency phase leg, while the other phase leg switches at the zero crossing of the 60 Hz AC reference current.

The disadvantages of the circuit are:

- There is a large common-mode current that flows through the parasitic PV panel capacitance to ground. There are regulatory and safety limits to how much current can flow through this path.
- A related problem to the common-mode current is the large filter that would be necessary to meet the EMI required standards. Electrical simulations of the circuit showed that a very large, complex common-mode filter is required to meet the EMI requirements. This filter would require a complex damping circuit due to filter and system resonances; this damping dissipates power and reduces the overall system efficiency.

Interleaved H-Bridge Converter

The Interleaved converter consists of a parallel connection of two H-bridges whose outputs are joined to generate the desired voltage, as shown in Figure 24. This connection adds the output currents of the two bridges but, if they are not switched at the same time in both legs, generates an undesired current circulating between the two circuits without going to the output. To limit this current, inductors are connected at each of the bridge output terminals as shown in Figure 24. The size of these inductors is determined by the acceptable circulating current and by the maximum voltage difference at the H-bridge outputs.

The H-bridge with the bipolar PWM already has a two level output. A parallel connection of two bridges allows for doubling the frequency of the effective ripple voltage at the output terminals. The minimum ripple for a given PWM carrier is obtained when both are switched at the same frequency, with the carriers phase shifted by 180 degrees. This ripple reduction is obtained at the cost of maximizing the volt-seconds across the inductors used to limit the circulating current.

The following traces in Figure 25 show the output voltages at the points indicated in the circuit above. Shown are the leg voltages with respect to the negative DC-bus, the output voltages at the bridges and the voltage across one of the circulating current limiter inductors. In Figure 25, *m* is the desired modulation index.

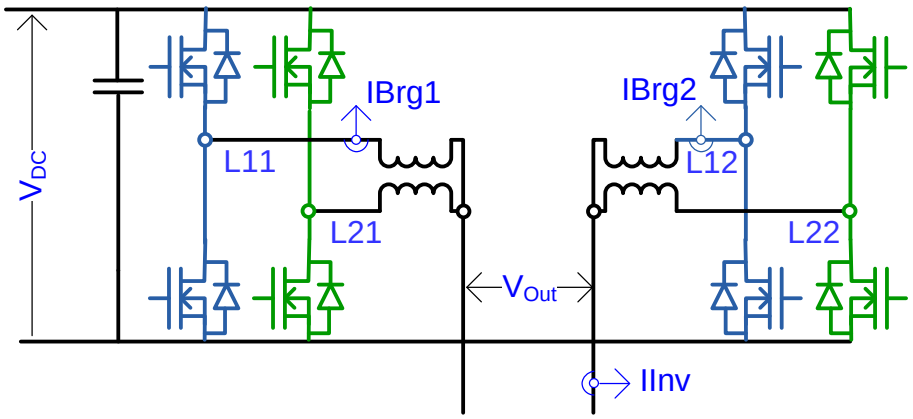


Figure 24: Interleaved Converter Parallel Connection of Two H-Bridges

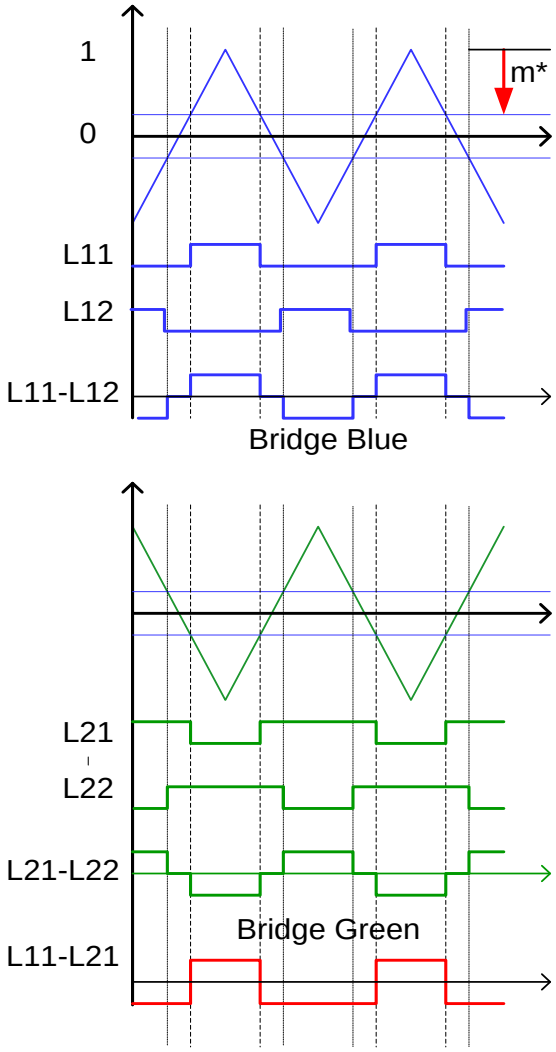


Figure 25: Gate Drive Command Signal Generation

The following traces in Figure 26 show results of a simulation of the H-bridges with two modulation indexes of opposite signs (+0.3, -0.3). The L-values are the voltages at each of the H-bridge's legs. The results are obtained measuring with a constant DC bus set at 400 V and the output terminals open. Doubling of the ripple voltage at the output terminals can be clearly identified. Also shown are the voltages across the reactors.

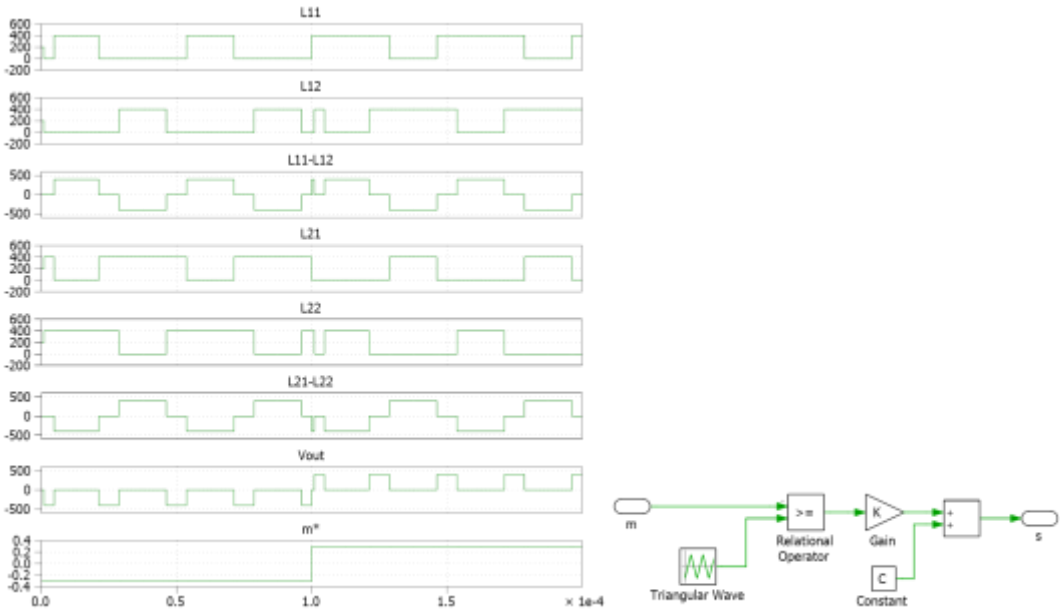


Figure 26: Simulation of the H-bridges with Two Modulation Index of Opposite Signs (+0.3, -0.3)

In the circuit, the circulating current limiting inductances could be connected as individual inductances per leg, or be replaced by interface reactors. The latter method has been chosen.
Figure 27 shows a simplified block diagram of the control for the generation of the PWM commands for both H-bridges with the 180 degrees phase shift used for the interleaving.

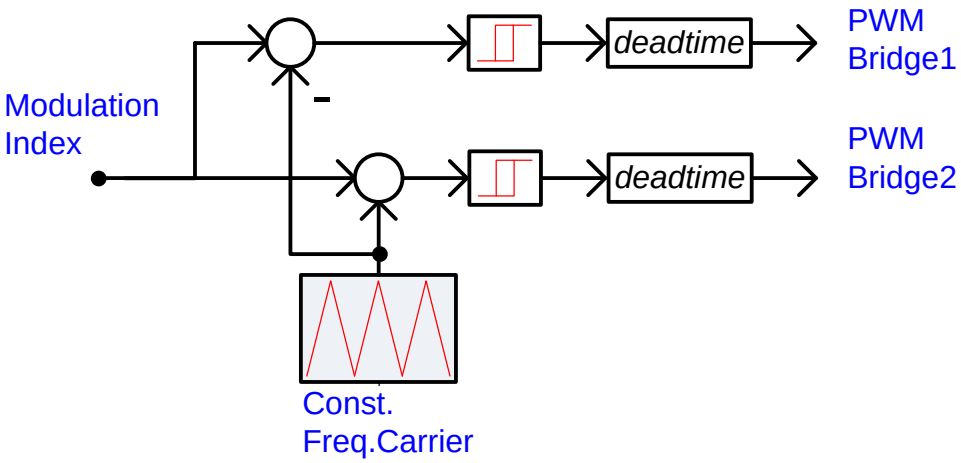


Figure 27: Simplified Block Diagram of the Control for the Generation of the PWM Commands

Some of the identified advantages and disadvantages of these topologies are:

Advantages:

- High frequency ripple, which reduces the size of the output filter needed to fulfill the grid requirements.
- One of the bridges could be disabled under light load, thus helping in keeping the circuit efficiency high under a wider operating region.
- Adequate behavior for transformer-less operation with respect to the common-mode noise.

Disadvantages:

- High number of switches (8).
- Interface reactors needed to limit the circulating current.
- One additional current sensor required to measure and to regulate the circulating current.

GE Z-Source Voltage Source Inverter (VSI)

GE investigated the Z-source inverter (ZSI), as shown in **Error! Reference source not found.**. The Z-source inverter can boost the PV voltage by introducing shoot through operation modes, which are not feasible for traditional voltage source inverters. Assuming two CIGS PV modules are connected in series, the input voltage Vdc to the ZSI ranges from 128 to 186 V. In this case, the ZSI has to boost Vdc to more than 400 V in order to connect to the 240 Vac line.
Error! Reference source not found. lists four traditional voltage source inverter switch s tates (mode #1 to #4) and five shoot through switch states (mode #5 to #9). For the convenience of implementation, mode #9 is chosen for the shoot through switch state.

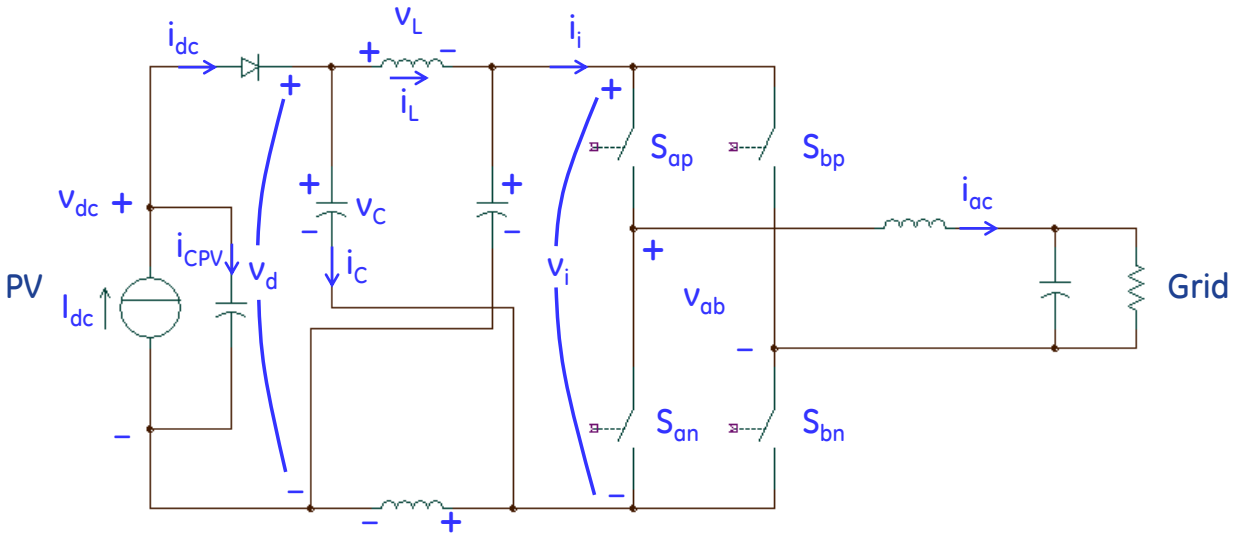


Figure 28: Z-Source Inverter

Table 8: ZSI Switch States

#	s_{ap}	s_{an}	s_{bp}	s_{bn}	v_{ab}	Mode
1	1	0	0	1	v_i	Active
2	1	0	1	0	0	Freewheeling
3	0	1	1	0	$-v_i$	Active
4	0	1	0	1	0	Freewheeling
5	1	1	0	1	0	Shoot-through
6	1	1	1	0	0	Shoot-through
7	1	0	1	1	0	Shoot-through
8	0	1	1	1	0	Shoot-through
9	1	1	1	1	0	Shoot-through

Shoot-through mode can be inserted in the freewheeling intervals w/o affecting the output

These five states are chosen in the following analysis

In order to generate the PWM signals for the switches, an enhanced sine-triangle modulation scheme is studied. As shown in **Error! Reference source not found.**, the v oltage reference signal (V_{ref}) is compared with the triangle carrier waveform (V_{car}) to generate the unipolar PWM signal V_{ab}. In addition to V_{ref} signal, two shoot-through reference signals $+V_{ST}$ and $-V_{ST}$ are added. The shoot-through signal is switched to "1" whenever $|V_{car}(t)|$ is greater than $|V_{ST}(t)|$. The voltage level of V_{ST} determines the boost ratio from PV input voltage V_{dc} to the Z-source network output voltage V_i. By setting V_{ST} level higher than V_{ref}, it is guaranteed that the shoot through operation modes only occur during inverter freewheeling intervals. **Error! Reference source not found.** depicts the l ogic to generate gating signals for the inverter. During shoot through operation modes, all the switches are turned on (mode #9 according to ZSI switch state table).

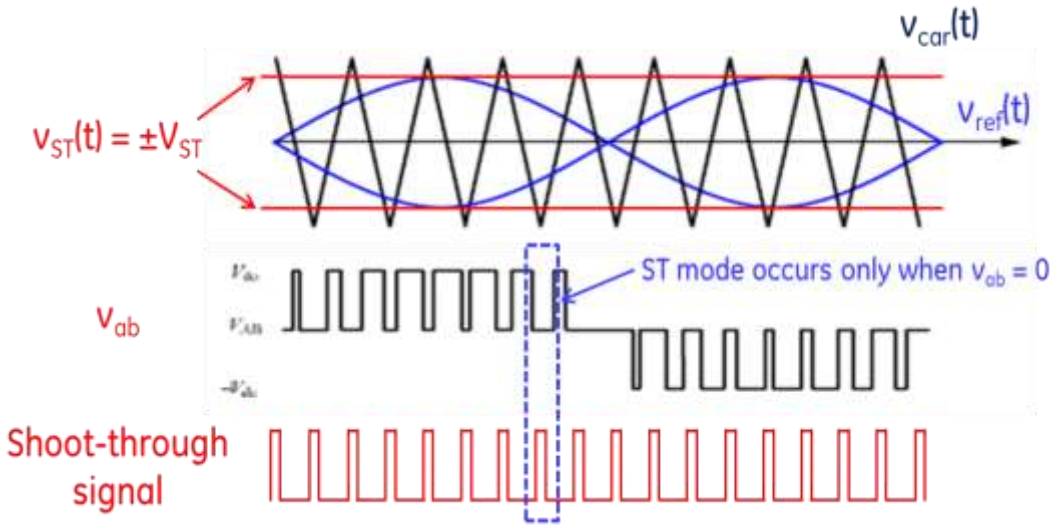


Figure 29: Modulation of ZSI – Shoot-through Signal Generation

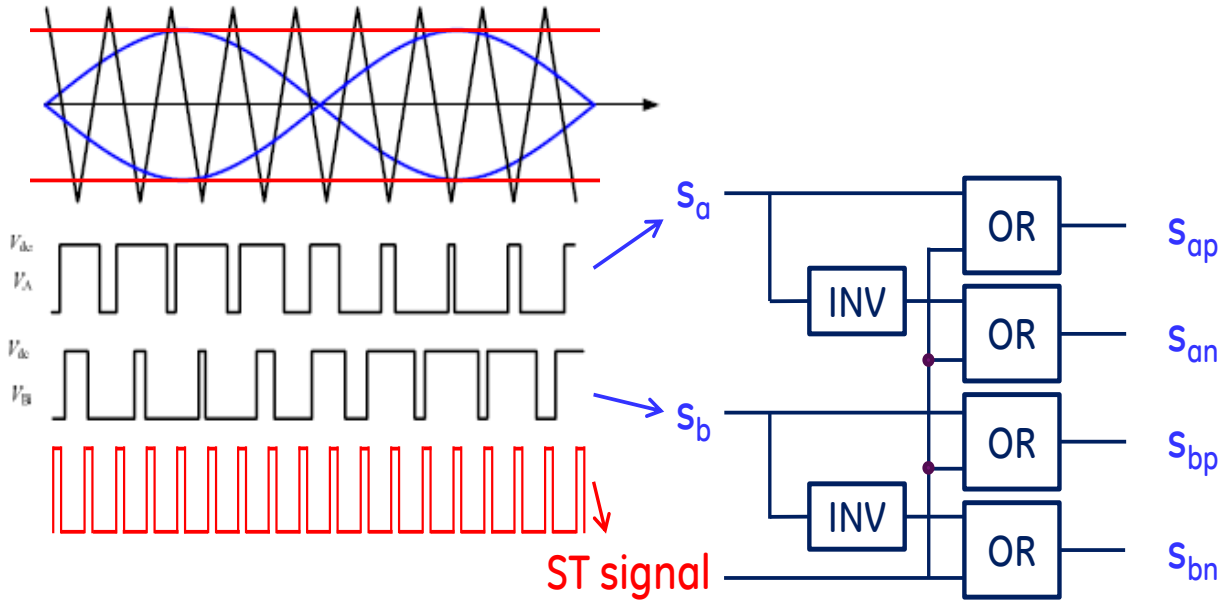


Figure 30: ZSI Gating Logic

The voltage gain for ZSI can be divided into two stages, as shown in **Error! Reference s ource not found.**31. The first stage is from PV input to the output of Z-source network. The gain is designated as *B*.

$$B = \frac{\bar{V}_{i\_NST}}{V_{dc}} \tag{4}$$

where $\bar{V}_{i\_NST}$ is the average value of output voltage of the Z-source network during non-shoot through modes.

The second stage is from V_i to V_{ab}. The maximum gain (or the modulation index of the inverter) *M* equals to

$$M = \frac{V_{ab\_pk}}{\bar{V}_{i\_NST}} \tag{5}$$

where V_{ab_pk} is the inverter peak output voltage.

Combing equation (4) and (5), the overall voltage gain from V_{dc} to V_{ab_pk} is derived as follows.

In the Z-source network, the two inductors have the same inductance, and the two capacitors are identical as well. Assume the ZSI switch period is *Ts* and the shoot through interval is *Tst*. The shoot through duty cycle is

$$d_{boost} = Tst/Ts \tag{7}$$

Refer to **Error! Reference source not found.**, during shoot through interval, the diode b etween the PV and the Z-source network is not conducting, and

$$\begin{aligned} V_d &= 2V_c \\ V_L &= V_c \\ V_i &= 0 \end{aligned} \tag{8}$$

During non-shoot through (NST) interval, the diode conducts and

$$\begin{aligned} V_d &= V_{dc} \\ V_L &= V_{dc} - V_c \\ V_i &= 2V_c - V_{dc} \end{aligned} \tag{9}$$

Applying the volt-second balance on the inductors and the moving average method over *Ts* on the state variables (i.e. *Vc*) we get:

$$\overline{V_c} d_{boost} + (V_{dc} - \overline{V_c})(1 - d_{boost}) = 0 \tag{10}$$

Hence

$$\overline{V_c} = \frac{1-d_{boost}}{1-2d_{boost}} V_{dc} \tag{11}$$

During NST mode,

$$\overline{V_{i\_NST}} = 2\overline{V_c} - V_{dc} = \frac{1}{1-2d_{boost}} V_{dc} = BV_{dc} \tag{12}$$

Therefore,

$$B = \frac{1}{1-2d_{boost}} \tag{13}$$

The Z-source inverter can only transfer power to the grid during NST mode. So, the maximum modulation index

$$M_{max} = 1 - d_{boost} \tag{14}$$

The maximum voltage gain from the PV to the inverter output voltage is

$$G_{max} = BM_{max} = \frac{1-d_{boost}}{1-2d_{boost}} \tag{15}$$

Under high AC line condition, the RMS value of inverter output voltage should be 269 Vrms. The peak output voltage is

$$V_{ab\_pk} = 380\ V \tag{16}$$

Table 9 shows the minimum required DC link voltage under non-shoot through conditions for the range of the PV inputs. In both cases (minimum and maximum MPPT tracking voltages), the DC link voltages are too high for 600 V CoolMOS devices, which means high voltage rated (800 or 900 V) CoolMOS devices are needed. Higher voltage CoolMOS devices are a lot more expensive than the 600 V ones. Therefore, from cost perspective, the Z-source topology is not a good choice for the GE micro-inverter.

$$G = \mathrm{B} \cdot \mathrm{M} \tag{6}$$

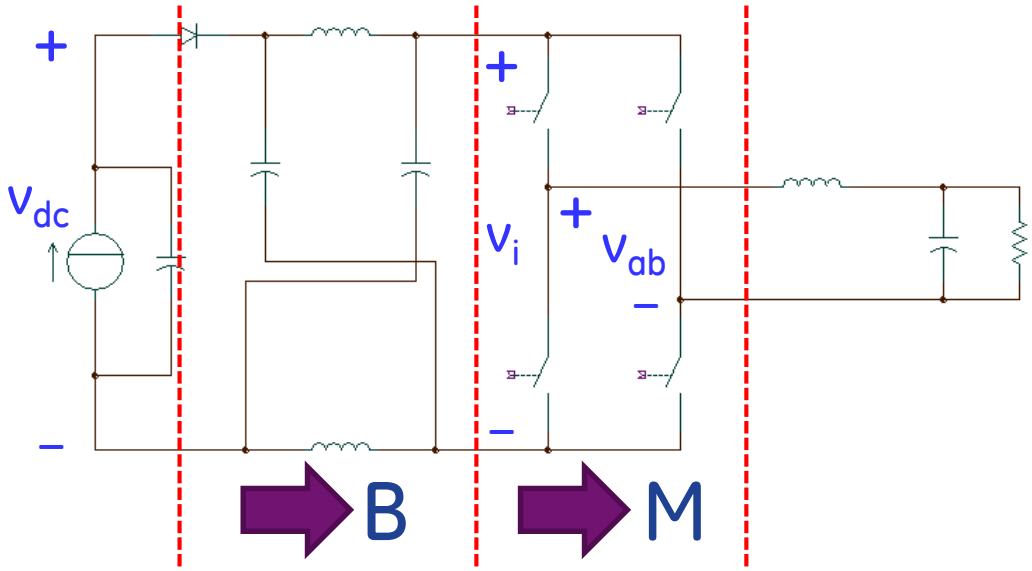


Figure 31: Voltage Gain of ZSI

Table 9: DC Link Voltage under Non-shoot through Condition

PV Input Voltage V_{dc} [V]	G_{max}	d_{boost}	B	$\bar{V}_{i\_NST}$ (V)
128	2.97	0.399	4.95	634
186	2.04	0.338	3.08	573

H-Bridges with Three-level Legs

The previous H-bridge topology uses two switches per leg generating a two level output while producing a three level at the bridge output terminal. Similar performance can be reached by replacing the two switches two-level legs by circuits capable of generating three levels at their outputs. This can be achieved with two different topologies, already known from the literature. Both require splitting the DC bus in two equal voltages and additional control to keep these two voltages equal in amplitude. This is achieved by changing slightly the modulation index for at least one of the legs, as will be later explained.

The first of these topologies is the NPC (Neutral Point Clamped converter). It requires four switches in series across the DC bus. Each of the switches has to be able to block a voltage at least half of the DC bus (and not the full DC bus as is the case for the two level H-bridge).

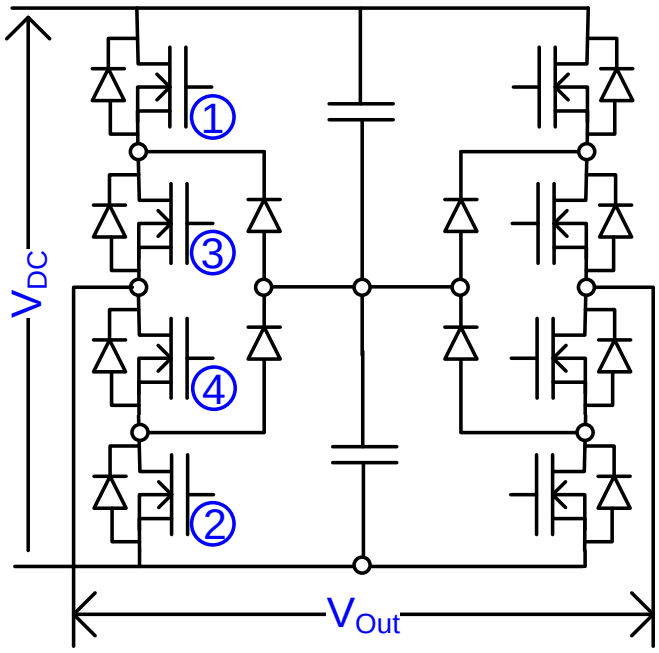


Figure 32: NPC (Neutral Point Clamped converter) Topology

With reference to Figure 32, the output voltage is connected to the positive terminal of the DC bus by turning ON switches 1 and 3, and to the negative DC-bus when 4 and 2 are fired. Firing only 3 or 4 will connect the output to the center tap of the DC link capacitor.
Similar results can be obtained with a slightly different topology commonly referred as NPP (Neutral Point Piloted converter). In the following Figure 33, firing switch 1 will connect the leg output to the positive bus, turning on 2, to the negative. Firing 3 or 4 connects the output to the capacitor center tap. In this configuration, switches 1 and 2 will have to support the full DC bus voltage, while 3 and 4 only half.
In both circuits, besides controlling the output voltage, it is required to control the voltage at the center of the DC bus. If this is not part of the control, irregularities in the output could force the DC bus center tap to drift up or down, thus limiting the maximum output voltage. This voltage can be regulated by modifying the command for one of the legs. This is especially critical when the capacitors of small values are use in the DC bus.
In both configurations, the carriers for the PWM can be shifted as desired. The best output ripple is reached with a 180 degree interleave.
For the generation of the PWM for each leg, the modified sine-triangle method was applied. It uses two carriers of the same frequency. One compares the positive part of the modulation index command with the carrier going between zero to one, generating the pulses for the switches 1 and 3, while a second, 180 degrees phase shifted, compares the negative part of the command with a carrier going from negative one to zero firing switches 2 and 4. To interleave between the legs, the carriers are again phase shifted by 180 degrees.

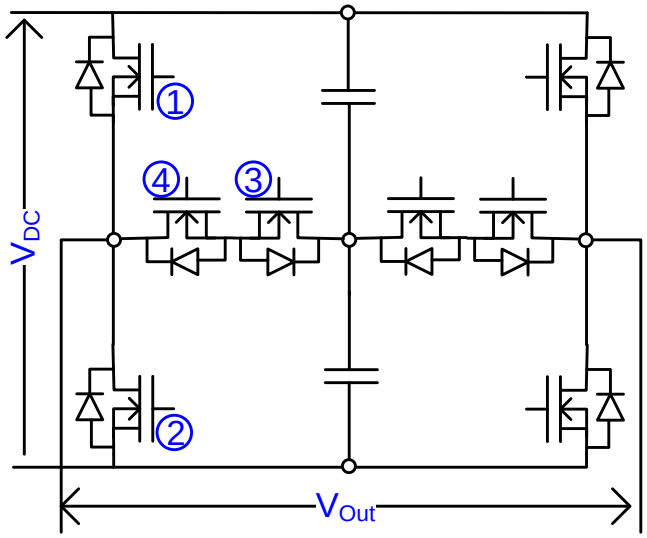


Figure 33: NPP (Neutral Point Piloted converter) Topology

Figure 34 shows results for the NPP configuration. The traces are the carriers for the positive and negative command, the modulation index (in red), the generated command for the legs and the output voltage. For the PWM pulse commands, when equal to one, switches 1 and 3 are fired; for equal to negative one, switches 2 and 4; and for equal to zero, switches 4 and 3. The same results are obtained when using the NPC Bridge.

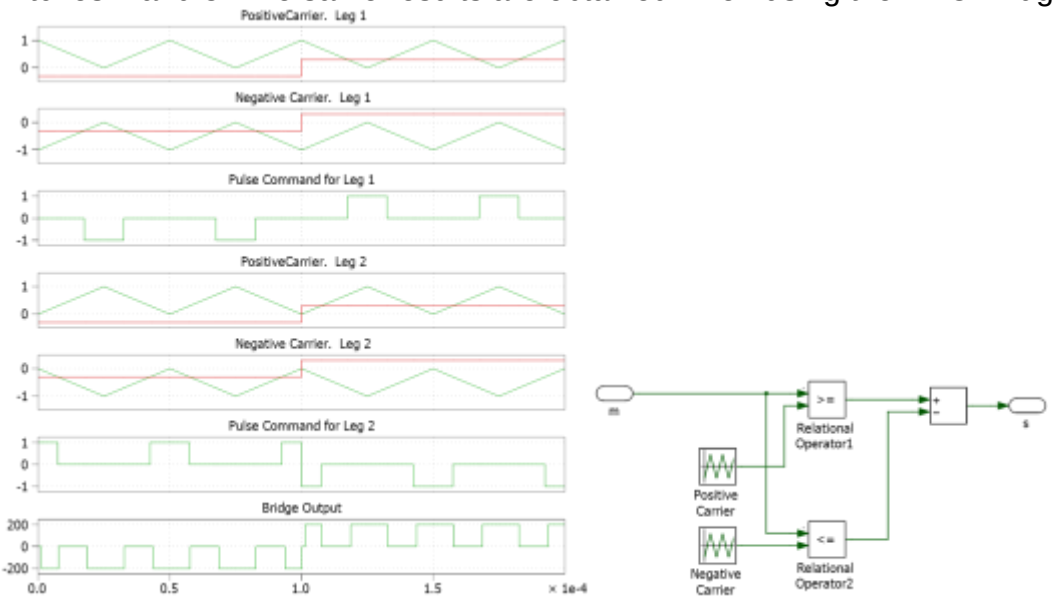


Figure 34: Simulation Results for the NPP Configuration

The center tap of the DC link capacitor voltage is controlled by adding a common mode to one of the commands for the legs modulation index. This error signal is generated by an integral regulator comparing the center tap voltage with half of the total DC link.
Some of the identified advantages and disadvantages of these topologies are:
Advantages:

- High frequency output ripple.
- Could have a half of the required voltage rating for some of the switches.

- Adequate behavior for transformer-less operation regarding the common-mode noise.

Disadvantages:

- High number of switches (8).
- Split DC bus capacitor required.
- An additional voltage sensor and control are needed to keep the DC bus balanced.

GE Full Bridge (FB) with Fast Diodes

Due to their simplicity and ease of control the FB inverters are probably the most popular converter topologies used in the grid-tied and stand-alone applications. However, the issues associated with semiconductor reverse recovery limit the use of MOSFETs as the main switches since the parasitic built-in body diodes of the MOSFETs behave poorly during this period. The reverse recovery period induces an instantaneous shoot-through which not only reduces the power conversion efficiency but also increases the electromagnetic interference (EMI) significantly. IGBTs co-packed with fast reverse recovery diodes are normally employed to solve the above mentioned issues. In low power applications, such as the PV micro-inverter applications, MOSFETs show significant performance and cost benefits over the IGBTs. Therefore we investigated possible solutions to improve the reverse recovery issues of MOSFETs FB inverters.
Figure 35 shows the topological variation of the FB inverter where two small coupling inductors are employed to redirect the load current flow to the fast diode when the corresponding main switch is turned off. For positive line cycle the inductor current I_L increases with a rate of (Vpv-Vg)/2L when S1 & S4 are ON and decreases with a rate of Vg/2L when S1 & S4 are OFF. This inductor current I_L flows through S1 & S4 when S1 & S4 are ON and through D2 and D3 (freewheeling current) when S1 & S4 are OFF. Due to the coupling effect of Tr1 & Tr2, the induced voltage prevents freewheeling current to flow through the body diodes of S2 and S3, and thus prevents shoot-through problem related to the conventional bridge-type voltage source inverter. By controlling the duty ratio of the switches the inductor current can be forced to follow the grid voltage with a unity power factor (PF), a leading or lagging PF. For a preferred operation mode S1 is turned ON & OFF in unison with S4; S2 is operated in unison with S3; and S1 and S2 are in complementary operation mode with an appropriate dead-time in between.

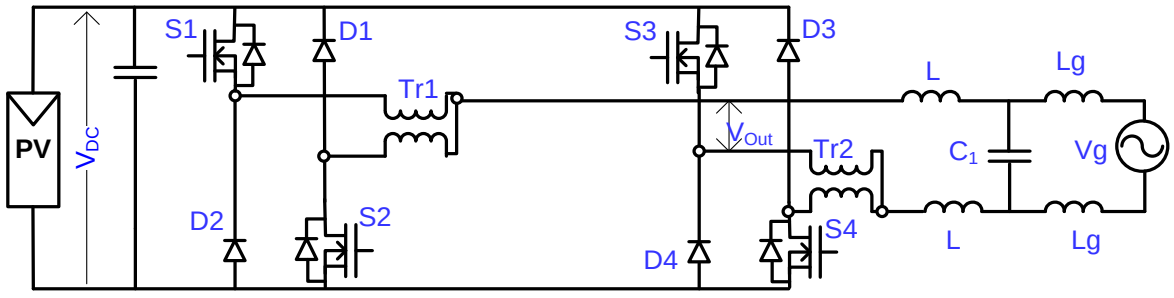


Figure 35: GE Full Bridge with Fast Diodes

The advantages of the proposed FB inverter with fast diodes are:

- High efficiency – the extra coupling inductors are very small, only a couple μH with a small volt-second needed. Fast diodes carry less load current during the line peak where the most power is delivered to the grid.
- Low cost – only four fast diodes and two small coupling inductors are added.

The disadvantages of the circuit are:

- Bi-polar modulation – for a transformerless application a bi-polar modulation must be used to mitigate the common-mode noise problem in PV applications. However, this modulation requires a use of a bigger output filter which will increase the cost of the inverter.

b) DC/DC Stage Converters

LLC with Two PV Modules Connected in Series

DC/DC converters are very important in the two-stage solution. They interface the power generation source (PV panels) and the down-stream inverter stage. Two main required functions are:

1) Extracting the maximum power from the PV panels and
2) Matching the PV maximum power point voltage (current) to the DC-link voltage.

The selection of the optimal DC/DC stage topology is mainly driven by the efficiency, reliability, and cost. The weighted CEC efficiency encourages us to find topologies that have inherently high efficiency during the light load condition. Reliability and physical size is determined mainly by the switching frequency and operation mode. Usually high frequency and zero voltage switching (ZVS) operation results in converters with a smaller size and enhanced reliability. LLC resonant converters became very popular recently in the telecommunication industries due to their superior light load efficiency and ZVS operation. GE Power Electronics business has Total Efficiency^{TM} (TE) [24] product line that employs LLC resonant DC/DC stage with proven field performance and a total efficiency approaching 97%.

To further increase efficiency, a partial power method is proposed. Figure 36a shows a block diagram of the partial power configuration and Figure 36b shows an implementation in a full bridge LLC DC/DC converter case. Clearly, from Figure 36a, the DC/DC converter is only processing a part of the input power that is used to modify the output characteristics of the PV panel(s). Therefore, the fraction of the power processed through the converter is in direct proportion to the voltage gain needed to match the DC-link voltage. This yields higher converter efficiency when connected to a higher PV voltage source.

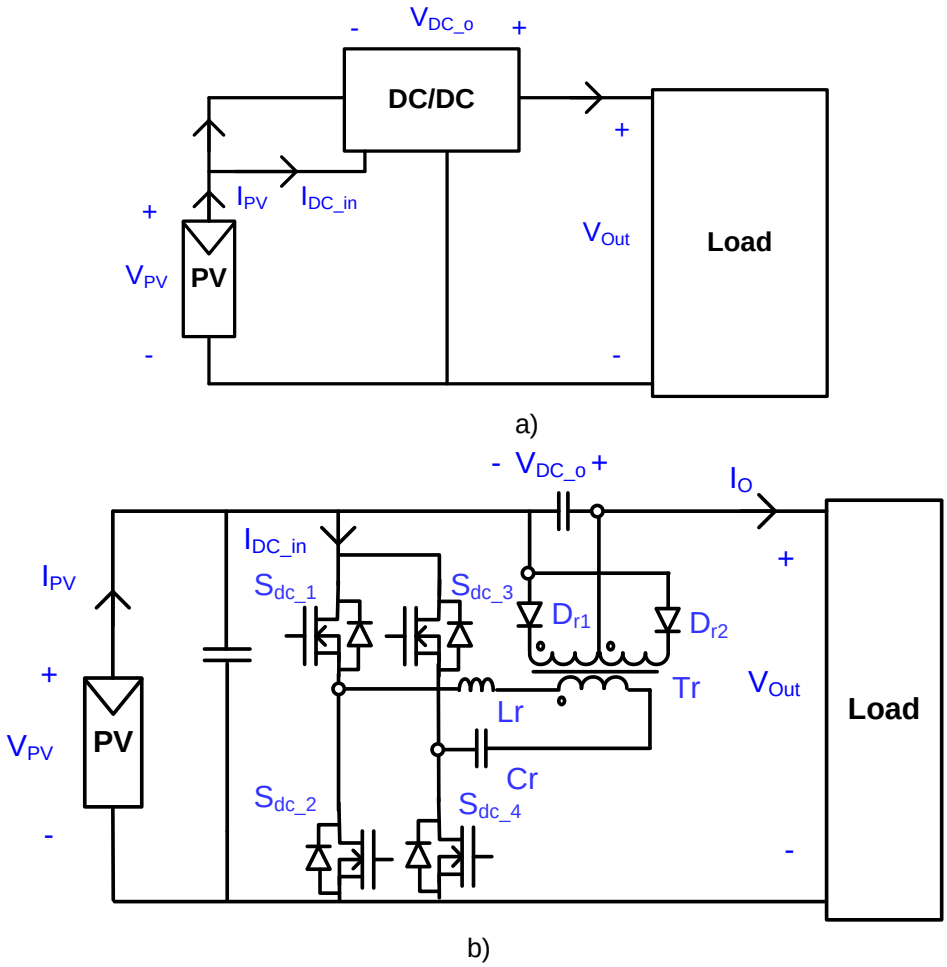


Figure 36: Full Bridge LLC DC/DC Converter Implementation

If we assume that the output capacitor is large enough, the output voltage is approximately constant. Six possible operation modes exist depending on input, output and load conditions.

Mode I:

The S_{dc_1} and S_{dc_4} are ON and the resonant current flows through D_{r2} charging the output filter capacitor. The Lr and Cr form a series resonant tank and Lm is clamped by the output voltage. The equivalent circuit is shown in Figure 37

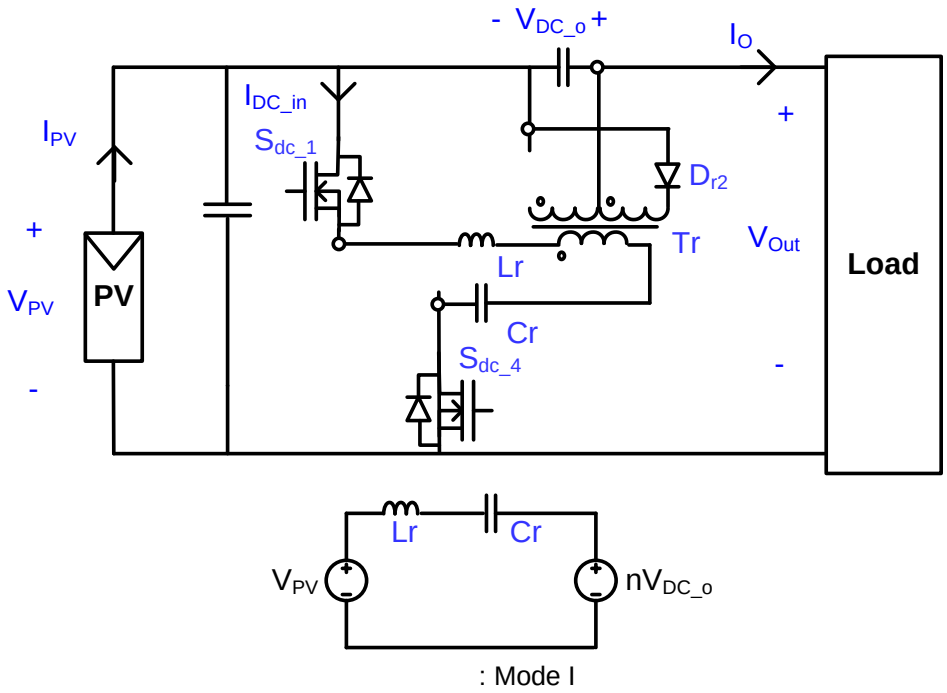


Figure 37: Mode I

Mode II:

The S_{dc_1} and S_{dc_4} are ON but the current flows through D_{r1} instead of through D_{r2}. This happens when the switching frequency is higher than the series resonant frequency, resulting in resonant inductor current being higher than the magnetizing current when S_{dc_2} and S_{dc_3} are turned OFF. The equivalent circuit shown in Figure 38 is similar to the Mode I with the source voltage of $V_{pv}+n*V_{DC\_o}$,

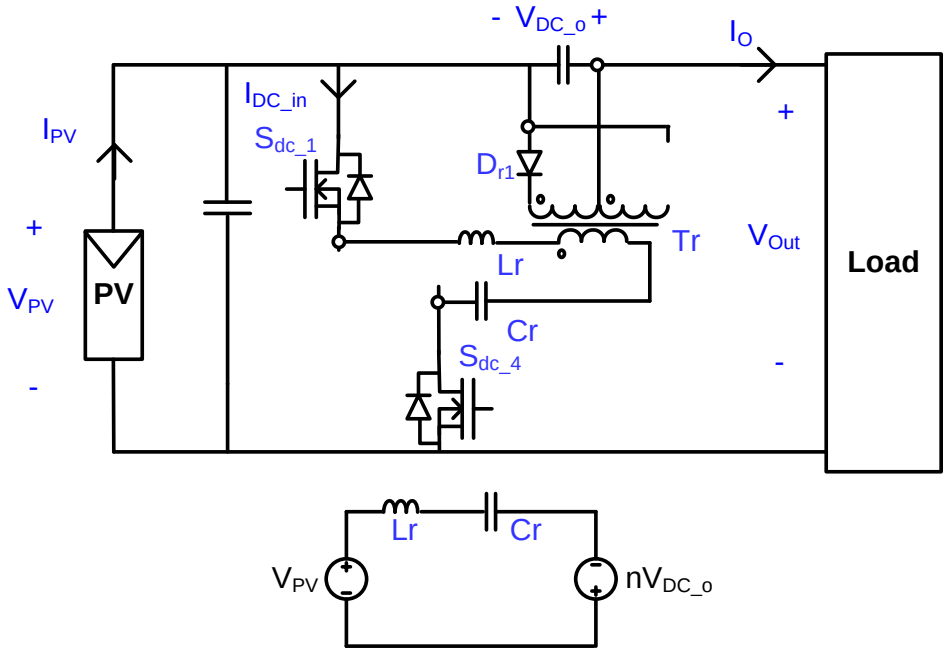


Figure 38: Mode II

Mode III:
The S_{dc_1} & S_{dc_4} are turned ON but no current flows through the secondary winding. Equivalent circuit is shown in Figure 39. This happens when the switching frequency is lower than the series resonant frequency and the magnetizing inductor Lm is the part of the resonant circuit during this mode. Since no current flows through the secondary this mode is also called discontinuous conduction mode (DCM) model. This results in a somewhat different behavior from the series resonant converter, because the output voltage gain is larger than one due to this extra energy storage mode.

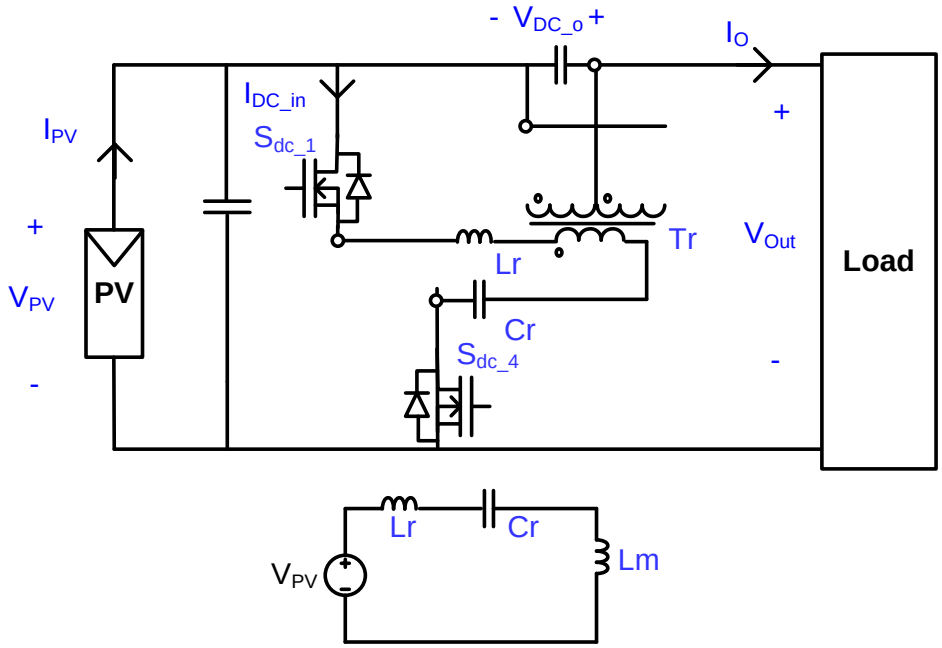


Figure 39: Mode III

Modes IV to VI:
During these modes the other pair of switches (S_{dc_2} & S_{dc_3}) is turned ON, generating similar three operating modes and equivalent circuits shown below in Figure 40.

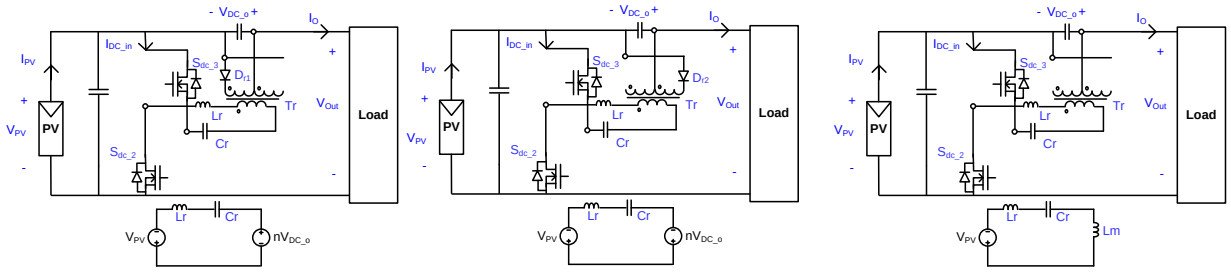


Figure 40: Mode IV to VI

Many design methodologies are available for the LLC DC/DC converter resonant tank design. Among them a design procedure proposed by S. De Simone from STMicroelectronics utilizes “First Harmonic Approximation” (FHA) [25] technique to obtain a simple yet conservative design. The ST approach addresses the design constraints related to ensuring soft-switching under all operating conditions and zero-load capability, which is important for the inverter application.

It is desirable to draw maximum DC power from the PV panel. However the instantaneous power being delivered to the grid is pulsating at a 120 Hz rate. The load seen by the DC/DC converter is also pulsating at the same rate. To study this effect a simplified model is developed, as show in Figure 41 where a unity power factor is assumed.

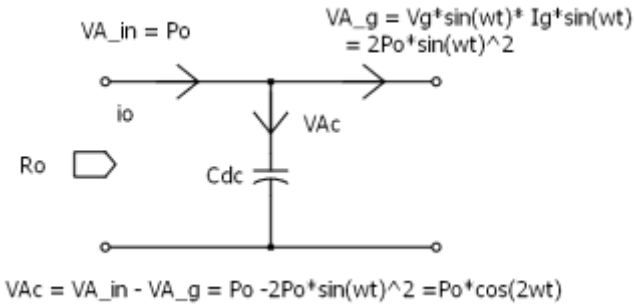


Figure 41: Power Flow

Based on the mode, the DC-link voltage can be estimated as:

$$V_c(t) = \sqrt{\frac{P_o}{\omega_l \cdot C_{dc}} \cdot \sin\left(2 \cdot \omega_l \cdot t\right) + V_{c\_ini}^{\ 2}} \tag{17}$$

Where V_{c_ini} is the DC-link voltage at line zero crossing.
The equivalent resistance therefore equals:

$$R_o(t) = \frac{V_c(t)^2}{P_o} = \frac{V_{c\_ini}^{\ 2}}{P_o} + \frac{1}{\omega_l \cdot C_{dc}} \cdot \sin\left(2 \cdot \omega_l \cdot t\right) \tag{18}$$

The peak-to-peak ripple voltage equals:

$$\Delta V_{c\_pp} = V_{c\_max} - V_{c\_min} = \sqrt{\frac{P_o}{\omega_l \cdot C_{dc}} + V_{c\_ini}^{\ 2}} - \sqrt{-\frac{P_o}{\omega_l \cdot C_{dc}} + V_{c\_ini}^{\ 2}} \tag{19}$$

Figure 42 shows the calculation result for a 30 μF DC-link capacitor with an initial 410 V and 300 W power. It can be seen that the resistance value changes from 474 Ω to 650 Ω with an average value of 562 Ω.

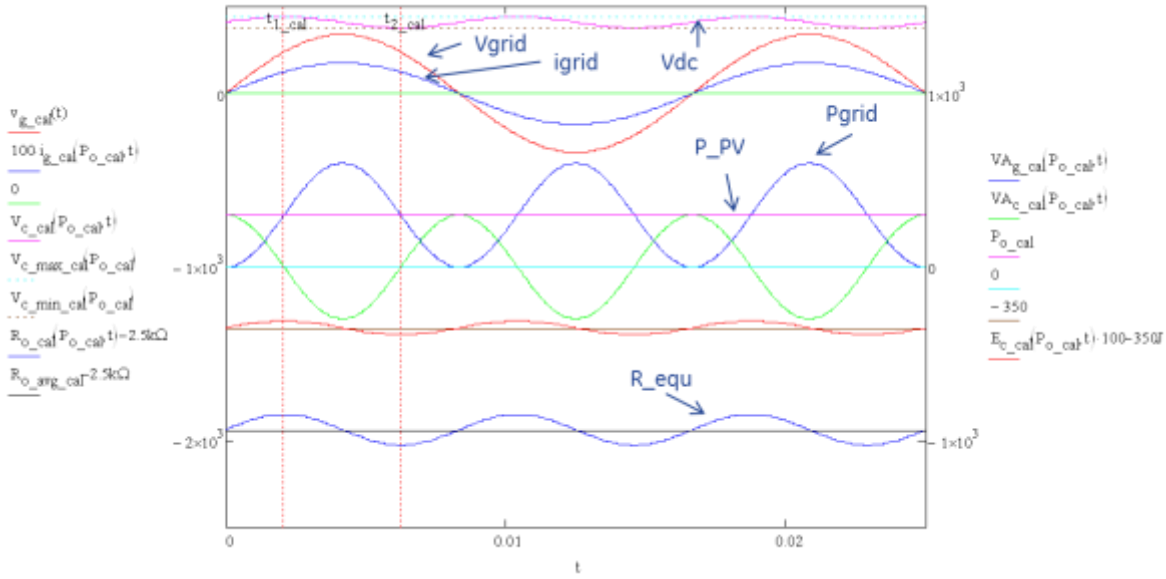


Figure 42: Simulation of 30 µF DC-Link Capacitor with an Initial 410 V and 300 W Power

Based on the ST design procedure a LLC resonant tank parameters are obtained as shown in Table 10:

Table 10: LLC Resonant Tank Parameters

Design Specs					Design			
Input voltage	[V]	128	138	148	Turn ratio	3	Qmax	0.594154
Output voltage	[V]	377	410	442	M_max	1.150411	Qzvs_1	0.564447
Output power	[W]	15	300		M_min	0.849008	Qzvs_2	0.937699
Resonant frequency	[kHz]	115						
fs_max	[kHz]	230			Fn_max	2	Qzvs_sele	**0.564447**
Requ	[ohm]	473.66	562.08	650.50	Rac	50.62283		
Parasitic capacitance	[pF]	1080			Lamda	**0.237128**		
Dead time	[ns]	800			h	**4.21714**		
					f_min	[kHz]	82.42194	
					Zo	[ohm]	28.57388	
					Cr	[nF]	48.4343	
					Lr	[uH]	39.545	
					Lm	[uH]	166.7668	

LLC with Two PV Modules Connected in Parallel

A higher PV output voltage of the series connected PV panels makes for an easier design for the DC/DC converter stage since a lower voltage gain is required. However, from the energy yield study a parallel configuration of two PV panels shows a better performance over the series configuration. The LLC stage is redesigned for this case accordingly, and the converter parameters are shown in Table 11. It can be seen that smaller tank characteristic impedance is obtained because the higher tank current is expected. Higher current rating MOSFETs with low Rdson are preferred to achieve high efficiency. Comparing to the series option, the resonant inductor is smaller but the transformer becomes larger. The higher current rating of the resonant capacitor allows the use of high performance low ESR ceramic type capacitors.

Table 11: LLC Resonant Tank Parameters

Design Specs						Design			
Input voltage	[V]	64	69	74		Turn ratio	6	Qmax	0.594154
Output voltage	[V]	377	410	442		M_max	1.150411	Qzvs_1	0.564447
Output power	[W]	15	300			M_min	0.849008	Qzvs_2	3.750796
Resonant frequency	[kHz]	115							
fs_max	[kHz]	230				Fn_max	2	Qzvs_sele	**0.564447**
Requ	[ohm]	473.66	562.08	650.50		Rac	12.65571		
Parasitic capacitance	[pF]	1080				Lamda	**0.237128**		
Dead time	[ns]	800				h	**4.21714**		
						f_min	[kHz]	82.42194	
						Zo	[ohm]	7.143471	
						Cr	[nF]	193.7372	
						Lr	[uH]	9.886249	
						Lm	[uH]	41.6917	

Dual Input Isolated Boost Converter

GE investigated the isolated, dual-input, current-fed, half-bridge converter with an active clamp as shown in Figure 43.

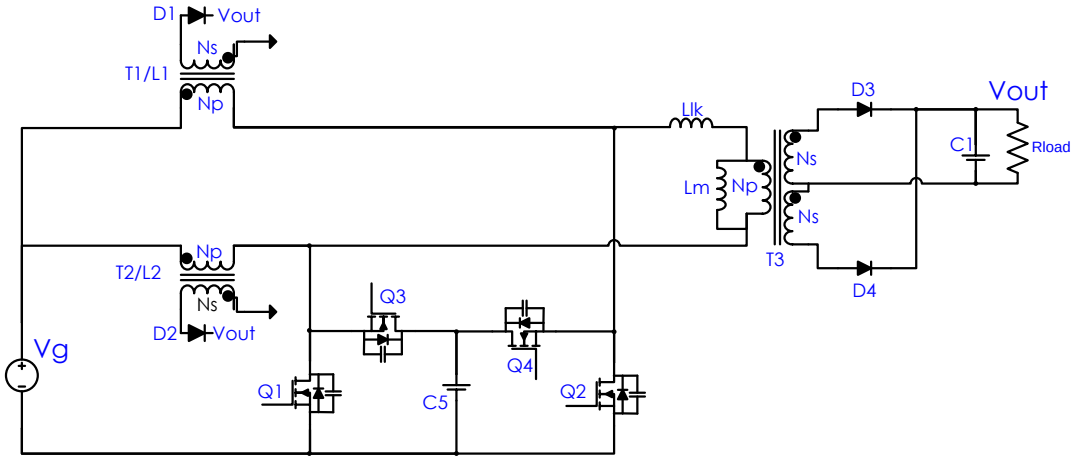


Figure 43: Isolated Boost Converter

The four main operating stages are:

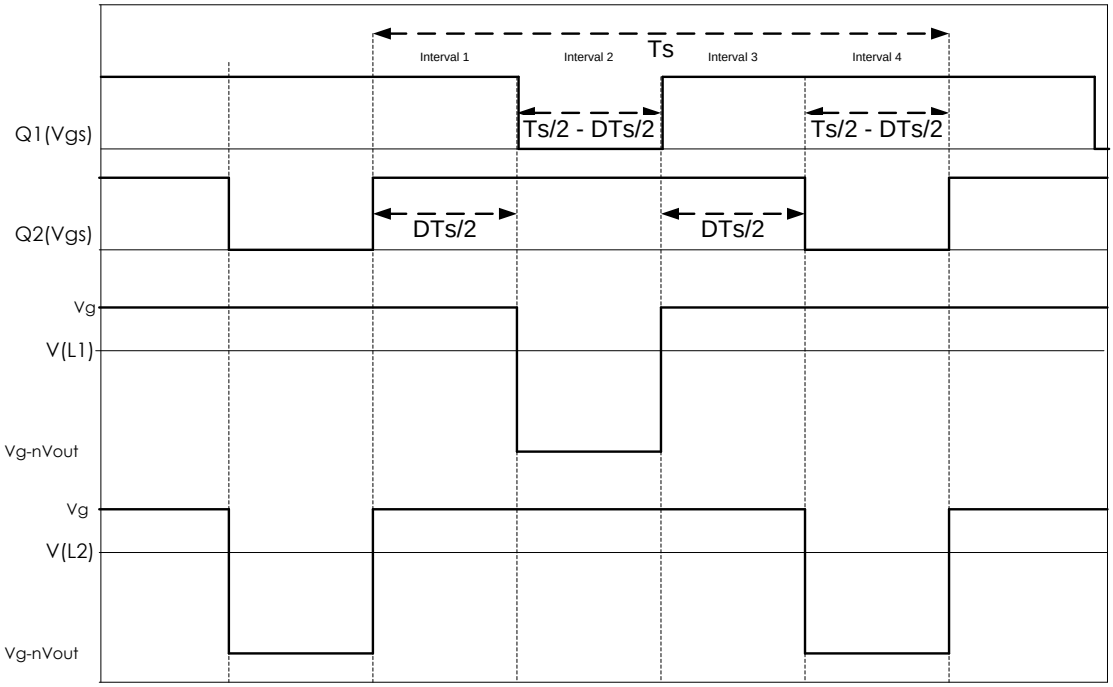


Figure 44: Isolated Boost Converter Main Operating Stages

By applying volt second balancing across an inductor and assuming an ideal transformer, across the 4 main operating stages:

Table 12: Isolated Boost Inductor Voltage

Interval	Switch Status	Inductor Volt*Time
1	Q1 on, Q2 on	$V_{L1} = \frac{D*Ts}{2} * Vg$
2	Q1 off, Q2 on	$V_{L1} = (Vg - (n*Vout)) * \left(\frac{T_S}{2} - \frac{D*T_S}{2} \right)$
3	Q1 on, Q2 on	$V_{L1} = \frac{D*Ts}{2} * Vg$
4	Q1 on, Q2 off	$V_{L1} = Vg * \left(\frac{T_S}{2} - \frac{D*T_S}{2} \right)$

The sum of inductor volt-second for all 4 intervals equals zero, which allows calculation of the converter DC transfer function. The duty cycle (D) is defined as the ON time overlap of Q1 and Q2.

$$\int_{Interval1} V_{L1} + \int_{Interval2} V_{L1} + \int_{Interval3} V_{L1} + \int_{Interval4} V_{L1} = 0 \qquad (20)$$

The voltage gain of this circuit is:

$$\frac{Vout}{Vg} = \frac{1}{n(1-d)} \qquad d \geq 0.5 \qquad (21)$$

Where $n = \frac{Np}{Ns}$

In this topology, the input current has very little ripple due to interleaving I_{L1} and I_{L2}. The power control is done with Q1 and Q2, while Q3 and Q4 are active clamping MOSFETS. In this topology, ZVS can be achieved on all primary switches, and ZCS on the secondary diodes. Best performance is achieved by operating Q1 & Q2 at >50% duty cycle, because below 50% auxiliary windings of L1 & L2 act as flyback type magnetics.
Despite many advantages of the Dual Input Isolated topology, one of the disadvantages is lower efficiency at light load due to either operating in 'flyback mode', circulation of magnetizing currents, or limited ZVS switching range.
This topology is most suited for applications with low input voltages, galvanic isolation, and high voltage gain. This topology is not the optimal for this application due to high input voltages.

Switched Capacitor with Three PV modules Connected in Series

GE investigated the switched capacitor DC/DC converter for the micro-inverter application. The circuit topology is shown in Figure 45. The circuit doubles the PV voltage. Assuming three CIGS PV modules are connected in series, the input voltage Vdc to the converter ranges from 192 to 279 V. The output voltage Vi is proportional to Vdc and will be between 384 and 558 V.

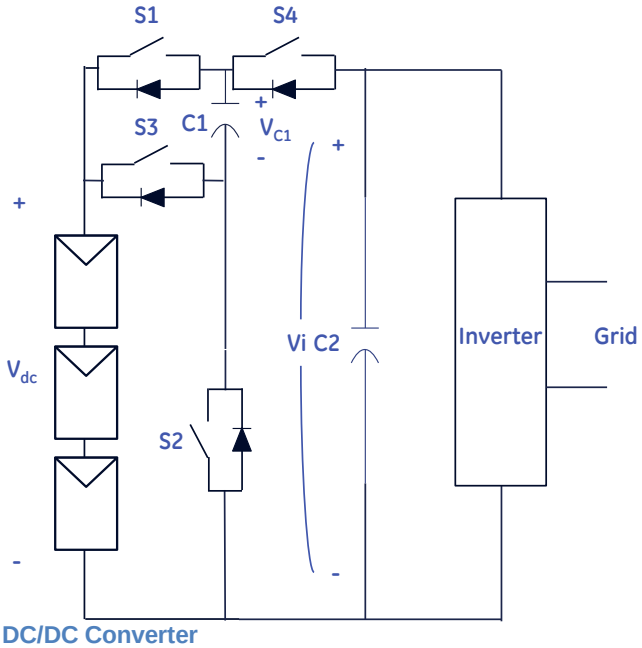


Figure 45: Switched Capacitor DC/DC Converter

The DC/DC converter has four switches. S1 and S2 are switched together; so are the S3 and S4. When S1 and S2 are ON and S3 and S4 are OFF, the PV source is charging capacitor C1. The capacitance is selected such that the ripple on C1 is less than 1%. The voltage across C1 is approximately equal to the PV voltage.

$$V_{c1} = V_{dc} \quad (22)$$

When S3 and S4 are ON and S1 and S2 are OFF, the PV source together with C1 are charging C2 so that the voltage across C2 is

$$V_i = V_{dc} + V_{c1} = 2V_{dc} \quad (23)$$

The advantages of the switched capacitor DC/DC converter are:

- High efficiency – the PV source is essentially a current source, therefore the circuit works differently from the conventional voltage source switched capacitor circuit. The capacitor charging current is limited by the PV source. The efficiency of the circuit can be very high.
- Simple control – only two switching modes are considered (S1, S2 ON or S3, S4 ON). The control of the circuit is simple.

The disadvantages of the circuit are:

- Fixed conversion ratio – output voltage is twice the value of the PV input voltage. This means that the DC link voltage of the micro-inverter is strictly twice the PV voltage.
- Large size capacitor needed – in order to achieve MPPT efficiency, the DC link voltage has to be held constant due to the fact that the DC link voltage is strictly twice the PV voltage. Therefore, a large size DC link capacitor is needed.
- Need three PV modules in series – again, the converter can only boost the PV voltage by 2X. In order to meet high line requirements (on the grid side), the PV input voltage can't be below 190 V, which requires three CIGS modules in series. This is not the preferred option from the energy yield point of view, as shown in the study done in section III.
- Complex MPPT control – due to the PV string IV curve (multiple peaks).

Trade-off Matrix

A starting point for the analysis and topology selection were the following project objectives:

- develop a high reliability, low cost micro-inverter
- incorporate Volt/VAR support and auto grid configuration to adapt to the smart grid features
- be in production by 2014

As previously discussed in section III, the parallel connection of the CIGS PV modules gives us the most benefits in terms of the installation and LCOE cost, with the smallest annual energy yield penalty. Analysis in section IV concluded that the two-stage converter approach gives us the most flexibility and ensures that we could meet the reliability and performance targets with a relatively small cost penalty. Therefore, we identified and analyzed ten candidate topologies, six for DC/AC inverter stage and four for DC/DC converter stage. Factors including reliability, cost, efficiency, safety and functionality were evaluated for each approach. Trade-off matrix shown in Table 5.6 was generated by associating each evaluation criterion with the Importance factor to weigh the influence of that criterion on the overall design. Upper and lower limits are also set for the quantifiable criteria. As can be seen from Table 13, the converters were evaluated with respect to efficiency, Volt/VAR capability, common-mode (CM) generation, control simplicity,

semiconductor voltage rating, number of switches, diodes and magnetic components, and output voltage waveform shape.

Table 13: Trade-off Matrix

New | Options | About

Title

Pass | Fail

Concept Sort: Number, Alphabetical, Score, Multi-CTQ — Sort

Score: Evaluate Score — Automatic

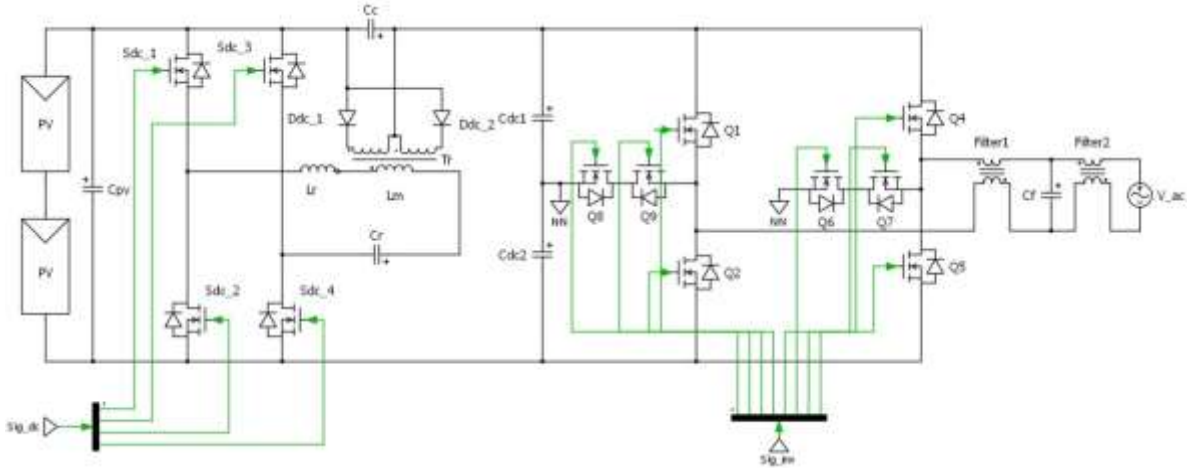
Concepts: Add | Delete | Hide | Show

Group: Modify

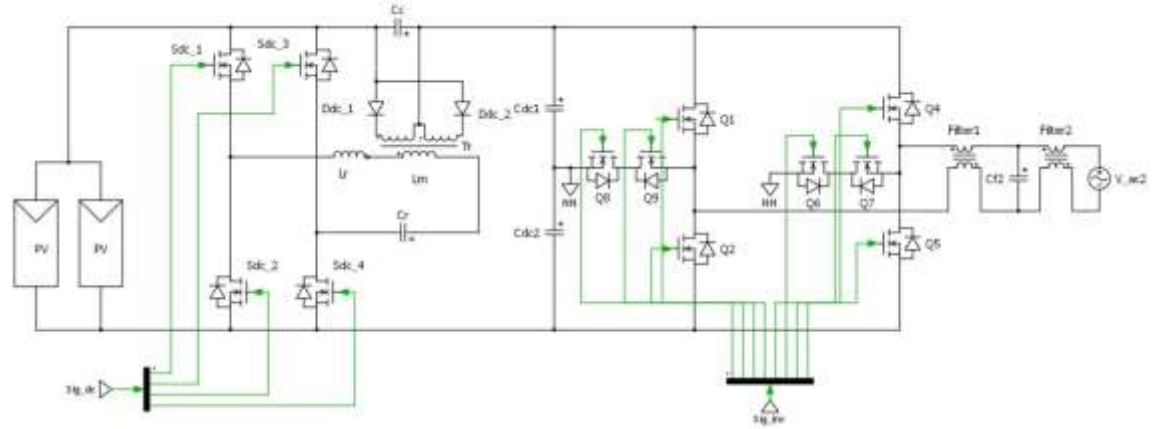
CTQs: Add | Delete | Hide | Show | Sort

			System			Relia	Manufacturability			
			CEC Eff	NO CM voltage generation	Easy to control	Low Device Stress	# of switches	# of magnetics	# of diodes	Differential Filter voltage (bipolar / unipolar)
		Importance	9	9	3	3	1	1	1	1
		USL				600	4	4	2	
		LSL	98%	1	1					1
		Tolerance		0.6						
		Units	%	0 or 1	0 or 1	Volt				0 or 1
	No.	Concepts	Score							
	1	FB with unfolding leg dc-ac	2.38	98%	0	1	600	4	4	0	1
	2	FB with inverleaving dc-ac	3.13	98%	1	1	600	8	6	0	0
	3	GE Z-Source VSI dc-ac	0.38	96%	0	0	800	4	6	1	1
	4	3-level NPC dc-ac	2.88	98%	1	0	150	8	4	4	1
	5	3-level NPP dc-ac	3.38	98%	1	1	300	8	4	0	1
	6	GE FB with fast diodes dc-ac	2.75	98%	1	0	600	4	6	4	0
	7	LLC 2 PV in series dc-dc	2.94	98%		1	250	4	2	2	1
	8	LLC 2 PV in parallel dc-dc	2.94	98%		1	150	4	2	2	1
	9	Isolated boost dc-dc	2.38	92.00%	1	1	600	4	2	2	1
	10	Switched capacitor 3 PV in series dc-dc	2.25	97.00%	1	1	600	4	0	3	1

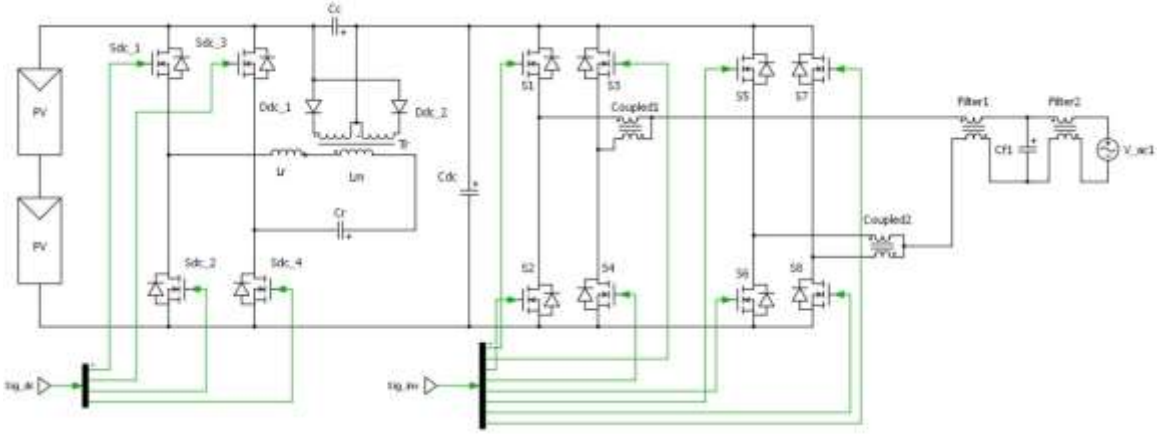
The analysis presented in Section V was used to populate the trade-off matrix and evaluate the total score for each converter. The NPP three-level converter and Interleaved H-bridge converter received the highest score for the DC/AC inverter stage, while LLC resonant converter for two PV connection options (parallel or series) had the highest score for the DC/DC converter stage. Combinations of these converters were used to create the four topologies for further testing for reliability and the rough cost estimation. Those topologies are shown in Figure 46.



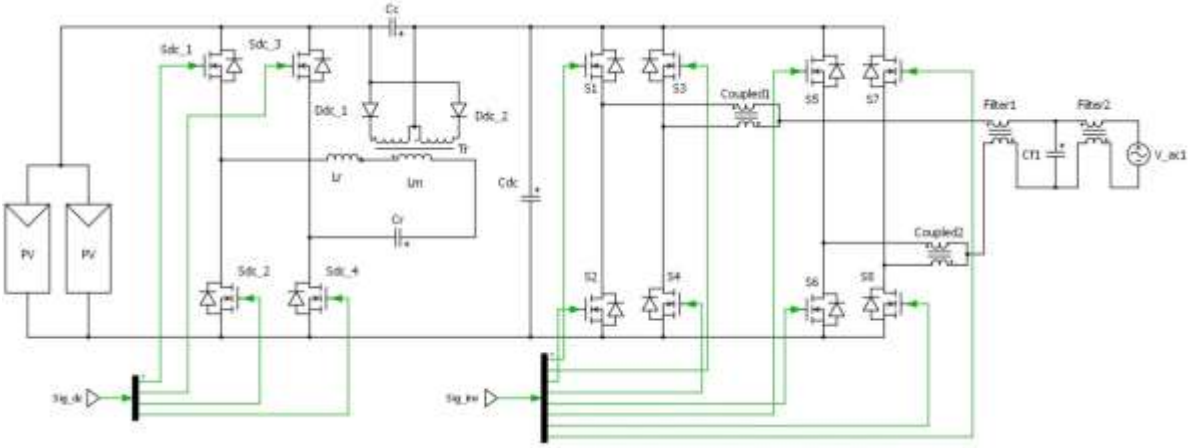
Topology 1



Topology 2



Topology 3



Topology 4

Figure 46: Best Topologies for Further Assessment

3.2.1.5 Cost analysis

The base case for the project is a residential solar electric system with a projected cost of $4.00/W. This system is built around a 235 W multi-silicon-based AC-module and a novel insert and capture racking system that is designed for installation by standard roofing and electrical contracting trades. [26, 27]

For a $4.00/W system the LCOE is ~$0.18/kWh which, without subsidies, is well-above the national average retail price of electricity. Some of the major costs of the system are distributed across the silicon module ($1.85/W) and the balance of system (BOS) which breaks down between the mounting hardware ($0.25/W), the micro-inverter ($0.50/W), and $0.40/W and $0.15/W for the roofing and electrical components of installation respectively. The base system has a best-in-class micro-inverter one can procure today. The cost of this micro-inverter is ~40% of the BOS cost.
In order for the solar LCOE to be lower than the projected average national retail price of electricity, the system price (without subsidies) has to drop below $3.00/W. Achieving this goal by 2015, requires a cost take-out of $1.00/W. A portion of the cost take-out can be realized through lowered module costs. GE projects a $0.75/W cost take-out from the module by 2015, leaving a balance of $0.25/W reduction from BOS. The objective of the project is to demonstrate a systems approach that will result in at least a $0.25/W cost take-out for the AC module that will be primarily driven by innovations in the micro-inverter design. More specifically, the cost take-out will be based on a new micro-inverter that is functionally integrated within the AC-module frame to reduce packaging/materials cost for both the micro-inverter and the module laminate and a new intelligent circuit breaker that reduces micro-inverter cost by offloading duplicate safety and protection functions in an AC module system to a dedicated branch circuit.

Table 14: Total system cost reduction

	Base Case ($/W)	GE Proposal ($/W)	Justification
Module (including J-box & Wiring)	1.85	1.10 -0.09	• CIGS module with J-Box • Elimination of J-Box
Microinverter	0.5	0.33 -0.10	• In-house manufacturing • Integration & simplification (Figure 6)
Racking System	0.22	0.22	
Installation	0.55	0.55	
Distribution & Margin	0.88	0.88	• In-house manufacturing
Total	**4.00**	**2.89**	

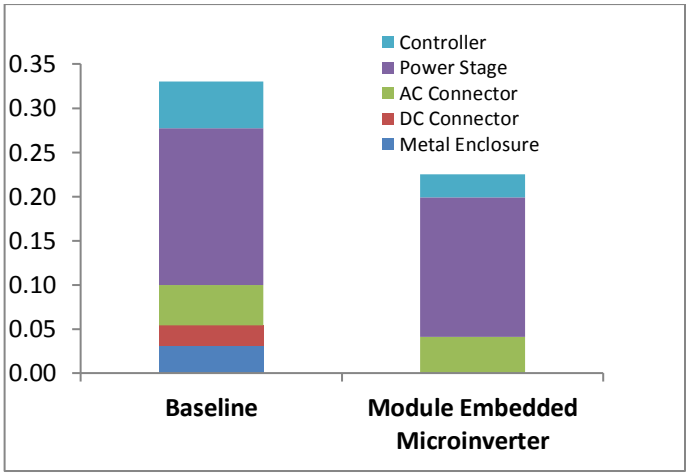


Figure 47: Cost reduction on micro-inverter

As mentioned in Section 3.2.1.2 up to one-third of the cost of a micro-inverter is in the metal heatsink, case, wiring, and connectors. The merger of a micro-inverter and PV module provides additional opportunities for cost reduction that is based on either the elimination of components or the functional sharing of components. Figure 47 and Table 14 show the proposed cost reductions for GE's proposed micro-inverter-based system. The baseline cost for the micro-inverter is projected at $0.33/W based on third-party benchmark analysis. This project will result in an additional reduction of $0.10/W through centralized grid support function and tighter packaging integration with the PV module.

The cost savings are $0.02/W on the power stage, $0.02/W for the controller, $0.01/W for the simplified AC connector, as well as $0.02/W and $0.03/W for the elimination of the DC connector and metal enclosure respectively. In addition, the micro-inverter also contributes to a $0.09/W cost reduction of the PV module due to the elimination of the J-box. The resulting projected system price is less than $3/W.

Table 15a to 15d show the comparison of the main components costs for the four front runner topologies selected after trade-off analysis in the section V. The selection of Topology 4 as the basis for the final design was based on this comparison. It offers the largest cost reduction due to the use of the most economical semiconductor devices without compromising the converter performance.

The voltage and current ratings for the semiconductor devices are dictated by the series/parallel connection of the CIGS modules at the input of the micro-inverter as well as the inverter topology. Currently, due to the broader application space, market prices for the semiconductor devices in the <150 V and around 600 V operating range are cheaper that the prices for the other voltage ranges, which influences the total price of the four topologies.

Table 15: Micro-inverter Preliminary Cost Estimation

(a) Topology 1 Main micro-inverter components pricing

Item	Category	Quantity	Reference	Value	Manf	Manf Part No.	price $	scalled price $	Total
1	Capacitor	2	Cdc1, Cdc2	30uF, 300V	EPCOS Inc	495-2955-ND	7.46	3.73	7.46
2	Capacitor	1	Cc	35uF, 450V	Kemet	399-6237-ND	7.93	3.965	3.965
3	Capacitor	1	Cf	0.56uF,450V	Panasonic - ECG	P14203-ND	0.293	0.1465	0.1465
4	Capacitor	1	Cpv	30uF, 300V	EPCOS Inc	495-2955-ND	7.46	3.73	3.73
5	Capacitor	1	Cr	33nF, 200V	Panasonic - ECG	P4555A-ND	0.091	0.0455	0.0455
6	Diode	2	Ddc_1, Ddc_2	1200V, 2A	Cree	C4D02120A-ND		0.5	1
7	MOSFET	4	Sdc_1 - Sdc_4	300V, 60A	ST	497-8463-5-ND	3.5675	3.5	14
8	MOSFET	4	Q1, Q2, Q4, Q5	650V, 9A	Infineon	IPB60R385CP-ND	1.3	0.55	5.2
9	MOSFET	4	Q6, Q7, Q8, Q9	300V, 50A	IXYS	IXFT50N30Q3-ND	5.72	3	12
10	Inductor	1	Lr	55uH				3	3
11	Coupled Inductor	1	Lfilter1	1mH, k=0.99				?	
12	Coupled Inductor	1	Lfilter2	0.125mH, k=0.99				?	
13	Transformer	1	Tr	135uH, transfer ratio 1:2				5.5	5.5
14	Isolated drivers	6		IR2181(4)(S)	International rectifier			0.8	4.8
15	Zigbee	1					2.8		2.8
16	F28065	2	DSP		TI		1.99		3.98
17	Housekeeping PS	1					1.49		1.49

(b) Topology 2 Main micro-inverter components pricing

Item	Category	Quantity	Reference	Value	Manf	Manf Part No.	price $	scalled price $	Total
1	Capacitor	2	Cdc1, Cdc2	30uF, 300V	EPCOS Inc	495-2955-ND	7.46	3.73	7.46
2	Capacitor	1	Cc	30uF, 450V	EPCOS Inc	495-3010-ND	7.93	3.965	3.965
3	Capacitor	1	Cf	0.56uF,450V	Panasonic - ECG	P14203-ND	0.293	0.1465	0.1465
4	Capacitor	1	Cpv	30uF, 300V	EPCOS Inc	495-2955-ND	7.46	3.73	3.73
5	Capacitor	1	Cr	132nF, 160V	Vishay BC Components	BC2094-ND	0.57	0.285	0.285
6	Diode	2	Ddc_1, Ddc_2	1200V, 2A	Cree	C4D02120A-ND		0.5	1
7	MOSFET	4	Sdc_1 - Sdc_4	150V, 9A	Infineon	BSB165N15NZ3 G-ND	1.96	2	7.84
8	MOSFET	4	Q1, Q2, Q4, Q5	650V, 9A	Infineon	IPB60R385CP-ND	1.3	0.55	2.2
9	MOSFET	4	Q6, Q7, Q8, Q9	300V, 50A	IXYS	IXFT50N30Q3-ND	5.72	3	12
10	Inductor	1	Lr	14uH				3	3
11	Coupled Inductor	1	Lfilter1	1mH, k=0.99				?	
12	Coupled Inductor	1	Lfilter2	0.125mH, k=0.99				?	
13	Transformer	1	Tr	88uH, transfer ratio 1:5				5.5	5.5
14	Isolated drivers	6		IR2181(4)(S)	International rectifier			0.8	4.8
15	Zigbee	1					2.8		2.8
16	F28065	1	DSP		TI		1.99		1.99
17	Housekeeping PS	1					1.49		1.49

(c) Topology 3 Main micro-inverter components pricing

Item	Category	Quantity	Reference	Value	Manf	Manf Part No.	price $	scalled price $	Total
1	Capacitor	1	Cdc	20uF, 600V	Kemet	399-6216-ND	6.13	3.065	3.065
2	Capacitor	1	Cc	35uF, 450V	Kemet	399-6237-ND	7.93	3.965	3.965
3	Capacitor	1	Cf	0.56uF,450V	Panasonic - ECG	P14203-ND	0.293	0.1465	0.1465
4	Capacitor	1	Cpv	30uF, 300V	EPCOS Inc	495-2955-ND	7.46	3.73	3.73
5	Capacitor	1	Cr	33nF, 200V	Panasonic - ECG	P4555A-ND	0.091	0.0455	0.0455
6	Diode	2	Ddc_1, Ddc_2	1200V, 2A	Cree	C4D02120A-ND		0.5	1
7	MOSFET	4	Sdc_1 - Sdc_4	300V, 60A	ST	497-8463-5-ND	3.5675	3.5	28
8	MOSFET	8	Q1 - Q8	650V, 9A	Infineon	IPB60R385CP-ND	1.3	0.55	10.4
9	Inductor	1	Lr	55uH				3	3
10	Coupled Inductor	1	Lfilter1	1mH, k=0.99			?	?	
11	Coupled Inductor	1	Lfilter2	0.125mH, k=0.99			?	?	
12	Coupled Inductor	2	Tr 1, 2	5mH, k=0.99			?	?	
13	Transformer	1	Tr	135uH, transfer ratio 1:2				5.5	5.5
14	Isolated drivers	7		IR2181(4)(S)	International rectifier			0.8	5.6
15	Zigbee	1						2.8	2.8
16	F28065	1	DSP		TI		1.99		1.99
17	Housekeeping PS	1					1.49		1.49

(d) Topology 4 Main micro-inverter components pricing

Item	Category	Quantity	Reference	Value	Manf	Manf Part No.	price $	scalled price $	Total
1	Capacitor	1	Cdc	20uF, 600V	Kemet	399-6216-ND	6.13	3.065	3.065
2	Capacitor	1	Cc	30uF, 450V	EPCOS Inc	495-3010-ND	7.93	3.965	3.965
3	Capacitor	1	Cf	0.56uF,450V	Panasonic - ECG	P14203-ND	0.293	0.1465	0.1465
4	Capacitor	1	Cpv	30uF, 300V	EPCOS Inc	495-2955-ND	7.46	3.73	3.73
5	Capacitor	1	Cr	132nF, 160V	Vishay BC Components	BC2094-ND	0.57	0.285	0.285
6	Diode	2	Ddc_1, Ddc_2	1200V, 2A	Cree	C4D02120A-ND		0.5	1
7	MOSFET	4	Sdc_1 - Sdc_4	150V, 9A	Infineon	BSB165N15NZ3 G-ND	1.96	2	15.68
8	MOSFET	8	Q1 - Q8	650V, 9A	Infineon	IPB60R385CP-ND	1.3	0.55	4.4
9	Inductor	1	Lr	14uH				3	3
10	Coupled Inductor	1	Lfilter1	1mH, k=0.99			?	?	
11	Coupled Inductor	1	Lfilter2	0.125mH, k=0.99			?	?	
12	Coupled Inductor	2	Tr 1, 2	5mH, k=0.99			?	?	
13	Transformer	1	Tr	88uH, transfer ratio 1:5				5.5	5.5
14	Isolated drivers	7		IR2181(4)(S)	International rectifier			0.8	5.6
15	Zigbee	1						2.8	2.8
16	F28065	2	DSP		TI		1.99		3.98
17	Housekeeping PS	1					1.49		1.49

More accurate cost estimation will be presented at the end of the prototype development phase. This preliminary costing of the main components was conducted to determine if there are any significant obstacles to achieving the proposed $0.25/W cost of the micro-inverter.

3.2.1.6 Reliability analysis

Overview

The objective of this analysis is to evaluate the reliability of different configurations of micro- inverters to be used as one of the criteria to select the topology to be used in the second phase of the project.
The reliability requirement for the micro-inverter is to survive 20 years at an average usage of 8 hours a day. That amounts to a total of 58440 hours.
Two topologies (Topology 1 and Topology 4, shown in Figure 5.26) were evaluated using the Reliasoft Lambda Predict software based on the Telcordia SR 332 Issue 2 standard [29, 30]. For each of the topologies, nine operating conditions were evaluated, three different power configurations: 25%, 70%, and 100%, and also three different voltage levels for each topology (128, 133, and 148 V for Topology 1 and 64, 69, and 75 V for Topology 4).
Both topologies show a Reliability greater than 97.5% for the target life of 20 years under the described operation conditions.
Method

The reliability of each topology was computed by applying the Telcordia SR 332 Issue 2 standard implemented in the Reliasoft Lambda Predict software. This is a well-known standard in the industry to predict reliability of electronic equipment for commercial applications. Its methodology combines generic failure rates with part stress factors to assess the impact of operating conditions on the reliability.
For each topology and load condition the system's Mean Time Before Failure (MTBF) is computed in hours. That number is used to compute the reliability of the system as the probability of reaching the goal of 58440 hrs.
Each component is specified based on its configuration and electrical ratings (voltage, current, power). For each operating conditions, the applied stresses (voltage, current, power) and increase in temperature (for diodes and transistors) are computed using PLECS simulation software. These are theoretical calculations since no physical device has been constructed and tested yet.
For these analyses it is assumed that the operating temperature is the maximum temperature specified in the micro-inverter specifications 85 ºC

Results

Table 16 shows the results for the Topology 1 where the front end is LLC DC/DC converter with two CIGS modules connected in series followed by the NPP inverter. The reliability for all input voltages under all operating conditions is greater than 97.8% for the target life of 20 years.
Error! Reference source not found. and **Error! Reference source not found.**49 show th e component failure rate for the 149 V input voltage and with 25% and 100% of rated power operating conditions, as an example. In the both cases the transformer is the component with the highest failure rate followed by the MOSFETS, which are similar. These plots are representative of the behavior of the Topology 1.

Table 16: Reliability Results for Topology 1

Input voltage [V]	Power [%]	MTBF (hours)	Goal (hours)	Reliability [%]
128	25	3.06E+06	58440	98.1
128	70	2.90E+06	58440	98.0
128	100	2.73E+06	58440	97.9
133	25	3.04E+06	58440	98.1
133	70	2.86E+06	58440	98.0
133	100	2.68E+06	58440	97.8
149	25	3.06E+06	58440	98.1
149	70	2.92E+06	58440	98.0
149	100	2.77E+06	58440	97.9

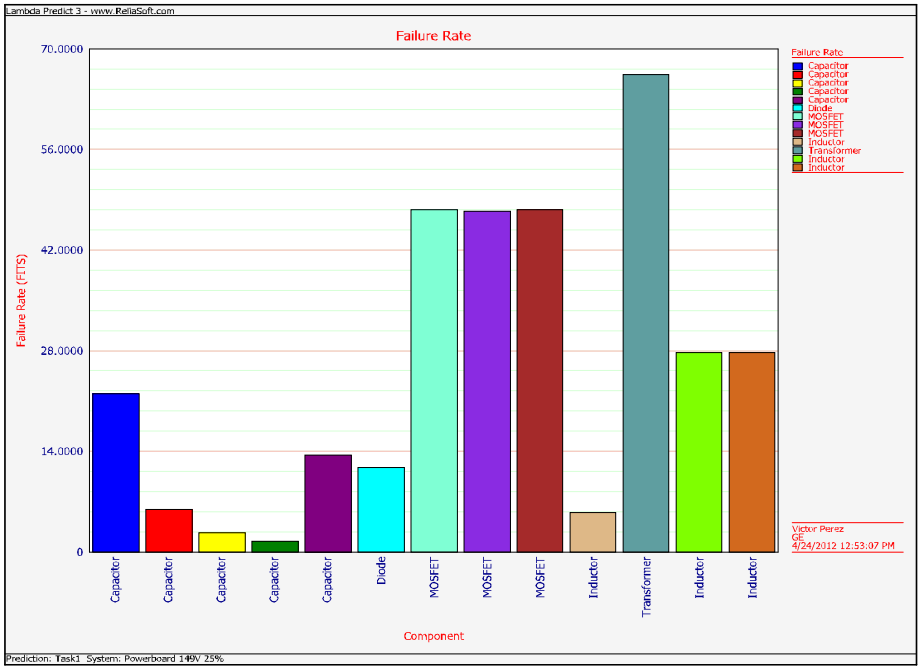


Figure 48: Component Failure Rate for Topology 1 with 149 V and 25% Power

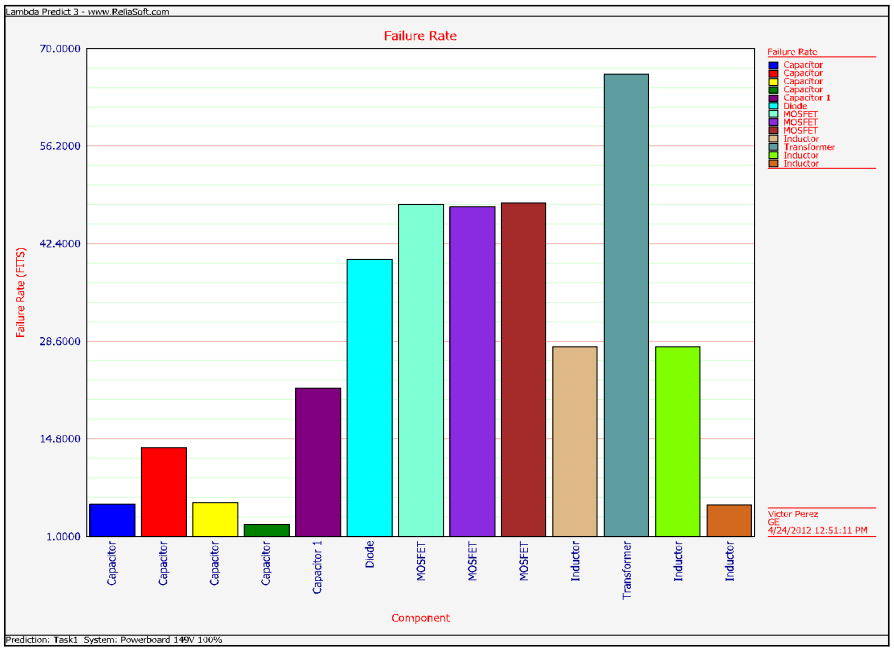


Figure 49: Component Failure Rate for Topology 1 with 149 V and 100% Power

The reliability results for Topology 4 where the front end is the LLC DC/DC converter with two CIGS modules connected in parallel followed by the Interleaved Full Bridge inverter are shown in Table 17. Again, for this topology the reliability is above 97.5%.

Error! Reference source not found. and **Error! Reference source not found.**51, show the failure rate for each of the components in Topology 4 for the 75V input voltage and with 25% and 100% rated power operating conditions. The 25% failure rate profile (Figure 7.3) is very similar for all the input voltage conditions (64 V, 69 V, and 75 V). Both MOSFET switches (in the DC/DC and the DC/AC stage) present the highest failure rate component. **Error! Reference source not found.** is a representative of the behavior for the 70% and 100% power for all the input voltage conditions (64 V, 69 V, and 75 V). In this case the DC/AC stage MOSFETs Q1 to Q8 are the components with the highest failure rate.

Table 17: Reliability Results for Topology 4

Input voltage [V]	Power [%]	MTBF (hours)	Goal (hours)	Reliability [%]
64	25	3.30E+06	58440	98.2%
64	70	2.55E+06	58440	97.7%
64	100	2.45E+06	58440	97.6%
69	25	3.22E+06	58440	98.2%
69	70	2.49E+06	58440	97.7%
69	100	2.38E+06	58440	97.6%
75	25	3.07E+06	58440	98.1%
75	70	2.42E+06	58440	97.6%
75	100	2.33E+06	58440	97.5%

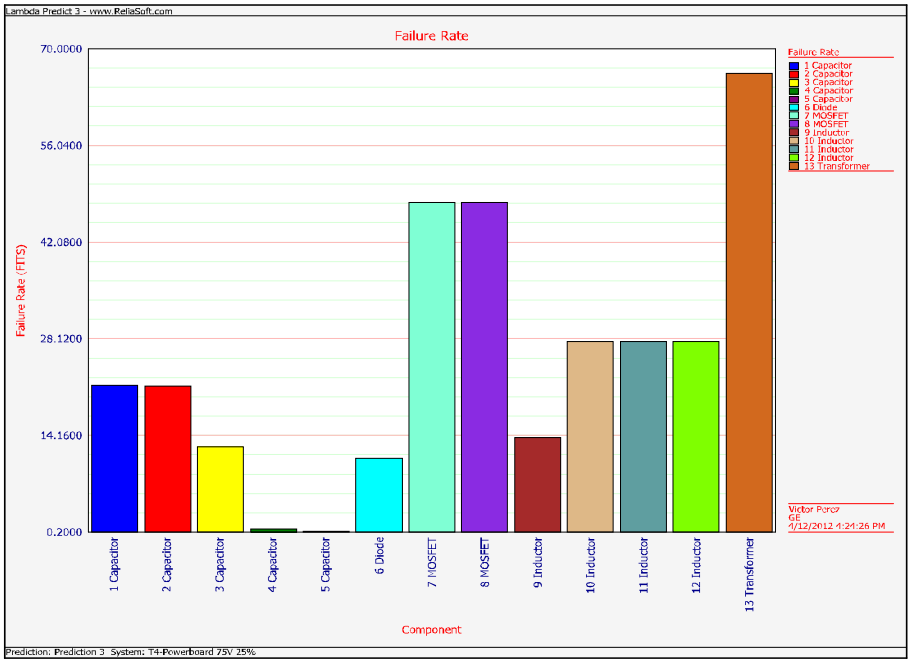


Figure 50: Component Failure Rate for Topology 4 with 75V and 25% Power

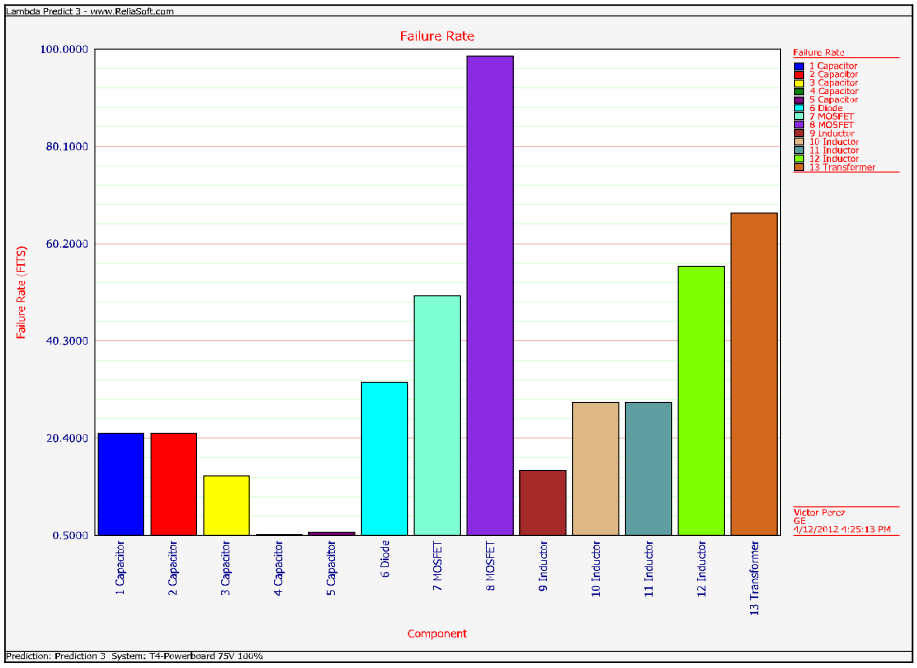


Figure 51: Component Failure Rate for Topology 4 with 75 V and 100% Power

Both topologies studied show reliability greater than 97% of reaching 20 years of service, assuming 8 hours per day under different loading conditions. The DC/DC and DC/AC stages in topologies 1 and 4 are designed using different converters from the pool of the best possible converter designs as previously discussed in Section V. Therefore, the reliability analysis presented here covers all possible building blocks and since the overall reliability is shown to be high in both topologies there is no need for separately testing topologies 2 and 3. Those topologies would use the same converters in different combinations and their reliability would be very similar to the shown cases.

3.2.1.8 Conclusion

As a result of the detailed design analyses and trade-off studies, the GE team down-selected one micro-inverter topology to be used for the rest of the program. The chosen topology is the LLC resonant converter designed for two PV CIGS modules connected in parallel with the partial power method followed by the Interleaved H-bridge inverter controlled with the team operation approach, referred to as Topology 4 after the trade of study.

3.2.2 Task2: Conduct the embedded µ-inverter conceptual design and testing

According to the analysis performed in section 3.2.1, a micro-inverter topology with a partial power processing LLC resonant DC/DC converter at the input and an interleaved H-bridge inverter stage is chosen. The topology is shown in Figure 52. Table 18 shows the specification of the converter for cases of two series connected CIGS panels and for two parallel CIGS panels. The design for two parallel panels is implemented.

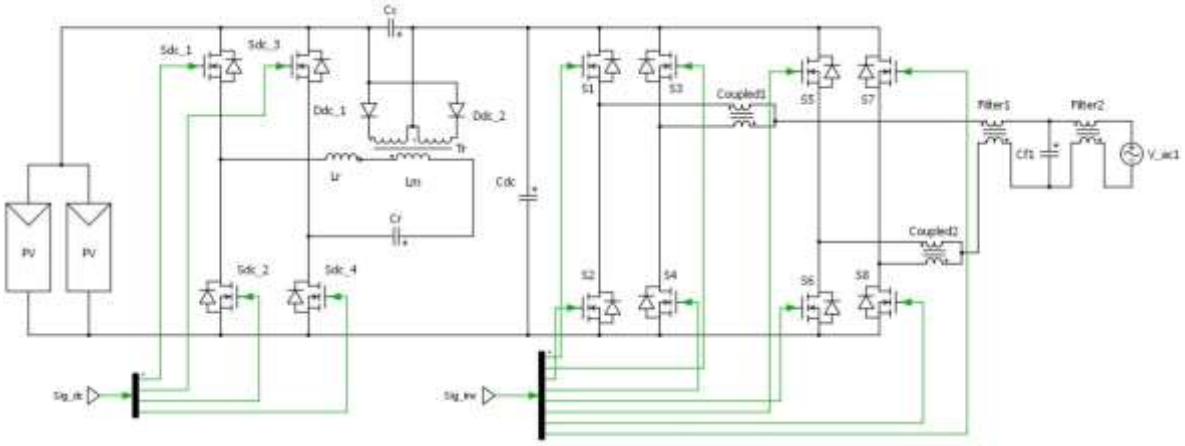


Figure 52: Circuit topology for micro-inverter with two parallel CIGS panels

Table 18: Micro-inverter specifications

Competitor / Specification	GE ThinFilm (studied)	GE 2 modules in series (studied)	GE 2 modules in parallel (proposed)
Power Level	157W	300W	300W
Max Input DC Voltage	130V	260V	130V
MPPT Tracking voltage	64-93V	128-186V	64-93V
Min/Max Start Voltage	64-93V	128-186V	64-93V
Maximum DC Short Circuit Current	2.11A	2.11	4.22
Maximum Input Current	2.1A	2.1	4.2
AC Output Voltage	US: 240V/(206-269V) EU: 220V(187-242V)	US: 240V/(206-269V) EU: 220V(187-242V)	US: 240V/(206-269V) EU: 220V(187-242V)
Maximum Continuous Output Power	152	305W	305W
Max units per branch	33	16	16
Nominal Output Current	US: 633mA EU:691mA	US: 1.27A EU: 1.39A	US: 1.27A EU: 1.39A
Maximum output fault current			
Frequency	US:60Hz(59.3-60.5Hz) EU:50Hz(49-51Hz)	US:60Hz(59.2-60.6Hz) EU:50Hz(49-51Hz)	US:60Hz(59.2-60.6Hz) EU:50Hz(49-51Hz)
Power Factor	>0.95	>0.95	>0.95
Volt/Var Support	Yes	Yes	Yes
Auto Grid Configurability	Yes	Yes	Yes
MPPT Efficiency	>99%	>99%	>99%
CEC efficiency	96%	96.0%	96.0%
Peak Efficiency	97%	96.5%	96.5%
Operating Temperature	-40-65degC	-40 to +85degC	-40 to +85degC
Cooling	Natural Convection	Natural Convection	Natural Convection
Package	NEMA6, Embedded within Solar Frame	NEMA 6	NEMA 6
Night Power Consumption	<30mW	<30mW	<30mW
LED Indicators	No	Yes	Yes
Sine wave (THD)	THD<5% Single Harmonic <3.5%	Total THD<5% Each Harmonic<3.5%	Total THD<5% Each Harmonic<3.5%
Telephone Interference	I*T<10,000		
Communication Arch	Powerline (TBD)	Powerline (TBD)	Zigbee
Communication Architecture (SCE 2.0 Zigbee? Neucleus?)	TBD	TBD	Zigbee
Dimensions (WXHXD in)	TBD	6.8" x 5.9" x 1.1" (TBD)	8" x 8" x 2" (TBD)
Weight (lbs)	TBD	3.0 lbs (TBD)	3.0 lbs (TBD)
Compliance	US: UL1741/IEEE1547/FCC Part 15 Class B EU: IEC60730, IEC61727, IEC 62116, IEC61000 Germany: VDE0126-1-1	UL1741/IEEE1547/FCC Part 15 Class B	UL1741/IEEE1547/FCC Part 15 Class B
Warranty	25 years	20 years	20 years
Connectors	GE Connector?	GE Connector?	GE Connector?
Configuration for Country	TBD	TBD	USA (TBD)

The converter prototype was built and the lab test setup is shown in Figure 53, with the input source being a Magna DC power source for open loop characterization and a Terrasas PV emulator for closed loop testing.

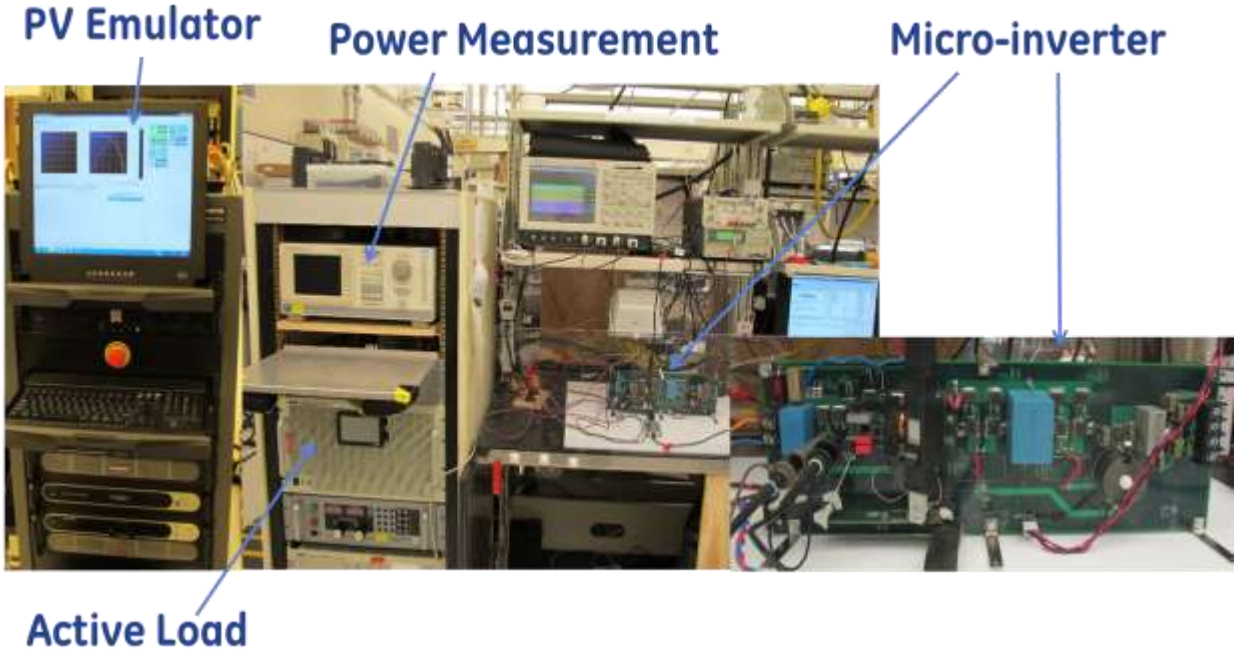


Figure 53: Micro-inverter test setup

The micro-inverter key tests are as follows:

Test 1.A) DC/AC stage efficiency: test setup is shown in Figure 54 and test conditions were as follows:
Control voltage 5V and 15V connected from outside power supply.
Set voltage to MPPT value:
DC-link voltage set to 430V
Load set to 75% load (225W).

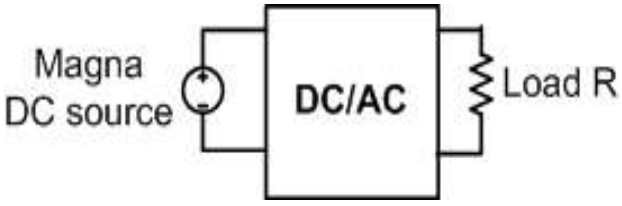


Figure 54: DC/AC stage efficiency test setup

The inverter output waveforms and measured values are shown in Figure 55 and table 19.

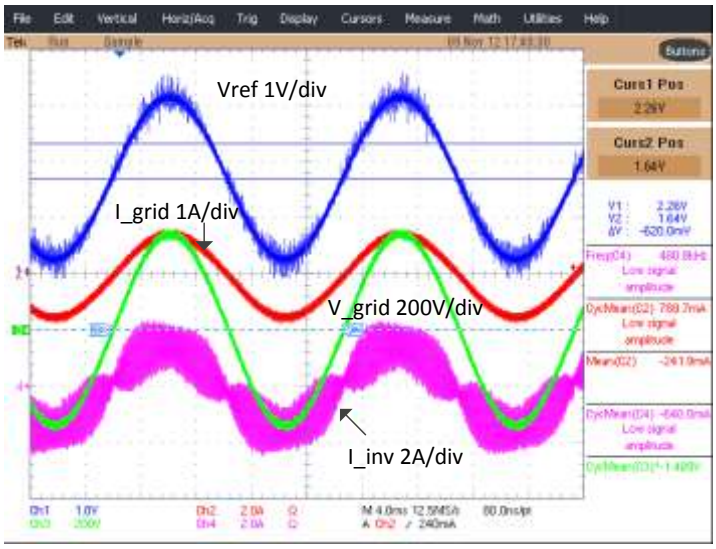


Figure 55: Output Waveform of DC/AC Stage at Open Loop

Table 19: Measured values in DC/AC inverter open loop test

I_{in}	V_{in}	I_{out}	V_{out}	Efficiency	Losses
0.026A	400.1V	1.084A	225.8V	98.3%	5.69W

Test 1.B) DC/DC stage efficiency: test setup is shown in Figure 56 and test conditions were as follows:
Control voltage 5V and 15V connected from outside power supply.
Set CIGS curve of 2 module in parallel:
DC-link voltage set to 430V
Irradiance set to 75% load.

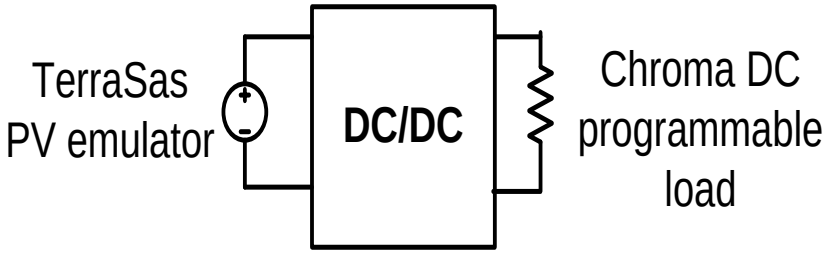


Figure 56: Test setup for DC/DC stage efficiency test

The inverter output waveforms and measured values are shown in Figure 57 and table 20.

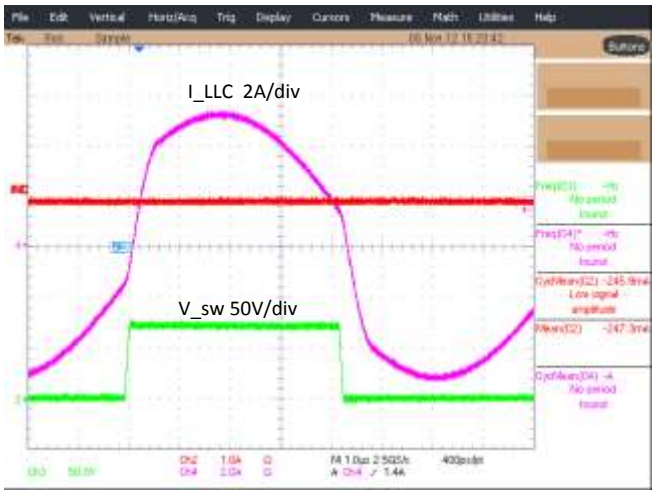


Figure 57: LLC Resonating Waveform ff DC/DC Stage at Open Loop

Table 20: Measured values for DC/DC converter open loop test

I_{in}	V_{in}	I_{out}	V_{out}	Efficiency	Losses
3.778A	71.3V	0.598A	440.1V	97.7%	6.19W

Test 2) Closed loop operation with both stages: test setup is shown in Figure 58 and test conditions were as follows:
Control voltage 5V and 15V connected from outside power supply.
Set CIGS curve of 2 module in parallel:
Set voltage to DC-link value: 430V
Line voltage nominal 240V

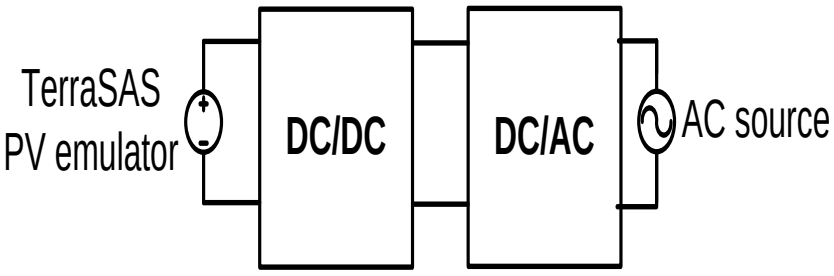


Figure 58: Test setup for closed loop test

MPPT efficiency is measured to be >99% as shown in Figure 59.

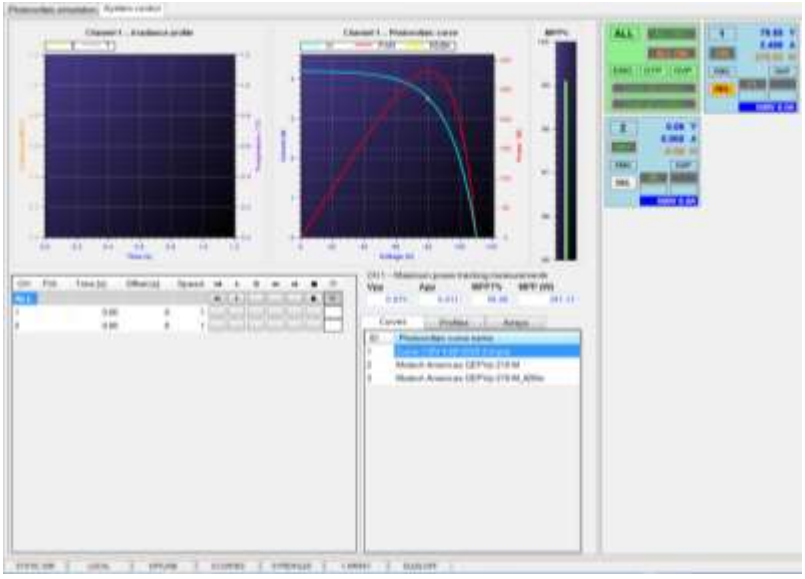


Figure 59: MPPT test

At the time of testing at November 15th , 2012, the relay has not been added in the circuit and the micro-inverter is started with grid voltage already applied. This required a soft start procedure to reduce inrush current at PV input side. It was implemented by adopting a ramp up time window to decrease LLC frequency gradually (the lower the frequency, the higher the current). Figure below shows the micro-inverter waveform when ramp-up time is 45ms. The LLC current rise gradually and never comes to its maximum. The energy delivered to DC-bus side is well limited, so in this case the DC-bus voltage is well maintained. The ac waveform is shown in Figure 60 for a case of pure active power and Figure 61 shows the soft starting of the inverter

.

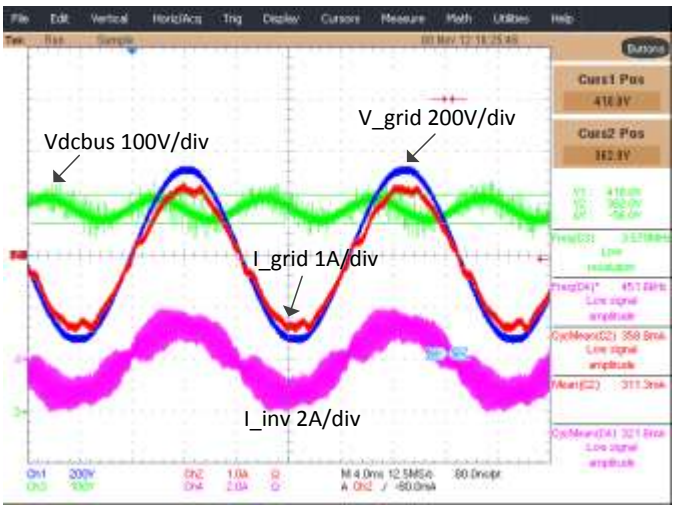


Figure 60:Output Waveform When Micro-Inverter Delivering Pure Real Power

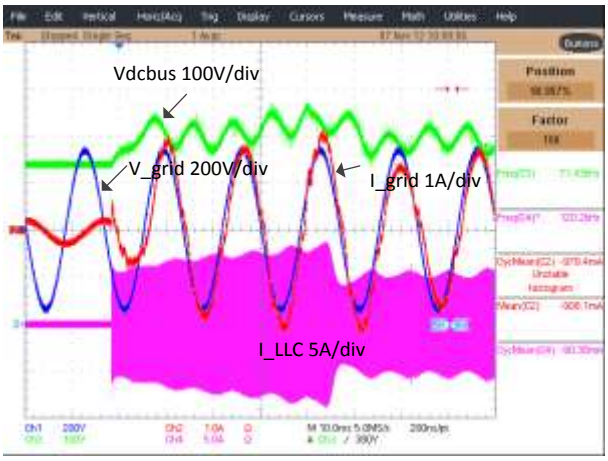


Figure 61:Soft Start: Startup at Ramp-Up Time 45ms

Figures 62 and 63 show leading and lagging reactive power operating conditions with ±80VARs.

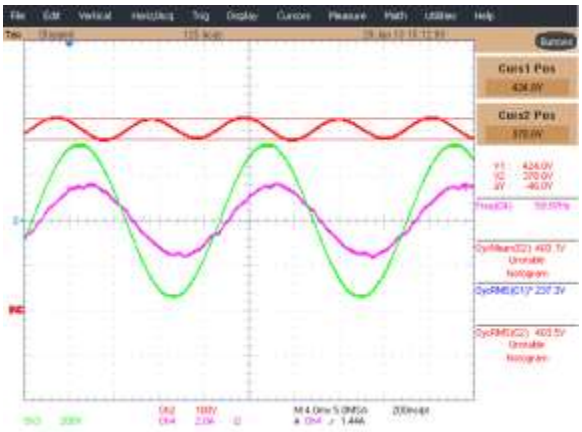


Figure 62:Output Waveform when the Micro-Inverter is Delivering Real Power and 80VAr Reactive Power

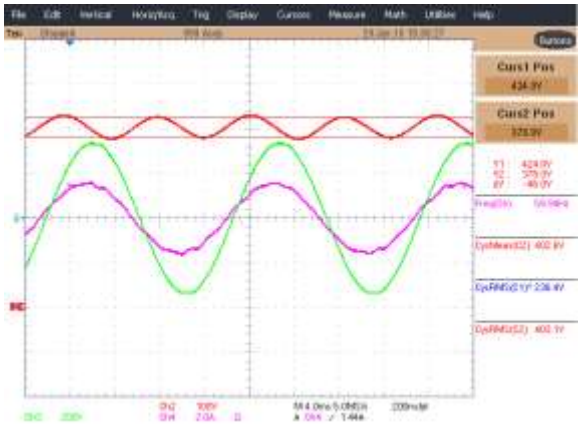


Figure 63: Output Waveform when the Micro-inverter is Delivering Real Power and -80VAr Reactive Power

Test 3) Passive anti-islanding demo with under voltage condition 203V

Figure 64 shows the results when the grid voltage has variation. When the grid voltage drops from 240V to 203V which is more than 15%, the controller will detect this and trigger the breaker after 1.6s. In the same way, if the grid voltage is increased to more than 10%, the anti-islanding algorithm will detect this change and trigger the breaker due to the grid standards requirement.

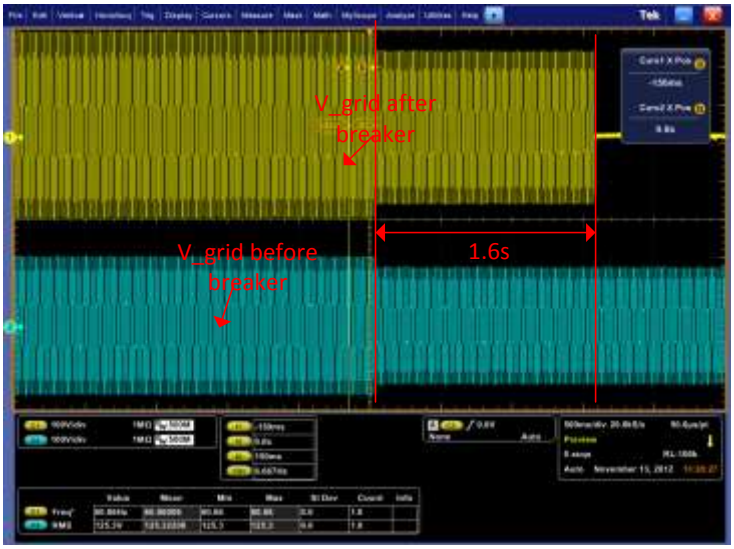


Figure 64: Islanding Detection for Low Voltage

Test 4) Efficiency vs. Power measurement

The efficiency curves of the micro-inverter for different power levels are shown in Figure 65, with about 2W consumed by housekeeping supply.

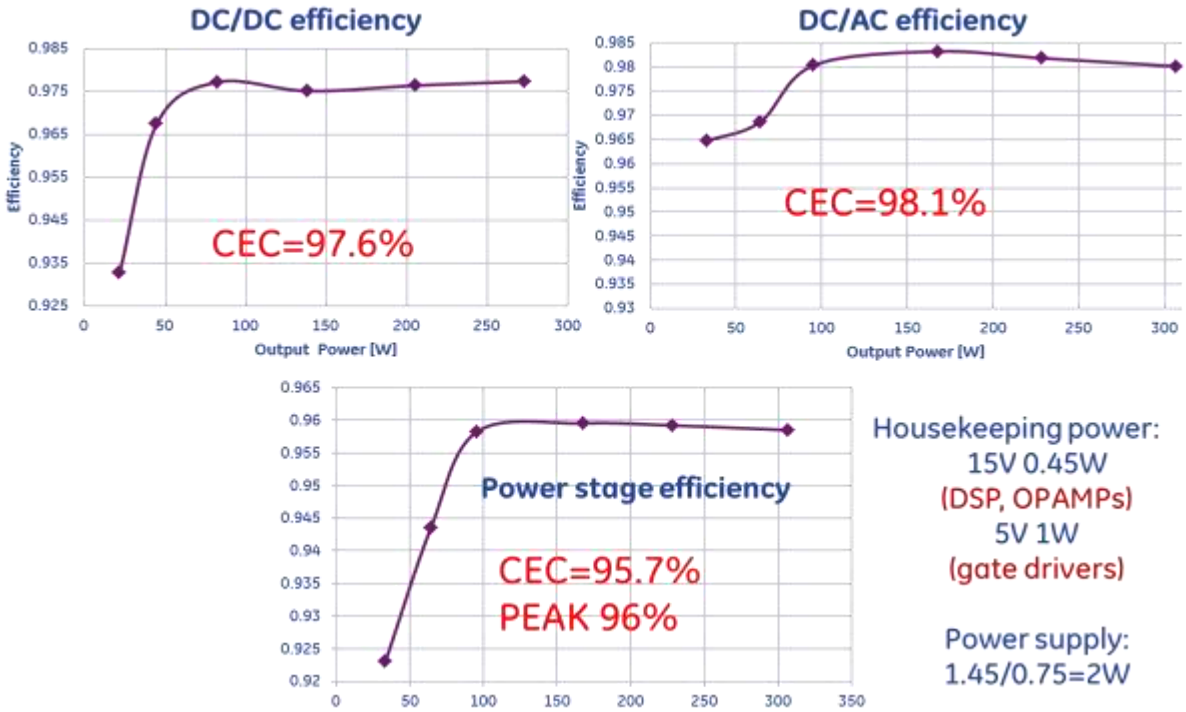


Figure 65: Micro-inverter efficiency measurement

3.2.3 Task 3: Configure photovoltaic panel and smart grid emulator

3.2.3.1 PV emulator setup

TerraSAS is an easily programmable system designed to simulate the electrical behavior of a photovoltaic array. The system provides a turn-key hardware and software approach to deliver all the functionality required to test the maximum peak power tracking (MPPT) characteristics of solar inverters and charge controllers. The ability to simulate any fill factor and material technology allows the system to characterize the inverter MPPT algorithm performance quickly and efficiently. Test software including items based on the Sandia National Labs “Performance Test Protocol for Evaluating Inverters Used in Grid-Connected Photovoltaic System” is incorporated to allow easy programming of the various test requirements. The TerraSAS is a fully integrated system that can simulate an IV curve of a PV panel from data normally found in the manufacturer data sheets with programmable open circuit voltage (Voc) and short circuit current (Isc), as required for a wide variety of inverters. The system software also allows the user to change the array fill factor by programming the peak power points, Vmpp and Impp, to simulate different solar cell characteristics. This combination of hardware allows the TerraSAS to simulate most test protocols and events that a solar installation will be subjected to. The TerraSAS also allows the user to program the following parameters: irradiance level, temperature value, βv (voltage temperature coefficient) and βp (power temperature coefficient), and simulation time to ramp the voltage, temperature or irradiance level.
TerraSAS consists of a rack mounted control computer with control software and PV simulation engine that controls each programmable DC power supply. The TerraSAS control computer runs the Windows 7 operating system. Hardware control is

accomplished by an application operating as dedicated IV curve generation processors, which communicates directly to the PV simulators using Ethernet. The local Graphical User Interface (GUI) is accomplished via another application that provides all of the user controls to the TerraSAS system. Imbedded in the application is the Ethernet parser for remote communication and control. All of the functions available locally through the control computer are also available remotely. Figure 66 shows the actual hardware setup on the bench.

Figure 66:TerraSAS PV Emulator with Two Channels

System Controller

The System Controller is a rack mounted industrial computer running Microsoft Windows 7 Professional. It is the primary interface for controlling the operation of the TerraSAS system and reading back measured data. The user interacts with the system through the controller's LCD monitor and keyboard or remotely through an Ethernet port located on the cabinet's rear panel. The System Controller communicates with one or more PV Simulators via an auxiliary Ethernet port and the local network designated as "TerraSAS Net". In large multi-channel systems, the System Controller is augmented with an industrial grade Ethernet switch, which connects to the simulators. Up to 48 simulators may be connected to a single system controller. TerraSAS Net may be extended to one or more slave cabinets in high-power systems, where more than one cabinet is required to house the simulators and power sources. In the smaller systems, the System Controller is typically augmented with a 5 or 8-port Ethernet switch.

The PV Simulator is at the heart of the TerraSAS simulator system. It receives the IV curve data from the system controller and continually monitors and influences the output voltage and output current being delivered by its associated power source(s). At the center of the PV simulator are two 80 MIPS RISC microcontrollers. One processor interfaces with a 16-bit measurement system that monitors the DC power supply's output

voltage and current at 40 µs intervals. At each interval, the processor sends computed data to its 16-bit D/A control system that adjusts the power supply's analog input controls to precisely follow the IV curve loaded in memory. The second processor is dedicated to the Ethernet interface and digital I/O.

While in Static Simulation mode, the PV Simulator executes a single IV curve. A typical PV panel IV curve is shown in Figure 67 below.

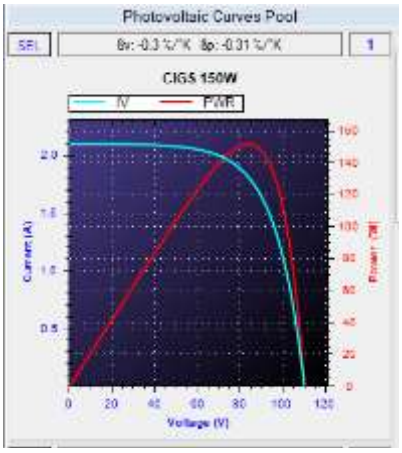


Figure 67: Example IV Curve

In the PV Simulator system, an IV curve is represented by 1024 data pairs or points. Each pair of values represents a single voltage/current point on the IV curve. The PV Simulator retains the active curve in memory and continuously programs the power supply to respond to changes measured in output voltage and current. The PV simulator interpolates the 1024 points in its curve memory with 16-bit accuracy, delivering an actual curve resolution of 65536 points.

DC Power Sources

The DC Power source(s) used in the TerraSAS system are enhanced versions of the Sorensen models DCS80-15, SGA600-XX and SGA1000-XX power supplies. Modifications have been made to improve the output response time by a factor of 10, compared to standard catalog models. On DCS power supplies, mainly used in micro-inverter test systems, the PV controller is embedded into the power supply, providing a complete solution in a 1U chassis.

System specifications

Number of PV Simulator Channels: 2
Remote Control: Ethernet
Operating System: Microsoft Windows 7
Ametek Part Number: 5702359-01
Control Computer: Ametek P/N 881-686-25 (Dual NIC, 1000 Mb/s, copper)

AC Input
Line voltage: 480 VAC ±10% , 3-phase, 50/60Hz , 4-wire (L1, L2, L3 , Ground)
Max input current at 440 VAC (Low Line): 50A per phase

Main circuit breaker: 50A, 600V

DC Output
Open Circuit Voltage, Voc: 0 - 600VDC
Short Circuit Current, Isc: 0 – 8A (per channel)

Maximum output power at MPP: 4.31 kW at fill factor 0.85

Accuracy
Voltage: 1% error of calculated curve formula at E>250 W/m2
Current: 2% error of calculated curve formula at E>250 W/m2
Voltage Readback: 0.2% of max voltage
Current Readback: 0.5% of max current

Curve equations
Equations used to calculate the IV curves are found in Appendices A1 and A2 of the publication “Performance Test Protocol for Evaluating Inverters Used in Grid- Connected Photovoltaic System", October 2004, Sandia National Labs.

PV Array Parameters
Irradiance level: 0 to 1999 W/m²
Temperature value: -100°C to +100°C
Voltage level: 0 to 600VDC
Current level: 0 to 8.3A (per channel)
Voltage and power temperature coefficients: -1.99%/°C to +1.99%/°C

Overview of the Basic Operation Modes
Detailed instructions for operating the TerraSAS simulator are given in the manual (TerraSAS Software Installation and User Manual Programmable Power Solutions). As an overview, key characteristics of the system enable the simulator to:

- Import photovoltaic curves created with third party applications
- Easily create photovoltaic curves from manufacturer supplied data
- Import irradiance / temperature profiles created in Microsoft Excel, third party applications or using real-time data acquisition from actual solar panels

- Organize any number of curves and profiles into graphic, filmstrip like pools for intuitive, easy access
- Create any number of solar array configurations, organized into a graphic, filmstrip like pool.
- Intuitive drag-and-drop interface to easily assign curves and profiles to individual array elements, to support accurate modeling of array shadowing patterns
- Static and dynamic simulation preview of each configured array
- Comprehensive remote interface based on the SCPI Language
- Fully configurable real time trigger, measurement and data logging features
- Full hardware monitoring and fault reporting system
- Real time control of TerraSAS digital photovoltaic simulator systems (up to 100 channels)
- Real time control of standalone, desktop TerraSAS digital photovoltaic simulator units

The Figure 68 below shows the System control tab from the main screen.

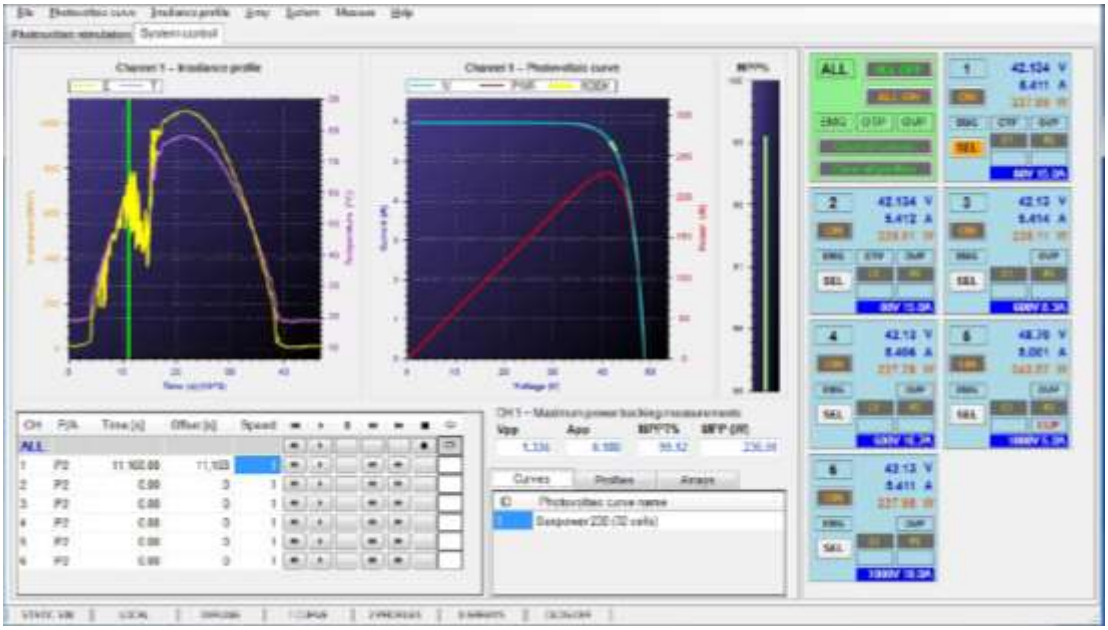


Figure 68: System control tab

Executing a static simulation

Load or create one or more curves as described in section "TerraSAS main menu items description". Curves in the pool also become listed in the System control tab:

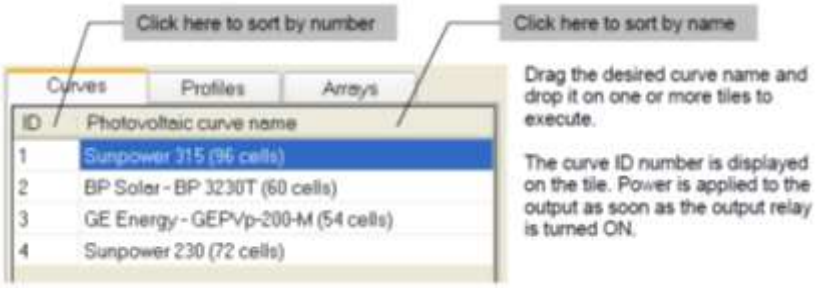


Figure 69:: Example of different PV curves loading

If a curve was already assigned to a channel, the new curve replaces it. Select the tile to display the additional data:

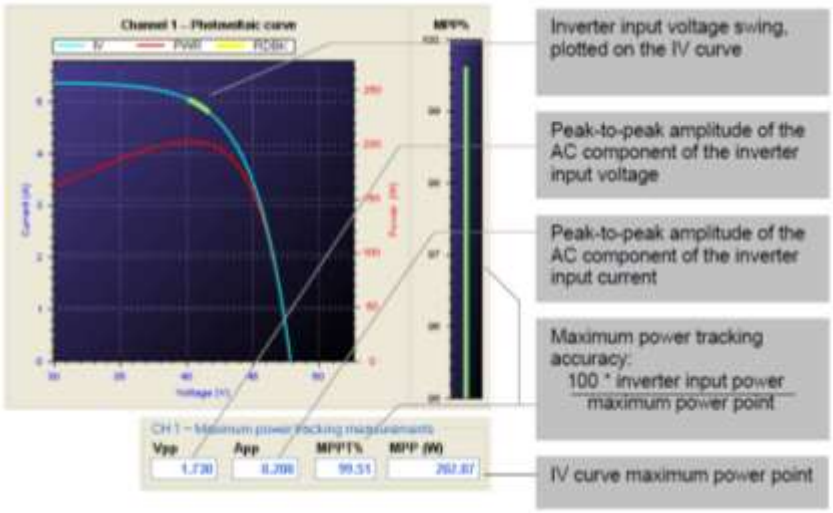


Figure 70: : After PV curves is loaded the I-V curve is shown

Executing a dynamic simulation

Load or create one or more curves and load one or more profiles as described in section "TerraSAS main menu items description". Curves in the pool also become listed in the System control tab:

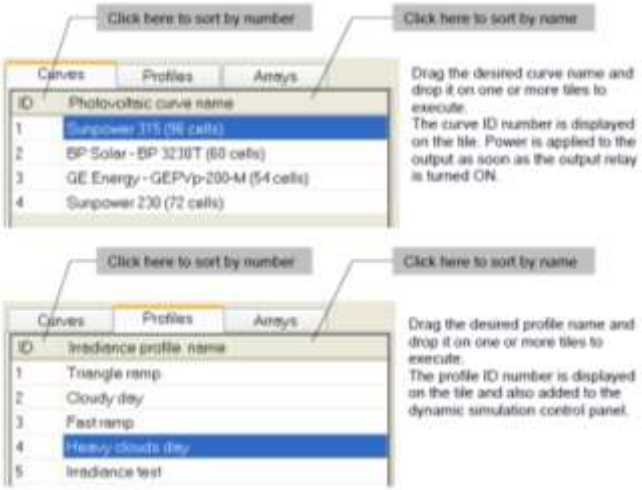


Figure 71: Example of different PV curves and irradiance profile loading

The dynamic control panel allows the complete control of the simulation:

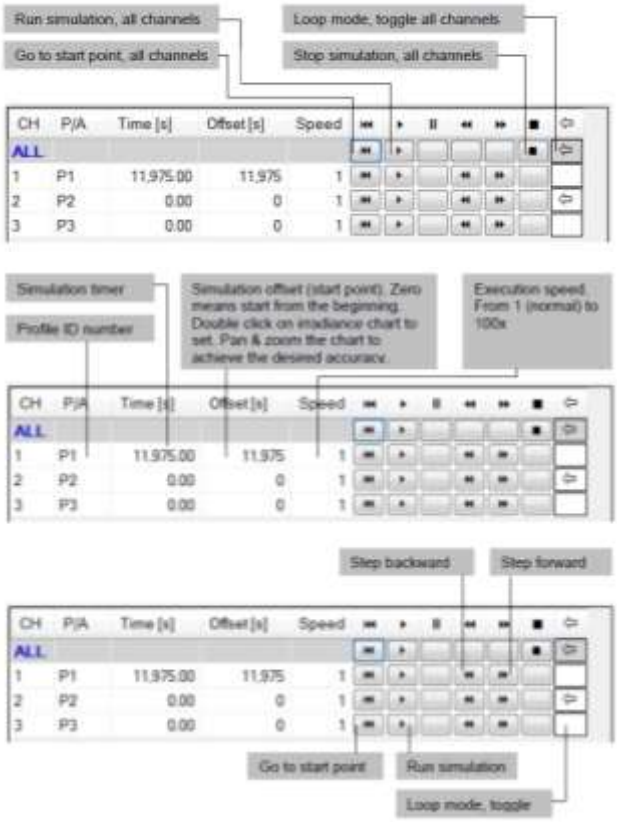


Figure 72:The dynamic control panel

When a simulation is running, the channel becomes highlighted in green:

Figure 73: The dynamic control panel when running

When a simulation is running, it can only be paused or stopped. No other parameter can be changed. Loop mode can be toggled while running.

When the simulation reaches the end on a particular channel it stops, unless loop mode is active. During a dynamic simulation, real time profile and curve data are displayed for the selected channel:

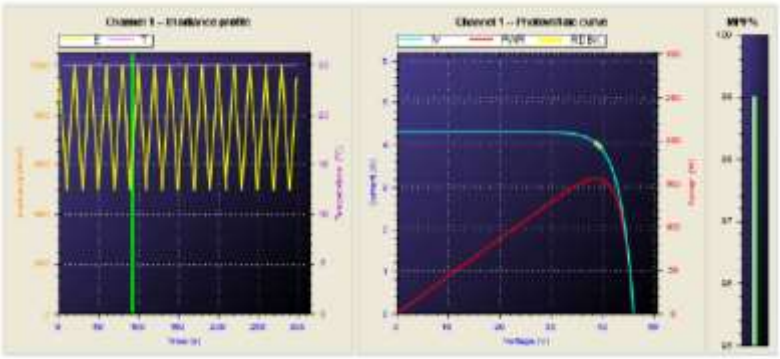


Figure 74: Real time profile and curve data are displayed for the selected channel

The following features are disabled when one or more channels are executing a dynamic simulation:

- Loading, creating and removing curves
- Loading and removing profiles
- Adding and removing arrays
- Changing curve and profile assignments on any channel running a simulation
- Manually setting irradiance and temperature on any channel running a simulation
- Manually setting irradiance and temperature on tile ALL when one or more channels are running a simulation
- Updating the system configuration table (the table can be displayed but the START button is unavailable)
- Changing channels grouping configuration

3.2.3.2 Grid emulator setup

In order to test the micro-inverter performance a set of grid DOE (design of experiments) tests to check the capability of the micro-inverter to sustain operation under different kinds of grid events are required. The grid events of interest are small signal disturbance (Test 1), large signal disturbance (Test 2), fault ride through (Test 3) and harmonic distortion (Test 4).

Error! Reference source not found.75 shows the one-line diagram of a typical distribution grid. The 20 MVA substation connects the 69 KV transmission line and the 12.47 kV distribution line. The load tap changer and the capacitor banks in the substation regulate the voltage within +/- 10% over the length of the feeder. A three phase feeder supplies different kinds of custom loads from the substation. A residential community is served by the individual single phase lateral circuits from a three phase primary feeder. A 50 KVA transformer is used to step down the voltage to 240 V for a single household.

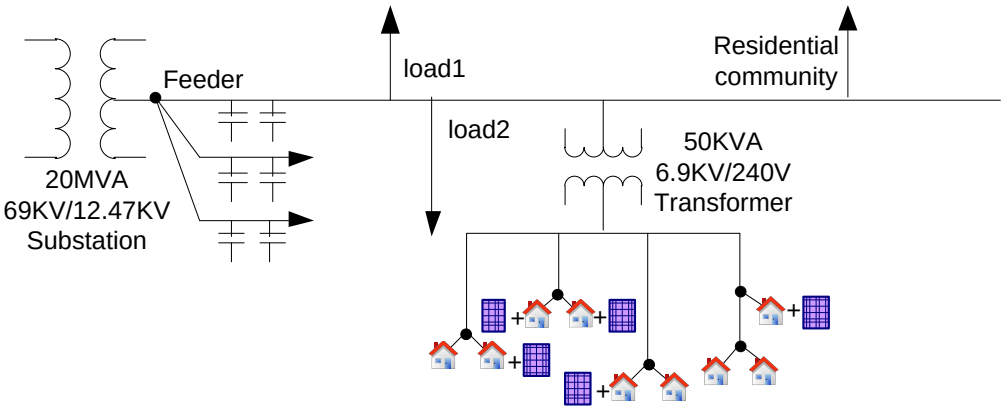


Figure 75: Typical distribution network for residential community

Since there are different kinds of loads and many possible grid configurations on the feeder, it is cumbersome to analyze the grid on a case by case basis. Usually the equivalent grid impedance is used to represent the different grid conditions, i.e. strong, medium and weak grid. The system short circuit ratio (SCR) and X over R ratio (XOR) are used to define the grid impedance value.
The grid impedance seen from the micro-inverter is a function of the local grid impedance and the impedance of the transformer leakage inductance, which can be approximated as the 5% of the transformer base impedance. The severity, location and type of faults can be simulated by varying the magnitude of the voltage drop seen by the micro-inverter. These parameters can be controlled by deploying programmable power supplies, variable inductors and programmable loads in the grid model. Therefore, the final experiment setup to test the grid behavior of the micro-inverter is shown in **Error! R eference source not found.**.

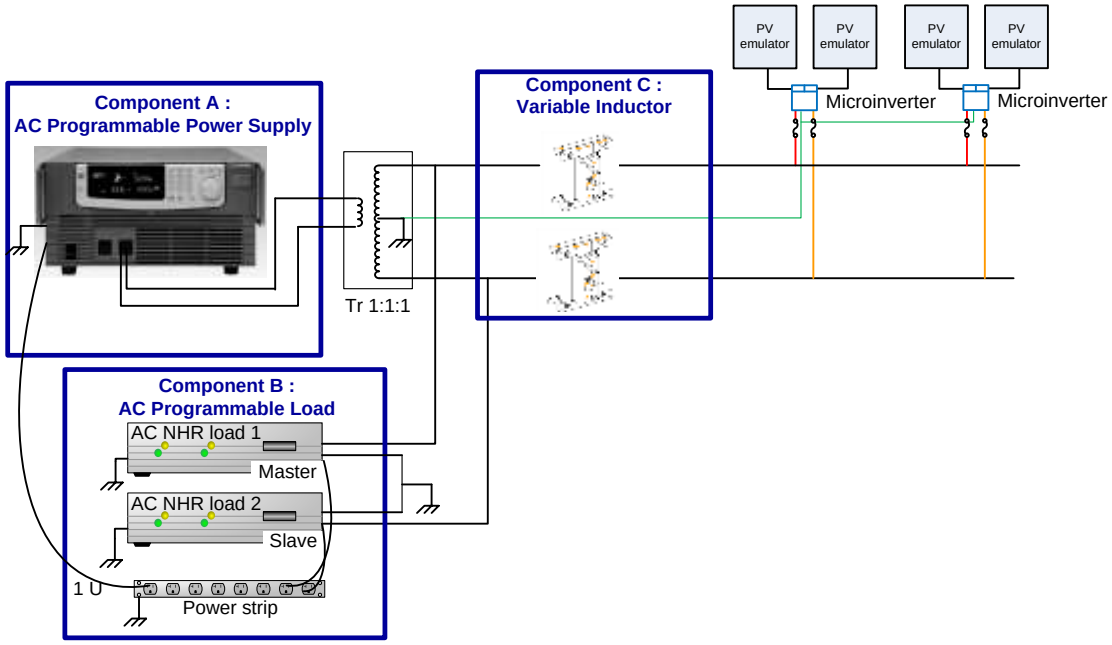


Figure 76: Diagram for lab demo setup to test the grid feature

Test Setup Description:

In the diagram in Figure 76, Component A is the AC programmable power supply (KIKUSUI Electronics Corp, PCR2000L). It has the maximum output voltage of 150 V and a transformer is needed to simulate the single phase center tap 240 V grid voltage. This programmable power supply is able to dynamically adjust the voltage magnitude, frequency and phase angle. Hence, it can simulate the different complex voltage and frequency events including the transient fault and grid harmonics distortion. Component B represents the local load and the grid loads if necessary. This AC programmable load (NHR, 4600AC) is capable of absorbing the variable 3 KW active or reactive power. Two units will be connected from each line to neutral and work in a master-slave configuration to share the power consumption. The variable grid impedance can be realized by using Component C. Two similar inductances are used to balance the system. The variable inductors have several taps whose values are designed according to different grid conditions.

Programmable Power Supply

The programmable power supply PCR2000L is able to perform various types of power supply environment tests, including the simulation of power failures and sudden voltage drops. This power supply also allows the measurement and analysis of harmonics current to be performed easily. In addition, it also can realize a high level of system compatibility and remote control through the available GPIB and RS-232C interfaces. **Error! Reference source not found.** provides the detailed specifications for this p rogrammable power supply. In our setup this power supply will be used to simulate the utility power under the different load/generation conditions.

Table 21: Specification of PCR2000L programmable power supply

Items	Specifications
Output modes	AC / DC mode
Voltage range	AC: 1-150 V/2-300 V DC: 1.4-212 V/2.8-424 V
Frequency range	1 - 999.9 Hz
Output voltage regulation	within ±0.1 / ±0.2 V
Output frequency regulation	within ±0.3%
Ambient temperature regulation	100 ppm/˚C
Output voltage response speed	30 us
Maximum RMS current	20 A/10 A (100 V/200 V)
Maximum output peak current	Maximum RMS current x 4
Power capability	2 kVA
Apparent electrical power	~4 kVA
Power line irregularity simulation function	Yes
Special waveform Output	Yes
User Defined waveform output	Yes
Output impedance range	0-1.0 Ω (100 V), 0-4.0 Ω (200 V)

Figure 77: Front control panel for PCR2000L programmable power supply

Error! Reference source not found.77 shows the front control panel of the power s upply. The basic functions such as changing voltage and frequency can be realized from here. However, some advance functions are required to have the use of an optional remote controller or interface boards with the computer. In our experiments, different fault conditions and the frequency ramp events will be programmed in Visual Basic or Labview and the power supply will be remotely set to execute the specific scenario.

Programmable AC load

The programmable AC load is intended for applications that require the entire range of non-linear loading to comprehensively test the AC output of the power conversion products such as the uninterruptible power supplies (UPS) and inverters. The benefit of such a wide range of load control is to assure product performance under every possible “real world” operating condition. **Error! Reference source not found.** shows t he detailed specifications for the 4600-3 AC loads. This equipment will be used to simulate the grid load.

Table 22: Specification of 4600-3 programmable AC load

Items	Specification
Output modes	Constant current / voltage / resistance / power mode
RMS current range	0-30 A
Voltage range	50 V-350 V
Frequency range	45-440 Hz
Resistance range	2.5-100 Ω / 100-1000 Ω
Power factor range	0-1 lead/lag
Voltage regulation	within ±0.1%
Frequency regulation	within ±0.1%
Resistance regulation	within ±0.1%
Maximum real power	3000 W
Maximum apparent power	10.5 KVA
Operating temperature	0-50˚C

Also, this load has its own graphic user interface as shown in **Error! Reference source n ot found.**. By using this interface, the load type can be set to different modes (constant voltage, constant current, constant power and constant resistance mode). The exact load impedance can be tuned through this interface as well, which simplifies the control of the load.

Figure 78: Graphic user interface for NHR 4600-3 AC load

In addition to the manual setup, this AC load also allows the remote control. It provides a hardware interface to the external computer and comes with the full Labview library. Since the load control should be synchronized with the AC power supply for the grid fault simulations, the control blocks of the AC power supply and AC load are needed to be built in Labview together.

Variable Inductor

For the purpose of the simulations described in this document, we considered three examples to represent the different grid conditions, i.e. SCR = 100 and XOR = 10

(strong grid), SCR = 6 and XOR = 5 (medium grid), SCR = 2.5 and XOR = 1 (weak grid). **Error! Reference source not found.** gives the values of equivalent grid i mpedances (X and R) which represent the impedance from the substation to the local transformer. Assuming the 50 KVA transformer leakage inductance is 5%, the total equivalent inductance value can be calculated as show in **Error! Reference source not f ound.**.

Table 23: Equivalent grid impedance for different grid conditions

Operating condition	SCR	XOR	X [mΩ]	R [mΩ]	Total L [μH]
Strong Grid (S)	100	10	14.33	7.19	190.8
Middle Grid (M)	6	5	235.34	58.59	777.05
Weak Grid (W)	2.5	1	407.29	464.89	1233.17

Test Cases

Error! Reference source not found. shows the overview of the small signal d isturbance test. **Error! Reference source not found.** provides the breakdown list of test cases. First, we will define the grid condition and operation points. Three different voltage and frequency combinations will be tested:

1. The rated voltage and frequency – under this condition, the required power factor is unity.
2. 1.1 pu voltage and 0.95 pu frequency – power factor requirement is -0.9.
3. 0.9 pu voltage and 1.05 pu frequency - power factor output is required to be 0.9.

For all these conditions, the tests should be performed on the operation point for full power and half power output under strong, medium and weak grid conditions. For each operating point, ±5% active power, ±5% reactive power, ±0.5% frequency step and ±5˚ phase angle difference will be added into the system as a disturbance.

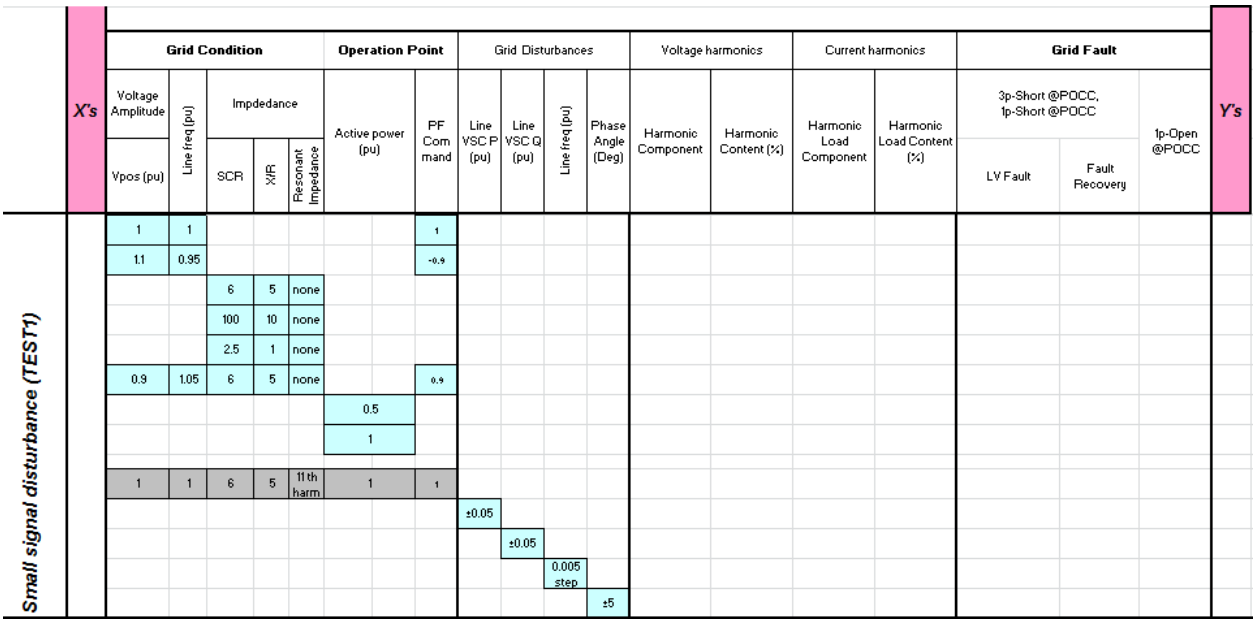


Figure 79: Overview of small signal disturbance test (TEST 1)

The different test cases can be explained more clearly in **Error! Reference source not found.**. **Error! Reference source not found.** only shows the medium grid conditions. The strong grid and weak grid can be found in the spreadsheet. The grid condition will be set by the tap change on the variable inductor (Component C).
Referring to the spreadsheet cells, Case A1-A24 is when the half output power is required. Case A25-A48 is for the rated power. The output power will be set through programmable load (Component B) as an operating point. At that time, programmable load is selected in a constant power mode and power factor can be set accordingly.
In Case A1-A24, three grid conditions are listed for:

1. line voltage at 0.9 pu, frequency at 1.05 pu and power factor requirement at 0.9 (Case A1-A8);
2. line voltage at 1 pu, frequency at 1 pu and power factor requirement at 1 (Case A9-A16)
3. line voltage at 1.1 pu, frequency at 0.95 pu and power factor requirement at -0.9 (Case A17-A24).

Line voltage and frequency will be set by the programmable power supply (Component A) and the power factor will be adjusted through the programmable load (Component B).
Once the system gets to the steady state for the given settings, then we can add the disturbances through the programmable power supply or load. In Case A1-A8, the disturbances will be introduced to active power, reactive power, line frequency and phase angle, respectively. The disturbances of the active power and reactive power will be controlled through the programmable load (Component B). Then the frequency and phase angle disturbances will be introduced through the programmable power supply (Component A). The system response to the disturbance will be recorded and evaluated for each case.

Rev	Case Index	X's	Xs																Grid Fault	Y's
			Configuration		Grid Condition							Operating Point				Grid Disturbance				
			Firmware version		Voltage Amplitude			Impedance				Irradiance (w/m^2)	Temperture (Degree)	Active Power (pu)	PF Command	Active Power Disturbance (pu)	Reactive Power Disturbance (pu)	Line Frequency Disturbance (pu)	Phase Angle Disturbance (Deg)	
					Vpos (%)	Vn/Vp (%)	Line freq (%)	SCR	X/R	Resonant Impedance										
20120719	A1				90	0	105	M		0		STC		0.5	0.9	0.05	0	0	0	
20120719	A2				90	0	105	M		0		STC		0.5	0.9	-0.05	0	0	0	
20120719	A3				90	0	105	M		0		STC		0.5	0.9	0	0.05	0	0	
20120719	A4				90	0	105	M		0		STC		0.5	0.9	0	-0.05	0	0	
20120719	A5				90	0	105	M		0		STC		0.5	0.9	0	0	0.005	0	
20120719	A6				90	0	105	M		0		STC		0.5	0.9	0	0	-0.005	0	
20120719	A7				90	0	105	M		0		STC		0.5	0.9	0	0	0	5	
20120719	A8				90	0	105	M		0		STC		0.5	0.9	0	0	0	-5	
20120719	A9				100	0	100	M		0		STC		0.5	1	0.05	0	0	0	
20120719	A10				100	0	100	M		0		STC		0.5	1	-0.05	0	0	0	
20120719	A11				100	0	100	M		0		STC		0.5	1	0	0.05	0	0	
20120719	A12				100	0	100	M		0		STC		0.5	1	0	-0.05	0	0	
20120719	A13				100	0	100	M		0		STC		0.5	1	0	0	0.005	0	
20120719	A14				100	0	100	M		0		STC		0.5	1	0	0	-0.005	0	
20120719	A15				100	0	100	M		0		STC		0.5	1	0	0	0	5	
20120719	A16				100	0	100	M		0		STC		0.5	1	0	0	0	-5	
20120719	A17				110	0	95	M		0		STC		0.5	-0.9	0.05	0	0	0	
20120719	A18				110	0	95	M		0		STC		0.5	-0.9	-0.05	0	0	0	
20120719	A19				110	0	95	M		0		STC		0.5	-0.9	0	0.05	0	0	
20120719	A20				110	0	95	M		0		STC		0.5	-0.9	0	-0.05	0	0	
20120719	A21				110	0	95	M		0		STC		0.5	-0.9	0	0	0.005	0	
20120719	A22				110	0	95	M		0		STC		0.5	-0.9	0	0	-0.005	0	
20120719	A23				110	0	95	M		0		STC		0.5	-0.9	0	0	0	5	
20120719	A24				110	0	95	M		0		STC		0.5	-0.9	0	0	0	-5	
20120719	A25				90	0	105	M		0		STC		1	0.9	0.05	0	0	0	
20120719	A26				90	0	105	M		0		STC		1	0.9	-0.05	0	0	0	
20120719	A27				90	0	105	M		0		STC		1	0.9	0	0.05	0	0	
20120719	A28				90	0	105	M		0		STC		1	0.9	0	-0.05	0	0	
20120719	A29				90	0	105	M		0		STC		1	0.9	0	0	0.005	0	
20120719	A30				90	0	105	M		0		STC		1	0.9	0	0	-0.005	0	
20120719	A31				90	0	105	M		0		STC		1	0.9	0	0	0	5	
20120719	A32				90	0	105	M		0		STC		1	0.9	0	0	0	-5	
20120719	A33				100	0	100	M		0		STC		1	1	0.05	0	0	0	
20120719	A34				100	0	100	M		0		STC		1	1	-0.05	0	0	0	
20120719	A35				100	0	100	M		0		STC		1	1	0	0.05	0	0	
20120719	A36				100	0	100	M		0		STC		1	1	0	-0.05	0	0	
20120719	A37				100	0	100	M		0		STC		1	1	0	0	0.005	0	
20120719	A38				100	0	100	M		0		STC		1	1	0	0	-0.005	0	
20120719	A39				100	0	100	M		0		STC		1	1	0	0	0	5	
20120719	A40				100	0	100	M		0		STC		1	1	0	0	0	-5	
20120719	A41				110	0	95	M		0		STC		1	-0.9	0.05	0	0	0	
20120719	A42				110	0	95	M		0		STC		1	-0.9	-0.05	0	0	0	
20120719	A43				110	0	95	M		0		STC		1	-0.9	0	0.05	0	0	
20120719	A44				110	0	95	M		0		STC		1	-0.9	0	-0.05	0	0	
20120719	A45				110	0	95	M		0		STC		1	-0.9	0	0	0.005	0	
20120719	A46				110	0	95	M		0		STC		1	-0.9	0	0	-0.005	0	
20120719	A47				110	0	95	M		0		STC		1	-0.9	0	0	0	5	
20120719	A48				110	0	95	M		0		STC		1	-0.9	0	0	0	-5	

Figure 80Part of detailed test conditions for small signal disturbance (TEST 1)

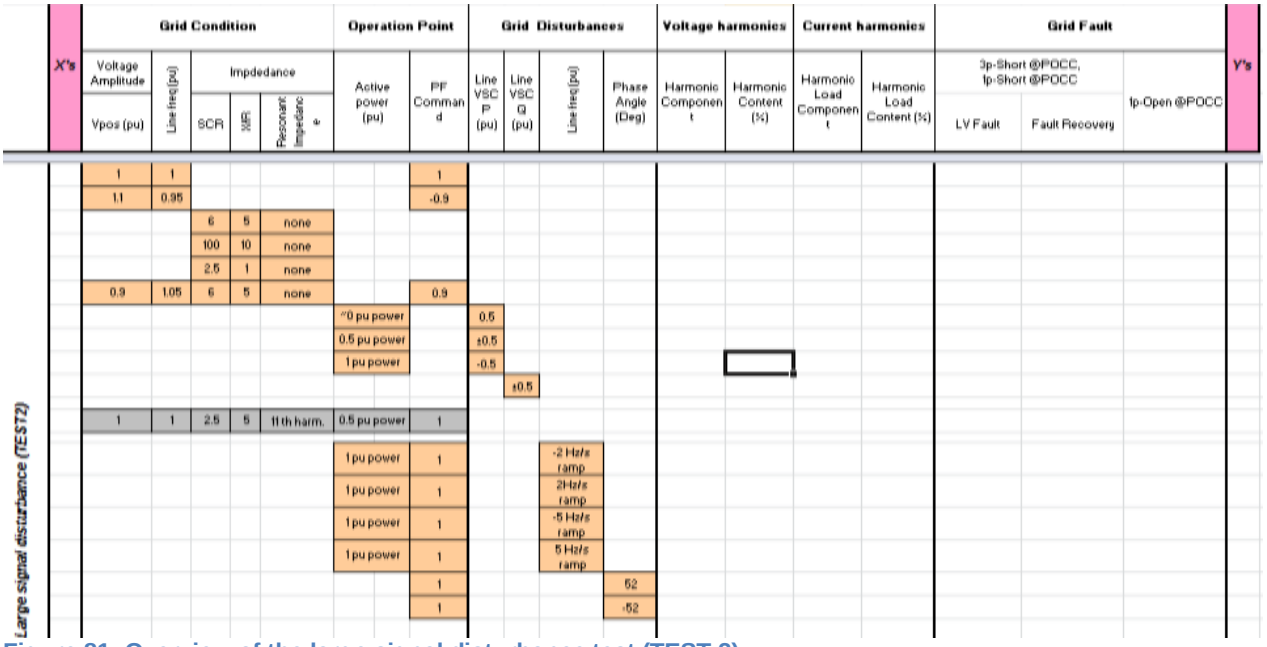


Figure 81: Overview of the large signal disturbance test (TEST 2)

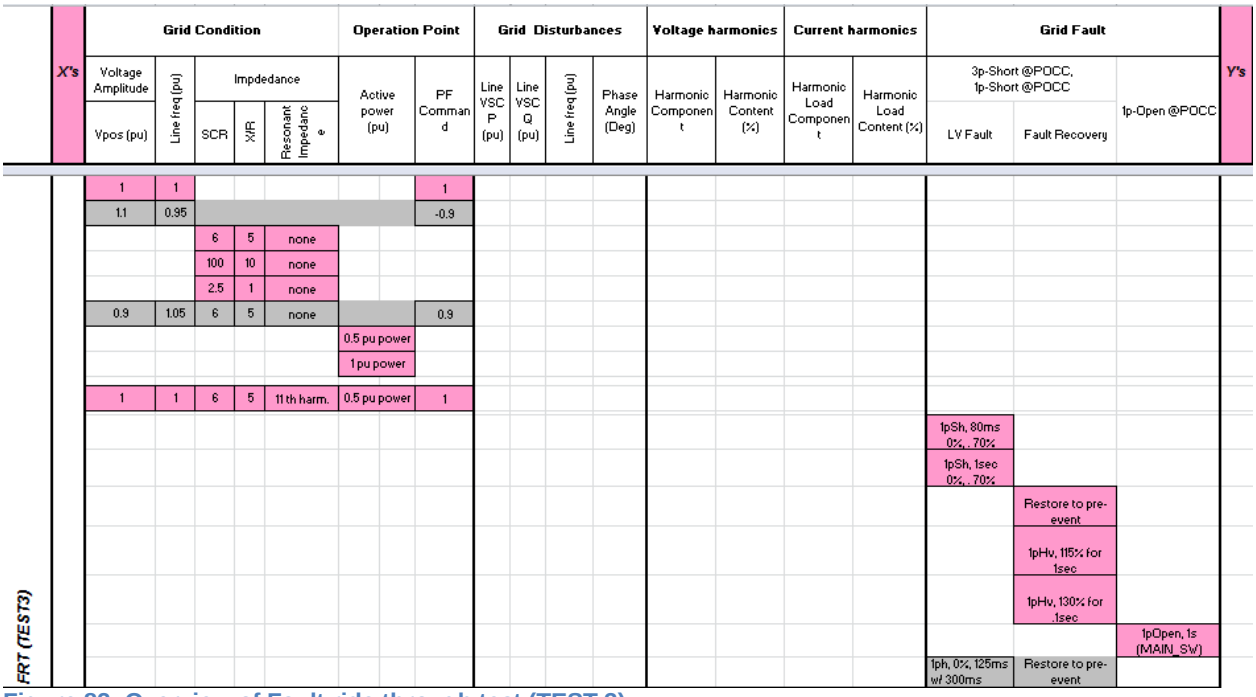


Figure 82: Overview of Fault ride through test (TEST 3)

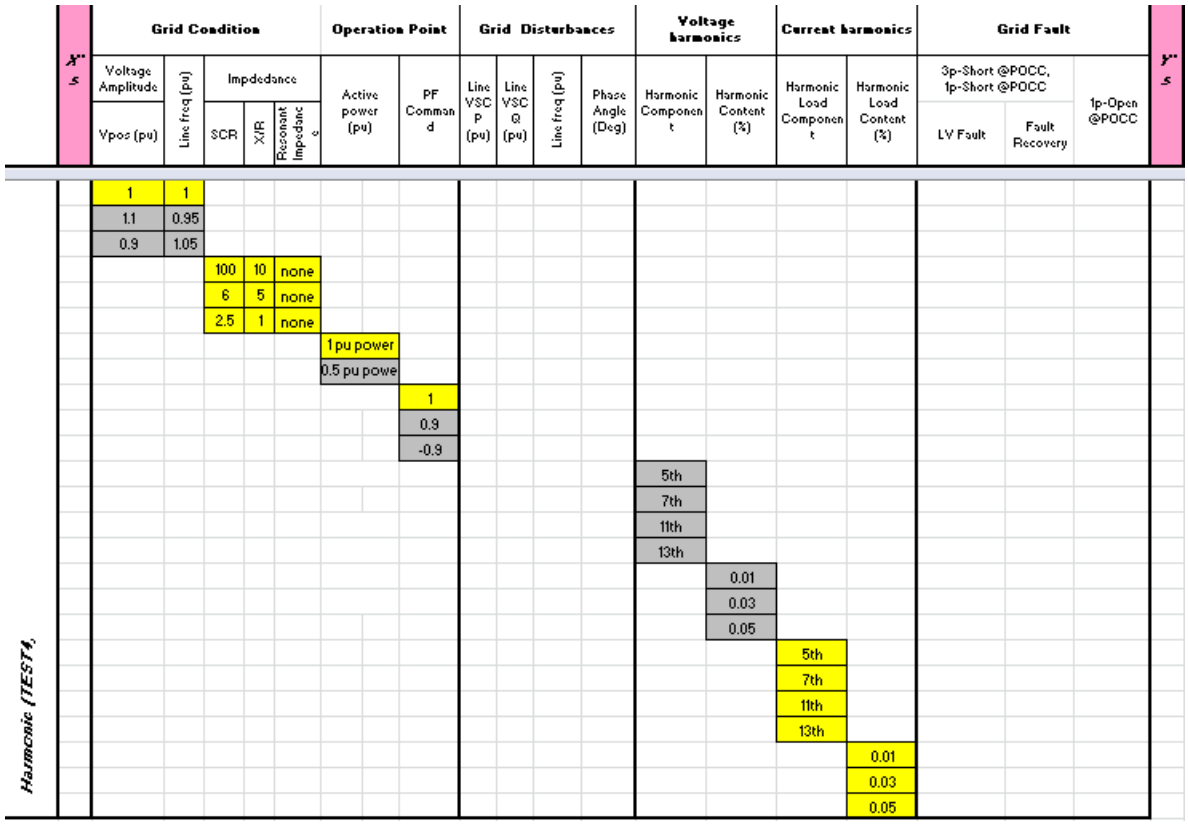


Figure 83: Overview of Harmonics test (TEST 4)

The same method applies to the large signal disturbance test (TEST 2) Figure 81, Fault ride through test (TEST 3) Figure 82 and Harmonics test (TEST 4) Figure 83.

The variable inductor (Component C) will be set first according to the different grid conditions (M, S, W). Then, programmable power supply (Component A) will set the voltage magnitude and frequency for the test grid condition. Programmable load (Component B) will tune the output active power and power factor for a certain operating condition. Once it goes to the steady state operation, programmable power supply (Component A) will introduce the line voltage and frequency disturbances. Programmable load (Component B) will provide active and reactive power disturbances instantaneously. For the fault test, programmable power supply (Component A) will be used to generate the transient fault and in the same time, programmable load (Component B) needs to switch the mode to constant resistive load mode.

3.2.4 Task 4: Evaluate and design the functional circuit including ACPV with safety, control and grid support functions

Task 4 entailed the integration of the breadboard micro-inverter with the programmable circuit breaker in order to form a functional circuit for the residential solar system. The implementation has incorporated the safety (i.e., anti-islanding), control (i.e., quiescent power control), and grid support functions (Volt/VAR) support) using the breadboard micro-inverter and the programmable circuit breaker. This report captures the benchmark testing of safety, control and grid support functions using the functional circuit with the smart grid emulator.

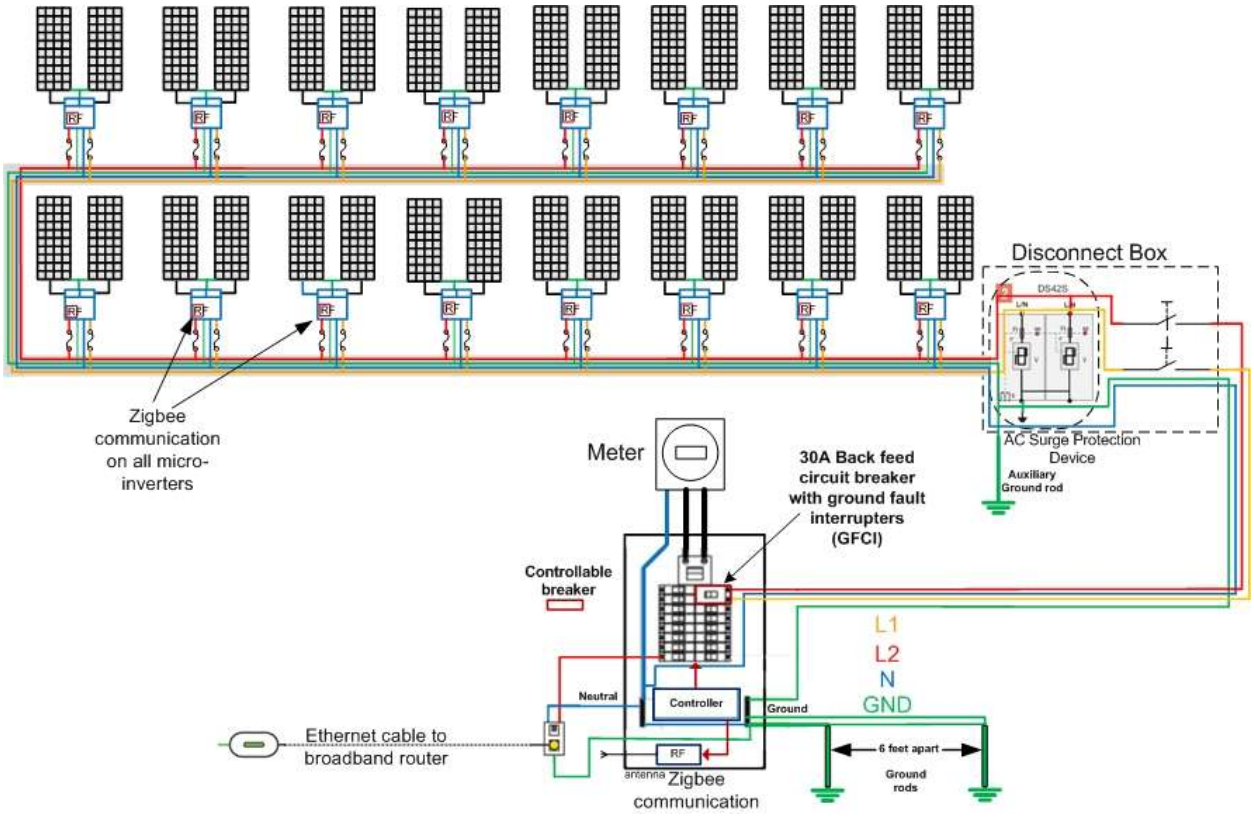


Figure 84: PV System Schematic

As shown in Figure 84, intelligently distributing the safety, control, and grid support functions between micro-inverters and the centralized programmable circuit breaker improves the system performance and reduces the micro-inverter cost. For instance, monitoring quiescent power in the circuit breaker can reduce the night power consumption from ~50mW per micro-inverter to nearly zero.

3.2.4.1 Smart Breaker Box Functionality

The functions identified in the third column of Table 24 were implemented through a Smart Breaker Box, intelligent distribution panel, shown in Figure 85. The system shown in Figure 1 includes a TEYRC230 (30A, 2 pole Remote operated circuit breaker (ROCB)) which is an electromagnetic relay device with a controller circuit that can be remotely operated to connect/disconnect the PV system to the grid.

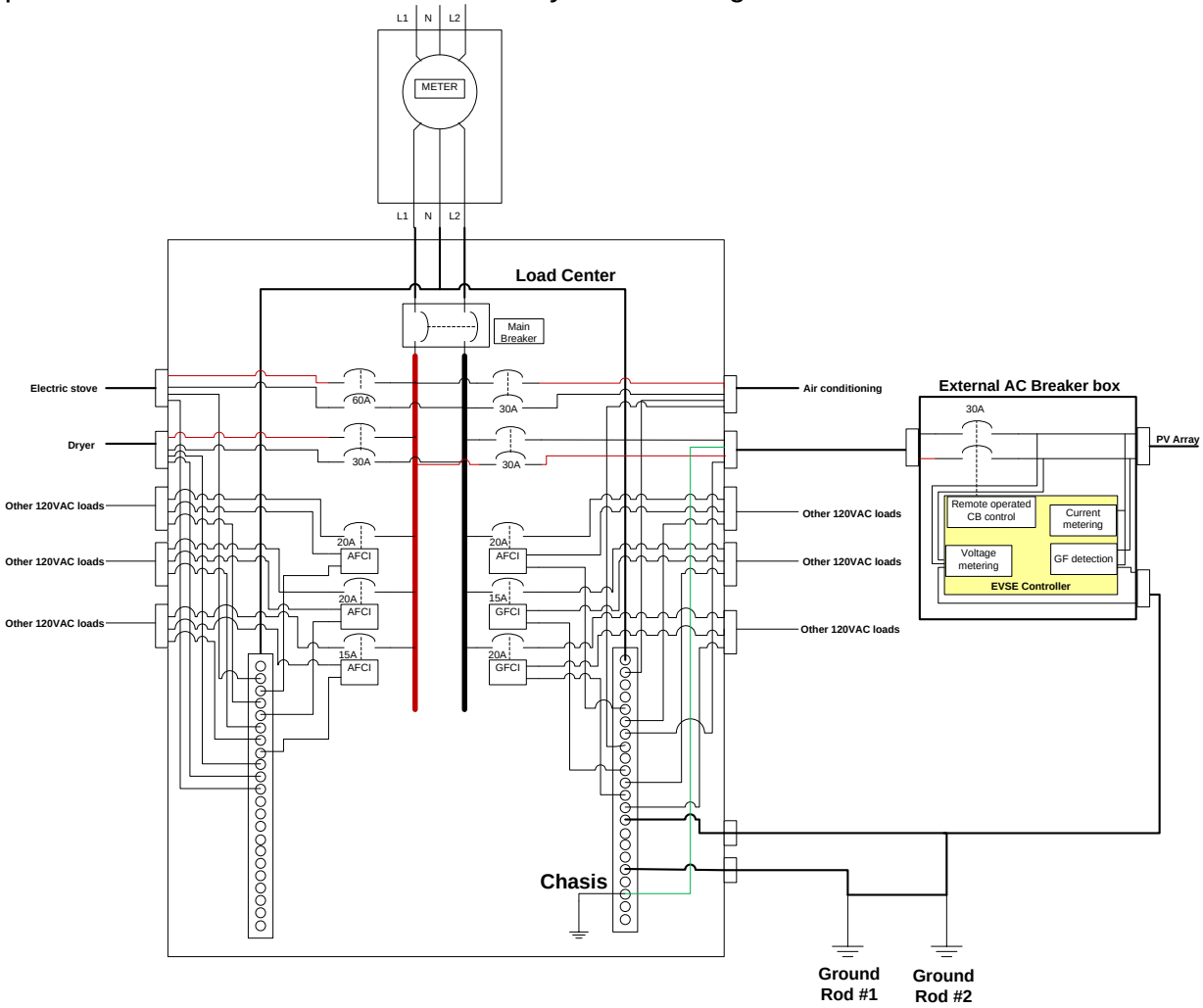


Figure 85: Smart Breaker Box

The ROCB conducts current under normal operating conditions via low resistance mechanical contacts. This back feed switch is capable of connecting/disconnecting remotely or manually, with current overload or short current surge. The controller, within

the Smart Breaker Box system, contains sophisticated algorithms used for real-time monitoring and control of this ROCB, which is connected to the electricity grid. The parameters that can be monitored and used for control include line frequency, voltage, and current. The micro-inverters will be connected into the grid through a Smart Breaker Box defining a dedicated branch circuit. In order to lower the cost of the system, the ROCB is housed in a separate External AC Breaker box, so there is no need for redesigning and changing the existing residential load center.

Table 24: Function Distribution

	Micro-inverter	Smart Breaker Box
Safety		GFCI
		AFCI
		Reverse power flow command
		Over current (> 1.1x rated)
		Over voltage
		Frequency
		Passive Anti-islanding
	Anti-islanding coordination	
Grid Monitoring		Voltage
		Current
		Frequency
Communication/Control		TCP/IP interface
	Day/night modeling	
	Volt/VAr support	
	LVRT	

3.2.4.2 SAFETY

Ground fault protection & Arc fault protection

The main objective of this function is compliance with UL1741 and IEEE1547 codes. System design assures the detection of ground faults, indication that the fault has occurred, and interruption of the current flow, as well as communication to the micro-inverters to stop producing power. In the event of the ground fault, the micro-inverter will locally annunciate the error and communicate its status to the other micro-inverters and to the central controller at the load center; at the same time it will also display the fault via front panel LED at the Smart Breaker Box. All micro-inverters will go in a stand-by mode until the ground fault is cleared. The only way to reset the fault is by de-energizing the chain of micro-inverters, clearing the ground fault, and then reenergizing the chain of micro-inverters.

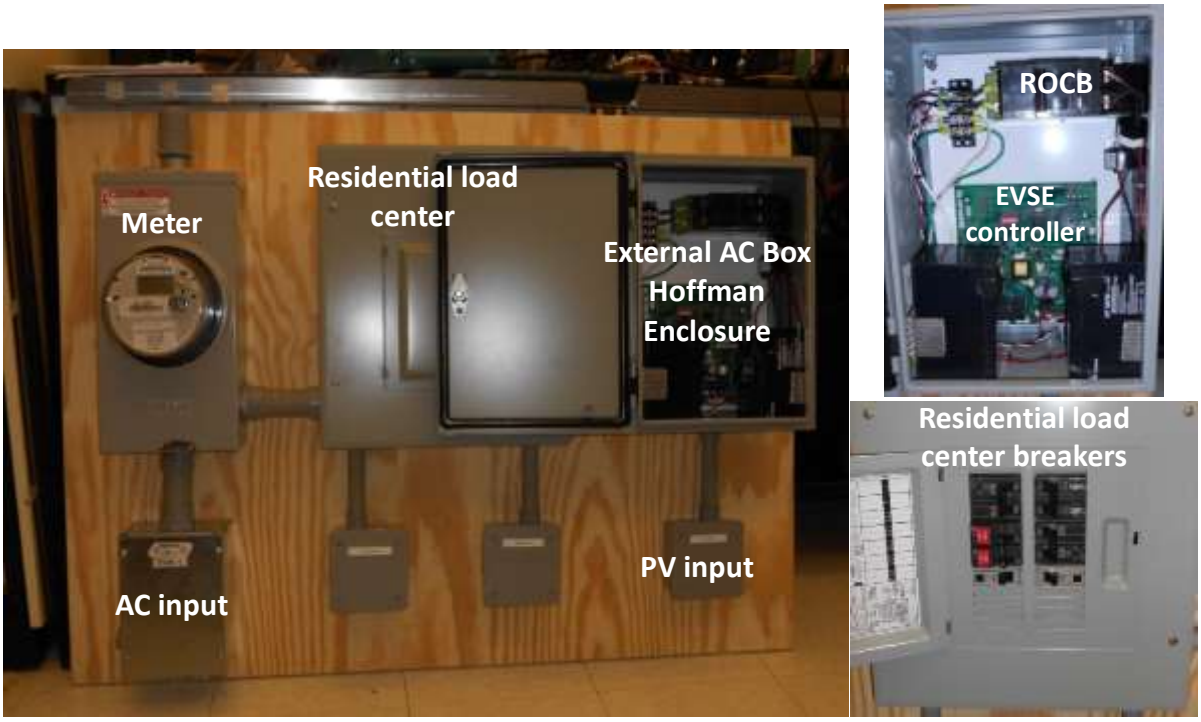


Figure 86: Smart Breaker Box Testing Prototype

To comply with codes and standards each live active line from each of the micro-inverters is to be fused at each of the micro-inverter outputs. In the present prototype disconnect is designed to brake the connection between the micro-inverter chain and the grid (two pole breaker at the load center is not an Arc flash type). At the residential load center a two pole 30A breaker protects the micro-inverter branch from over current.

In order to simulate the real residential home load center we have installed several circuit breakers in the residential load center, shown in Figure 86 (Main breaker 100A, 240V, 2 pole; 30A, 120V, 2 pole; two 30A, 120V, 1 pole; two 120V, 20A GFI and two 120V, 20A AFCI). Figure 2 shows the detailed schematic and placement of these breakers.

Within the Smart Breaker Box, a General Electric Industrial Systems (GEIS) Durastation electric vehicle supply equipment (EVSE) control board, shown in Figure 86 (upper right), is used for real-time monitoring and control of this ROCB. This EVSE controller board is used in the GE vehicle charging stations. Its original intended use is to control the AC power supplied to the electric vehicle plug-in and to monitor the power consumption, provide overload prevention and protection features, as well as the local user interface and networking options. Since the system is already implementing a ground fault protection (GFI), both at the smart breaker box and at each of the micro-inverters, the branch circuit breaker did not include the arc-flash function. The safety requirements, as we interpret the documentation, are such that if there is a GFI on the branch circuit the arc-flash function therefore is not required.

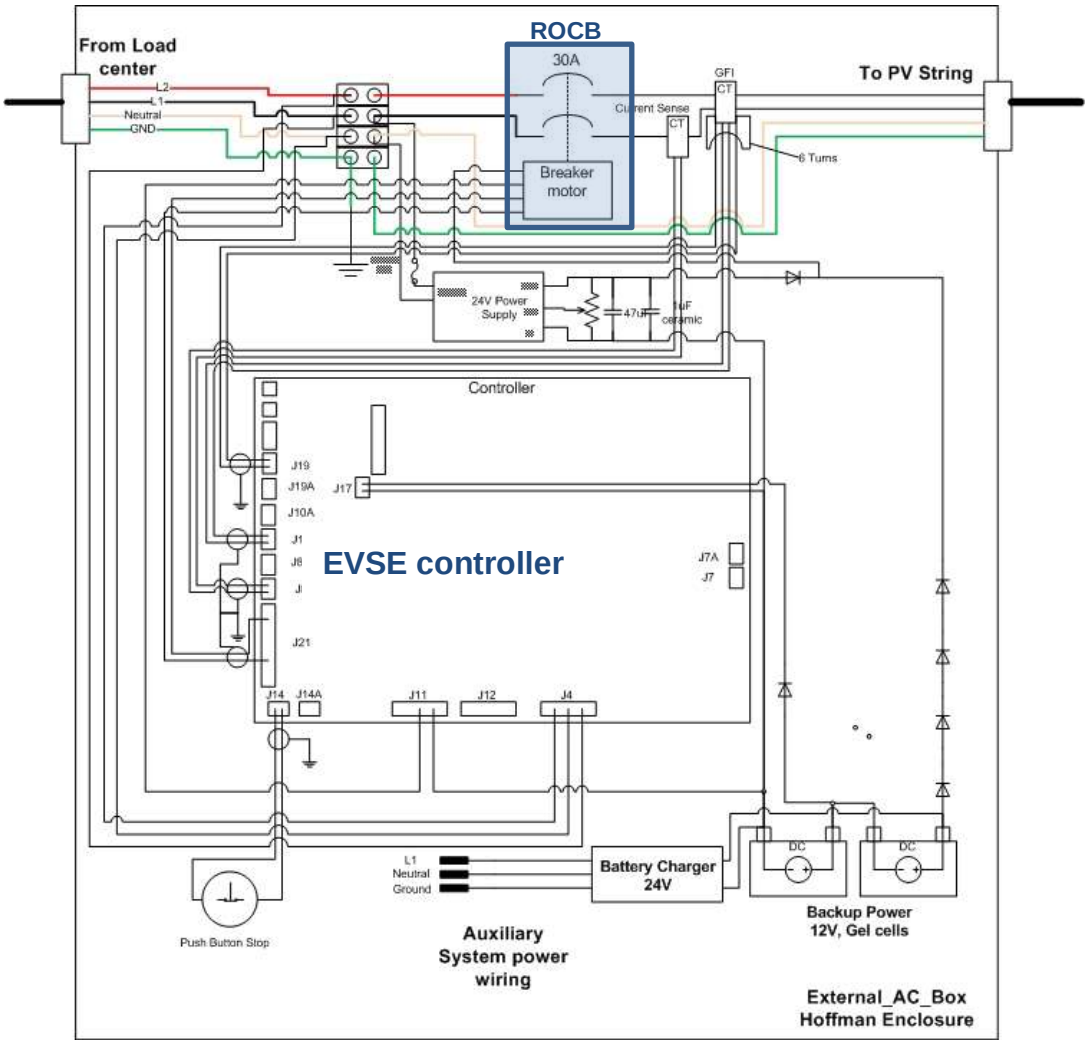


Figure 87: External AC Box Detailed Schematic

Figure 87 shows the detailed schematic of the EVSE board connections inside the External AC box with the auxiliary power (batteries) to the ROCB motor (in the case when the grid connection is lost), power supply powered from the grid during the normal grid operation to the ROCB motor, and monitoring devices.

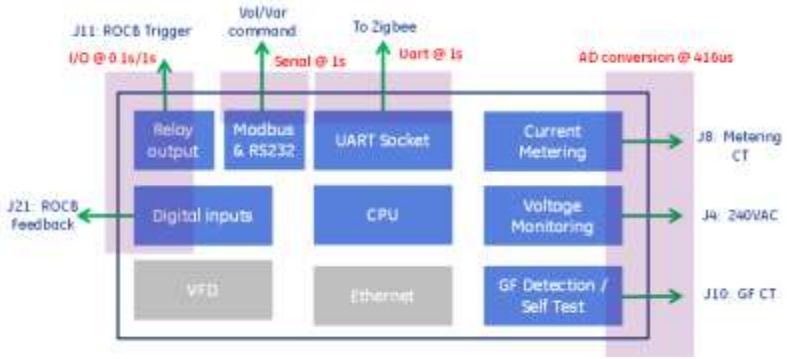


Figure 88: EVSE Controller Board Functions

Figure 88 highlights the functions that were used from the EVSE controller. We need one digital I/O (Figure 87) to read the breaker status and provide the breaker command through relay output. A serial port is setup to get Vol/VAr command by communicating with the operator through a computer or a server. Zigbee is using one UART serial port to communicate the command from/to the microinverter. Also, current and voltage meters are used to monitor the system operation status. If current, voltage or frequency exceeds the normal operating range, the controller will trigger the ROCB breaker.

Ground Fault circuit; Self-Test circuit

Implementation of the GFI function circuit is accomplished via the EVSE micro's A/D converter. The firmware implements interrupting and reclose requirements per UL2231-2. A zero sequence CT (GFI CT), with a 2000:1 turn ratio is used to sense the fault current. The minimum fault level is 1A, with a required trip time of one second. A 20mA ground fault current, develops a secondary current on the GFI CT of 0.5mA. With a burden resistor of 40Ω, the corresponding voltage is 20mV. This sensed voltage is then fed to a non-inverting amplifier, with a gain of 5.75. Thus, for 20mA of GF current, 5.75mV is observed. Note that due to low level of sense voltage (20mV/A), and an associated gain of 5.75, MCP602, a dual OpAmp with low input offset error (+/- 0.7mV) is chosen.

The controller has circuits to inject a test signal through the zero-sequence GFI CT for the purposes of self-test. A wire loop is connected through GFI CT, such that one end of the loop is connected to the EVSE board and other end runs through the GFI CT and back to the EVSE board. The EVSE electronics drives a PWM signal to provide a test current of +/- 20mA through the loop of the GFI CT to generate a test signal.

Metering:

Phase 1 of the EVSE controller supports single phase, non-revenue grade metering for both IEC and NEMA. Non-revenue metering accuracy is claimed to be ± 2% for voltage and current, and ± 4% for power, at rated levels not including inaccuracy contributed by the CT's.

Current Sensing Circuit:

Metering CTs are connected to the EVSE board with two burden resistors. Difference amplifiers with different gains (for better resolution) are used to measure current signals. These signals are fed to the A/D channels of the EVSE micro. To obtain optimum measuring range signals are biased by $2.5V_{DC}$ to capture the signal swing in the 0-5V range of the A/D converter.

Furthermore, each of the burden resistors provides different voltage levels which allows the micro to more accurately determine high and low level currents, including overcurrent sensing.

Voltage Sensing Circuit:

A difference amplifier circuit and associated electronics are used to sense input voltage. Connections are made to the EVSE board depending whether it is NEMA or IEC specified. In turn the board then is compliant with either standard. Overall, the circuit attenuates the AC line voltage by a factor of approximately 0.160 and adds a 2.5V bias to center the AC voltage in the 0-5VDC range of the A/D.

ROCB Driver; Emergency Stop

A seven Darlington array package, with freewheeling diodes is used to drive the relays and LED display bar within the EVSE. The driver chip is powered by $13.2V_{DC}$, which allows for approximately 1.2V volt drop across the Darlington array, to provide 12V dc to

the relays and LEDs. One of three relays in the EVSE board, rated at 12A and 230VAC is used in the design to activate the ROCB.

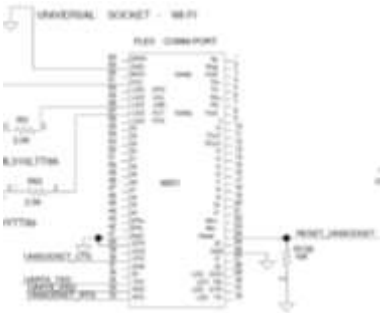
The controller has sensing inputs to connect a normally closed switch to stop or disable the system in case of an emergency. This is how an emergency stop (E-Stop) function is implemented in this design. The logic is such that when the switch is closed, the system is in normal condition, and when the switch is open the system is in the E-Stop mode (disabled).

Low Voltage I/Ps

Controller has four 13V_{DC} digital inputs, which can be used as various inputs. Currently the plan is for the inputs to be used as follows:

Input 1 -Status of the ROCB
Input 2 -Labview digital output -option for a control
Input 3 -Labview digital output -option for a control
Input 4 -Labview digital output -option for a control

a) Board



b) EVSE Connection Point

Figure 89: Additional Board for Zigbee Communication and Zero Voltage Detection

An additional board to the EVSE was been designed to allow connections of the EVSE to a Zigbee communications board. The additional board which connects to the UART socket on the EVSE board contains the Zigbee board connectivity, and a Zero cross detection circuit. This board is shown in Figure 89.

3.2.4.3 CONTROL & COMMUNICATION

Grid monitoring and configuration (fast grid voltage/frequency detection)

1. Taking suitable measurements on grid voltage and monitoring the magnitude and frequency in order to detect transient interruptions of voltage and frequency events.
2. Providing appropriate current measurements to limit the short-circuit current from the PV inverter to the grid, also prevent reverse power flow from the grid. If the reverse power flow is allowed, it also can be used to protect the inverter from over-current fed-back from the grid.

3. Be able to trip when voltage and current exceeds the certain value, i.e. voltage is within 0.8 to 1.15 rated value and current is higher than 1.1 rated value (for about 300ms according to maximum ride through time of the micro-inverter).

The wireless communication between the micro-inverter and the EVSE board is enabled using Zigbee radios (IEEE 8015.4 2006 Zigbee). The micro-inverter and EVSE board are integrated with Texas Instruments' Zigbee system-on-chip kits (TI CC2530), shown in Figure 90 which run Zigbee PRO 2006 software stack. The communication between Zigbee board and EVSE/micro-inverter board is done over the UART (serial communication protocol). The Zigbee board attached to the EVSE board acts as a network coordinator while the board(s) attached to the micro-inverter(s) acts as the end device(s). In the initial phase, the communication between the coordinator and the end device is established, where the coordinator assigns the short address to the end device, after which the bi-directional data transmission can start. The EVSE board sends control messages (breaker status) to the micro-inverter, which upon the successful reception sends the acknowledgment message back. Similarly, messages from micro-inverter received by EVSE board are immediately acknowledged by the EVSE board.

Communication gateway

Figure 90: Zigbee System-On-Chip Kits (TI CC2530)

Internal communication: implemented via the wireless bidirectional link between each micro-inverter and central controller and used to transmit control signals and measurement data.

Gateway communication: wireless Zigbee based link used to communicate aggregated monitoring data for the entire installation to enable monitoring and troubleshooting. Future capabilities may include the ability to integrate control functions over multiple installations at the local/regional level.
The system software will present current and historical system performance tendencies, and it informs the user when the PV system is not performing as expected.

On/off control

Enables user to initiates the power up and power down procedure on the PV system.

Day/night model control

Downloading Sun rise and Sun down time for the current date. Communicate in order to switch on and off the PV system.

Quiescent power monitoring

The micro-inverter will shut down during the night. A wake up signal shall be sent from the ROCB panel controller to the micro-inverter when sun rises. This can reduce the night power consumption from ~50mW per micro-inverter to nearly zero.

3.2.4.4 GRID SUPPORT FUNCTION

Volt/VAR support coordination

The team has segmented the grid support function into two blocks based on the location of the hardware/software that will carry out the functions, as shown in Figure 91. Grid support functions/algorithms of the Smart Breaker Box have been defined and include VAR support based on the power levels and anti-islanding detection. This part was fully implemented and tested. The remaining grid support functions will be carried out in the micro-inverter's controller and include low voltage ride through and VAR support based on the voltage level.

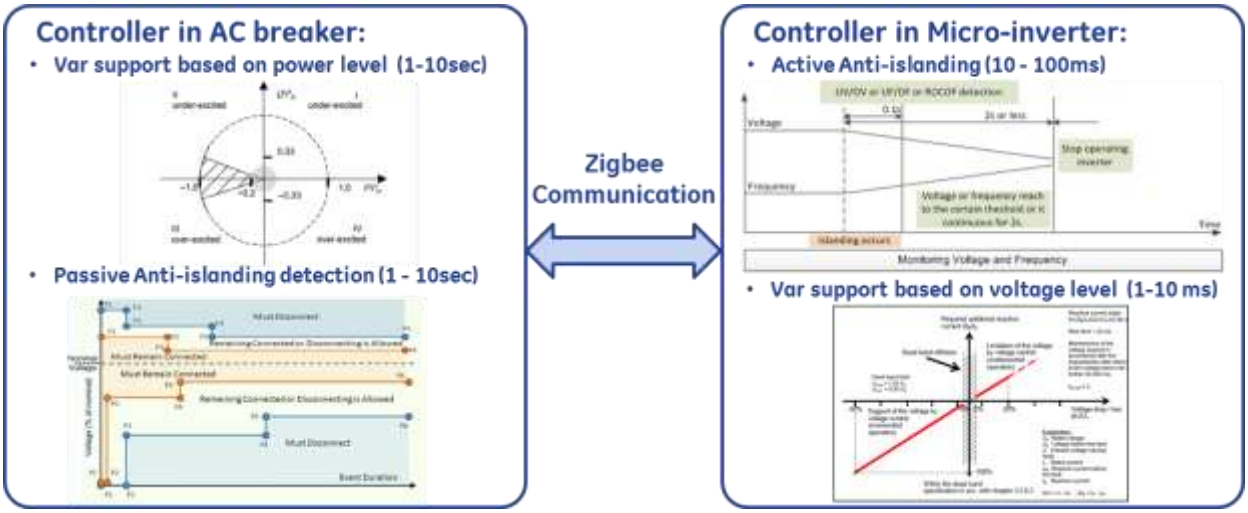


Figure 91: Grid Support Function Location

This residential solar system has unique capability to provide the reactive power command to micro-inverter according to the external command from the network operator or the internal command from the predefined operating curve. This operating curve can be based on active power command or real-time power or voltage measurement (time constant is about 1- 10s).

The experimental setup is shown in Figure 92, grid is emulated by an AC programmable power supply (Kikusui), while the load is emulated by the resistors.

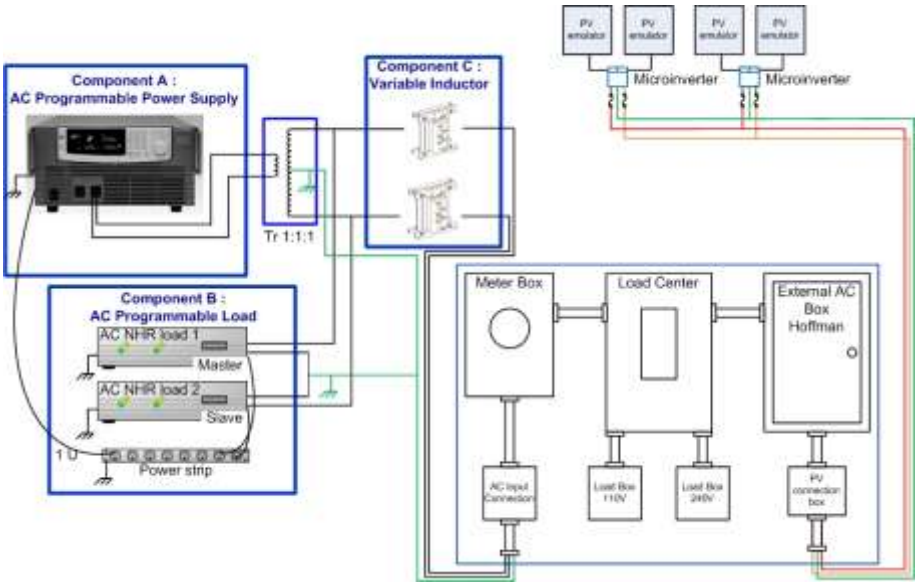


Figure 92: Diagram for Lab Demo Setup to Test the Grid Feature

For the following experiments, grid voltage is set at 240V rms unless mentioned differently.

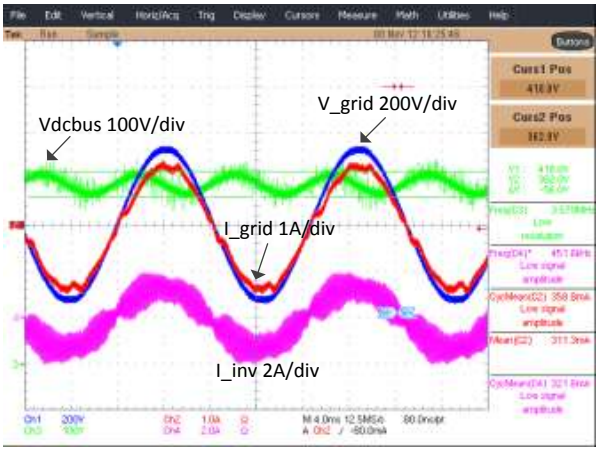


Figure 93: Output Waveform When Micro-Inverter Delivering Pure Real Power

Firstly, the micro-inverter operation is verified by delivering only the real power to the grid. That can be easily observed in Figure 93, where the grid current is in phase with the grid voltage and the output power is around 240W. Also we can see that the imposed 120Hz two phase ac system voltage ripple is 56V (peak to peak value), because of a relatively small bus capacitance. However, by using the advanced control, this fluctuation does not affect the output current waveform.

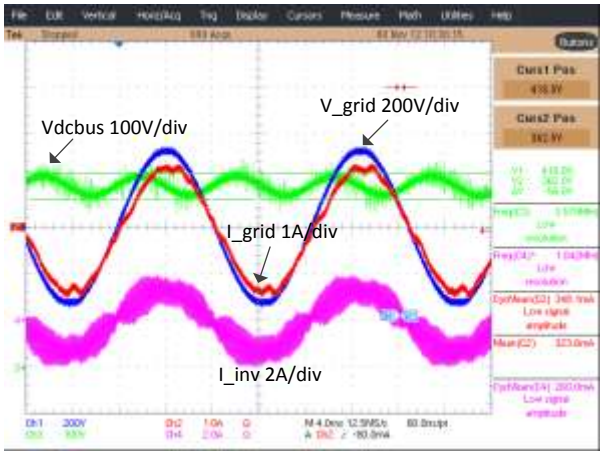


Figure 94: Output Waveform when the Micro-Inverter is Delivering Real Power and 15VAr Reactive Power

Figure 94 shows the operational waveforms when the micro-inverter is delivering real power plus 15VAr reactive power, which is confirmed by the grid current lagging the grid voltage. Output real power is kept constant at 240W. As can be seen, the dc-bus voltage ripple is still 56V (peak to peak value). Usually, when reactive power is added to the demand, the dc-bus voltage ripple will increase, but in this case, since the reactive power is small percentage of the real power, little difference is found.

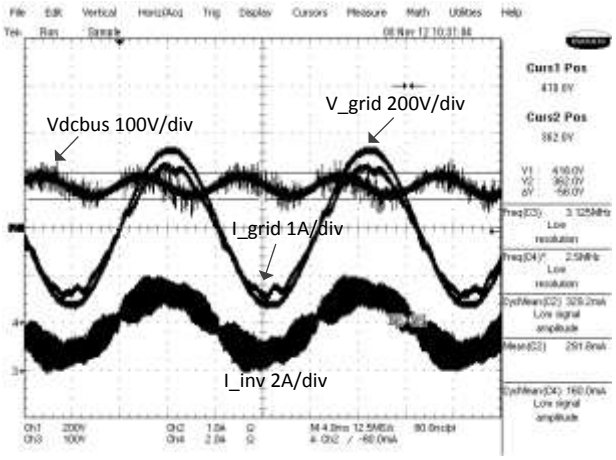


Figure 95: Output Waveform when the Micro-inverter is Delivering Real Power and -15VAr Reactive Power

Figure 95 shows the operational waveforms when the micro-inverter is delivering real power plus -15VAr reactive power, which is confirmed by the grid current leading the grid voltage. Output real power is kept constant at 240W. As can be seen, the dc-bus voltage ripple is still 56V (peak to peak value).

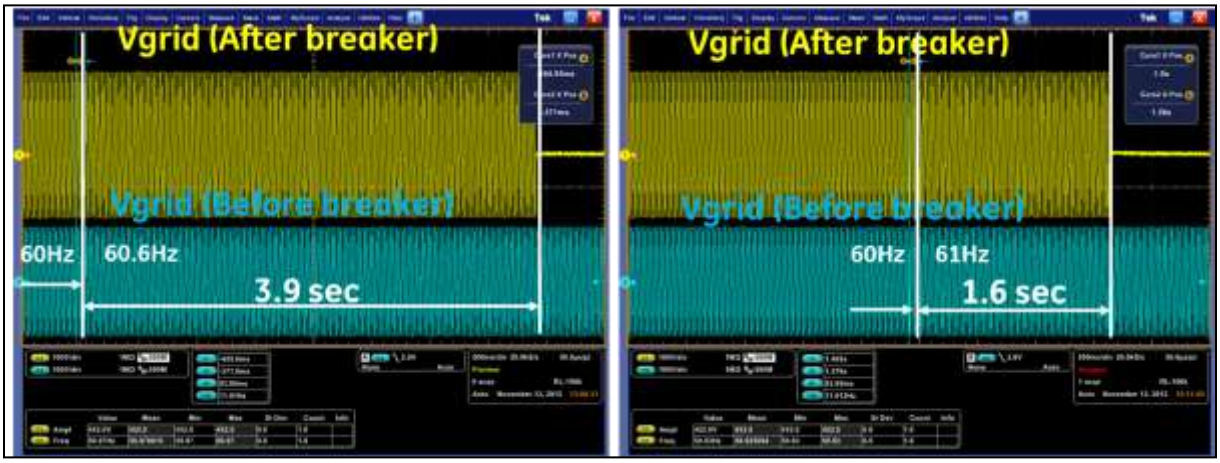
Passive Anti-islanding (AI)

Passive anti-islanding methods look for transient events on the grid. Usual passive methods include under/over voltage detection, under/over frequency detection, voltage phase jump detection, and harmonics detection. The key metric for anti-islanding algorithm is whether it has a non-detection zone (NDZ). The NDZ is a condition in which the anti-islanding algorithm fails to detect and disconnect the distributed generator within two seconds from the grid disappearance. All the passive algorithms have NDZs. Therefore, active algorithm is needed in order to avoid the NDZ and this algorithm will be implemented in the micro-inverter controller.

Table 25 lists the passive anti-islanding methods that were implemented in the ROCB controller. Upon detection of the islanding event, the back feed ROCB connected with the PV system shall be open. The back feed ROCB shall be reclosed after 2.5 minutes when the grid is restored.

Table 25: Passive Anti-Islanding Methods

Method	Pick up Threshold	Delay Setting	Implementation
UV/OV	Set at –15% and +10%. Loose range or large time constant to avoid false trip	Delays (100ms?) for breaker to react.	Standard protective relay elements
UF/OF	Set at 60-0.5Hz and 60+0.5Hz	Delays (300ms?) shall be implemented to avoid false trip.	Zero crossing method
ROCOF (Rate of Change of Frequency)	Set at 0.5 Hz/s ROCOF	Pick-up setting can be transiently exceeded. To avoid nuisance tripping under these conditions a time delay should be applied. For setting lower than 1Hz/s a time delay longer than 300ms is suggested.	Zero crossing method or GE Phasor measurement method



a) 60.6Hz Frequency Change **b) 61Hz Frequency Change**

Figure 96: AC Breaker Will Turn Off When Over-Frequency Event Occurs

Figure 96 shows the response of the breaker for the over-frequency event. Figure 96.a and Figure 96.b show the two voltage waveforms before and after the breaker. We can see that when the grid frequency is moved out of the normal operating range, the breaker will turn off after some time. Because currently we are measuring the frequency by using zero-crossing detection, the algorithm counts the zero crossing point over a period of time. So the resolution will be limited for a short period. Therefore, we can see from the Figure 13.a that if the frequency is changed to 60.6Hz, it needs 3.9s to detect the fault. On the other hand, if the frequency is changed to 61Hz, shown in Figure 13.b it only needs 1.6s to detect the fault.

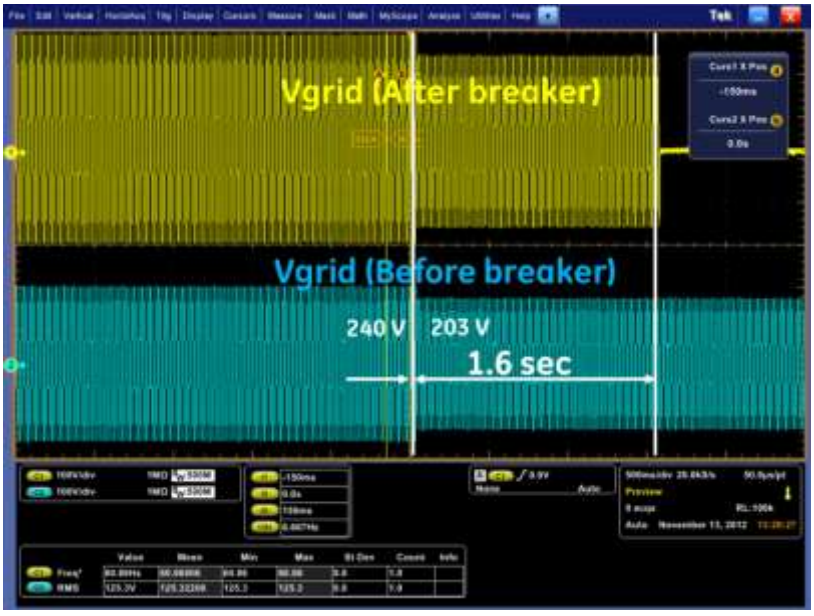


Figure 97: Testing Results for Voltage Event

Figure 97 shows the results when the grid voltage has variation. When the grid voltage drops from 240V to 203V which is more than 15%, the controller will detect this and trigger

the breaker after 1.6s. In the same way, if the grid voltage is increased to more than 10%, the anti-islanding algorithm will detect this change and trigger the breaker due to the grid standards requirement.

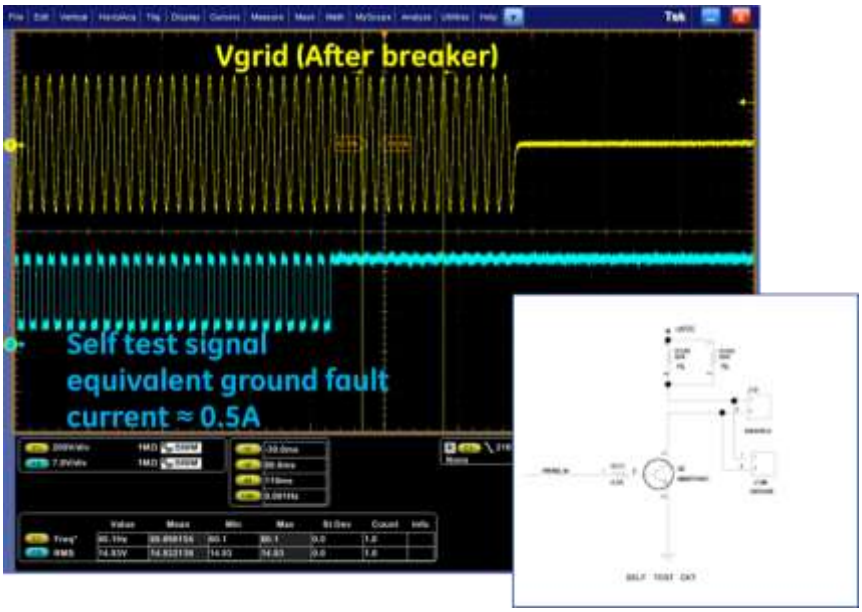


Figure 98: Testing Results for Ground Fault Test

Figure 98 shows the test result for the ground fault test, one of the features of EVSE controller board. The self-test circuit can generate on/off voltage pulses on the embedded load resistance. A CT shown in Figure 4 was used to monitor the current going through the line. Due to the board limitation (smaller load resistance), this self-test circuit could only generate 0.5A current on the load. Therefore we have lowered the threshold in the code to detect this condition. We can see the behavior of the circuit during the self-test operation from Figure 15, the pulse (blue waveform) and the voltage after breaker (yellow waveform). The pulse is only applied for a short period. Once the calculation has confirmed that the current is about 0.5A, the breaker trigger signal will be sent out. In the normal condition, for the system rated to 5kW, the ground fault detection should be set to 1A.

Anti-islanding (AI) coordination

The residential solar system that we are designing in this project includes 16 micro-inverters which are connected in parallel to the grid. As we mentioned before, the active anti-islanding algorithm is operated at the micro-inverter level. The anti-islanding algorithm is coordinated in this system in the way that at any point in time only one micro-inverter has the activated algorithm to monitor the grid. When the predetermined time slot is over, the next micro-inverter will take the role of the grid monitoring. In the case when the anti-islanding algorithm in one of the micro-inverters detects the islanding condition,

that information will be communicated to the central controller from where the disconnect signal will be sent to the rest of the system.
In the Smart Breaker Box, we have the passive anti-islanding detection algorithm active all the time. The controller will monitor the output voltage and frequency and decide whether to trigger the breaker.

Fault ride through
Within the certain range of voltage and frequency variations, i.e. frequency from 59.3Hz to 60.5Hz and voltage from 0.8Vrated to 1.15Vrated, PV inverter should be able to stay connected for a short period of time, i.e. 100ms to 200ms. If the grid event lasts longer than that, the inverter should be disconnected from the grid. AC breaker should function when voltage is lower than 0.8V or higher than 1.15V for 250ms to 300ms.
Fault ride through will be implemented in the micro-inverter and AC breaker, on both sides. The algorithm in the micro-inverter should ensure the inverter stays online for a short fault. The implementation of this algorithm will be developed in the next phase of the project. Upon the algorithm implementation, the native algorithm in the AC breaker will not require the fast response. The time constant for the AC breaker will be required to be within 1-10s when voltage is lower than 0.8V or higher than 1.15V.

3.2.5 Task5: Conduct conceptual design of the PV functional circuit including AC photovoltaic module

One of most important objectives of this project is integration of the micro-inverter and PV module to reduce system price by at least $.25/W through a) accentuating dual use of the module metal frame as a large area heat spreader reducing operating temperature, and b) eliminating redundant wiring and connectors.
Up to one-third of the cost of a microinverter is in the metal heat sink, case, wiring, and connectors. The nature of an AC module as the merger of the micro-inverter and PV module provides additional opportunities for cost reduction that are based on either the elimination of components or the functional sharing of components.
The GE team conducted the mechanical design of the AC photovoltaic module, the rail and the AC connectors. The GE team also conducted a thermal analysis of the metal frame to specify the ambient conditions of the embedded micro-inverter.
Reducing the cost of the micro-inverter relative to the best-in-class is a goal of the project. A more far-reaching objective is to have the micro-inverter drive the additional cost reduction of other system components. Integration with the aluminum frame of the module as shown in Figure 99 allows the inverter to utilize the frame as an extended heat sink. Integration of the AC connector into the frame saves wiring costs at the same time simplifying installation. Use of a simple DC connector that is integrated with the module laminate and the inclusion of bypass diodes into the micro-inverter eliminate the costly j-box with wires and connectors.

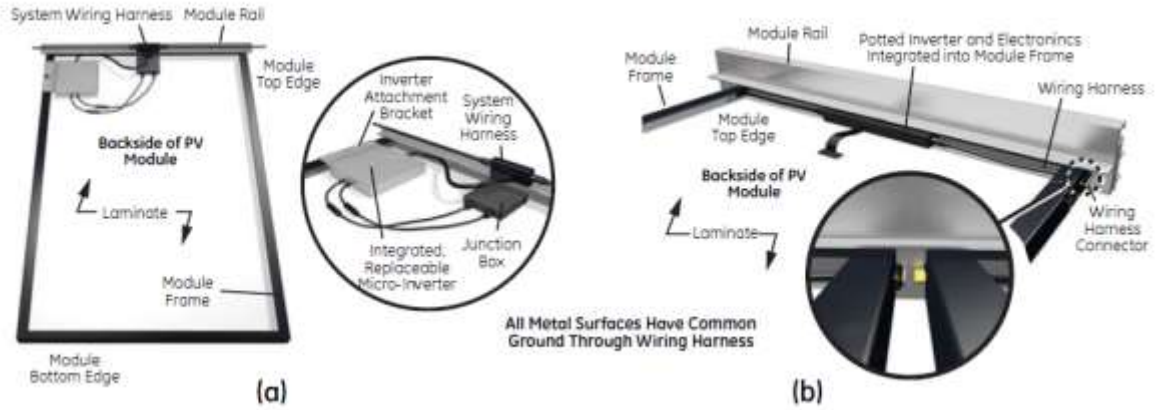
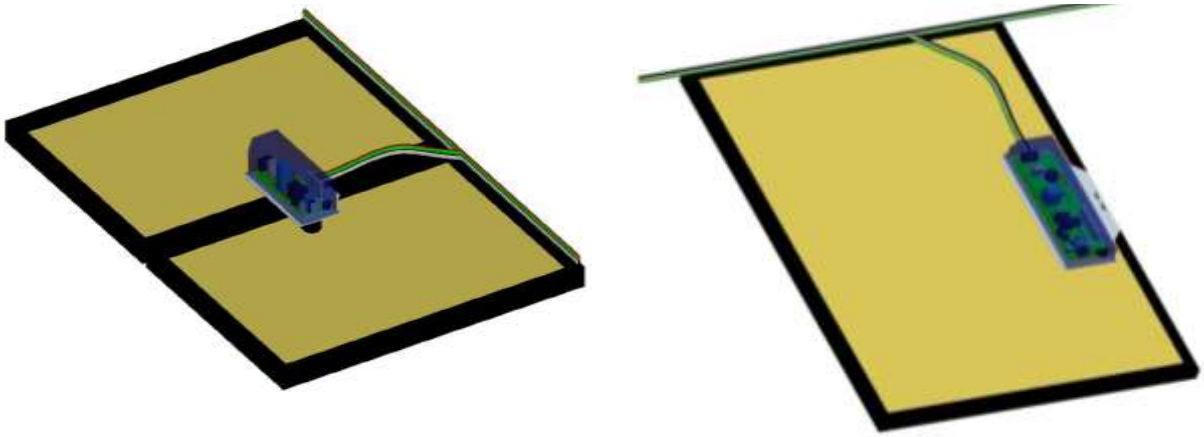


Figure 99: (a) GE's present product configuration with detachable micro-inverter that is interfaced through wiring and connectors; (b) the lower cost implementation of a micro-inverter that is embedded in the frame and uses a plug & play interface

3.2.5.1 Mechanical strategy

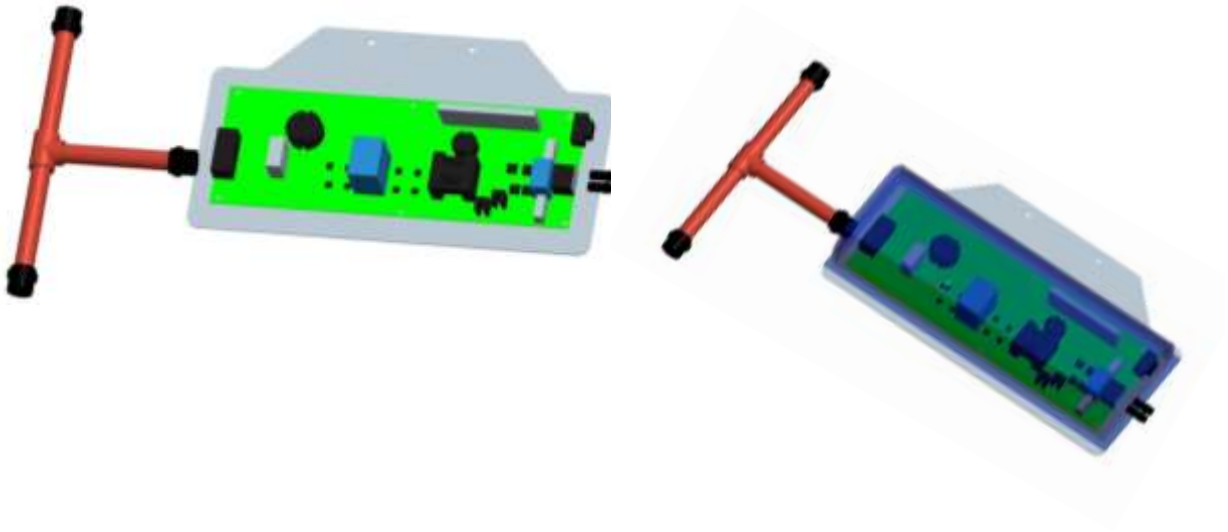
A 3D Pro/Engineer envelope model was created for conceptual layouts on CIGS modules and Si-module. The micro-inverter was mounted between two CIGS modules and required the CIGS to be mounted back to back with the junction box area moved to a symmetric location, as shown in Figure 100.a.



a) CIGS module option **b) Si-module, GaAs option**

Figure 100: Micro-inverter mounting position

Figure 100.b shows that the micro-inverter was also mounted in the central portion of one end of the Si-module. This envelope model was developed from the current micro-inverter circuit layout, shown in Figure 101, containing simple extrusions representing the electrical components in the circuit for the first pass thermal FEA model baseline.



a) without plastic cover b) with plastic cover

Figure 101: Envelope model developed from the current micro-inverter circuit layout

An aluminum base plate was modeled and intended for the base structure to mount the micro-inverter circuit card to the module, as can be seen in Figure 101.a. The base plate will also serve as the heatsink. The card will be mechanically mounted to this plate. The plate will also serve as the grounding connection for the micro-inverter. A plastic cover was modeled on top of the aluminum plate and the remaining volume was filled with a potting material, as can be seen on Figure 101.b.

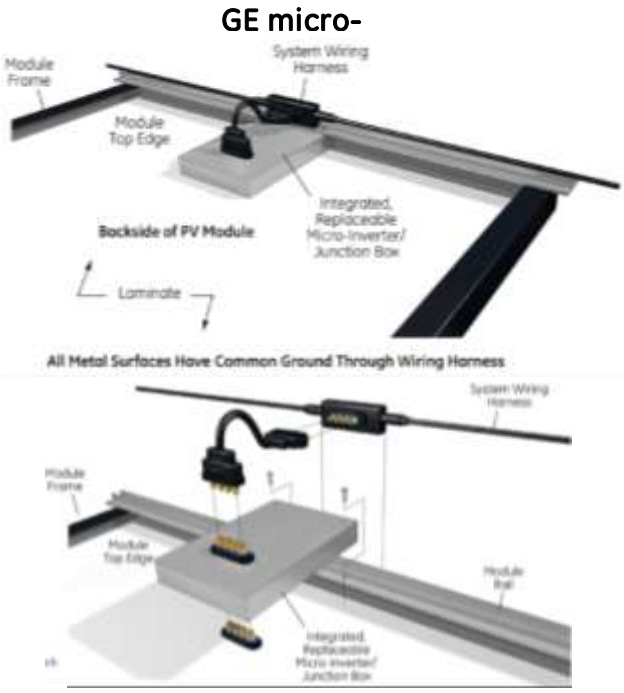


Figure 102: Concept for future product configuration with detachable micro-inverter that is interfaced through wiring and connectors

A DC harness and an AC harness were initially modeled. The DC harness was eliminated and the micro-inverter will plug into the module back, as shown in Figure 102. A DC connector concept is developed and will be shown in more detail in Task 7.

3.2.5.2 Thermal strategy

Given the high efficiency and low cost expected for this inverter, the small thermal loads need to be rejected via natural convection. Also, the module must be constructed for outdoor environments. An initial concept thermal FEA was conducted using the prototype circuitry as it was modeled. A potting compound was made to occupy the 3D model in-between the metal mounting plate and the plastic cover but excluding the volumes occupied by the electrical components. Filling this negative space with potting epoxy will help seal and mechanically protect the circuits as well as spread heat and provide a conductive path to the case. The heat dissipated from the power conversion circuits will leave the module via natural convection on the open face (not facing the module). Radiative heat transfer and the photovoltaic module were not modeled as the prototype design is preliminary and does not justify a modeling effort that detailed. Instead a simple natural convection boundary condition of 5 W/m^2-K and 80 °C was imposed on the metal plate that faces away from the panel. Temperature and heat flux fields were then computed with distributed loads generated in circuit components. The result showed that part proximity and distance from the convection surface were both important parameters in determining junction temperatures. Although the solution is preliminary and sensitive to loads that are not final, maximum temperatures did not exceed allowable limits.

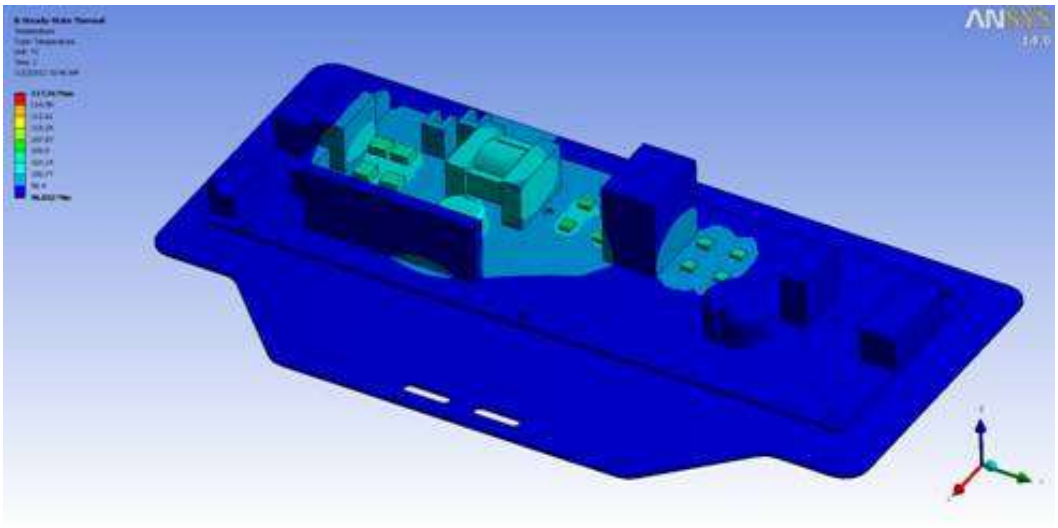


Figure 103: Initial concept thermal FEA with h = 5 W/m2-K; On shell Tamb=80 °C

3.2.6 Task 6: Design and build the embedded micro-inverter prototype

3.2.6.1 Micro-inverter power circuit

Micro-inverter has been redesigned to operate with a mc-Si panel of low voltage input. The ratings of the micro-inverter designed in Phase 2 are listed in Table 26.

Table 26: Micro-inverter Specifications

INPUT DATA (DC)	**Low voltage GE micro-inverter**
Recommended input power (STC)	300 W
Maximum input DC voltage	50 V
Peak power tracking voltage	23-41 V
Operating range	14-50 V
Min/Max start voltage	16-41 V
Max DC short circuit current	15 A
Max input current	9.8 A
OUTPUT DATA (AC) @240 VAC	
Peak output power	300 W
Rated (continuous) output power	288 W
Nominal output current	1.25 A
Nominal voltage/range	240 V/ 211-264 V
Nominal frequency/range	60.0/ 57-62 Hz
Power factor	>0.99
Reactive Power Capability	full rated power reactive power capable
Maximum units per 20 A branch circuit	13
Maximum output fault current	2.2 A
EFFICIENCY	
CEC weighted efficiency, 240 VAC	under evaluation (Target 96%)
Peak inverter efficiency	under evaluation (Target >96%)
Static MPPT efficiency (weighted, reference EN50530)	> 99%
Night time power consumption	0 W
MECHANICAL DATA	
Ambient temperature range	-40°C to 65°C
Operating temperature range (internal)	-40°C to 85°C
Dimensions (W x H x D)	348 mm x 172 mm x 34 mm (with junction box integrated with Micro-inverter) Just micro-inverter 241 mm x 172 mm x 34 mm
Weight (u-inv + junction box)	1.4kg (Not potted)
Cooling Natural convection	Natural convection - No fans
Enclosure environmental rating	NEMA6, Embedded within Solar Frame
FEATURES	
Compatibility	Compatible with 60-cell Si PV modules.
Communication	Zigbee

Integrated ground	The DC circuit meets the requirements for ungrounded PV arrays in NEC 690.35. Equipment ground is provided in the Engage Cable. No additional GEC or ground is required.
Monitoring	Nucleus
Compliance	UL1741/IEEE1547, FCC Part 15 Class B, UL1703 (IPC 9592A in progress)

In order to provide sufficient voltage gain with a low voltage mc-Si input source the resonant converter topology designed for the CIGS modules was modified to have a voltage doubler output and the LLC resonant tank parameters are chosen as: series inductance (L_r)= 5.2µH, series capacitor (C_r)= 329nF and transformer magnetizing inductance (L_m)=34µH. The resonant frequency is 125Hz. The output stage remains an interleaved full bridge inverter with interface inductors as it was with the high voltage version of the micro-inverter. Figure 104 shows the modified circuit topology. Figure 105 shows the micro-inverter prototype printed circuit board. Preliminary tests to verify operation of the input stage, output stage and housekeeping power supply were performed as shown in waveforms in figure 106.

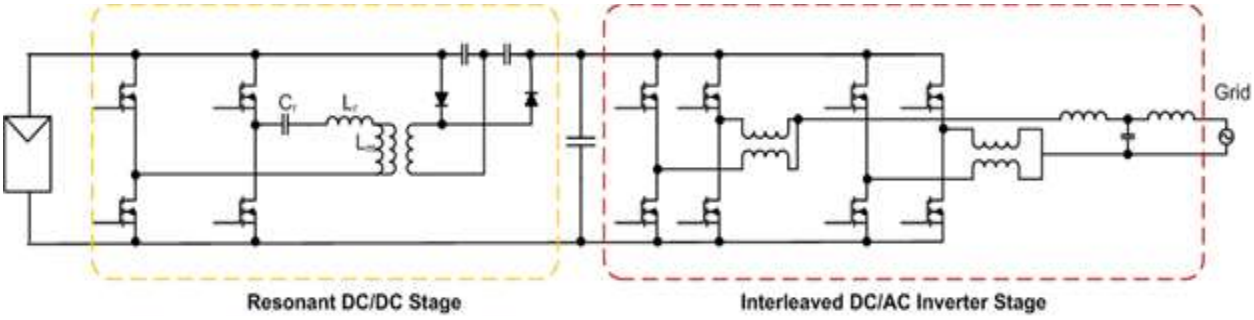


Figure 104: Circuit topology with modified input stage

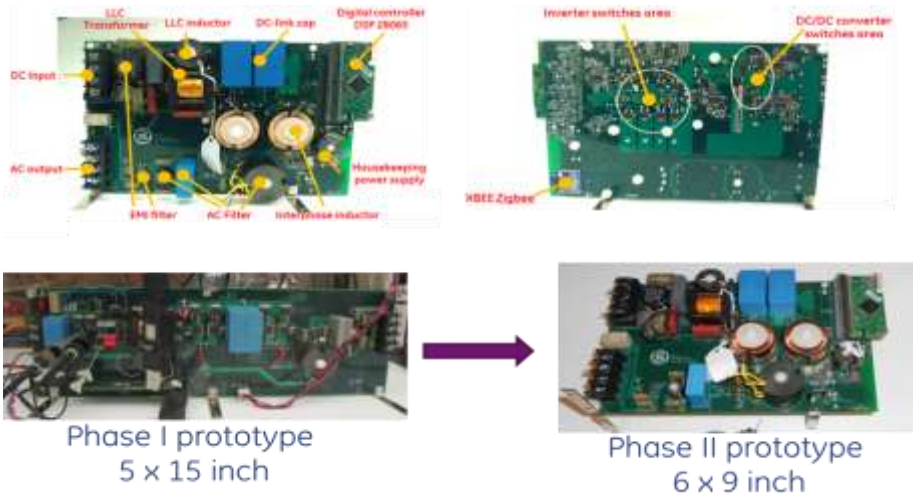


Figure 105: Micro-inverter prototype

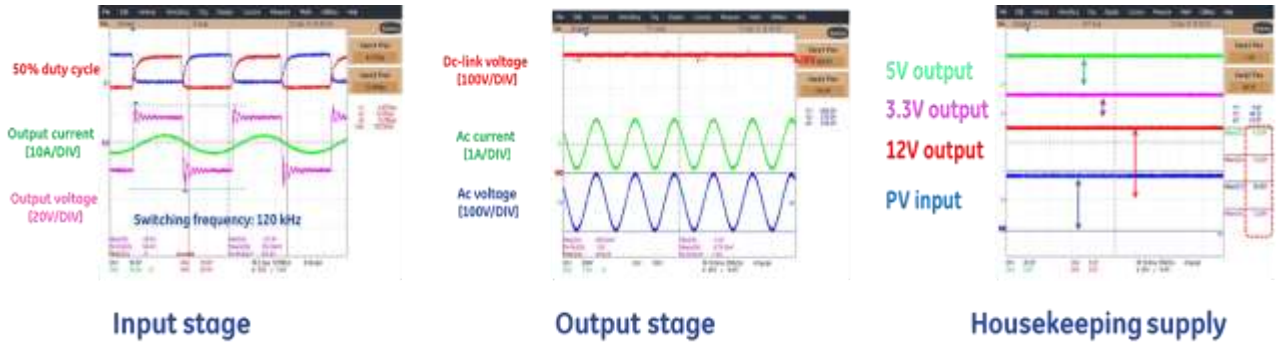


Figure 106: Basic waveforms of each micro-inverter power stage

Detailed analysis on the resonant converter operation was performed to identify the most efficient mode of operation. Trade-off between frequency and phase-shift control showed the superiority of frequency control in minimizing the circulating current and thus minimizing conduction losses in the resonant converter switches. To limit excessive switching frequency, which will impact the reverse recovery losses of the output diodes, a phase shift control is applied to reduce the gain even more. The reduction in gain through phase shift leads to current circulation on the primary side as shown in Figure 107. Figure 108 shows a comparison between resonant tank current for different power levels with variable frequency control vs. phase shift control at the series resonant frequency 125kHz.

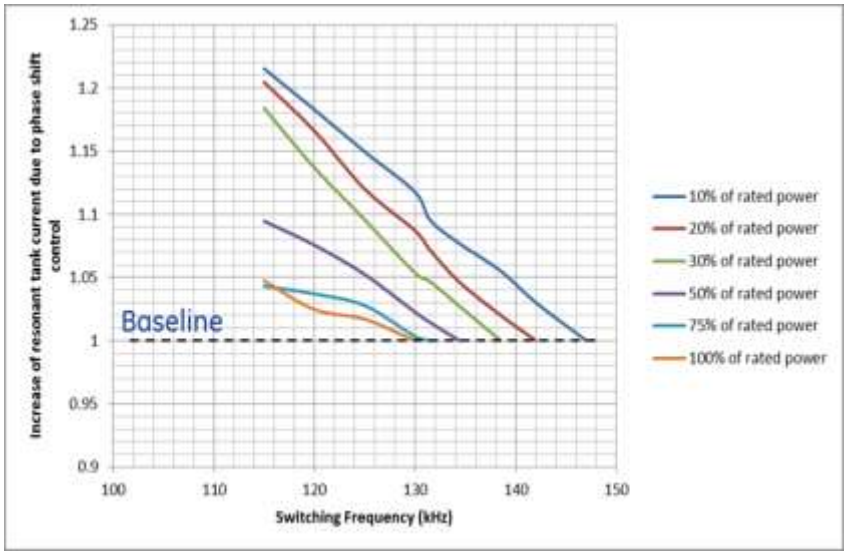


Figure 107: The plot shows the increase in resonant current due to phase shift control

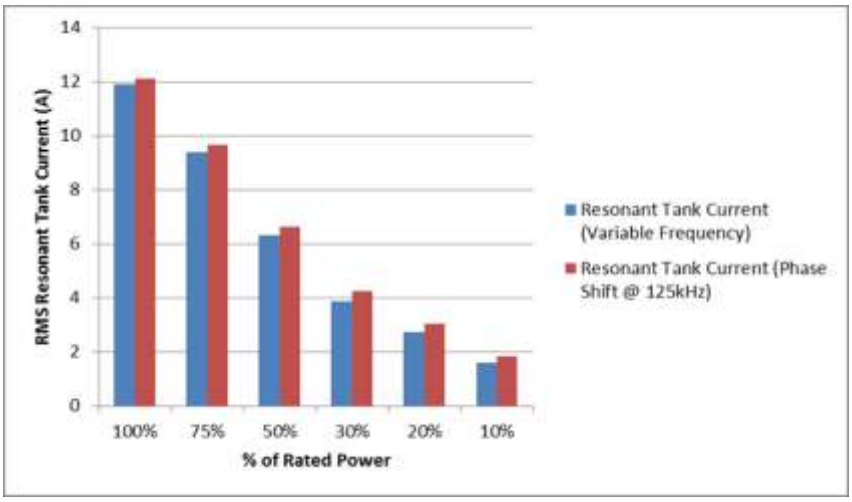


Figure 108: Comparison between resonant current with variable frequency control vs. phase shift control at 125kHz

Assessment of optimal DC-link voltage level was performed and ideally 370V was found to provide the least losses, however, control implementation will relate the DC-link voltage to the AC line voltage such that line voltage and 120Hz ripple are accommodated in the converter operation. Figure 109 shows a comparison between the resonant tank current required for different DC-link voltage levels.

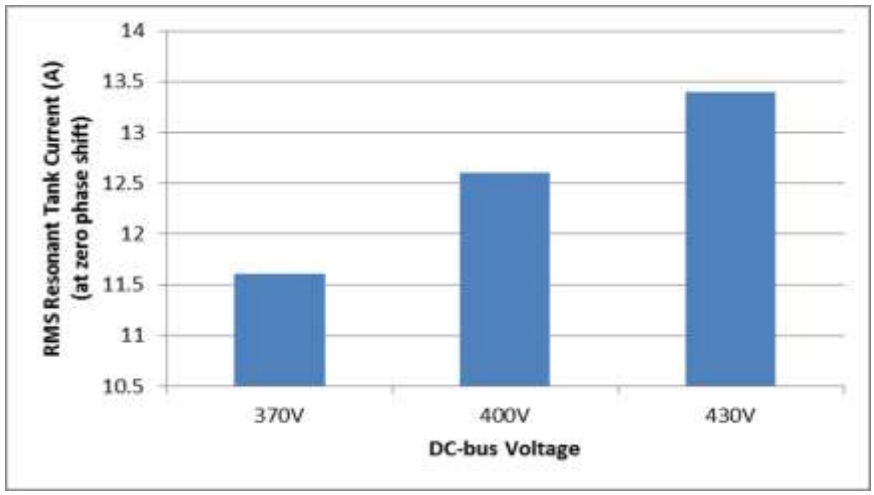


Figure 109: Resonant tank current for different DC-link voltages at rated power

Loss breakdown analysis of the inverter stage was performed, which indicated that a major part of the inverter loss is due to diode reverse recovery losses. A trade-off was performed between diode reverse recovery losses and MOSFET conduction losses as shown in Figure 110, to select the device that gives the minimum overall inverter losses. Since reverse recovery losses are dominant reducing the dc-link voltage helps improve the efficiency.

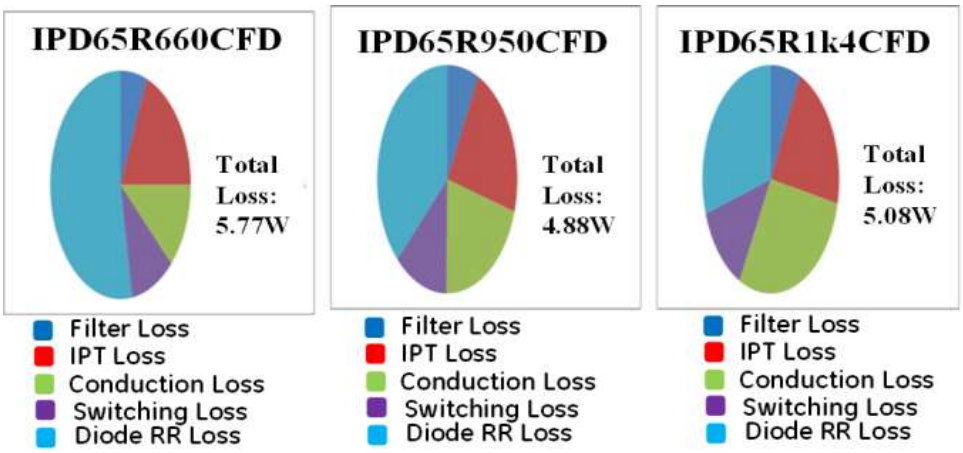


Figure 110: Inverter loss breakdown using different switches

Efficiency tests were performed on each of the micro-inverter stages. Preliminary efficiency of the input DC/DC converter stage was measured to be 97.6%. For the DC/AC inverter stage, the peak efficiency was measured to be 97.9% at switching frequency of 15 kHz and peak efficiency of 98.1% at switching frequency of 10 kHz. It should be noted that the MOSFETs used in the inverter stage are not the optimal parts identified through calculation due to their unavailability, so this efficiency can be improved as the devices become available and used in the converter.

Further improvements to the housekeeping power supply were made to reduce the operational voltage to 11V and also eliminate part of the steady state losses by adding a Zener diode in series with the pre-loading resistor. The measured micro-inverter efficiency and MPPT tracking efficiency is shown in Figure 111. It should be noted that the resolution of the 600V power supply was a little low for perfectly characterizing the MPPT efficiency of a 27~28V converter input voltage range. The measured converter CEC efficiency was 95.4% and the measured MPPT efficiency was 98.35%.

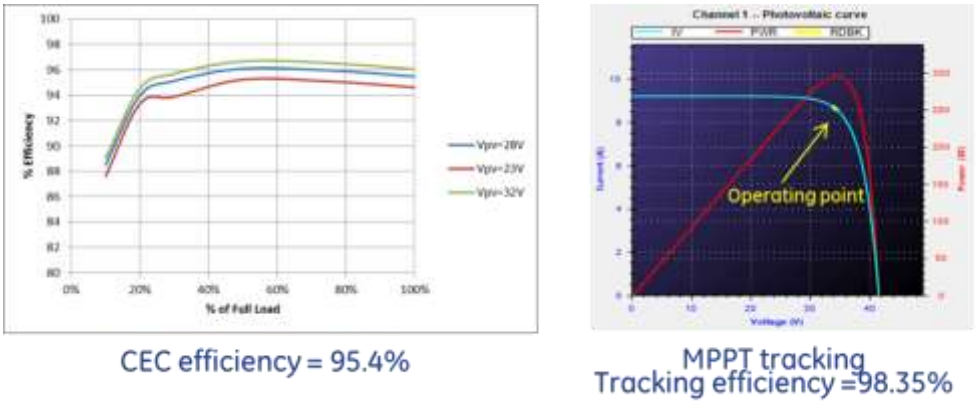


Figure 111: Micro-inverter efficiency and MPPT efficiency

3.2.6.2 Controller design and implementation

Closed loop control of the overall system as well as protection functions were tested and verified. It was noted that pull down resistors were needed on all gate signals and the relay logic drive signal. An attempt has been made at using the TI control chip

TMS320F28065UPZT, however, due to memory limitations we reverted back to TMX320F28069PZA. Work is also performed to reduce the processing time by simplifying the PI controller code and splitting the operation of the PLL over several computational cycles. So far the control simplification achieved a reduction of the processing time by 21.8% (from 44µs to 34.4µs) as shown in Figure 112. Look-up tables for frequency control of the resonant converter are being studied to avoid complex non-linear control implementation.
The control of the micro-inverter is shown in Figure 113. The MPPT function is realized by the first-stage dc-dc converter. MPPT tracks the maximum power and sends out the PV voltage reference. A simple PI regulator generates the phase-shift angle command to the first-stage. The dc-dc converter monitors the dc-link voltage and smoothly changes its switching-frequency to maintain the soft-switching as well as a proper boost-up gain-ratio. The second-stage dc-ac inverter has a double-loop control scheme: outer dc-link voltage regulation loop and inner ac current regulation loop. The dc-link voltage signal first passes through a digital notch filter by eliminating the large double line-frequency ripple, and then compares with a reference. A PI regulator generates a d-channel current reference. In order to increase the outer loop speed to handle fast load-step transient, additional feed-forward loop is built by monitoring the input power as well as ac voltage. As such, a d-channel current reference is generated directly by applying a power balance calculation. Both PI regulator output and feed-forward output build up the d-channel reference. An ac current error signal is generated by combining both d and q-channel error signals. An inner PI regulator utilize such error signal to generate the duty-cycle command. Notice that the inner current loop also contains a feed-forward loop to expedite the regulation performance.
Anti-islanding detection is a build-in function in the phase-locked-loop. The inverter output frequency will deviate from the steady-state when the islanding occurs. The voltage/frequency monitoring and protection is also implemented in the control system to fully comply with the grid-codes.
A state machine and communication diagram is shown in Fig. 114, where the local control of the micro-inverter communicates with the centralized control hub via zig-bee communications for commands such as ON/OFF, P/Q, as well as data logging.

Anti-Islanding test with constant power AC load was conducted as well, and it is meeting the requirements. On the other hand, Unintentional islanding test procedure requires connecting the resistance, inductance, and capacitance (RLC) load (resonant tank generation) in parallel with the equipment under test (EUT) which will mimic the 60Hz source once the grid is disconnected.
Open phase test was also conducted in the lab during this quarter. The purpose of this test is to verify that the micro-inverter ceases to energize the area EPS upon loss of an individual phase. Clearing time was recorded.

Trip zone protection was also tested on the new board. DSP 2806x Piccolo family of microcontrollers has a built in trip zone protection function. The trip zone input signals alert the ePWM module of fault conditions external to the ePWM module. Signals connected to these inputs were intentionally driven beyond the threshold value to test the response.

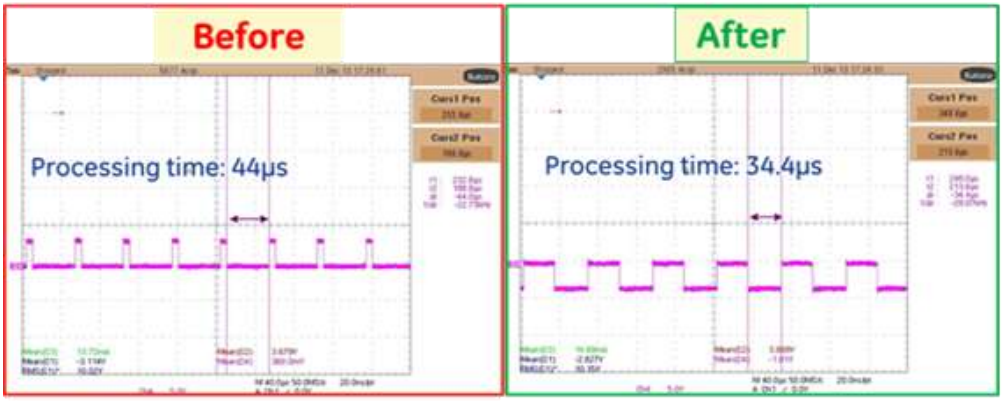


Figure 112: Reduction in control processing time

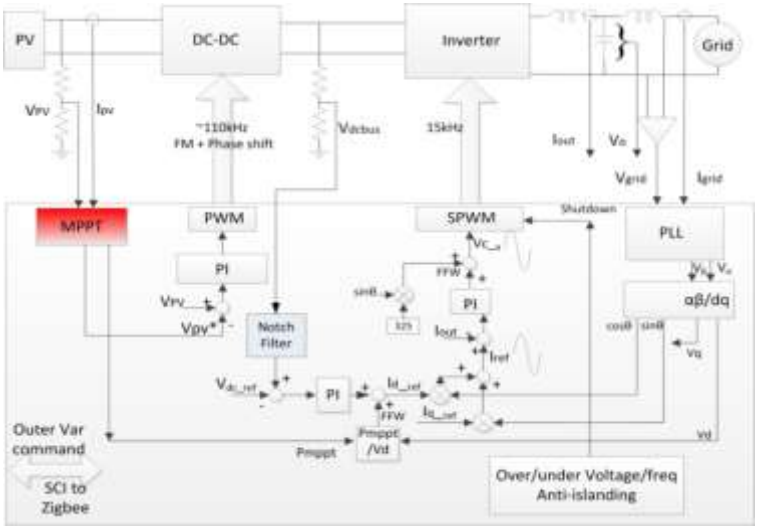


Figure 113: Control block diagram of micro-inverter

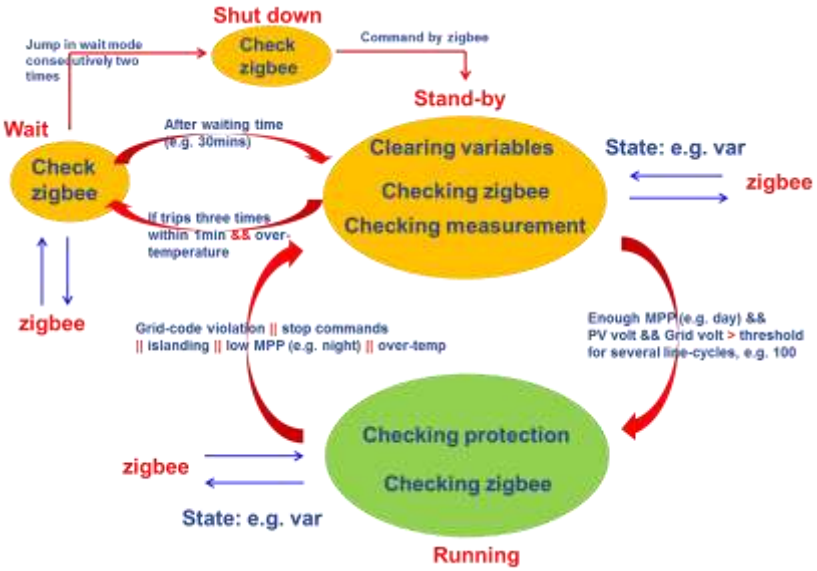


Figure 114: State-machine and communication

3.2.6.3 Micro-inverter testing

Figure 115 shows example waveforms at different fault and operating conditions, including soft start, normal operation and trip due to different error conditions. A summary of IEEE 1547 tests is given in Table 27.

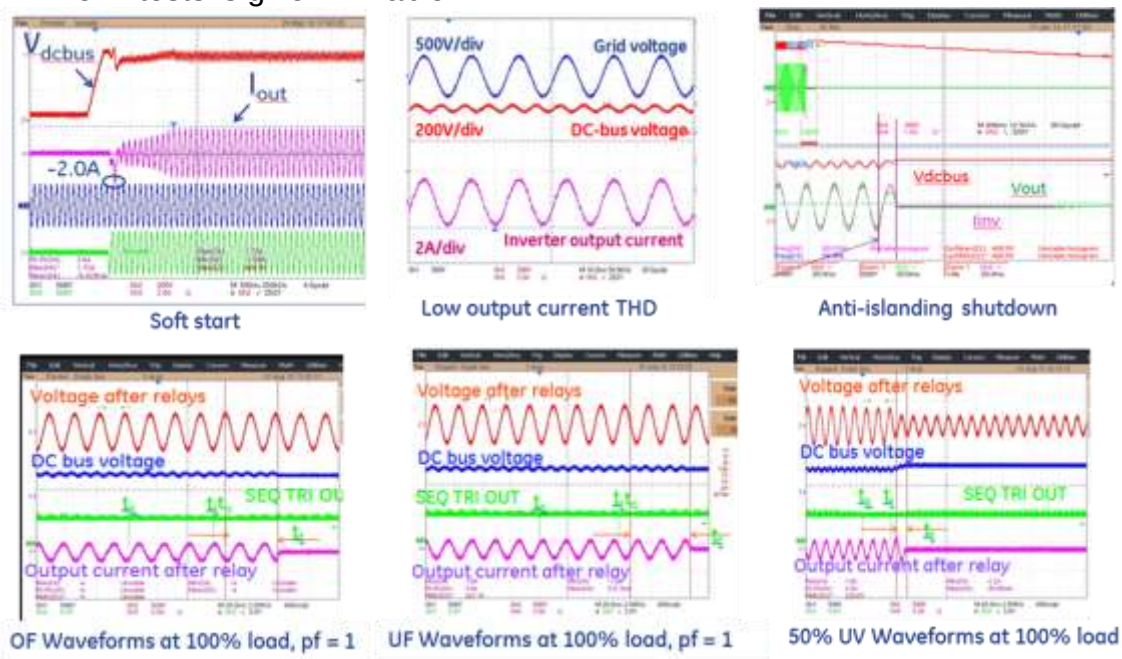


Figure 115: Operating and trip conditions of the micro-inverter

Table 27: IEEE 1547 testing summary

Test	Status
Voltage Test (over-voltage, under-voltage different loads and PF)	**Complete/Passed**
Frequency Test (over-frequency, under-frequency)	**Complete/Passed**
Synchronization	**Complete/Passed**
Interconnection integrity	**Complete/Passed**
Limitation of dc injection for inverters without interconnection transformers	**Complete/Passed**
Unintentional islanding test	**Complete/Passed**
Open phase	**Complete/Passed**
Reconnect following abnormal condition disconnect	**Complete/Passed**
Harmonics test for inverters	**Complete/Passed**

In order to improve the quality of the output AC current waveform the inverter control loop was changed as follows:

1. Sampling frequency 15kHz

2. Fine tuning Notch filter (N)
3. Adding feedforward loop in dc-link voltage loop
4. Adding feedforward loop in current loop
5. Use PLL to construct current reference rather than voltage feedback signal

The modified inverter control block diagram is shown in Figure 116. Figure 117 show the simulated and experimental results of the AC current THD.

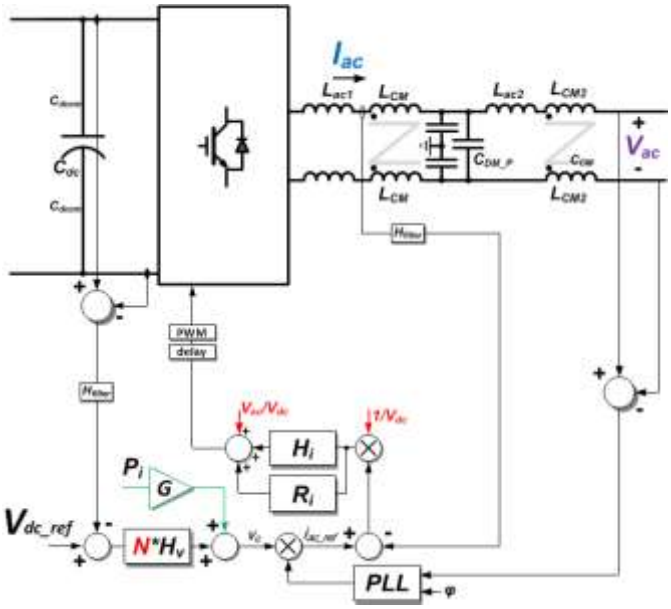


Figure 116: Modified controller block diagram to improve THD

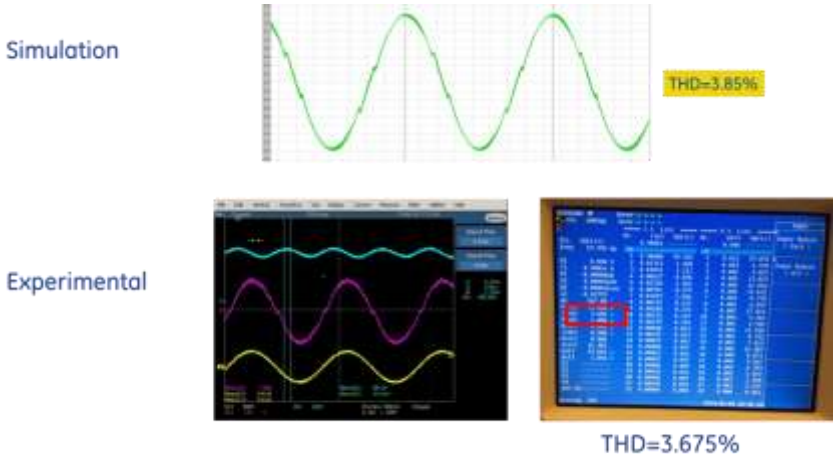


Figure 117: Simulated and measured THD with modified controller design

3.2.6.4 EMI Testing

EMI testing was performed for conducted EMI. The test setup is shown in Figure 118. And block diagram and circuit diagram of the LISN are shown in Figure 119. The first test results are shown in Figure 120. The inverter fails the test for both common mode and differential mode EMI by a margin of 45dB.

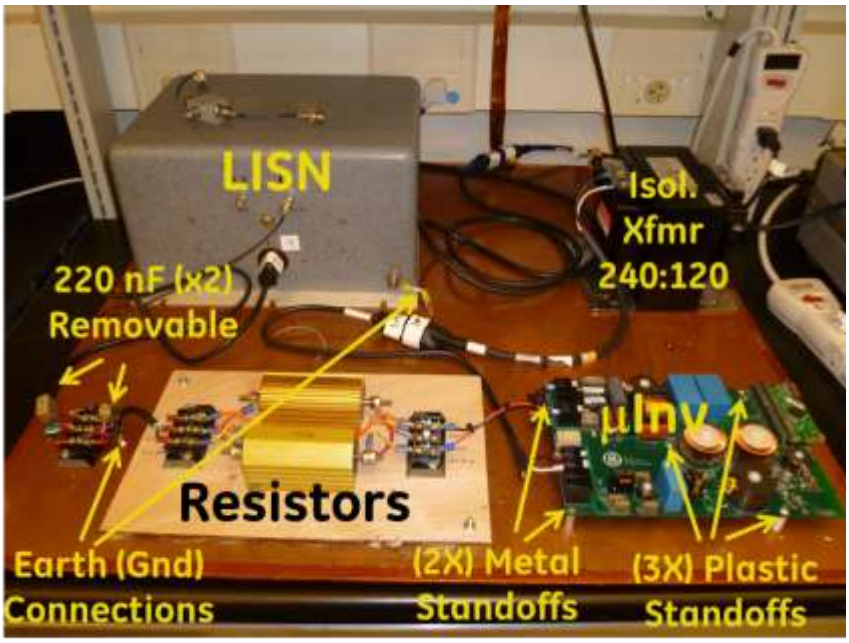


Figure 118: EMI test setup

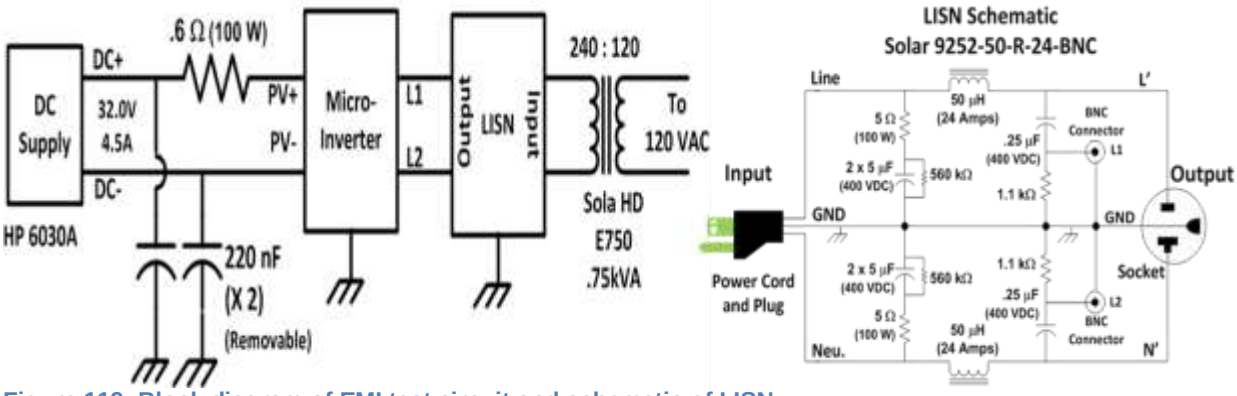


Figure 119: Block diagram of EMI test circuit and schematic of LISN

Figure 120: Baseline EMI measurement

The following modifications were made to the micro-inverter board:

- Improve power decoupling
    - Remove Big C / Small C Resonance
- Improved parts placement
    - Minimize radiation coupling
- Improved output filter design
    - Higher CM rejection
- Remove large dv/dt surface areas
    - Improves CM performance
- Can improve HF response
    - Probably due to semiconductors
        - Diode reverse recovery suspected

The waveforms of the modified unit are shown in Figure 121 and it passes the test.

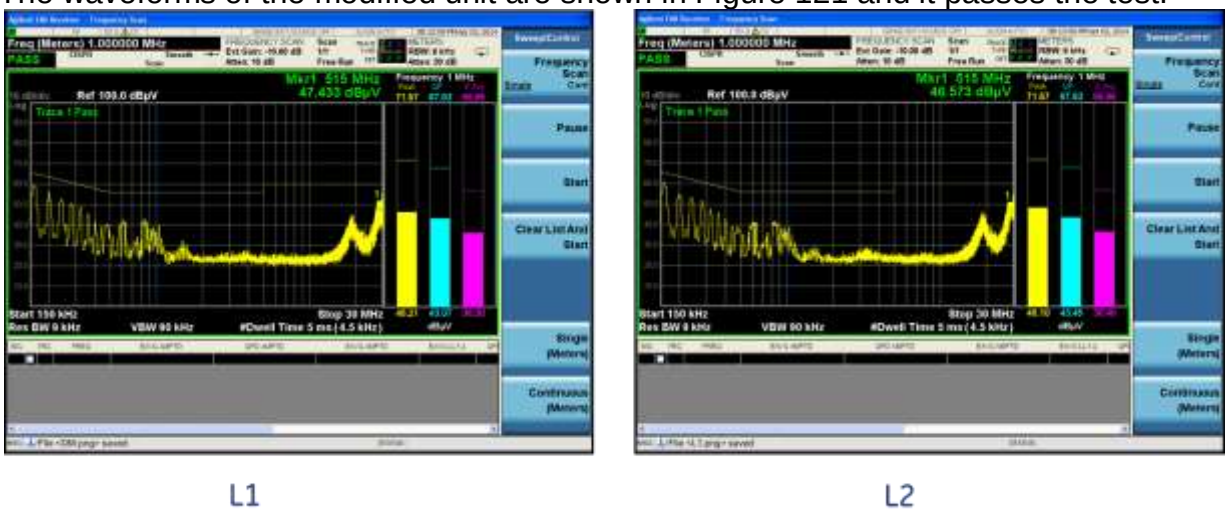


Figure 121: EMI measurement for the modified micro-inverter

3.2.6.4 Communication Testing

Selected XBee ZB - Zigbee communication modules from Digi International Zigbee /IEEE 802.15.4, with 1mW output power was purchased and tested. Advantages of this module are the support for point to multipoint and mesh, small size, range of ~40m indoor, operating conditions -40°C to +85°C. Planned Network Configuration is configured so that each micro-inverter communicates with Xbee module (acting as end device/router) over the serial port (UART). One Xbee module will be used as a network coordinator (gateway) for data gathering. Several tests were conducted to estimate the communication effectiveness in the real life scenario. We have measured the number of the successfully received packets out of 100 sent packets from different locations. First Zigbee node was placed at the roof (shingles), enclosed in a metal enclosure and powered through power cable. Second Zigbee node was placed in different rooms in a house. Quality of the communication was almost always at the maximum and could be improved by increasing the transmission power. Tests with battery operated Zigbee radio were also conducted to exclude the possibility of power cable acting as an antenna. Metal enclosure box was

closed with or without the metal gasket to prevent RF leaking. Test setup and signal integrity are shown in Figure 122.

Preliminary EMI testing was performed on the micro-inverter unit. Issues of high common mode and differential mode noise were identified in the low frequency range (150 kHz<f<1 MHz) and was compliant at higher frequencies (f>1 MHz). EMI filters were revised to address these issues.

Bill of material has been updated in accordance with issues found during converter testing and HALT outcomes in Task 8.

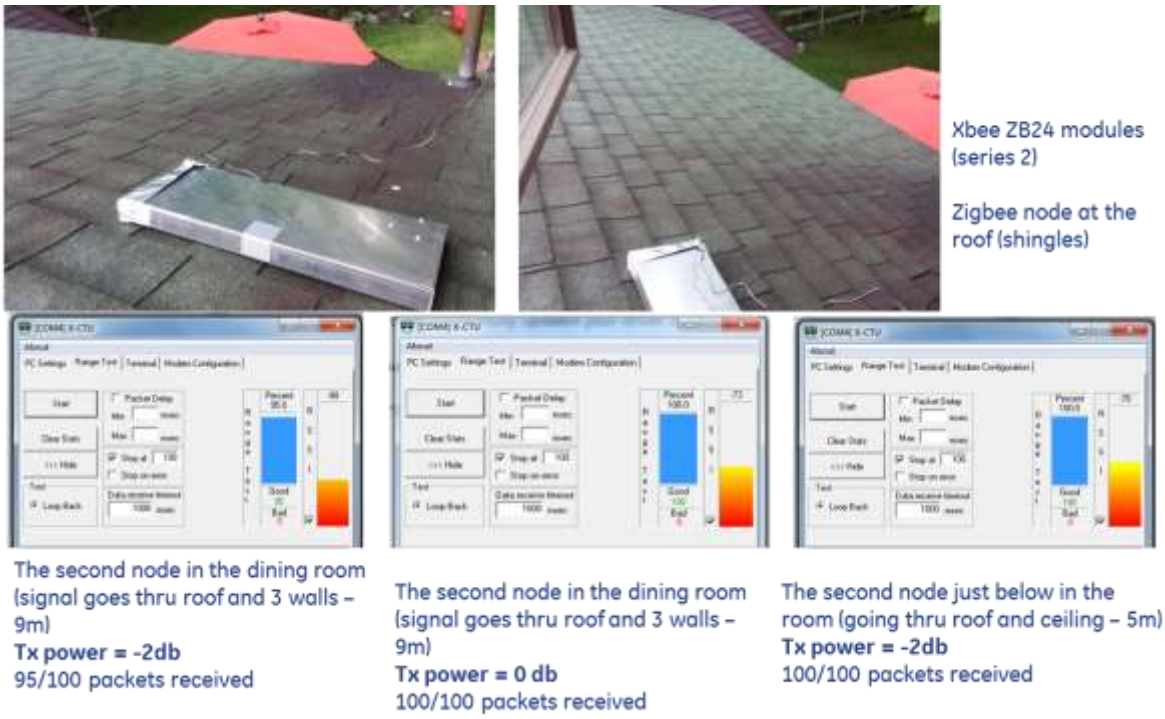


Figure 122: Zigbee communication testing

3.2.7 Task 7: Integrate and test AC photovoltaic module system

3.2.7.1 ACPV panel design and build

The purpose of ACPV integration is to simplify system installation, enhance safety and reduce installation cost. The junction box of the PV panel is eliminated and integrated with the micro-inverter enclosure. All DC cables are eliminated and a simple plug and securement mechanism is developed to integrate the panel and micro-inverter. Panel frame grounding is simplified by grounding the frame through the ac ground line. A simple AC harness is designed where amount of wiring is reduced and micro-inverters are easily plugged into the harness.

Amphenol completed the design and build of molded plastic box, metal top, DC & AC connectors and AC harness for multi-panel system. The molded box is designed to house the micro-inverter board and bypass diodes. The enclosure will then be filled with potting material to provide environmental isolation and mechanical support for components.

Concept box design is shown in Figure 123. The enclosure and panel connector dimensions are shown in Figure 124.

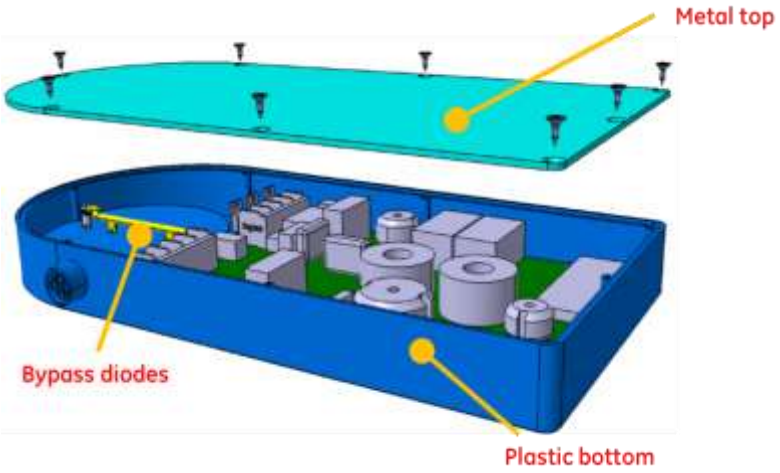


Figure 123: New micro-inverter box concept design

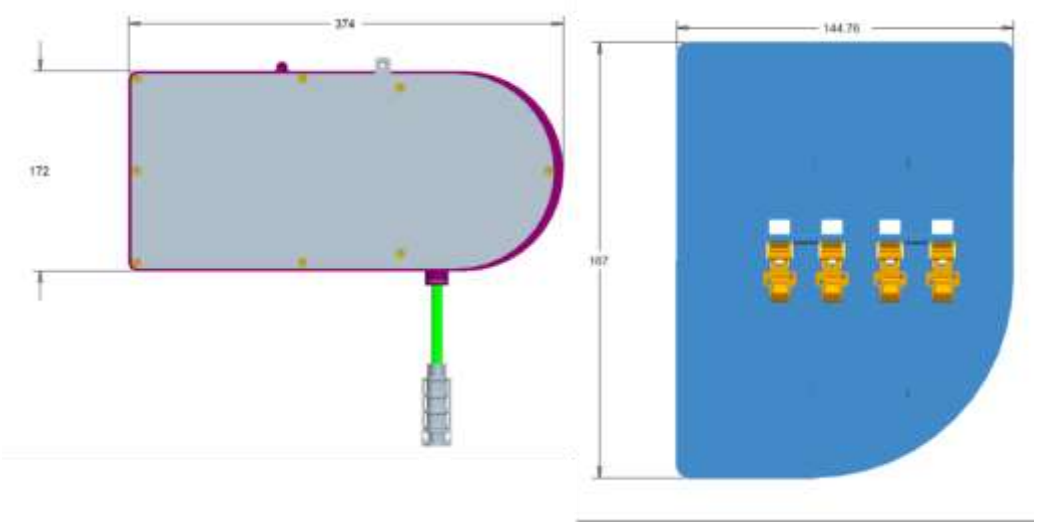


Figure 124: Dimensions of enclosure and panel connector (dimensions are in mm)

The micro-inverter is aligned with the panel dc-connectors and secured to the frame by two screws. Grounding of the PV system is also provided through the corner screw on the micro-inverter board. Figure 125 shows the integration concept of the micro-inverter and the rail of the PV panel. Figure 126 shows a 3d-printed mock-up box tied to a Motech panel to prove the concept.

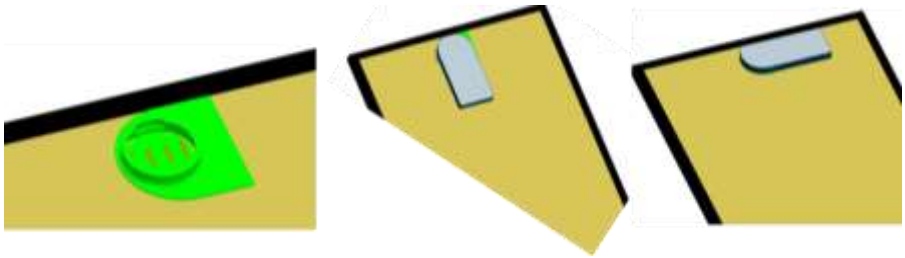


Figure 125: Concept integration of ACPV panel

Figure 126: Proof of integration concept

Figure 127 shows a more detailed view of the micro-inverter support and grounding connections. The following can be noted from the figure:

1. Enclosure secures to panel with screw at right position after 90 degree rotation into position
2. Left most screw provides ground to panel frame
3. Two screws with arrows provide circuit ground to aluminum cover
4. Base indexes off the edge of the panel
5. Panel Ribbon is pinched in base similar to existing junction boxes
6. Micro-inverter circuit will be potted and the diodes. Internal walls will limit potting material volume.

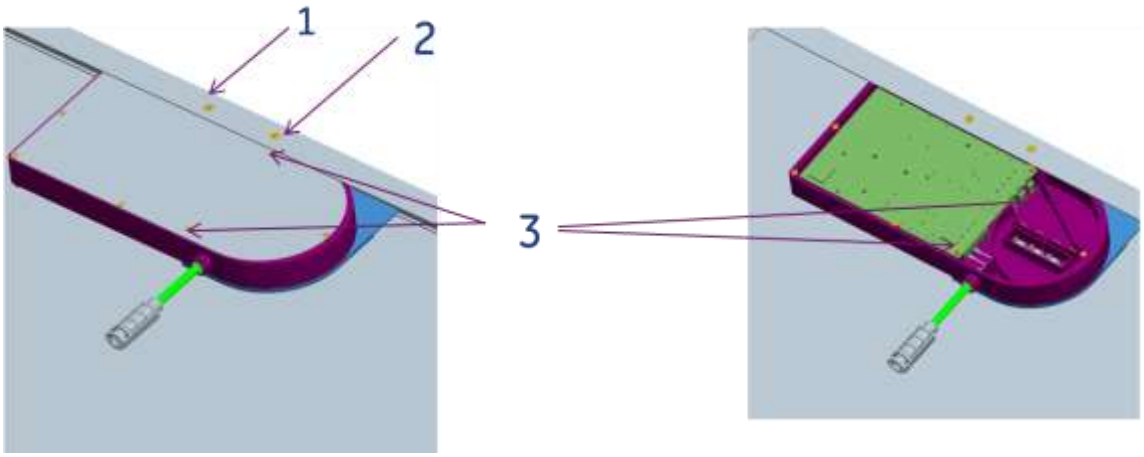


Figure 127: Mechanical support and panel grounding

An AC harness that runs across the array was also implemented. The ac output line of each micro-inverter plugs into the AC harness, as shown in Figure 128. This reduces the AC wiring to half what is used in a standard implementation as shown in Figure 129. An alternative connection with a harness that has single plugs is shown in Figure 130. This is similar to the harness that was implemented in this work as it is an available plug design and would be more cost effective for the purpose of this project. The spacing between connectors on the harness in this case has to fit within one panel width.

Figure 128: AC Harness

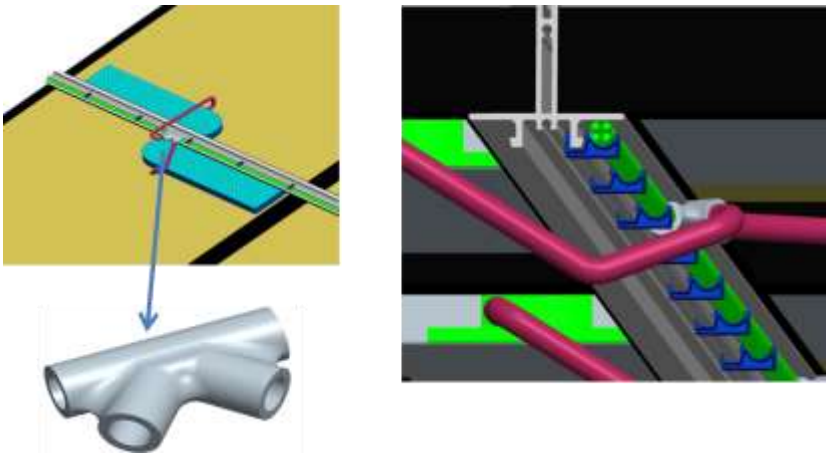


Figure 129: Integration of modules with AC harness

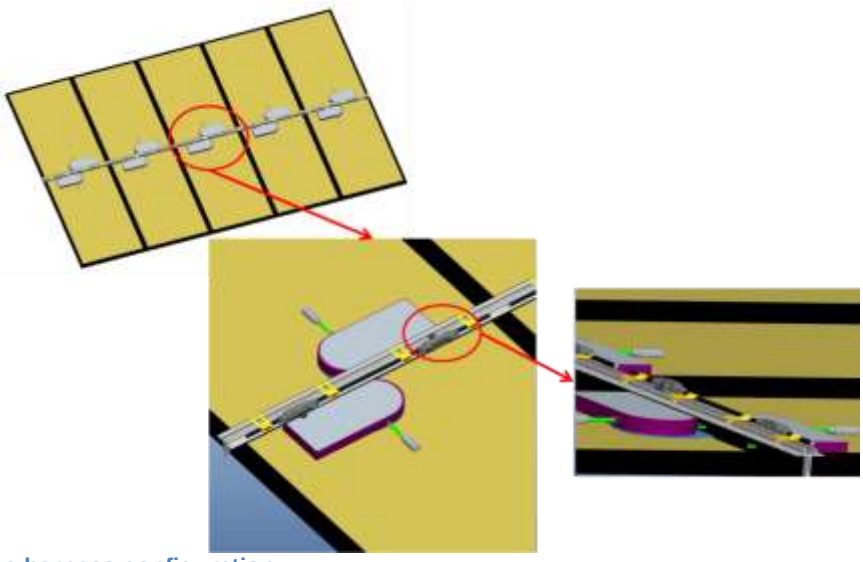


Figure 130: Alternative harness configuration

Seven units were built, tested and sent out to Amphenol to integrate in the enclosure. Two of the units were potted to test the effect of potting on performance and thermal management and also assess its effectiveness in providing mechanical support to components as well as isolation from external environmental factors (water, dust, humidity..etc.), which have been forwarded to Intertek for testing. Boxes and connector built by Amphenol are shown in Figure 131. Pockets have been molded to house the large components in order to reduce the weight of the box when potted. The final panel assembly sequence is shown in Figure 132

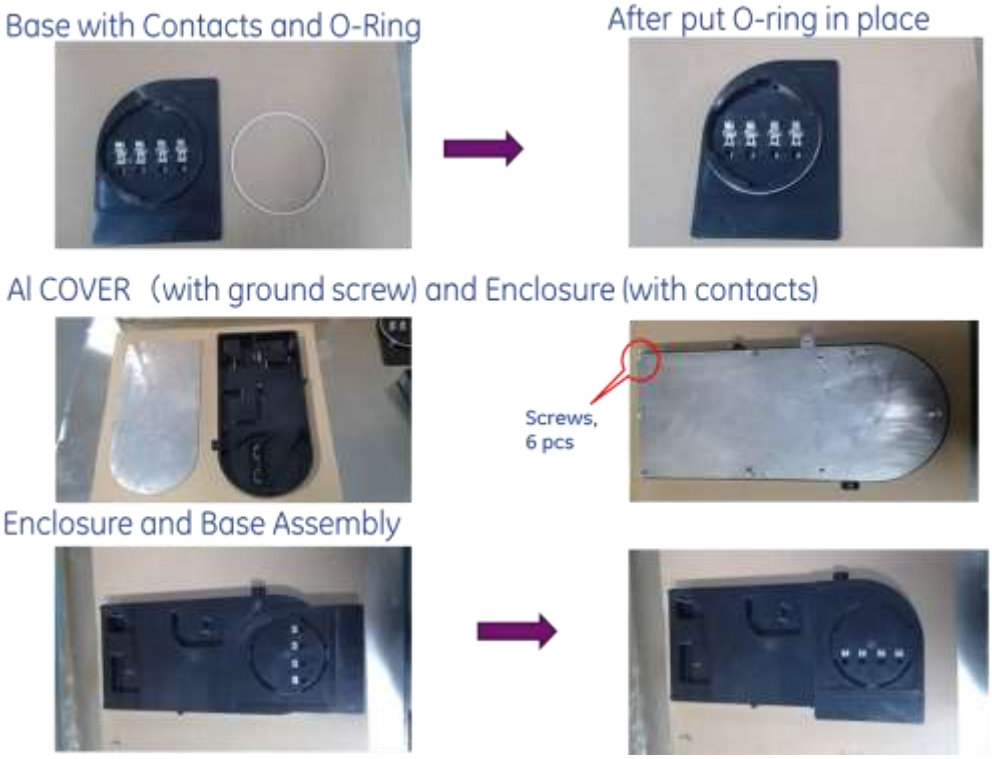


Figure 131: Pocketed inverter boxes and panel connector from Amphenol

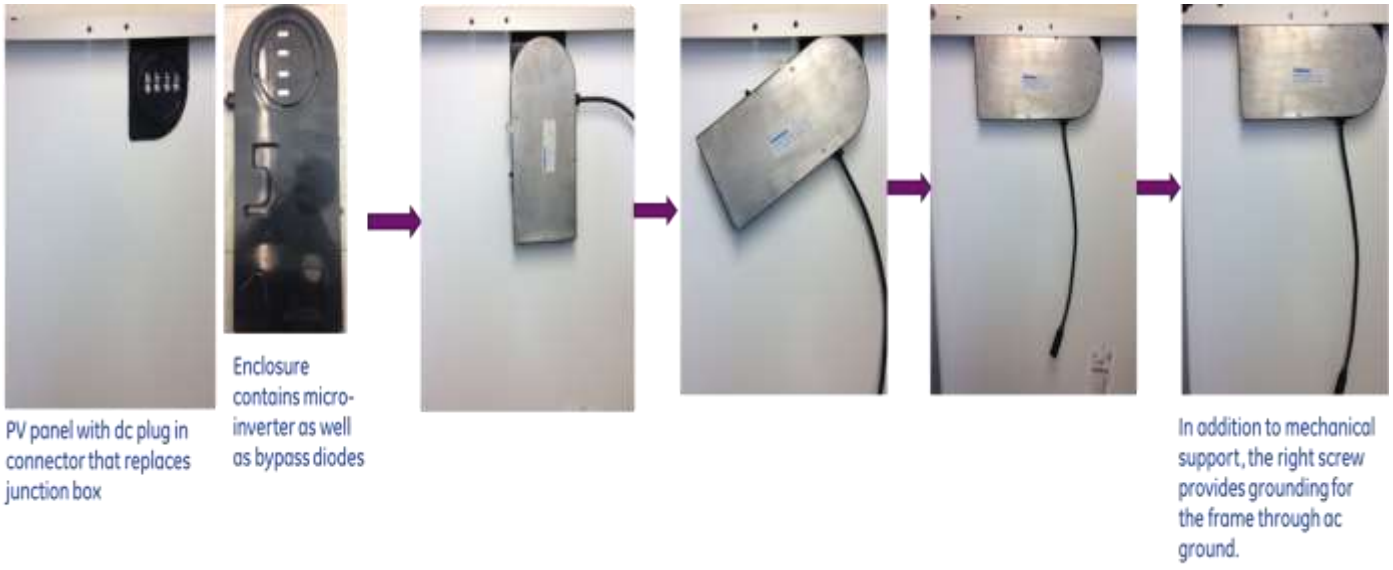


Figure 132: Final ACPV panel assembly with Motech panel

3.2.7.2 Compatibility with other panel manufacturers

The panel dimensions play a key role in this design as the inverter has to fit under the panel frame and the terminals of the panel have to be at the correct location to be able to reach the spring connectors in the panel back connector. Figure 133 shows the minimum dimensions of panel frame and distance between connector and frame and diameter of connector, that if met this design can be directly used. Several panel manufacturers have been identified where these dimensions apply as shown in Figure 134.

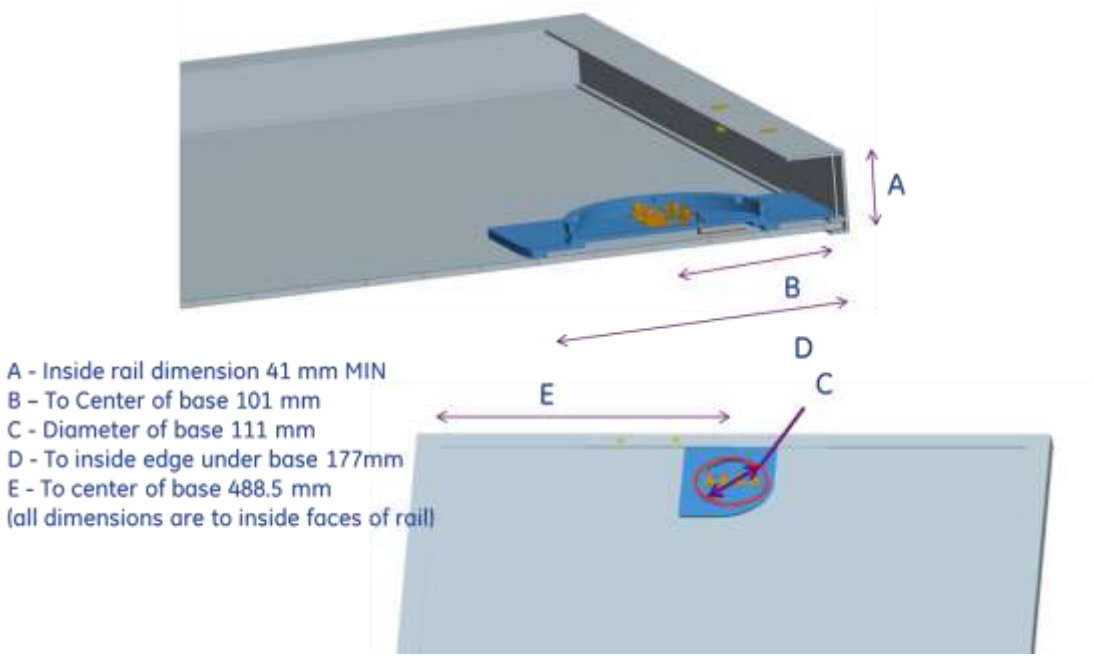


Figure 133: Minimum dimensions needed for Integration with Other PV panels

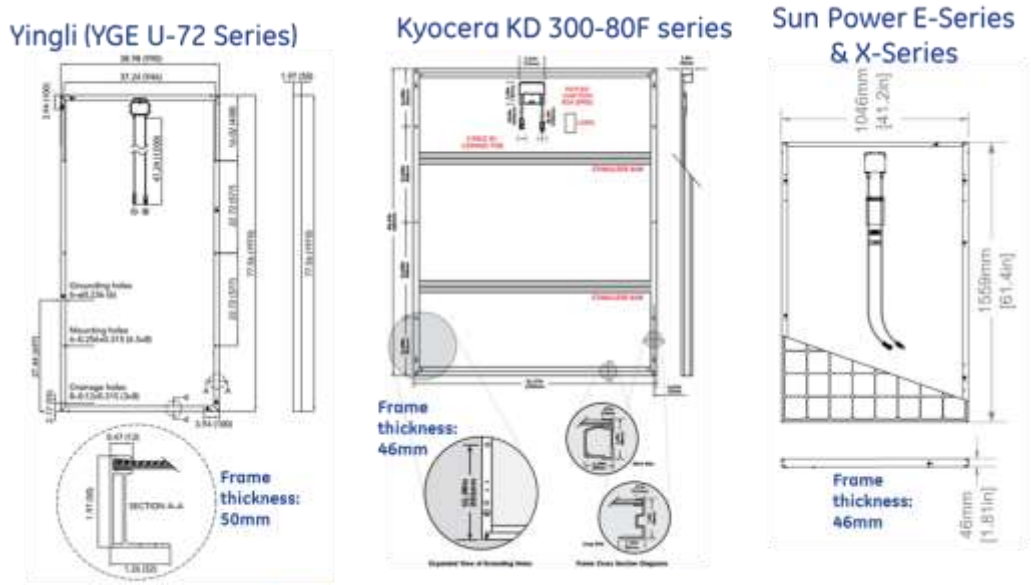


Figure 134: Examples of other PV Panels that Can Directly Integrate with the Designed Connector

3.2.7.3 Testing at Intertek

Four tests out of the UL 1741/1703 standard were identified to be performed at Intertek to test the integrity of the ACPV panel design.

1. Temperature and humidity cycling test
2. Rain and sprinkle test and water submersion test
3. Shear force test
4. Strain relief test

Figure 135 shows a block diagram summary of these tests.

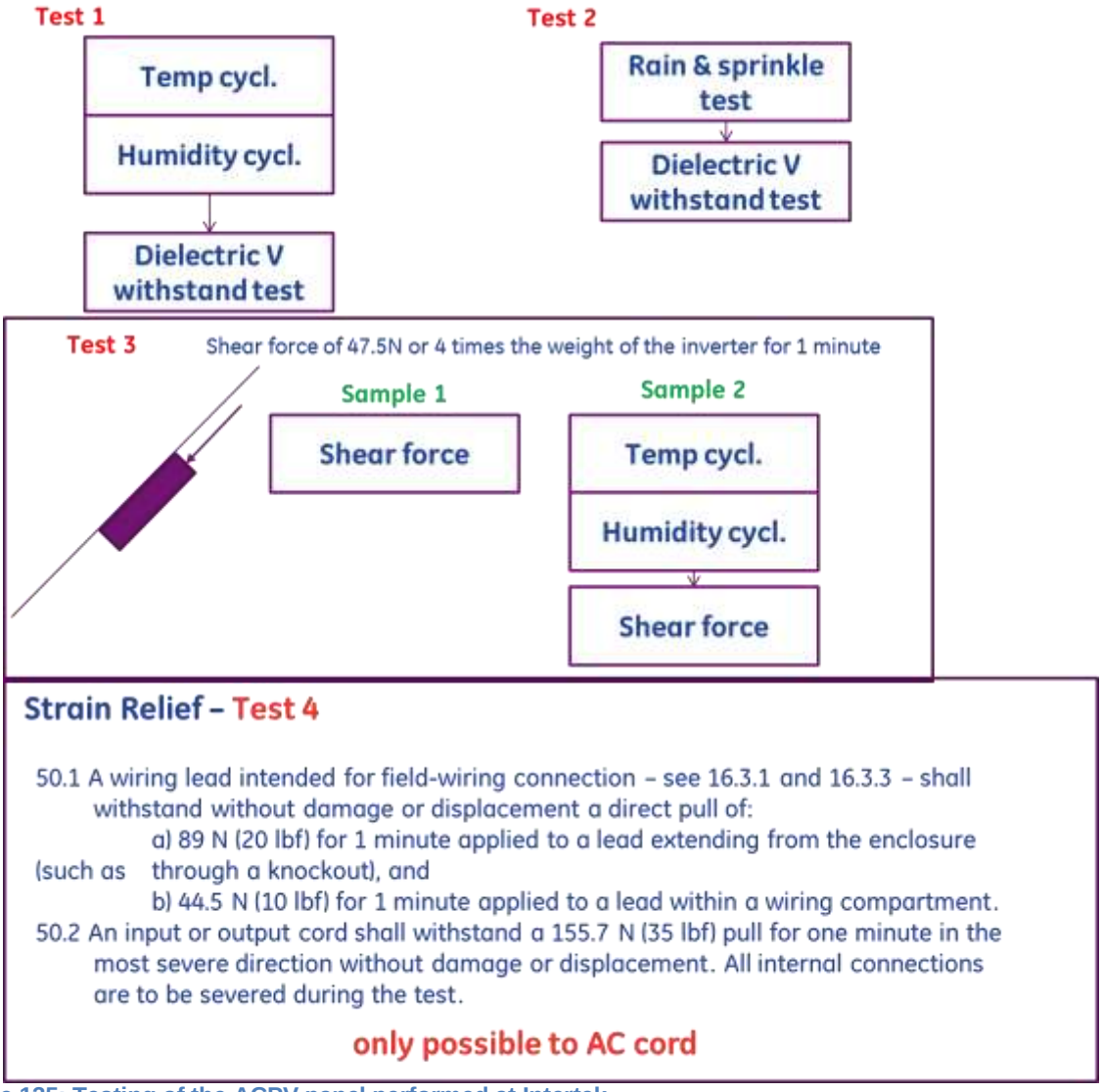


Figure 135: Testing of the ACPV panel performed at Intertek

The primary target of this testing was to verify the performance of the potted units. The unpotted units were being assessed to see the potential of weight reduction.

Test 1: Wiring Compartment Securement Test

Was performed on all 4 panels. Two panels have gone through humidity/thermal cycling and two panels have not.

Results show that all four panels passed the test.

Test 2: Shear Force Test

Similar to test 1 all four panels went through the test, two after humidity/thermal cycling and two without going through the humidity cycling.
Results show all four panels passed the test.

Dielectric Test:

A voltage of 1480Vac was applied between ac line and ground for all micro inverters and held for 60 seconds.
Potted units passed the test.
Unpotted units failed the test.

Test 3: Rain and Sprinkle Test:

This test was performed on two panels: one potted panel and one unspotted panel. Dielectric test was performed on the panels before and after the test indicating no degradation. The potted unit passed and the unspotted unit showed the same performance as was shown in the dielectric test before the rain and sprinkle test. This indicates that the dc connection and micro-inverter enclosure do not allow any water leakage that may affect the dielectric strength.

Test 4: Humidity and Thermal Cycling

The humidity was cycled from 0% to 85% and temperature was cycled from -60C to 85C in each cycle. This was repeated for 10 cycles over 10 days. Two units were put through this test: 1 with potting and one without potting. A dielectric test was performed before and after the test.
Results of the test were as follows:
Potted unit:
Passed dielectric test before test but insulation degraded and could not withstand the 60s period after test.
Unpotted unit did not pass the dielectric test before the test and did not show further degradation after.
Assessment of the dielectric test performance and resolution of issues that were observed:
A larger package of inverter switch (IPD65R660CFD) were used in this test bringing the terminals close to the ground plate of the micro-inverter, which explains the arc flash failure in the dielectric test. This was verified through a hi-pot test we ran in the lab.

- ➔ Resolution: these devices were being used as a temporary substitute due to the long lead on the device originally chosen (IPD65R950CFD), which has a smaller package and will be used in the final design.

Similar to the HALT test, the relay is expected to have degraded significantly as it has a smaller temperature range.

- ➔ Resolution: the relay selected after HALT testing will be used in the final design.

The two potted units will be analyzed and the one that went through the humidity/thermal cycle will be compared to the one that has not to assess whether there has been any deformation or cracks in the potting material that led to dielectric degradation.

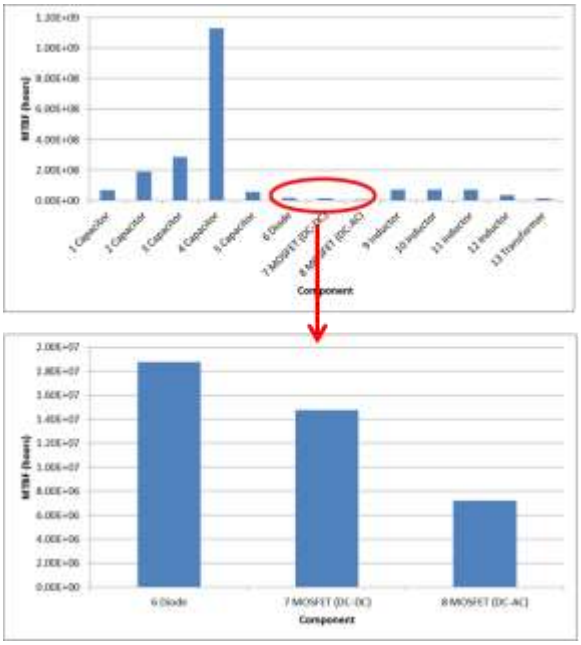
➔ If any irregularities are found in the potting it will be addressed with Amphenol to mitigate this issue in the final set of boards.

The dielectric breakdown test issue has been resolved as will be shown in section 3.2.9 for Task 9

3.2.8 Task 8: Review system compliance, reliability, manufacturability, and cost

3.2.8.1 Reliability Calculation

λ- Predict was used to predict the power circuit reliability according to Telecordia reliability model. The model is fed with component stresses (voltage, current and power) and the component rating. Based on normal operation of a PV micro-inverter (average of 8 hour working time at different power levels (25%, 70% and 100%) and at nominal, minimum and maximum voltages (22V, 28V and 40V), the probability of achieving 20 year lifetime is > 97.44%. the least reliable components are the MOSFETs and diodes as shown in Figure 136.



Board	Power	MTBF (hrs)	Goal (hrs)	% Reliability
PowerBoard 23V	25%	3.13E+06	58440	98.1
PowerBoard 23V	70%	2.76E+06	58440	97.9
PowerBoard 23V	100%	2.29E+06	58440	97.4
PowerBoard 28V	25%	3.13E+06	58440	98.1
PowerBoard 28V	70%	2.75E+06	58440	97.9
PowerBoard 28V	100%	2.25E+06	58440	97.4
PowerBoard 40V	25%	3.11E+06	58440	98.1
PowerBoard 40V	70%	2.79E+06	58440	97.9
PowerBoard 40V	100%	2.44E+06	58440	97.6

Figure 136: Reliability analysis of low voltage micro-inverter

3.2.8.1 Highly accelerated life test (HALT) of micro-inverter

HALT testing was performed in order to expose the micro-inverter to high electrical, thermal and mechanical stresses to verify weak links and move toward product readiness. Two micro-inverter units were built and placed in 3D-printed enclosures, along with multiple thermal sensors. The control code was flashed to the DSP control card and the units were tested to verify operation in the lab.

The Highly Accelerated Life Test (HALT) document was prepared following the guidelines of telecommunication converter reliability testing (IPC-9592A). The team worked with GE Critical Power to adapt the test sequence to fit the micro-inverter application and a test setup was prepared at GE Critical Power. Test setup is shown in Figure 137. The micro-

inverter units used for the test are shown in Figure 138, each micro-inverter was equipped with thermal sensors around the hottest spots identified on the circuit board (inverter MOSFETs and DC/DC converter rectifier diodes)

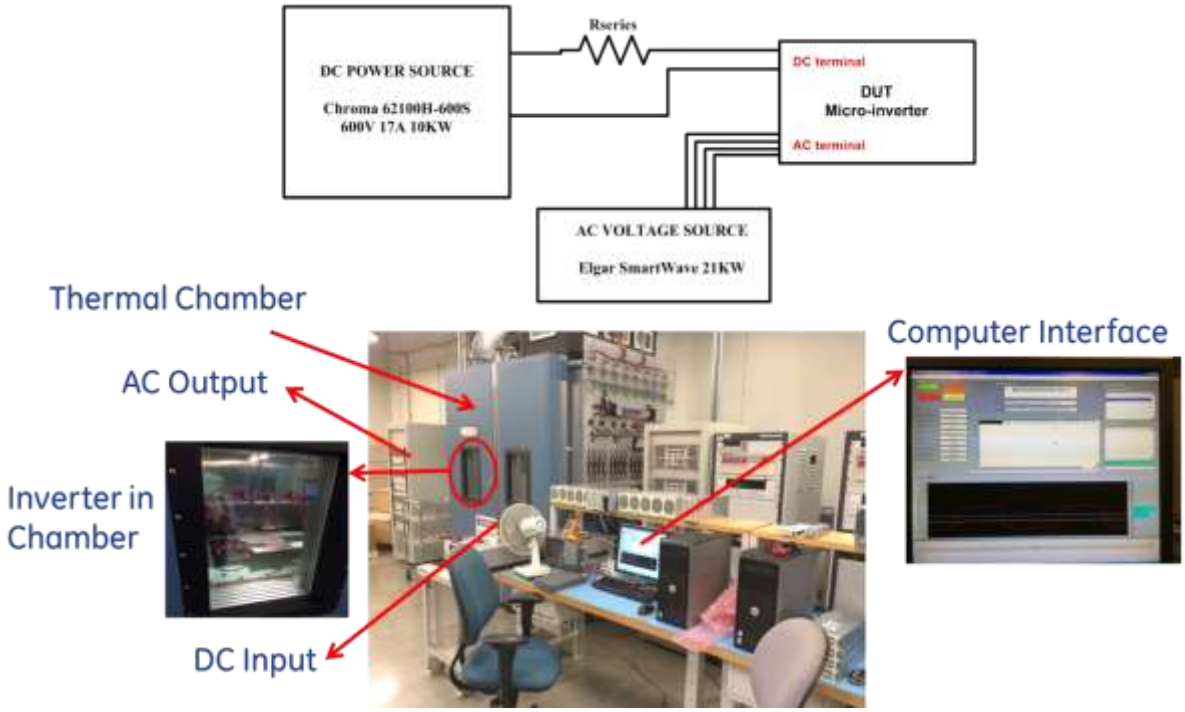


Figure 137: HALT setup

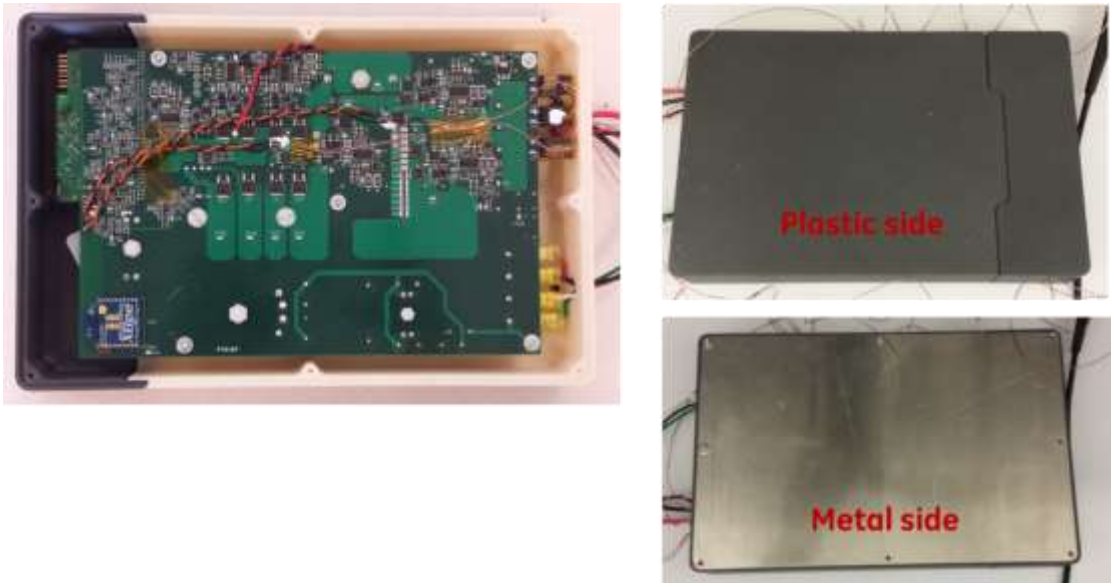


Figure 138: Micro-inverter samples used for HALT

A set of seven tests were planned, four of which are non-destructive tests and the last three were destructive tests. The test plan was as follows:

1. Rapid thermal cycling (non-destructive): where the units were operated with no vibration between the thermal lower operating limit (LOL)+10^{o}C (-30^{o}C) and the

thermal upper operating limit (UOL)-10ºC (55ºC) at the maximum possible thermal transition at half rated power and at full rated power. Both units passed the test.

- Test was performed for a total time period of 12.5hrs
- Full power applied to the input and 240Vac output voltage.
- The temperature of the resonant converter rectifier diode and that of an inverter MOSFET are monitored and the temperature span detected was (12.5ºC →74.2ºC for the diode and 4.3ºC → 69.5ºC for the MOSFET)
- The micro-inverter passed the test for a longer duration than required

  Temperatures of the different components are shown in Figure 139.

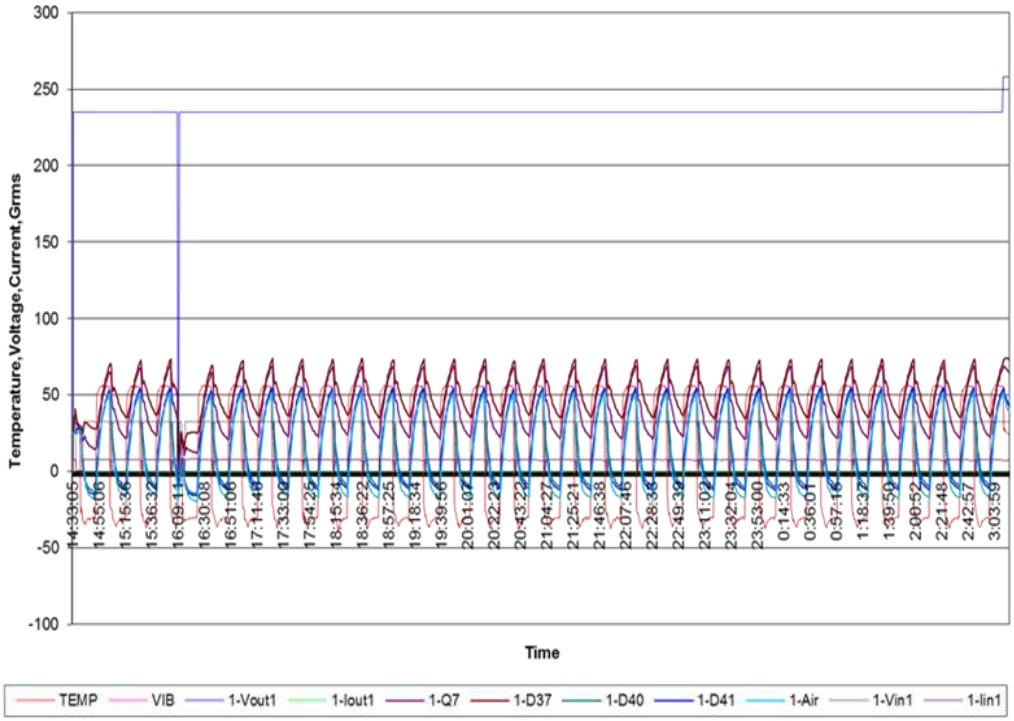


Figure 139: Rapid Thermal Cycling Test Results

2. Output voltage HALT (non-destructive): consists of decreasing and increasing the output voltage in order to find the minimum and maximum operating and destructive limits. Both boards passed the test and the protection circuitry was able to isolate the converter as soon as the voltage went outside the specified operating limits (211V-264V). However, chattering was observed around the lower voltage limit, which will be addressed in the control code.

   Experimental results for this test were obtained over a period of over 16hrs for the 3 temperatures (-35ºC, 25ºC and 60ºC) rather than 10hrs. Rated input power was applied and an additional step up ramp was added after segment #1 in the output voltage profile, which added more stress on the micro-inverter. Figure 140 shows the test results.

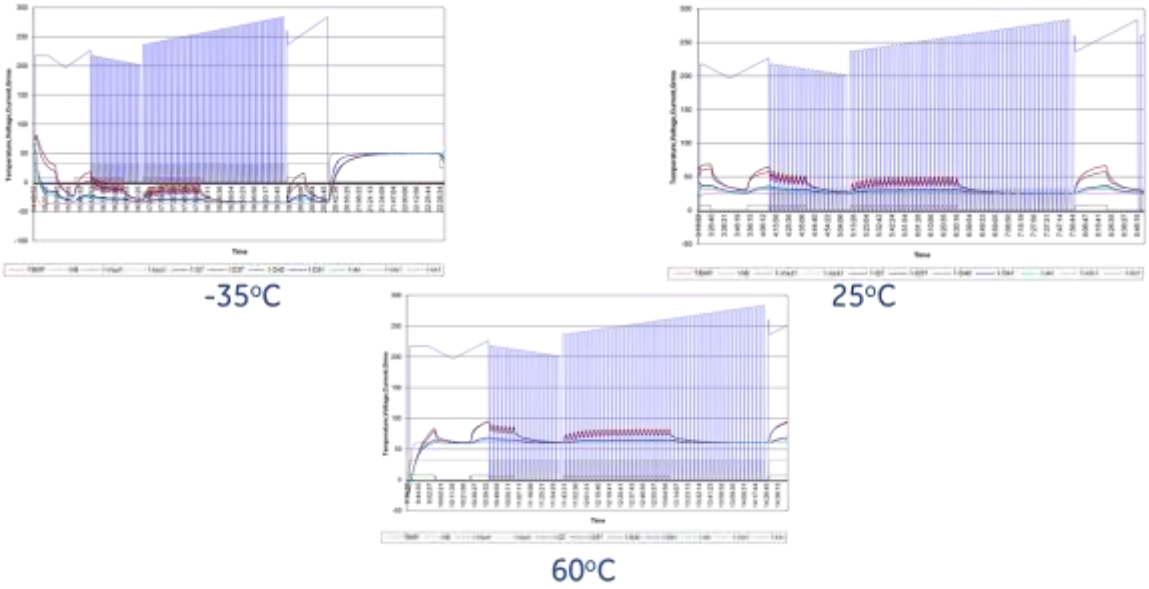


Figure 140: Output Voltage HALT Test Results

3. Temperature step stress (non-destructive): the temperature is stepped from LOL to UOL along with input power transition from no-load to full-load. The thermal protection is enabled during this test. The micro-inverter passed the test.

   This test was split in two phases. First a test with ambient temperature rising from 55°C to 75°C was performed at half power and then at full power. The following step is repeating the test for a temperature range of 75°C to 85°C to find the destruct limit of the micro-inverter. The micro-inverter passed temperature HALT at full power at 10°C above rated temperature. Test results are shown in Figure 141.

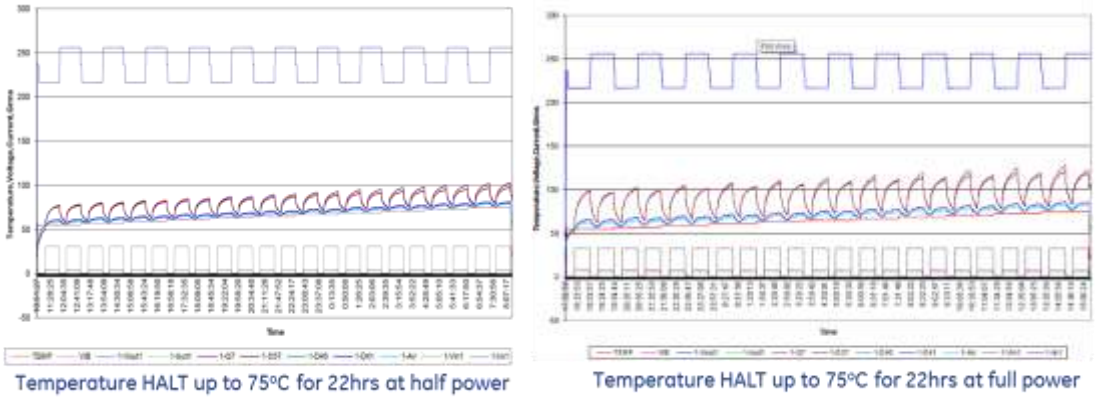


Figure 141: Temperature HALT Test Results

4. Short circuit HALT (non-destructive): This test was performed in the lab at GRC due to difficulties setting it up at GE Critical Power. Multiple output short circuits were applied to the micro-inverter and the protection circuitry successfully isolated the unit under test.

5. Temperature HALT (destructive): The objective of this test is to determine the operating and destruct limits. Any over temperature protections on the unit under test will be disabled in order to identify the component(s) or circuits that may be damaged due to excessive temperature. Micro-inverter board was damaged at 77ºC (UOL+12ºC), damaged components agree with the thermal stress results obtained in the lab. In addition to that, the relay, which was identified to be rated for a maximum ambient temperature of only 60ºC, need to be replaced with higher temperature rated part.

   Micro-inverter passed temperature HALT at half power at 20ºC above rated temperature. Boundary limit for ambient temperature identified at full power at 12ºC above rated. Figure 142 shows the test results and Figure 143 shows the damage to the board after thermal HALT.

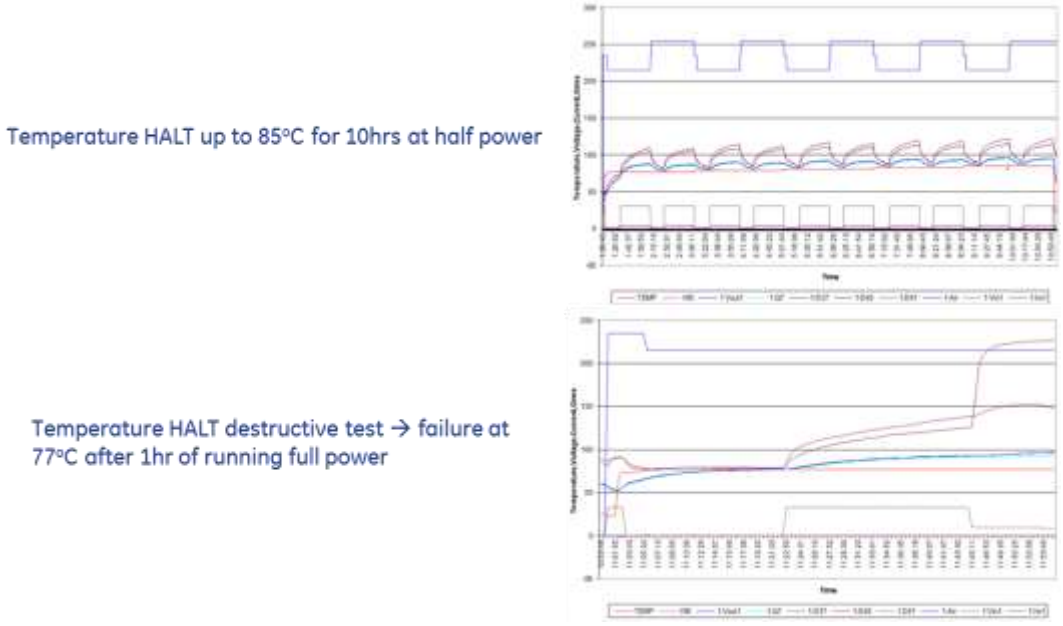


Figure 142: Temperature HALT (Destructive Test)

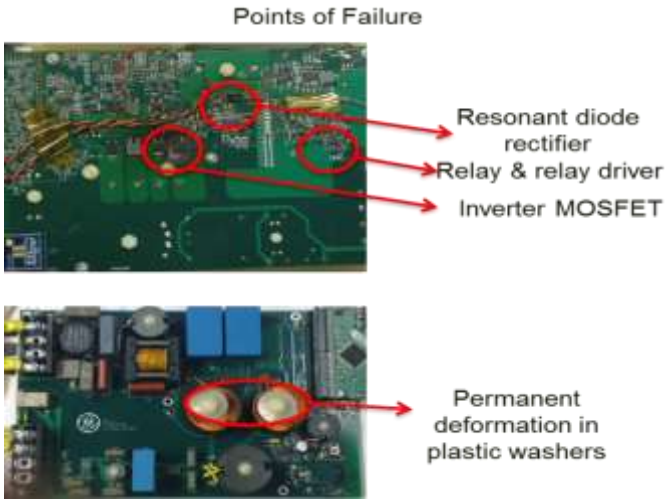


Figure 143: Points of damage after destructive test

6. Vibration HALT (destructive): was not performed due to board damage in test 5. However, mechanical weak points were identified in the shipping process of the units, where the nylon screws sheared off. Input from GE Critical Power engineers on methods to improve mechanical sturdiness of the board was provided.
7. Combined stress HALT (destructive): not performed due to board damage in test 5.

Table 28 shows a summary of the tests and their outcomes.

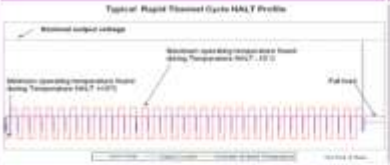
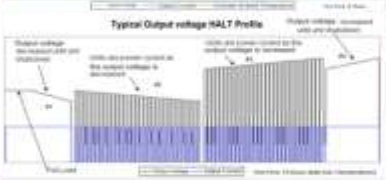
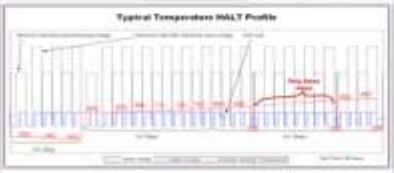
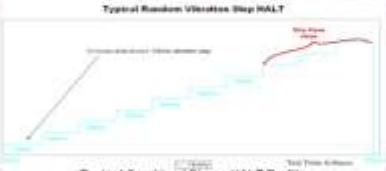
The following concluding remarks can be made after HALT was completed:

- Micro-inverter prototype was successfully run at the maximum limits of its specifications and proved that there is additional margin on top as well.
- Minor component changes were identified to push the operating limit to 85^{o}C and add more mechanical support.

Changes to be made as a result of HALT are:

- Relay with higher temperature rating is selected (DSP2a-DC12V changed to G5LA-1 DC12 to withstand 85^{o}C)
- Pull down resistors added to all logic signal lines to avoid misfiring of devices or false turn on command to relay at startup
- Large components to be glued down to provide added mechanical sturdiness. Potting will also help with mechanical support.
- Diode to be changed to larger package to improve thermal management (MURS360T3G (package SMC) changed to SCS210AJTLL (package TO-263))
- Hysteresis band added at voltage trip limits.

Table 28: Summary of HALT and micro-inverter performance

	Test	Description	Profile	Status
1	Rapid Thermal Cycling	Rapid Thermal Cycle HALT consists of operating the device with no vibration between the thermal LOL+10°C (-30°C) and the thermal UOL-10°C (55°C) at the maximum possible thermal transition		Passed
2	Output Voltage HALT	The Output Voltage HALT consists of decreasing and increasing the output voltage in order to find the minimum and maximum operating and destructive limits.		Passed
3	Temperature Step Stress	The objective of the Temperature HALT test is to determine the operating and possibly the destruct limits. Since the protection circuits are enabled, the unit under test should shut down at the over temperature condition and remain undamaged.		Passed
4	Short Circuit HALT	The Short Circuit HALT test consists of applying a series of short circuits at no load and full load. A total of ten shorts are applied, at no load, within a four-minute window.		Passed
5	Temperature HALT	The objective of the Temperature HALT, with the protection circuit disabled, is to determine the operating and destruct limits. Any over temperature protections on the unit under test will be disabled in order to identify the component(s) or circuits that may be damaged due to excessive temperature.		•Passed at half power up to 85°C •Passed test at full power up to 75°C •Failed at final test at 77°C st full power
6	Vibration HALT	Random Vibration Step HALT consists operating the device under test at 25°C ambient and starting at no vibration. The vibration is incremented until the device under test fails or the chamber maximum vibration is reached.		Not performed due to failure in test 5
7	Combined Stress HALT Test	The Combined Stress Test operates the device under test while combining the environmental effects of random vibration and rapid thermal cycling along with Output Voltage and Output Load transients. The objective of the Combined Stress HALT is to stress the product mechanically and determine the operating and destruct limits.		Not performed due to failure in test 5

3.2.8.3 Cost and manufacturability analysis

This analysis was done in collaboration with Flextronics and Amphenol for the electronic circuit and mechanical parts, respectively.

Assumptions

- Costing was made assuming production volume of 250,000 units/year
- Material cost corresponds to purchasing price of components (electronic or mechanical)
- Price of each reference is realized on the basis of catalogues, CDs, websites of component manufacturers and distributors. It was often necessary to ask for specific quotations for some parts.

- Prices are based on quantity
- PCB cost varies according to the technology used and size of board
- The manufacturing time takes into account the set up time of each equipment

The costing of micro-inverter and enclosure is expected to meet the project target of **¢ 25 /W.** This cost number achieves the overall system installed cost of $\leq$ **$ 3/W**

3.2.8.4 SAFETY: Ground fault protection & Arc fault protection

- System design assures the detection of ground faults, indication that the fault has occurred, and interruption of the current flow, as well as communication to the micro-inverters to stop producing power
- In the event of the ground fault, the micro-inverter will locally annunciate the error and communicate its status to the other micro-inverters and to the central controller at the load center
- All micro-inverters will go in a stand-by mode until the ground fault is cleared
- The only way to reset the fault is by de-energizing the chain of micro-inverters, clearing the ground fault, and then reenergizing the chain of micro-inverters
- To comply with codes and standards each live active line from each of the micro-inverters is to be fused at each of the micro-inverter outputs
- In the present prototype disconnect is designed to brake the connection between the micro-inverter chain and the grid

Several fault scenarios were considered and simulated:

1. PV plus to ground
2. PV minus to ground
3. PV plus to minus
4. DC bus to ground
5. DC bus to DC minus
6. Bridge output – point A to ground
7. Bridge output – point B to ground

In these fault conditions the following protection options were assessed:

1. Baseline no protection control or relay
2. Only protection via control
3. Protection control and relay

Figure 144 shows the different locations of faults that were simulated. Simulation waveforms for different faults and different protection methods are shown in Appendix A.

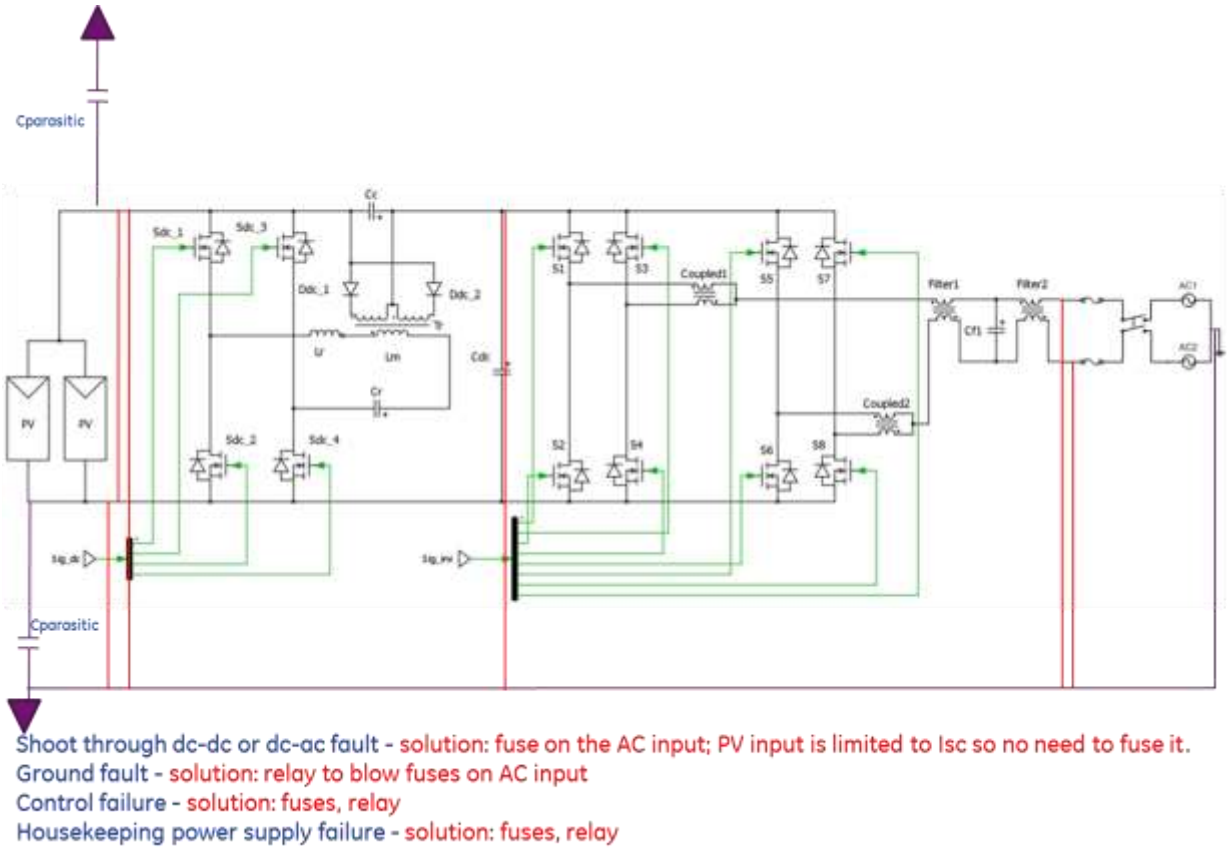


Figure 144: Model used to analyze fault conditions

3.2.9 Task 9: Design, Build and Install Pilot Demonstration Systems

This task is the one of two tasks planned for Phase 3 of the project. Two field demonstrations have been planned for this task: the first site is in Schenectady, NY and the second is at SolarWorld site in Hillsboro, OR. In preparation for this demonstration three major subtasks were addressed here: building a revised converter based on the issues identified in Phase 2 and reduce the size of the board. The second is to update the enclosure design and adapt the ACPV panel integration method to a SolarWorld panel, and finally, the third sub-task is to setup and test the communication system for an array of 10 panels.

3.2.9.1 Converter board revision and build

During the UL 1703 testing, high leakage current and occasional HV breakdown was observed. The test result was replicated in the lab as shown in Figure 145. It was observed that the current would rise linearly with the applied voltage and based on the current and voltage levels the impedance seen by the source is approximately 800kΩ per line. This issue was found to be a result of the line side AC voltage feedback circuit, shown in Figure 146 where the resistor values were not high enough, which leads to the high leakage. The resistor packages were also found to be too small, therefore they cannot withstand the high voltage requirement (1480 VAC) of the UL testing. Therefore, the resistors were changed from (200kΩ each) to (1MΩ) each and a larger package with higher voltage withstand was selected. With these changes the micro-inverter was

exposed to the high voltage test again and passed the 60s withstand requirement of 1480VAC, as shown in Figure 147. Control performance was verified not to be affected by the resistor value change.

Figure 145: Ground leakage current test setup and test result at 1480VAC

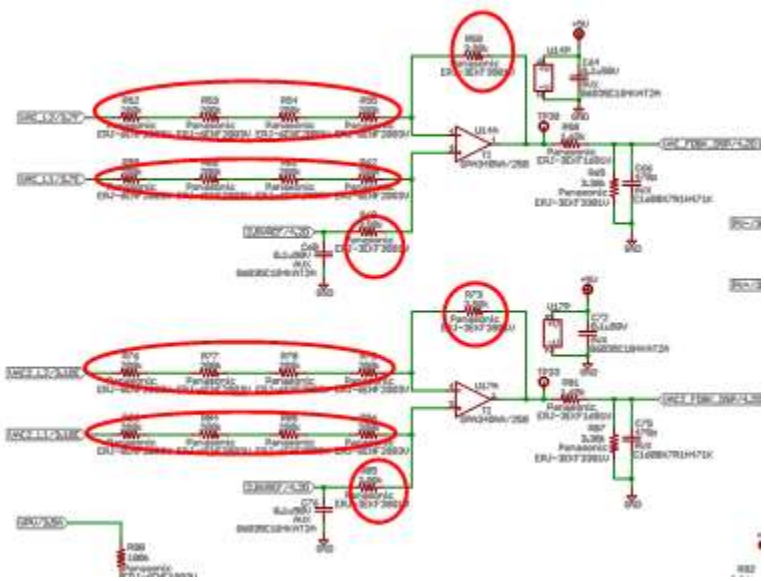


Figure 146: Feedback resistor changes

Figure 147: Dielectric test after modifying resistors - unit passes

The building of second revision of micro-inverter boards was completed and the boards were fully assembled. The micro-inverter board is shown in Figure 148.

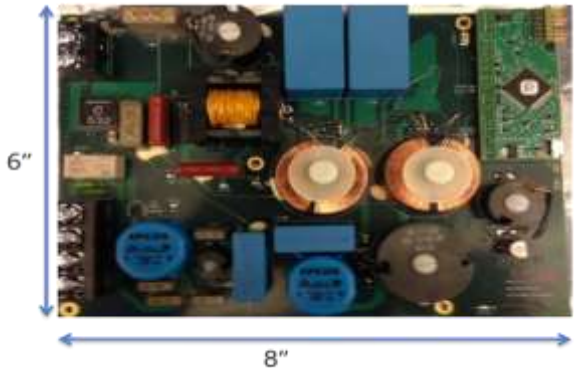


Figure 148: Revised micro-inverter board

The micro-inverter boards were tested as follows:

Test 1: Check Bias Power Supply Voltage.

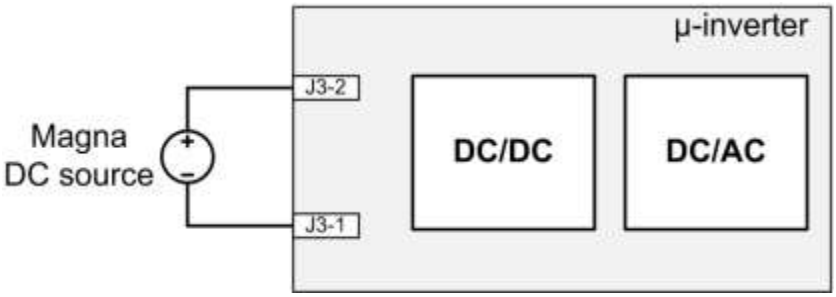


Figure 149: Test setup for power supply voltage test

Step 1. Connect the magna dc source to the board input pin. Use two meters to exam +12v, +5v and +3.3v pin on the board. +3.3V pin on the board is TP64. +5V pin on the board is TP66. +12V pin on the board is TP63.
Step2. Gradually increase the output voltage to 30V. Check the meters readings.
Table 29 is the result from no. 1 board.
Note: the +12V pin reading range should be 11.5V to 14V. The +5 pin reading range should be 4.91V to +5V. The +3.3V pin reading range should be 3.300V to 3.309V.

Table 29: Measured power supply voltage levels

PIN	+3.3V	+5	+12V
Meter readings	3.306V	+4.962V	+12.81V

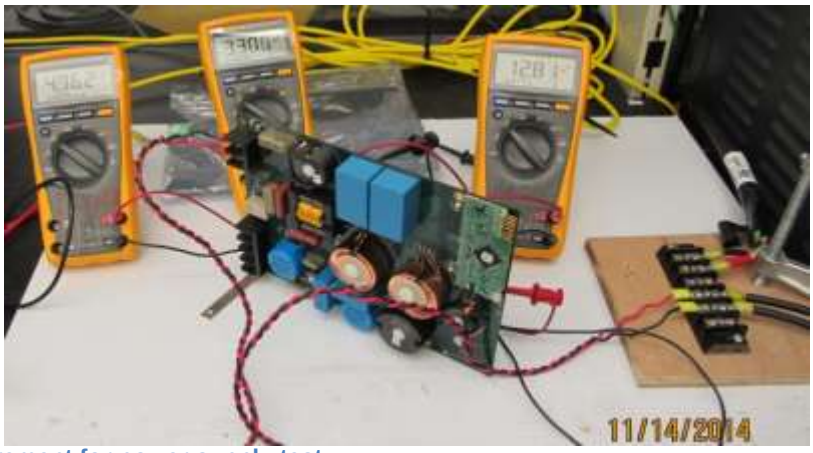


Figure 150: Measurement for power supply test.

Test 2: Check DC/DC and DC/AC converter PWM signal

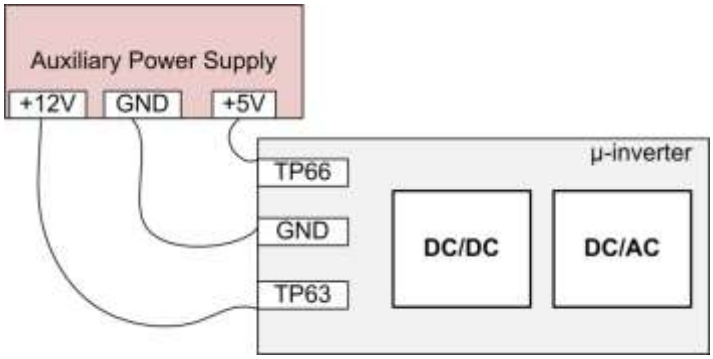


Figure 151: Test setup for gating signal test

Step 1. Connect the external +5V and +12v to the board. +5V pin on the board is TP66. +12V pin on the board is TP63.
Step 2. Check the gating signals one by one.
Results:

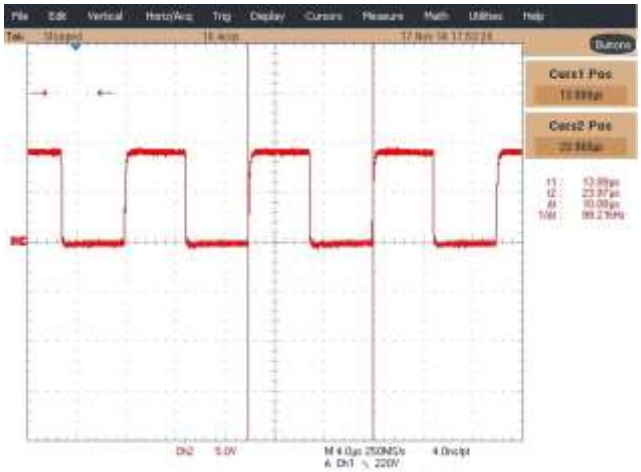


Figure 152: DC-DC converter gating signal. The duty cycle is 50%. The high and low voltage is 10V and 0V, respectively. The switching frequency is 100kHz

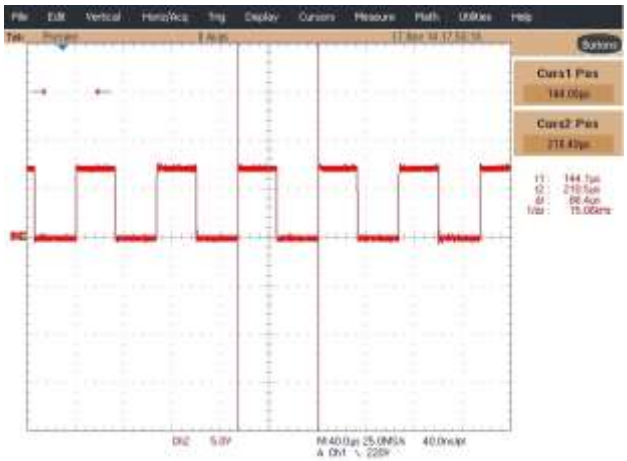


Figure 153: DC-AC converter gating signal. The duty cycle is 50%. The high and low voltage is 7V and 0V, respectively. The switching frequency is 15kHz

Test 3: DC/DC converter closed-loop test with constant voltage load

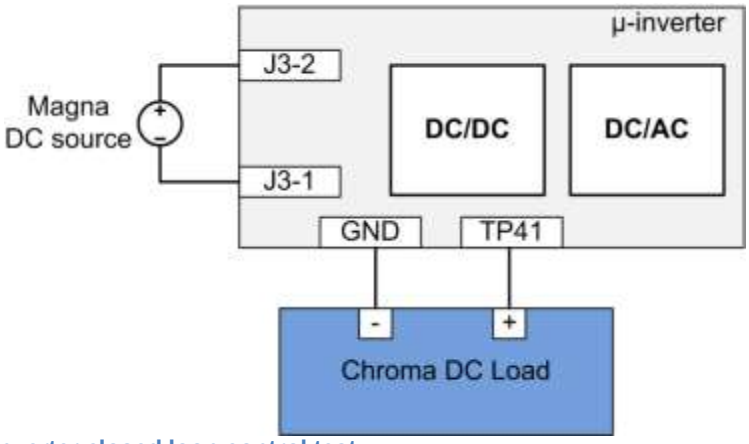


Figure 154: DC/DC converter closed loop control test

Step 1. Connect the magna dc source to the board input pin (J3-1 and J3-2). Connect the dc load to pin TP41 and GND pin. Connect one meter to monitor the dc bus voltage. The meter can be connected to pin TP41 and GND pin.
Step 2. Set up the Chroma dc load to constant voltage load. The voltage is set to 400V.
Step 3. Check the meter readings. The meter reading should be 398V.
Results:

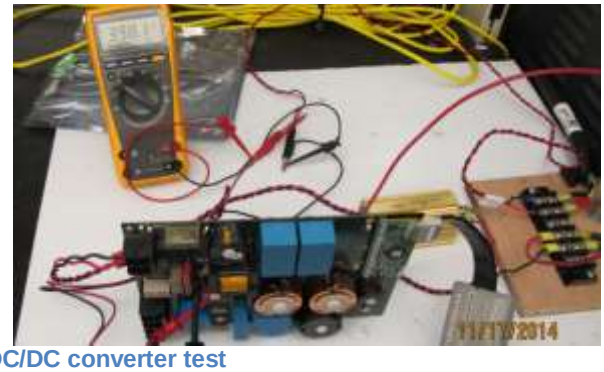


Figure 155: Test result for DC/DC converter test

Test 4: DC/AC converter open-loop test with resistive load

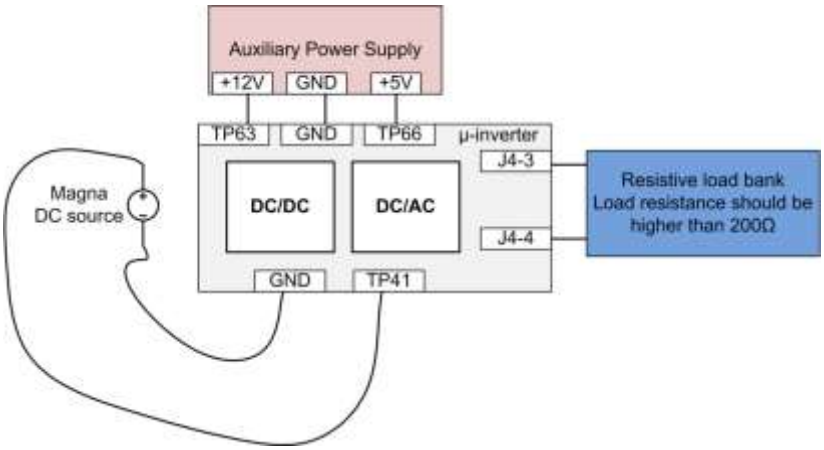


Figure 156: Test setup for inverter stage test

Step 1. Connect the magna dc source positive rail to pin TP41 and negative rail to the GND pin. Connect the board J4-3 and J4-4 to the load. The load resistance can not be higher than 200Ω. Connect the current probe to measure the load current.
Step 2. Connect the external +5V and +12v to the board. +5V pin on the board is TP66. +12V pin on the board is TP63.
Step 3. Gradually increase the magna dc power supply voltage from 0 to 400V. Monitor the load current by checking if it is a 60Hz sinusoidal waveform or not.
Results:

Figure 157: Inverter output current. The frequency is 60Hz. The current amplitude should be increased when gradually increasing the input voltage

Test 5: The micro-inverter whole system closed-loop test

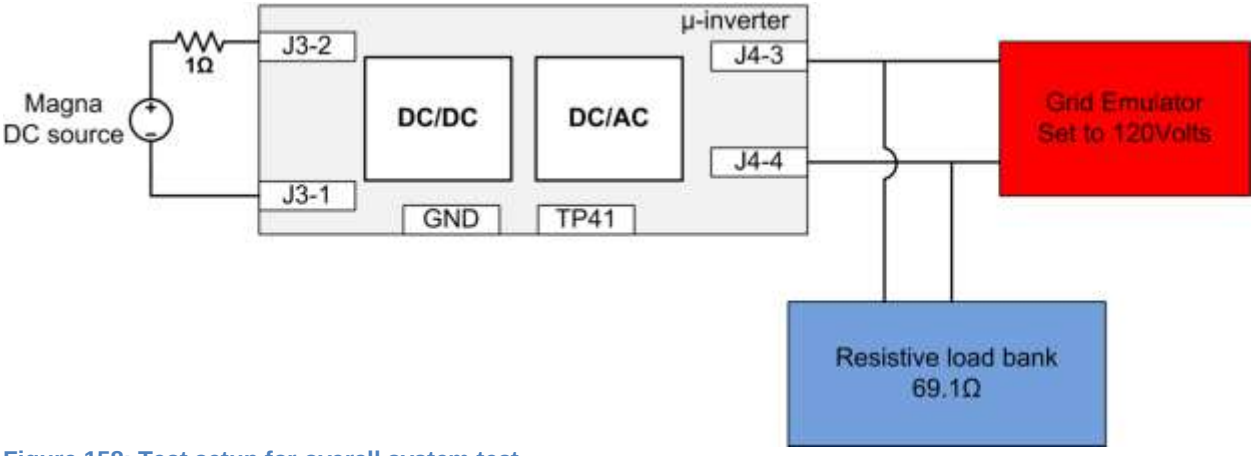


Figure 158: Test setup for overall system test

Step 1. Connect the magna dc source positive rail to J3-2 and negative rail to J3-1. Connect the board J4-3 and J4-4 to the load and emulator. The load resistance is set to 69.1Ω.
Step 2. Connect the current probe to measure the load current. Connect the voltage probe to pin TP41 and GND to measure the dc-bus voltage.
The converter efficiency is shown in Figure 160, the peak efficiency is 96.1% and CEC efficiency 95.4%.

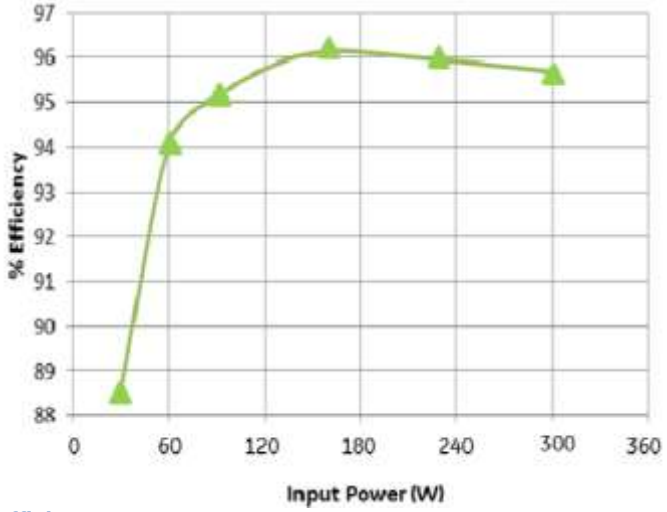


Figure 159: Micro-inverter efficiency

3.2.9.2 Reducing inverter board size

The micro-inverter board size has been reduced compared to the previous revision by 11.1%. Further reduction could have been made had a major layout change been made, but this would have required a much longer time which would have affected the project schedule. As seen in Figure 149, the output filter and interleaving transformers take up a very large space on the printed circuit board.
In order to significantly reduce the size of the board the output filter size has to be reduced and this can only be achieved by increasing the switching frequency. However, a higher switching frequency will lead to significantly higher switching and reverse recovery losses.

Therefore, higher switching frequency can be achieved by either replacing the CoolMOS devices by wide bandgap devices such as GaN devices. The other option would be to have a soft switching inverter, which eliminates the reverse recovery losses and thus the switching frequency can be increased while still using CoolMOS devices. If the switching frequency is tripled, the filter will be reduced to one third its size.
For GaN devices, the losses will be significantly reduced compared to CoolMOS, as shown in Figure 160. At a switching frequency of 15kHz, the losses can be reduced to less than a quarter of its baseline value with CoolMOS devices. Two GaN devices were used in this comparison, one from Transphorm and one from GaN systems.

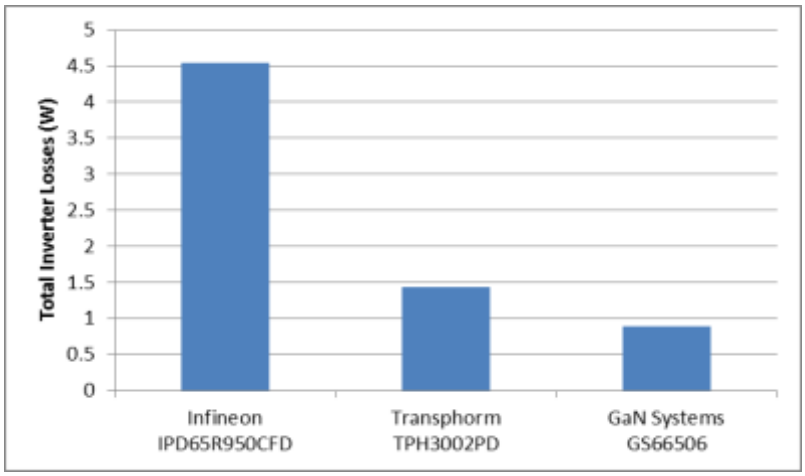


Figure 160: Loss comparison between GaN devices and CoolMOS devices at 15kHz

Alternatively the switching frequency can be raised up to 80kHz while maintaining the same inverter efficiency as shown in Figure 161. A 50kHz inverter was built as shown in Figure 162. The new inverter is 60% smaller than the inverter stage of the micro-inverter. Therefore, the overall micro-inverter board size can be reduced by 35% compared to the latest revision and 43% reduction compared to the revision in Phase2, while achieving the same efficiency.

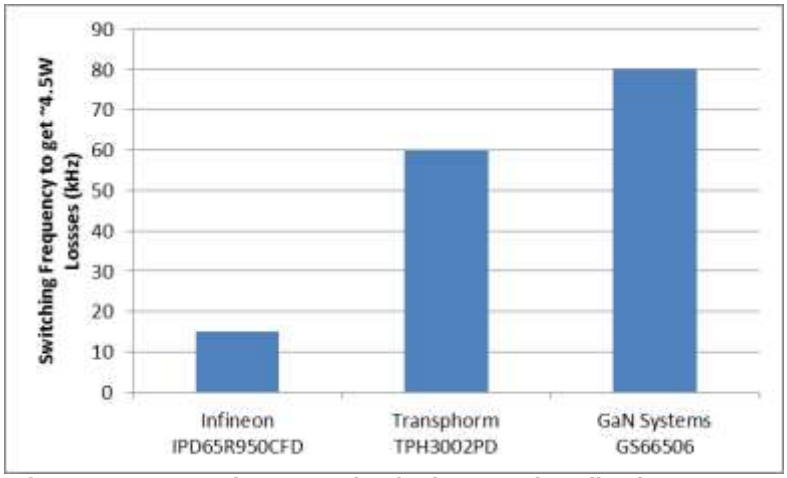


Figure 161: Switching frequency comparison to maintain the same baseline losses

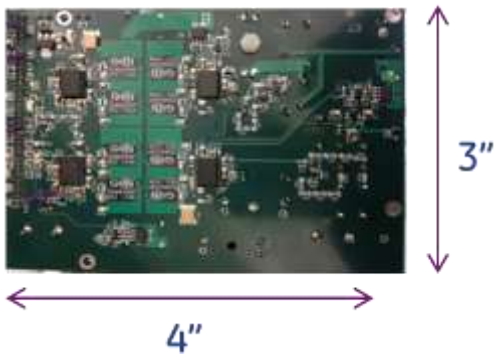


Figure 162: GaN inverter prototype

The other solution is to redesign the inverter control to achieve soft switching in order to eliminate the reverse recovery losses. The bulky inter-leaved inductors (L_{c1} and L_{c2}) are required to limit the circulation current. Those two inductors' cost is relatively high (15% of total cost). Based on the modulation signal, the phase shift angle φ can be controlled in a way which can always maintain the soft-switching conditions for all the switches.
The analysis shows that to main the soft-switching conditions, φ < min (D, 1-D). However, the optimized trace of φ needs more research. The key inverter waveforms are shown in Figure 163. This solution does **not** add any extra cost to the existing system. The further optimization conditions to track the optimized phase shift angle needs more research. The modified control flowchart is shown in Figure 164. Figure 165 shows a comparison between the baseline method and modified control indicating a much wider soft switching range. With proposed solution, the switching frequency can be pushed up to 50kHz. The estimated total loss is still smaller than the baseline. The estimated efficiency is 98.1% at 50kHz, the loss breakdown is shown in Figure 166.

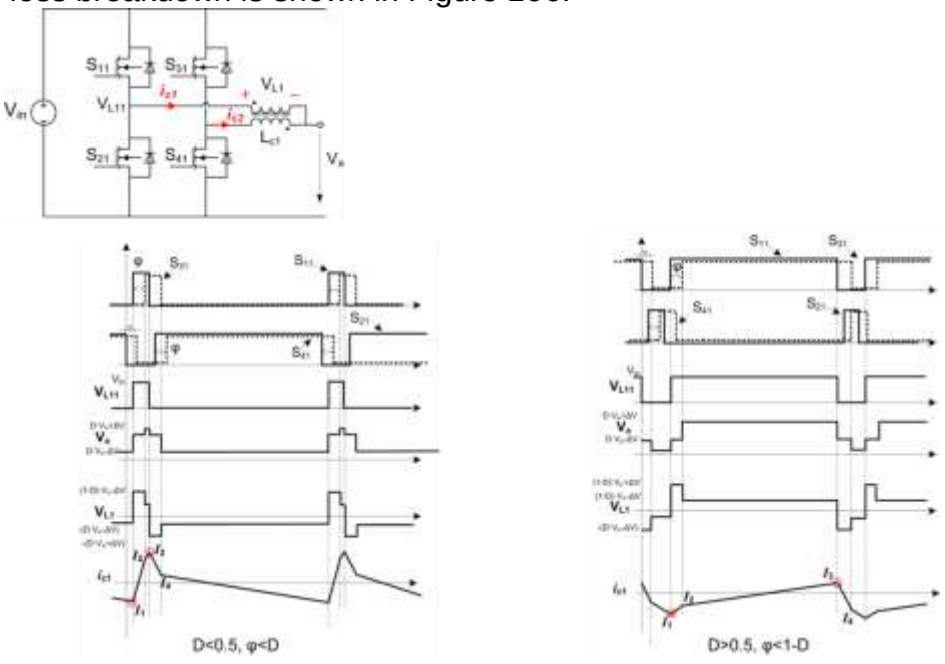


Figure 163: Key inverter waveforms for soft switching operation

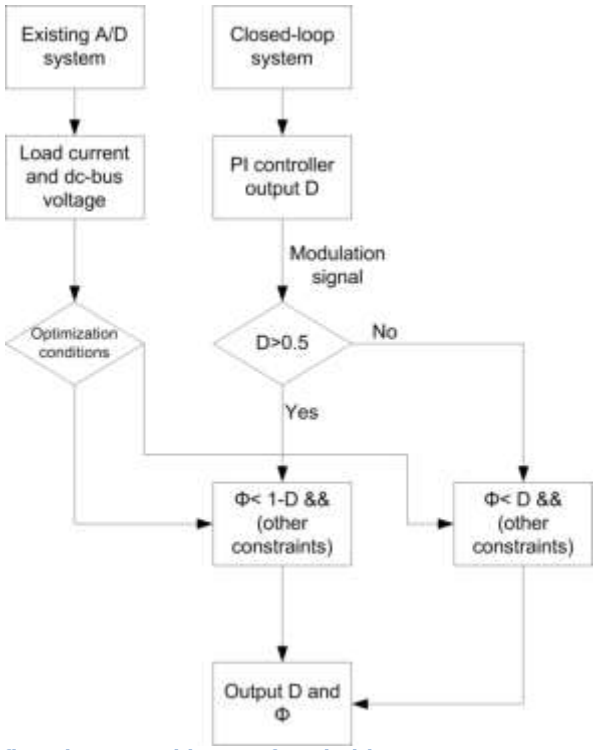


Figure 164: Modified control flowchart to achieve soft switching

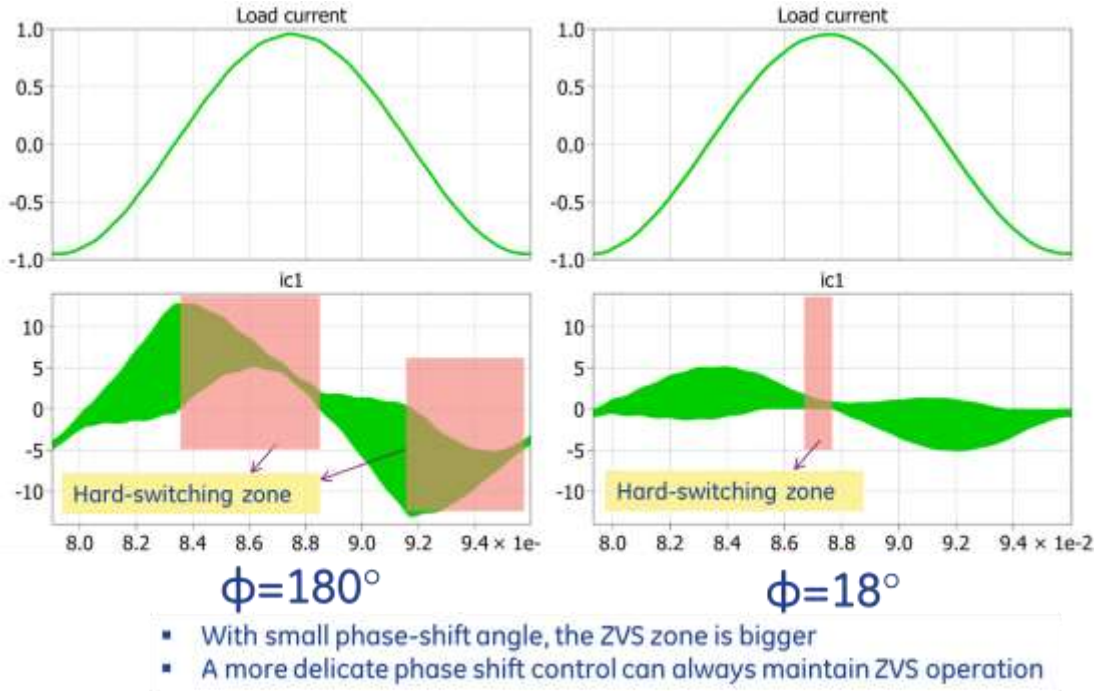


Figure 165: Simulation waveforms of baseline operation (left) and soft switching operation (right)

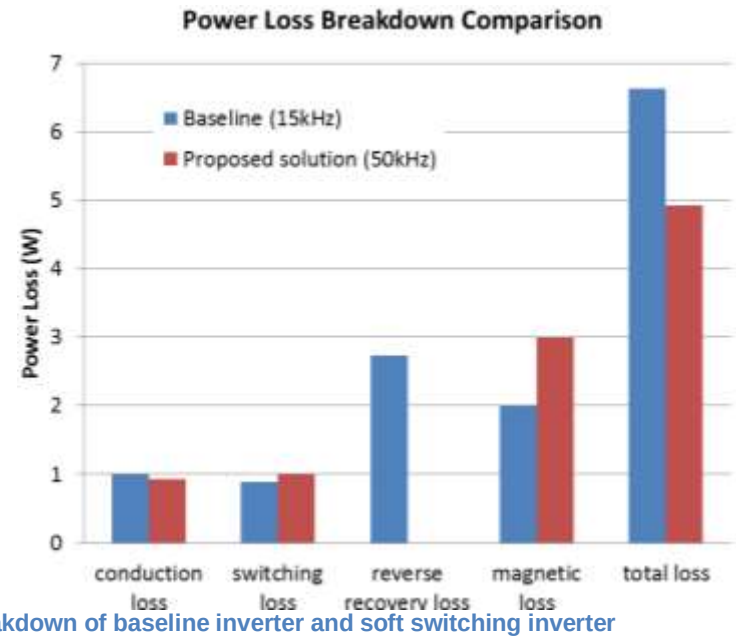


Figure 166: Loss breakdown of baseline inverter and soft switching inverter

3.2.9.3 SolarWorld ACPV panel

The mechanical development effort was focused on adapting the ACPV integration design to work with the Solar World panels that have a significantly thinner frame (31 mm vs 50mm for Motech panels). The second part was the development of clips for mounting the AC harness to the rail.

In order to fit the micro-inverter on the thinner Solar World frame, a bracket was designed to emulate the Motech panel thickness for different PV panel frame structures ranging between 20mm-40mm thickness. The bracket shape and the micro-inverter integration to the Solar World panel are shown in Figure 167. The bracket is to be built using sing piece of aluminum and the bend of the intermediate flange is decided by the panel frame thickness. A 3D printed mock-up is shown in Figure 168 and a bracket prototype is currently being built in the GE-GRC machine shop.

Finite element loading simulations were performed on the integrated ACPV panel, with loading of 40N applied at the ac output cable in directions along the panel length as well as normal to the panel. The stress analysis shows that the integrated ACPV panel using Solar World module and bracket should pass UL 1703 tests. Stress analysis for load along panel length is shown in Figure 9 and normal to the panel is shown in Figure 169. Maximum deformation reported from the analysis is 0.8mm in the case of normal force.The loading test will be performed in the lab upon receipt of bracket from the machine shop. The integrated bracket and micro-inverter do not interfere with the Solar World railing.

Analysis of the ACPV panel using SolarWorld modules was performed to verify that the integration method using a bracket as was presented in the previous report can withstand loading conditions similar that regular SolarWorld panels are exposed to. The panel mounted on SolarWorld racking system was simulated as shown in Figure 170 and the following cases were simulated:

- Fixed supports were used at the ends of the rack system in the simulation
- Several cases that were analyzed
  - Distributed load (baseline)
    1. 2000 lb distributed load across entire panel equivalent to 8896 Newtons
  - Localized load
    2. Localized 2000 lb/17.3 ft^2 load on red square (6 inch x 6 inch) modeled as 261.6 Newtons
    3. 2x Localized force to ensure design integrity 523.2 Newtons
    4. Directly above microinverter base mount location (x baseline, y baseline)
    5. 2x force moved localized load towards short end of panel (x direction reduction, Y baseline)
    6. 1.5x force moved localized load towards short end of panel (x direction reduction, Y baseline)
    7. 2x force centered load across short end of panel (x baseline, Y direction adjusted)
    8. 2x force moved localized load to 1/3 of the distance across short end of panel (x baseline, y direction readjust)

Different simulation scenarios are listed in Table 30.

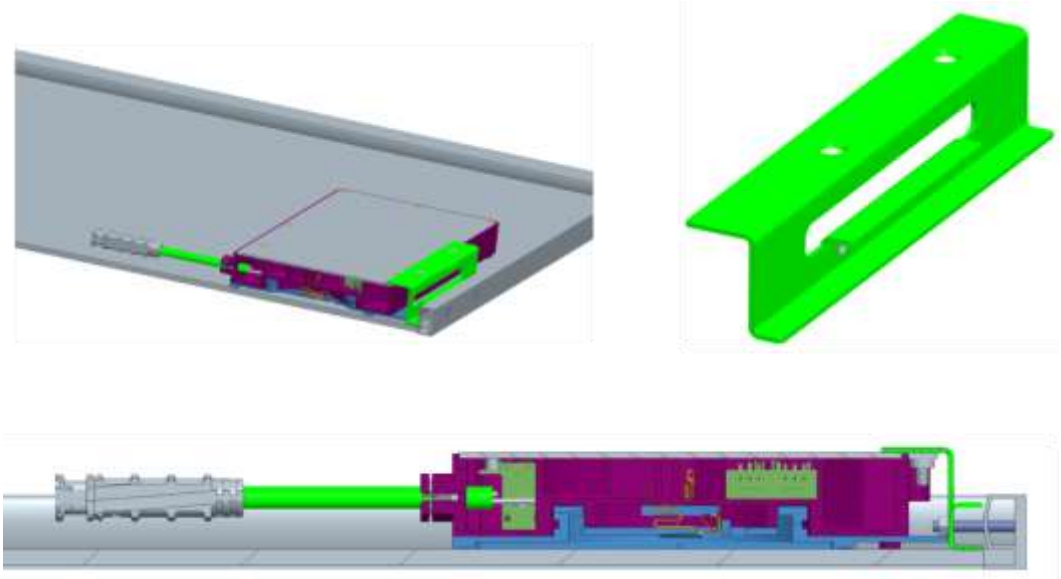


Figure 167: Bracket design and panel integration

Figure 168: Actual size 3D printed bracket

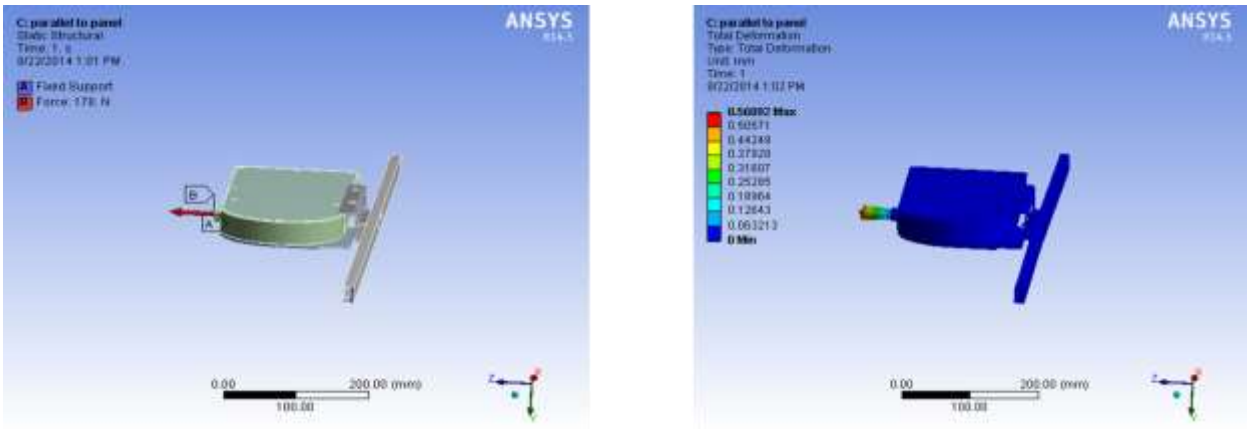


Figure 9 Stress analysis with 40N force applied along direction of the panel

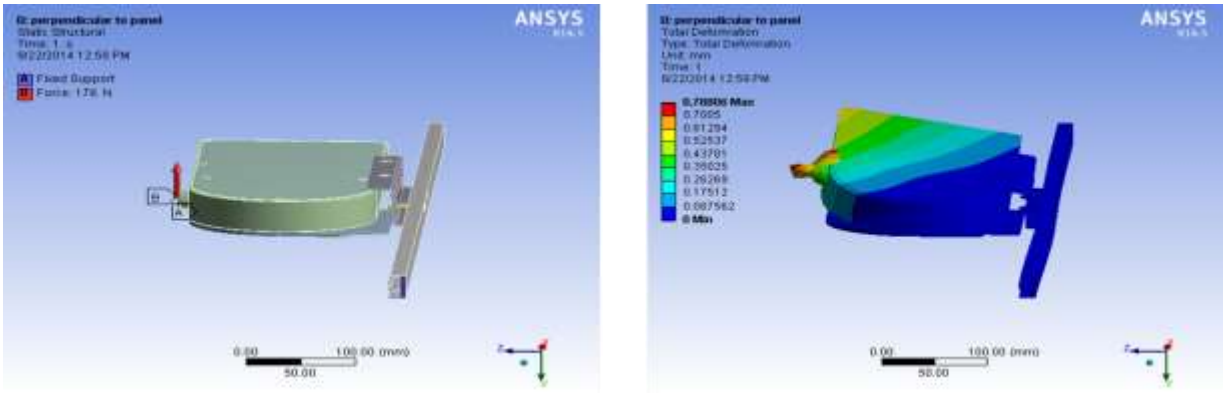


Figure 169: Stress analysis with 40N force applied in a normal direction of the panel

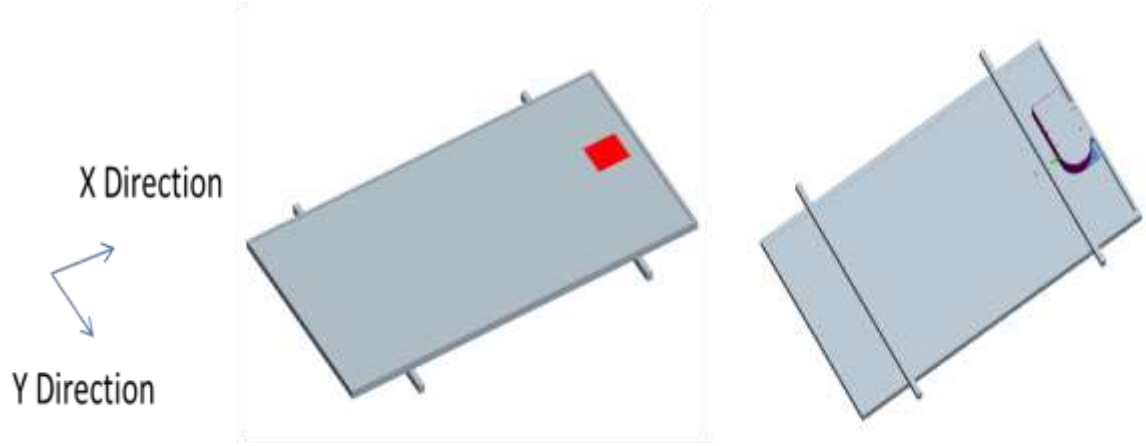
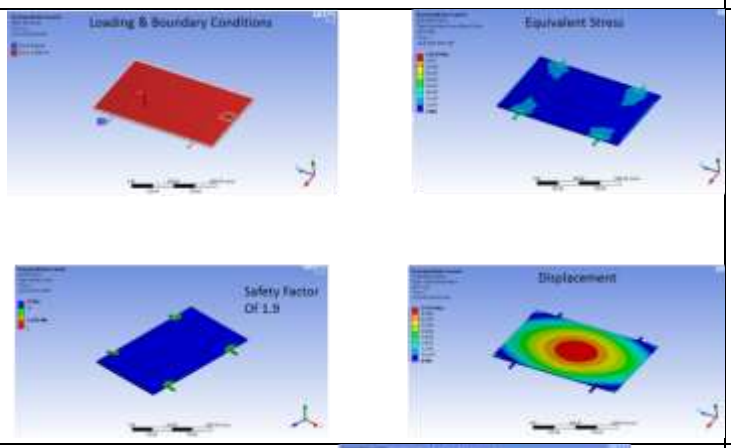
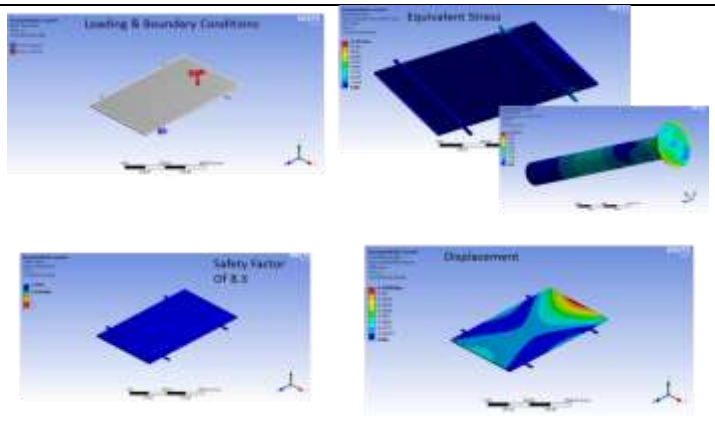
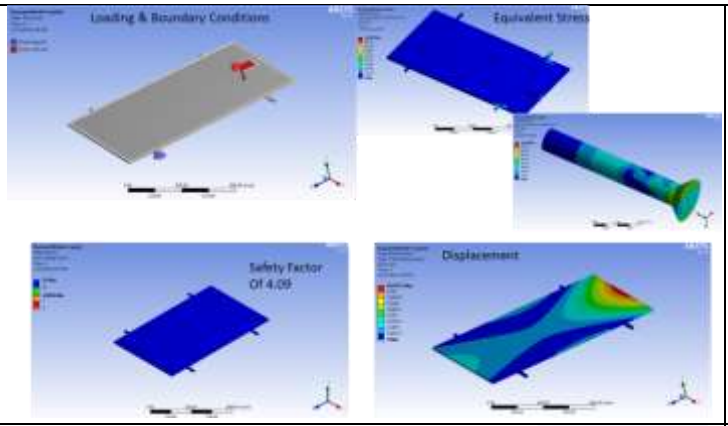
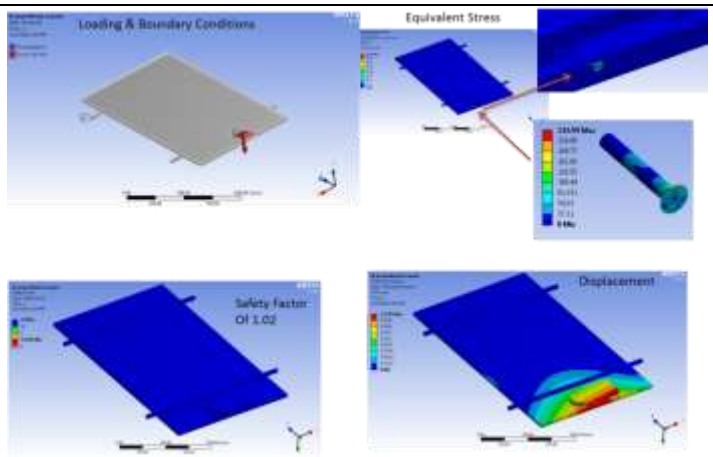
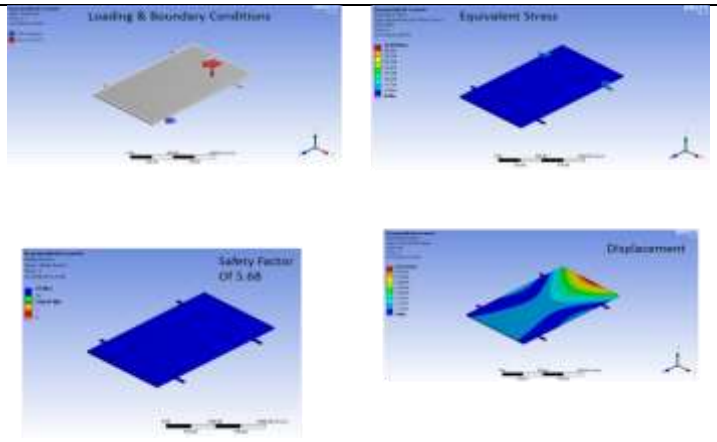
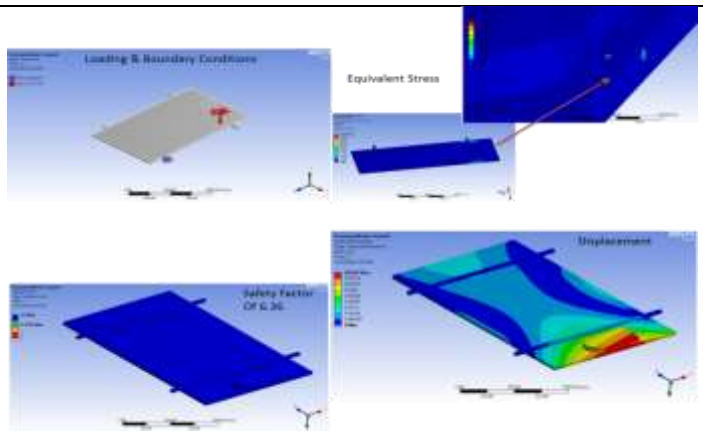


Figure 170: System assembly used in simulation

Table 29: Panel stress modeling

Case	Simulation Results	Result Interpretation:
Distributed 8896 N Force		High stress seen at panel frame intersection (~ 145 MPa) Max displacement is at the center of the panel (less than 1/4 inch)
Localized 261.6 N Force		High stress seen on Stainless Steel fastener securing universal bracket to frame (below 25MPA) Max displacement is at the top edge of the panel (~1/64 inch)

Localized 532.2 N Force		High stress seen on Stainless Steel fastener securing universal bracket to frame (below 44MPA) Max displacement is at the top edge of the panel (~1/32 inch)
Localized 392.4 N Force		High stress seen on Stainless Steel fastener securing universal bracket to frame (244 MPa) Max displacement is on Stainless Steel fastener (~1/16 inch)
Localized 532.2 N Force		High stress seen on Stainless Steel fastener securing universal bracket to frame (44 MPa) Max displacement is on Stainless Steel fastener (~1/32 inch)

Localized 532.2 N Force		High stress seen on Stainless Steel fastener securing universal bracket to frame (39 MPa) Max displacement is on Plastic Microinverter Enclosure(~1/32 inch)

- Deflections were below 1/4 of an inch in all cases, considering the overall panel size this seems acceptable.
- No high stresses were seen in the panel or other system components, only in fasteners. With a fastener failure the micro-inverter could dislodge from the system.

The SolarWorld panel was then loaded at the AC output cable in two directions: along the panel length and normal to the panel as shown in Figure 171. Starting from smallest to the largest weight, it was 5kg, 10kg, 15kg, and 18kg. Both experiments (vertical and horizontal) held the weights for over 1 minute without any noticeable damage to the mounting. This test indicated the panel can pass the UL 1703 requirement

Figure 171: Mechanical loading of SolarWorld ACPV panel

3.2.9.4 Enclosure modification and build

Some modifications to the micro-inverter enclosure were made to improve board mounting, improve isolation from external environment and improve the robustness of the back connector. The model of the enclosure is shown in Figure 172.

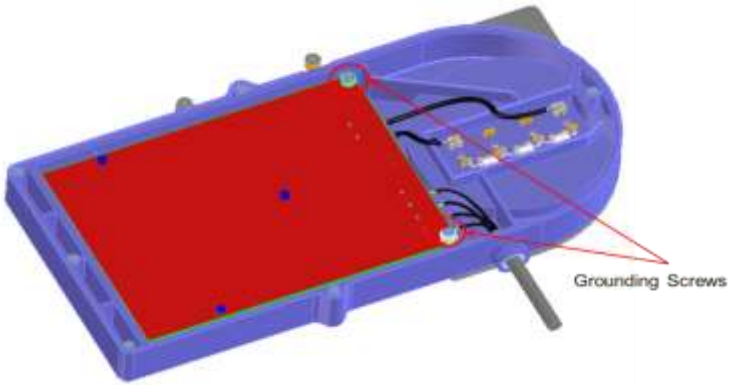


Figure 172: Modified micro-inverter enclosure

The grounding screws were modified to have silicone rubber for sealing as shown in Figure 173. The spring contacts were also modified to have two bends rather than three, as shown in Figure 174, in order to reduce the stress on the bends improve the contact robustness. An internal path of 3.5 mm width is also added to allow adding silicone for sealing as shown in Figure 175. The enclosure build was completed as shown in Figure 176.

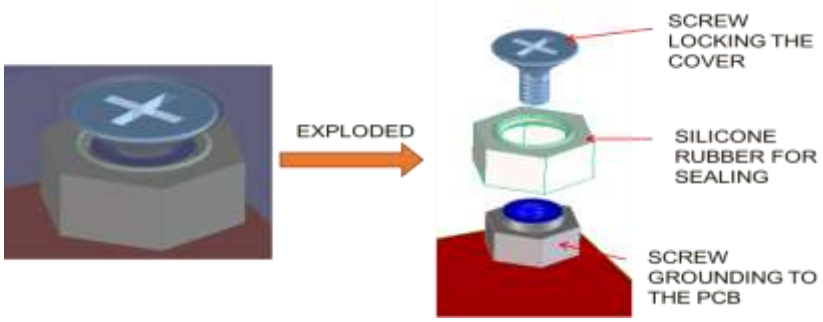


Figure 173: Grounding screw modifications

Figure 174: Modifications to spring contacts

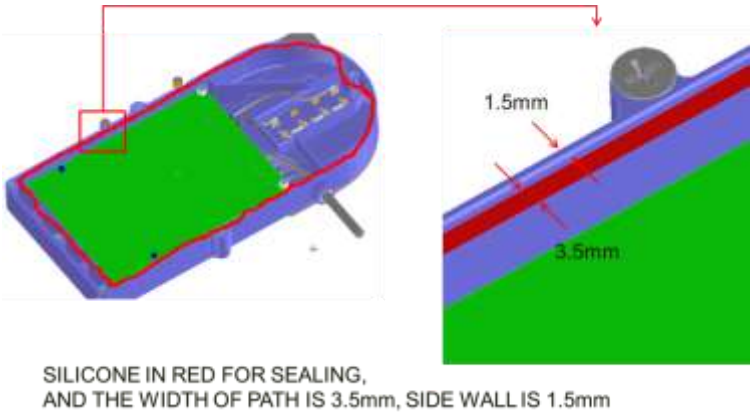
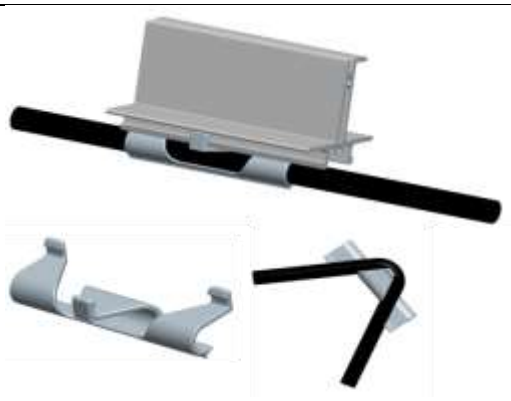


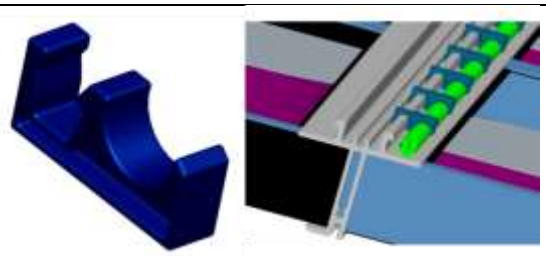
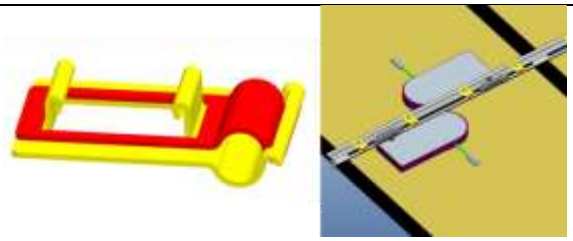
Figure 175: Modifications to spring contacts

Figure 176: Micro-inverter enclosure and panel connector

Clips for AC harness mounting to the rail were also developed. Several clip concepts are listed in Table 31:

Table 30: Clip design concepts

1. Single molded plastic spiral clip • Pros » Simple installation • Cons » Plastic life vs UV exposure » Need slack in AC harness to install	

2. Single molded plastic clip • Pros » Simple installation • Cons » May require many to support AC harness » Plastic life vs UV exposure	
3. Two piece plastic or metal clip • Pros » Metal stronger than plastic, better support • Cons » If metal could need protective layer from environment » 2 piece versus 1 piece, confusion assembling, or if one part lost, can't use » More expensive	

The first design was selected to be implemented in the demo. A clip was 3D printed and mounted to a section of the rail as shown in Figure 177. Further, the rail clip assembly was exposed to thermal cycling in a thermal chamber as shown in Figure 178, where temperature was cycled between -40°C and +40°C with a dwell time of 2 hours to verify that it can with stand the varying weather conditions. The clip passed the test and there were no issues removing it or reattaching it at both ends of the temperature range tested.

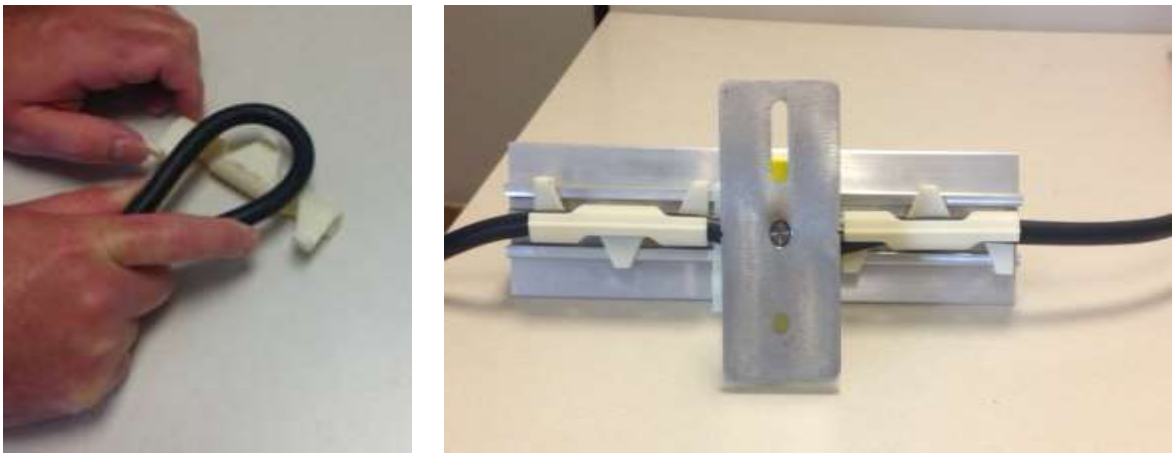


Figure 177: 3D printed clip: harness attachment and rail mounting

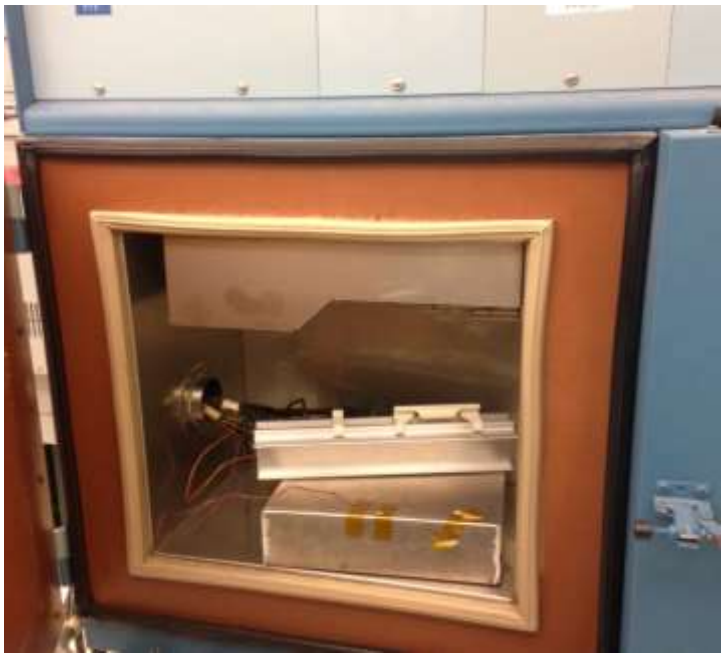


Figure 178: Clip, rail assembly in thermal chamber

3.2.9.5 Communication

A radial communication network, shown in Figure 179, is designed to link individual micro-inverters to a central hub that coordinates the operation of the array. The Zigbee communication nodes on micro-inverters and on the central hub will be operated in router mode. The hub is responsible for communicating with the grid operator according to IEC 61850, either by only receiving broadcast commands or by bidirectional communication with the grid operator. The signals required to be received at the hub according to IEC 61850 are shown in Figure 180

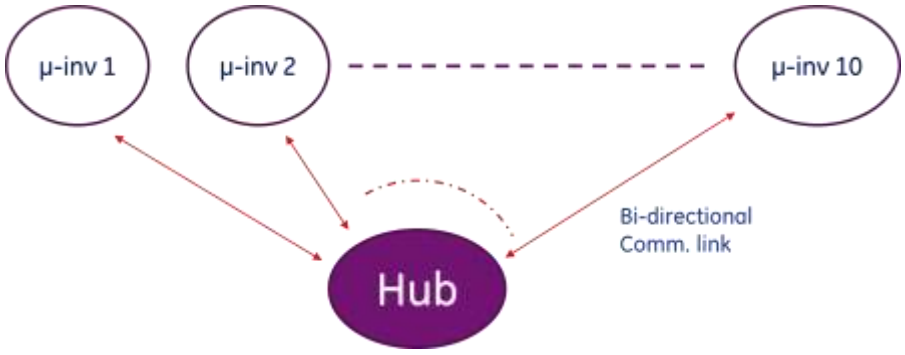


Figure 179: Communication Network

Status Point	Description
Primary Information	
Connect status	Whether or not the device is currently connected at its ECP.
PV output available	Yes/No
Storage output available	Yes/No
Status of var capability	Yes/No
Inverter active power output	Present real power output level (Watts). This is an instantaneous (minimum averaging) reading.
Inverter reactive output	Present reactive power output level (Vars, leading or lagging). This is a signed quantity.
Current PV Mode	Identity of mode or function that the PV/Storage is in, including "owner mode" (Enumeration with range left open for proprietary vendor)
Detailed Information	
Inverter status	Inverter is switched on (operating), off (not able to operate), or in stand-by mode (capable of operating but currently not operating)
DC Current level available for operation	Indicates whether or not there is sufficient DC current to allow operation. – Value, not yes/no
Inverter active power output	Present real power output level (Watts). This is an instantaneous (minimum averaging) reading.
DC inverter input power	Use for determining efficiency of inverter
Local/Remote control mode	Inverter is under local control or can be remotely controlled
Real power setpoint	Value of the real power setpoint
Reactive power setpoint	Value of the output reactive power setpoint
Power factor setpoint	Value of the power factor setpoint as angle
Frequency setpoint	Value of the frequency setpoint
Power Measurements	
Active power	Active power value, plus high and low limits
Reactive power	Reactive power value, plus high and low limits
Phase to ground voltages	[illegible] plus high and low limits
Power factor	Power factor value, plus high and low limits
Battery Storage Status (If Storage is Included in PV System)	
Capacity rating	The useable capacity of the battery, maximum charge minus minimum charge from a technology capability perspective (Watt-hours)
State of charge	Currently available energy, as a percentage of capacity rating (percentage)
Available energy	State of charge minus storage reserve (Watt-hours) See storage settings section for definition of "storage reserve"
Maximum battery charge rate	The maximum rate of energy transfer into the storage device. (Watts) This establishes the reference for the charge percentage settings in function PC4a.
Maximum battery discharge rate	The maximum rate of energy transfer out of the storage device (Watts) This establishes the reference for the discharge percentage settings in function PC4a.
Internal battery voltage	Internal battery voltage
DC inverter power input	Used for determining efficiency of inverter

Figure 180: Information in data packet as per IEC 61850

This section provides necessary information about the wireless network used for communication of the control signals and report data from a group of photo-voltaic panels and a data collector (Hub). Each solar panel in this network has a wireless radio that communicates with a Hub device which collects the report data and sends control messages to the nodes in the network. This section provides the information about the network functions and underlying communication protocol, as well as information on message types and packet structures used for communication.

Radio Modules

A solar panel communicates using Xbee S1 radio module from Digi International [31]. Xbee S1 radio module operates in ISM 2.4 GHz range. The board and pin layout is shown in Figure 181.

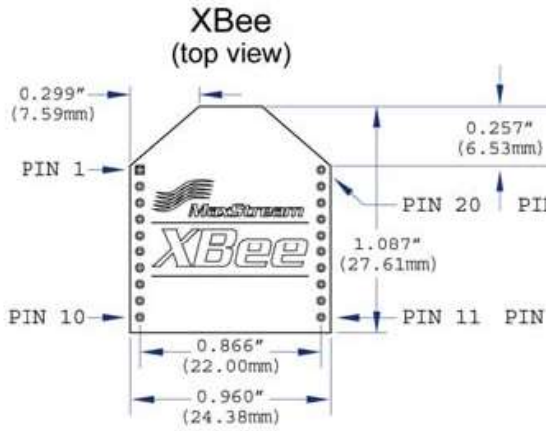


Figure 181: The board of Xbee S1 wireless module.

Xbee S1 module is connected to the host processor (a DSP processor on the solar panel) via UART serial port. The connection between Xbee S1 module and host processor is established using four pins, as shown on the Figure 182. The UART data rate can be changed in the firmware of S1 module (currently set to 19200 bauds).

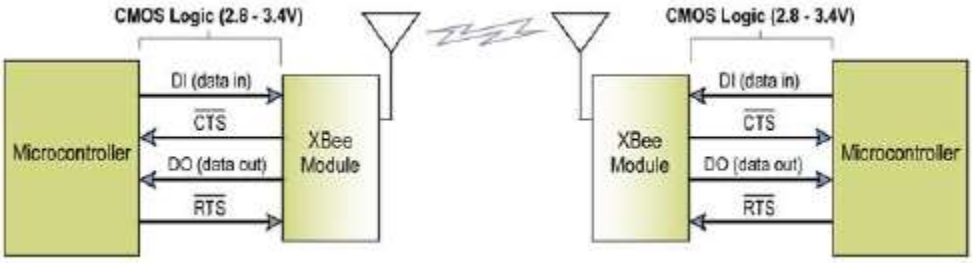


Figure 182: Serial Communication between Xbee module and host processor

Wireless Network Topology and Communication Protocol

XBee S1 modules run IEEE 802.15.4 protocol, which is a standard protocol for low power and low data rate networks. The protocol defines physical and medium access control (MAC) layer of the network stack. Each node has a unique ID number which is preprogrammed on the DSP controller. For a typical configuration of ten solar panels on the roof, this wireless network is designed to support the communication from ten wireless nodes (each for one solar panel) and a data collector (Hub) that is usually placed inside the house. The network is configured to support star topology, where each radio node communicates directly with the Hub device. In the first design of the wireless network the modules supported Zigbee protocol. Zigbee is a mesh protocol, meaning that each node can communicate with other nodes in a range, which increases the network reliability. However, Zigbee routing protocol introduces a significant network overhead that comes from continuous updates of the routes. This in turn decreases the network available bandwidth significantly.

In order to minimize the collisions of the packets from different nodes a time-division-multiple-access (TDMA) protocol is designed, where each node communicates with the Hub in an assigned time slot. The Hub device and the nodes share the same hardware and firmware.

Control and Monitoring Application

The Hub node is connected to the laptop that runs an application (shown on the Figure 3), which displays the received reports from the nodes and is used to send control messages to the nodes. The supported control messages are: “Start”, “Stop”, “Set Max Power” and ”Set Power Factor”. The Hub needs to be connected to the laptop before the application is started so that the application can read the data from the serial port at which the Hub is connected. To start the communication between the Hub and the rest of the network the appropriate serial port from the drop down menu has to be selected and then click to Connect button. The Hub disconnects from the network simply by pressing Disconnect button. The control application interface is shown in Figure 183.

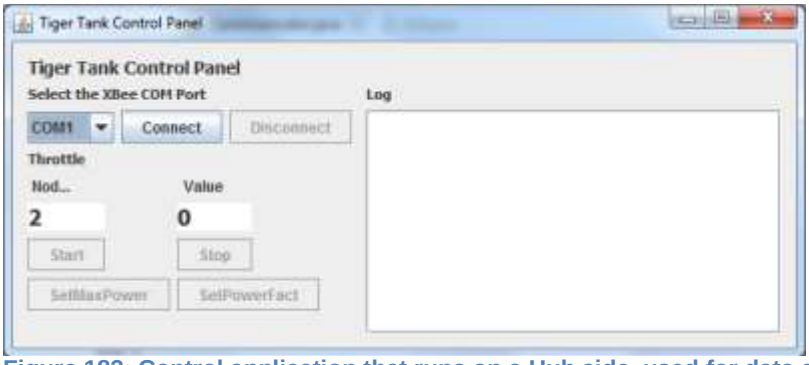


Figure 183: Control application that runs on a Hub side, used for data collection and control of the network

Packet Types

The communication protocol defines four types of packets that are used to support different network functions:

1. Request Report Packet (RRP) – sent from the Hub to a node requesting the current data readings,
2. Update Parameter Packet (UPP) – sent from the Hub to a node with a certain value of the parameter that has to be updated on the node,
3. Fault Report Packet (FRP) – sent from a node to the Hub to notify the Hub about faulty state,
4. Report Packet (RP) – sent from a node to the Hub periodically, to report the current values of monitored parameters.

Request Report Packet (RRP)

RRP is sent by the Hub to each wireless node periodically to pull the node for the new data. When a node receives an RRP packet it generates a report packet (RP) that is sent back to the Hub. RRP packet consists of the fields given in Table 32.

Table 31: Packet structure of Request Report packet

Filed Name	Preamble	Sequence Number	Node ID	Command	Data Field
Size [Bytes]	2 bytes	1 byte	4 bytes	1 byte	4 bytes
Value	FF		Packet destination address	1 - Start 2 - Stop 3 - SetMaxPower 4 - SetPowerFact 5 - Request Report	Applies for command 3 and 4

Update Parameter Packet (UPP)

UPP is the packet send by the Hub to the node with a new value of a certain parameter that has to be updated. When a node receives the UPP, it checks its sequence number, updates a parameter according to the command and sends back the same UPP as an acknowledgement to the Hub. RRP packet consists of the fields given in Table 33.

Table 32: Packet Structure of the Update Parameter Packet (UPP)

Filed Name	Preamble	Sequence Number	Node ID	Command	Data Field
Size [Bytes]	2 bytes	1 byte	4 bytes	1 - Start 2 - Stop 3 - SetMaxPower 4 - SetPowerFact 5 - Request Report	4 bytes applies for commands 3 and 4

Report Packet (RP)

RP is sent by the PV node to the Hub. When a node receives RRP from the Hub, it generates the RP that contains the current state of the system and sends it back to the Hub. This is a long packet, and it consists of the fields given in Table 34.

Table 33: Packet Structure of the Report Packet (Rp)

Filed Name	Preamble	Node ID	Data Field
Size [Bytes]	2 bytes	4 bytes	Data [54 bytes]
Value	FE	Sender address	

The data field of a packet includes the following information given in Table 35.

Table 34: Data field information included in a report packet

Variables	Size [Bytes]
Status Variable	2
Inverter_active_power_output	4
Inverter_reactive_output	4
DC_Current_level_available_for_operation	4
DC_inverter_input_power	4
Real_power_setpoint	4
Reactive_power_setpoint	4
Power_factor_setpoint	4
Frequency_setpoint	4
Power_factor	4
InputPVVoltage	4
InputPVCurrent	4
OutputACVoltage	4
OutputACCurrent	4

The meaning and values of the first transmitted variable (status variable) is given in the Table 36.

Table 35: Status variable sent in report packet

Status variable states	Status variable value
`(ConnectStatus ==1) &&(Inverter_status == 0)`	11
`(ConnectStatus == 1) &&(Inverter_status == 1)`	33
`((ConnectStatus == 0)&&(Inverter_status == 0))`	22

ConnectStatus and Inverter_status are variables that are defined in the DSP code.

Network Operation

All nodes and a Hub need to share the same Group ID number in order to be able to communicate. This number is stored on the Hub as well as on each node. Each node has assigned unique ID number, which currently goes from 0-9.

The Hub periodically sends the status request to one by one node using Report Request packets. These packets are based on the timer that triggers sending of RRP. After the message is received the node fills out the Report Packet with the monitored data and sends it back to the Hub. When a Hub receives the report message it displays the received data in the text box of the application.

The commands such as “Start”, “Stop” and “Set Power Factor” and “Set Max Power” can be sent to each node from the Hub. The “Start” and “Stop” functions are sent simply by pressing Start or Stop button on the application. For “Set Power Factor” and “Set Max Power” a value of the corresponding parameter needs to be entered into the text box before pressing Start button. These are event based functions and the control is send immediately to the node. After receiving the packet the node sends back the acknowledgement packet back to the Hub.

Interoperability

Network’s functionality should not be compromised if the Hub is replaced with a new device. Since all nodes in the network operate using IEEE 802.15.4 standard protocol, the Hub device should always support this protocol as well. When a Hub is replaced with a new device (the same S1 module) the new device should be flashed with the same version of firmware as the previous one. Digi International [32] provides the X-CTU software (shown on the Figure 184) that is used to read and write the firmware onto the S1 devices (wireless node and Hub). The current version of the firmware can be selected from the X-CTU menu. In addition the same current firmware file is provided in Figure 185. The current version of the firmware is given in Table 37.

Table 36: Firmware protocol and version used for Hub and nodes in the network

Protocol	Version
802.15.4	ec

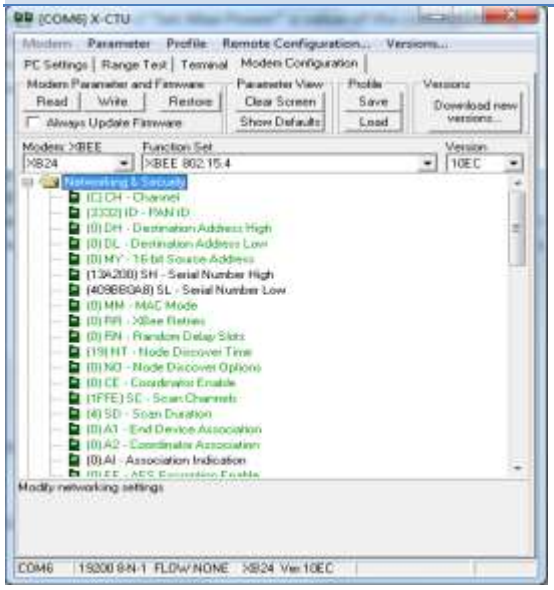


Figure 184: X-CTU software from Digi International used for writing a firmware into the wireless node

The radio profile of the nodes and Hub is given below. If a node or a Hub needs to be replaced in the network it is recommended to flash using X-CTU software [33] the new device with the following code (that needs previously to be stored into the .xml file).

```
<?xml version="1.0" encoding="UTF-8"?>
<data><profile><description_file>xb24_15_4_10ec.xml</description_file><settings><setting command="CH">C</setting><setting command="ID">3332</setting><setting
command="DH">0</setting><setting command="DL">0</setting><setting
command="MY">0</setting><setting command="MM">0</setting><setting
command="RR">0</setting><setting command="RN">0</setting><setting
command="NT">19</setting><setting command="NO">0</setting><setting
command="CE">0</setting><setting command="SC">1FFE</setting><setting
command="SD">4</setting><setting command="A1">0</setting><setting
command="A2">0</setting><setting command="EE">0</setting><setting
command="KY"/><setting command="NI">0x20</setting><setting
command="PL">4</setting><setting command="CA">2C</setting><setting
command="SM">0</setting><setting command="ST">1388</setting><setting
command="SP">0</setting><setting command="DP">3E8</setting><setting
command="SO">0</setting><setting command="BD">4</setting><setting
command="NB">0</setting><setting command="RO">3</setting><setting
command="AP">0</setting><setting command="D8">0</setting><setting
command="D7">1</setting><setting command="D6">0</setting><setting
command="D5">1</setting><setting command="D4">0</setting><setting
command="D3">0</setting><setting command="D2">0</setting><setting
command="D1">0</setting><setting command="D0">0</setting><setting
command="PR">FF</setting><setting command="IU">1</setting><setting
command="IT">1</setting><setting command="IC">0</setting><setting
command="IR">0</setting><setting command="P0">1</setting><setting
command="P1">0</setting><setting command="PT">FF</setting><setting
command="RP">28</setting><setting
command="IA">FFFFFFFFFFFFFFFF</setting><setting
command="T0">FF</setting><setting command="T1">FF</setting><setting
command="T2">FF</setting><setting command="T3">FF</setting><setting
command="T4">FF</setting><setting command="T5">FF</setting><setting
command="T6">FF</setting><setting command="T7">FF</setting><setting
command="DD">10000</setting><setting command="CT">64</setting><setting
command="GT">3E8</setting><setting
command="CC">2B</setting></settings></profile></data>
```

Figure 185: Firmware file

For a node to node communication, the package received rate is 100%. A network of 10 nodes was set up to test network traffic and rate of package receipt where all nodes achieve > 91% rate of packet delivery.

3.2.9.6 Panel testing and demo site installation

The micro-inverter was then assembled with both the Motech and SolarWorld PV panels and the micro-inverter was tested outdoors, directly connected to the grid. The test setup is shown in Figure 186. Test waveforms and communication interface for outdoor test are shown in Figure 187.
Three panels were then connected to the same harness and operated in parallel as shown in Figure 188.

Figure 186: Outdoor test of ACPV panels

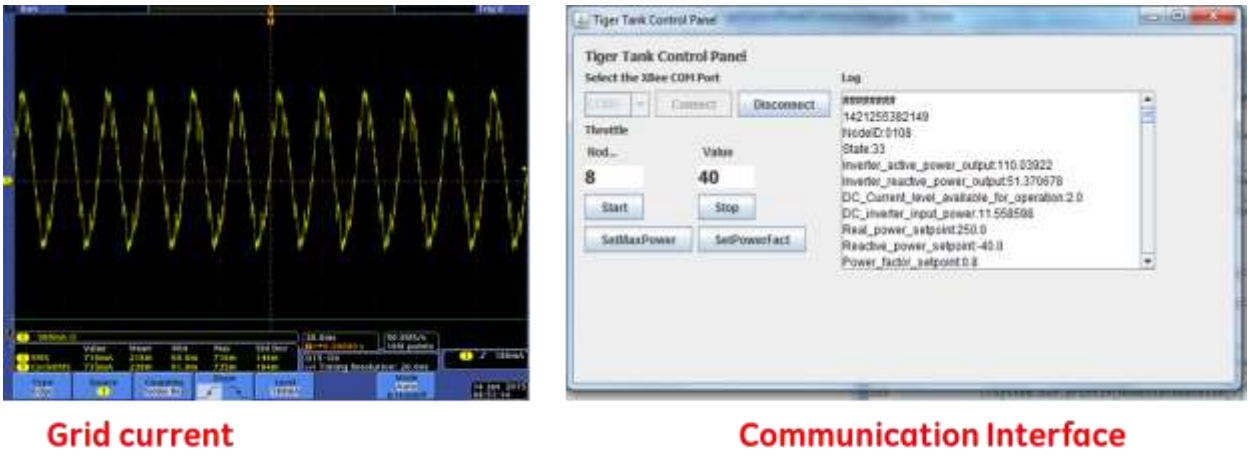


Figure 187: ACPV panel operation

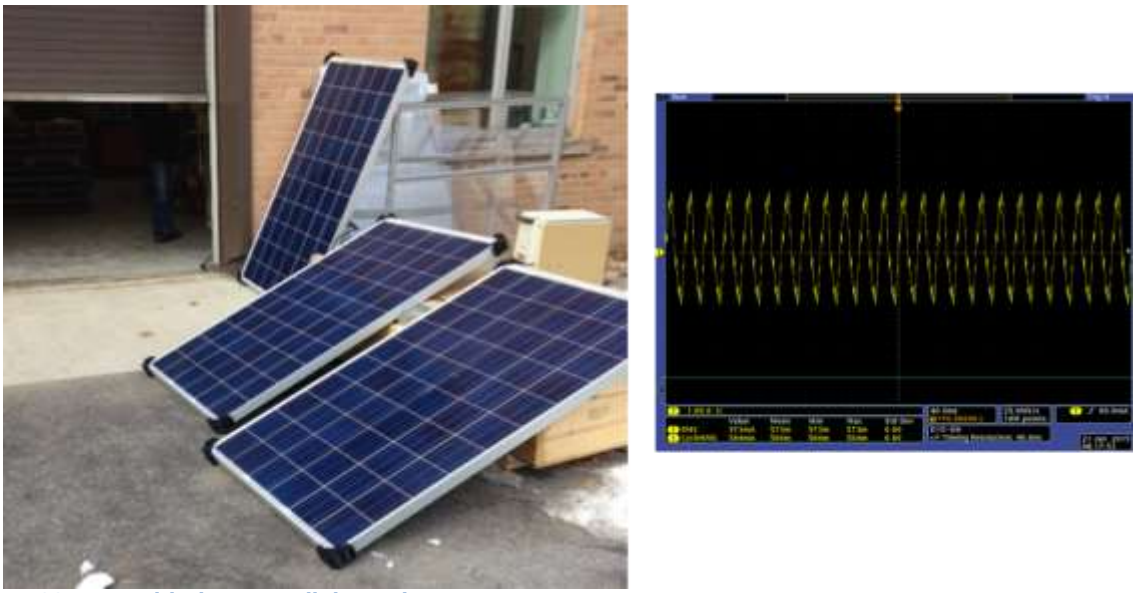


Figure 188: Test with three parallel panels

Figure 189: Schenectady test site installation

Figure 190: SolarWorld test site installation

3.2.10 Task 10: Operate Pilot Demo Sites & Commercialization

This final task covers the testing of the micro-inverter to verify compliance with IEEE 1547 and collect data from demo installations. The commercialization sub-task involved providing a plan for transition to market of the developed technologies.

3.2.10.1 Micro-inverter testing

Micro-inverter was tested for IEEE 1547 compliance. Figure 191 shows the operational waveforms of the micro-inverter at startup and for several fault conditions. Where the converter met the IEEE 1547 requirements. Appendix B show the detail trip time measurement vs. standard requirement for each fault type. The test was repeated for two boards and the pass/fail results are summarized in Table 38.

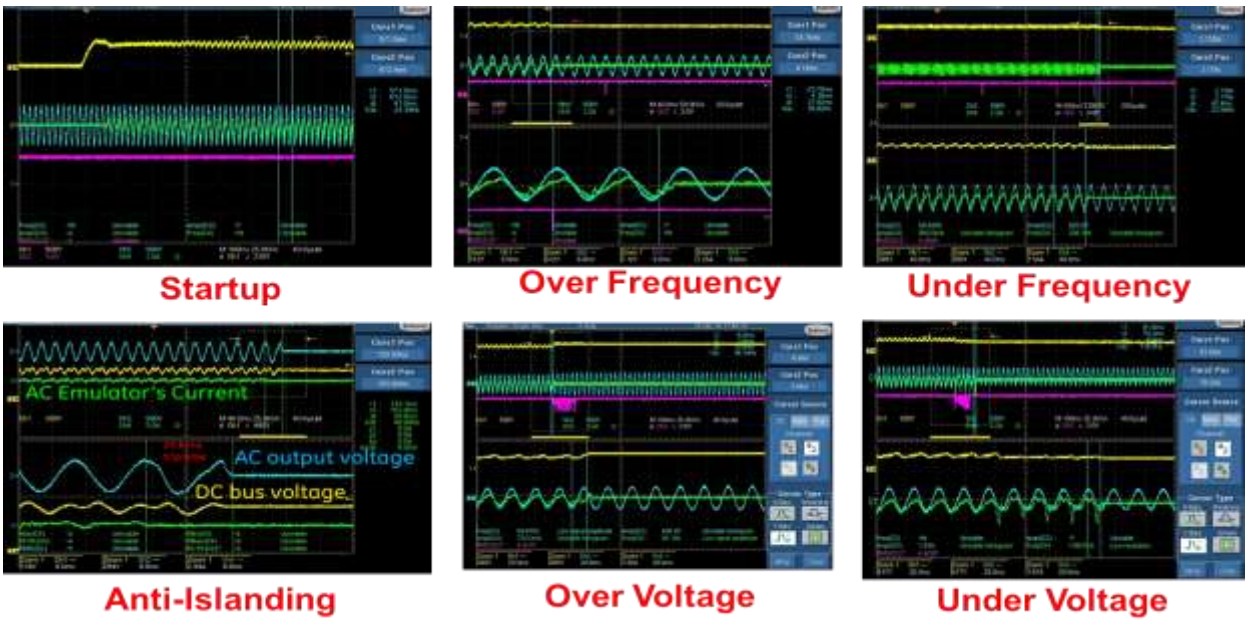


Figure 191: Micro-inverter startup waveforms and response to faults

Table 37: IEEE 1547 testing summary for demo prototypes

Test	Board 2	Board 16
Voltage Test (over-voltage, under-voltage different loads and PF)	**Passed**	**Passed**
Frequency Test (over-frequency, under-frequency)	**Passed**	**Passed**
Synchronization	**Passed**	**Passed**
Interconnection integrity	**Passed**	**Passed**
Limitation of dc injection for inverters without interconnection transformers	**Passed**	**Passed**
Unintentional islanding test	**Passed**	**Passed**
Open phase	**Passed**	**Passed**
Reconnect following abnormal condition disconnect	**Passed**	**Passed**
Harmonics test for inverters	**Passed**	**Passed**

EMI Testing was also performed. The first test showed a large spike around 1.1MHz as shown in Figure 192. Investigation of this issue showed that the newly selected common mode chokes had a resonance frequency around 1MHz range. Therefore, replacing the common mode choke resulted in a much improved EMI measurement as shown in Figure 193. However the differential mode measurement is right on the edge of compliance limit with no margin, which is an issue that needs to be improved in the next design iterations.

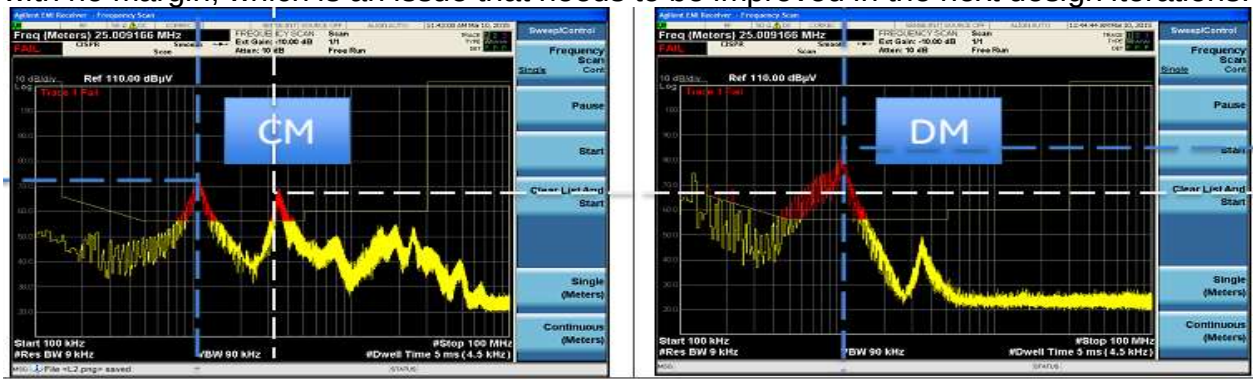


Figure 192: Baseline EMI measurement

Figure 193: EMI measurement with modified common mode choke

Micro-inverters were also tested in parallel operation. Two inverters were run in parallel and the waveforms are shown in Figure 194 and three units were run with 3 solar panels as was shown earlier in Figure 188. No oscillation or stability issues were observed.

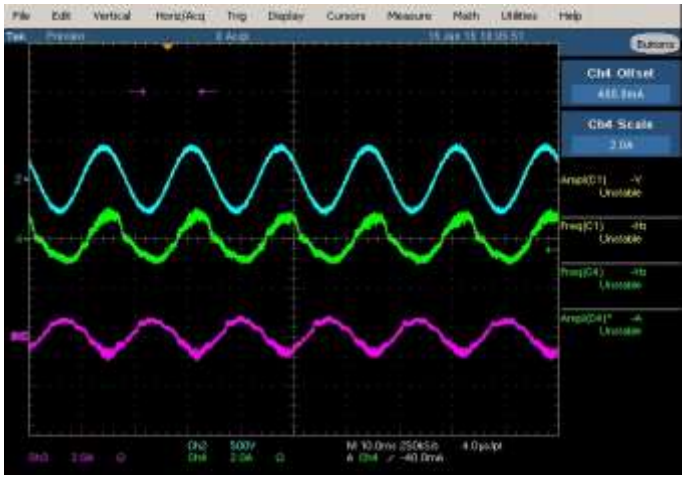


Figure 194: Micro-inverter parallel operation: Blue: ac voltage, Green: current of inverter 1, Magenta: current of inverter 2

The micro-inverter VAR capability was also tested. Figure 195 shows the cases of leading and lagging power factor of 0.9.

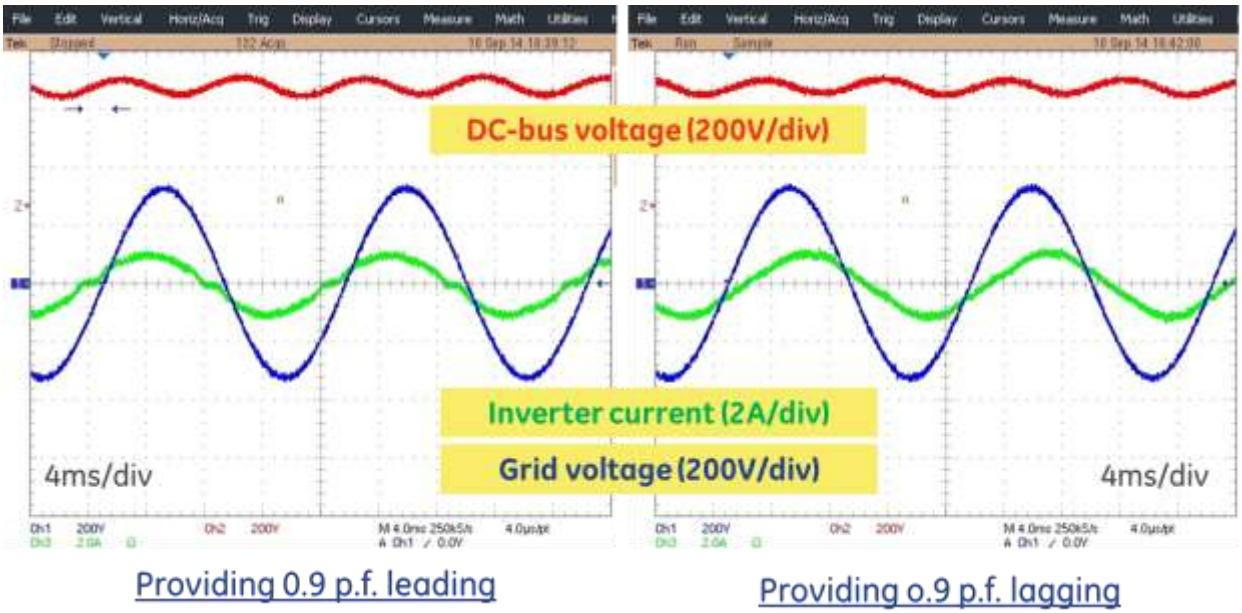


Figure 195: Micro-inverter VAR support capability

3.2.10.2 Field Data

Data was collected from the two demo sites over a period of 4 months. The Schenectady demo site data is shown in Figure 196 and Figure 197, Figure 196 shows sample waveforms from two of the units one from the top row of panels (left) and the other form the bottom row. Figure 197 shows a comparison of the ACPV string to a baseline commercial string of panels. The baseline string generated about 2% higher energy. This

indicated more optimization of the MPPT algorithm as well as inverter topology is still required.

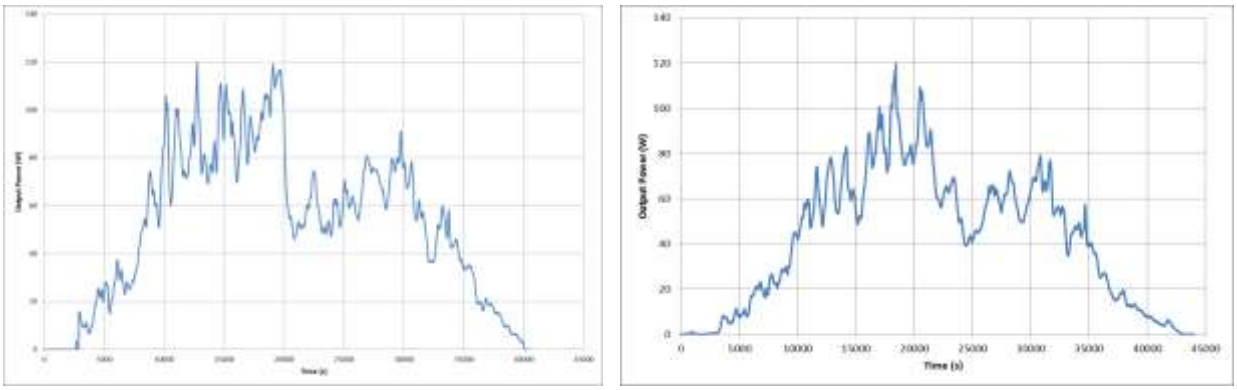


Figure 196: Micro-inverter power profile over a day at Schenectady demo site (left plot is for a panel on the top row and the right is for a panel on the bottom row)

Figure 197: Energy yield of ACPV string with Motech panels (blue) vs a baseline system (red)

The SolarWorld ACPV string has experiences issues of repeated tripping at higher power conditions. The SolarWorld site setup was at a higher line voltage, and the panels were higher power (280W compared to 255W Motech panels). These panels worked well at the GRC site, but the issue with tripping at SolarWorld site still requires more debugging of the control code to maintain operation at higher voltage and power. The shutdown is due to a high DC link voltage. Figures 198 shows individual micro-inverter daily power curve with the units tripping a few hours after startup and then restart at a later time.

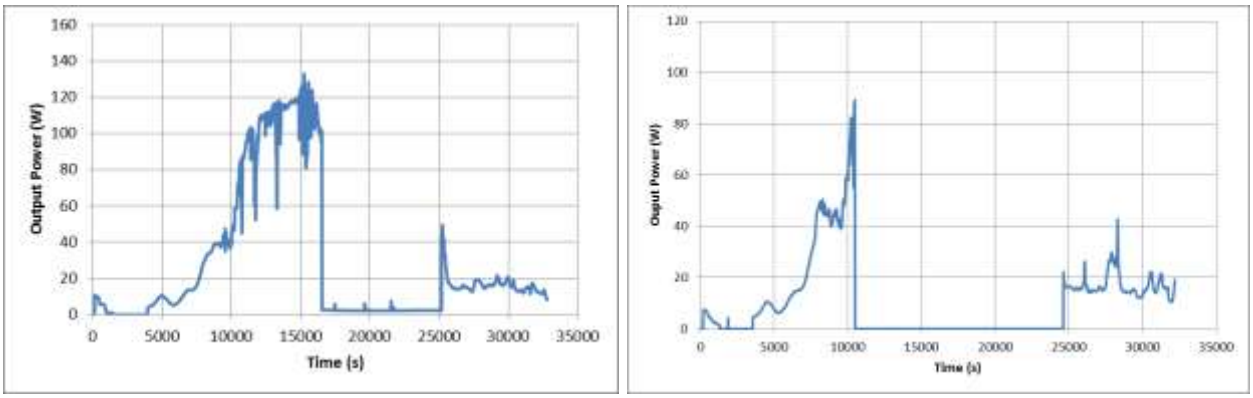


Figure 198: Micro-inverter power profile over a day at Hillsoboro demo site (left plot is for a panel on the top row and the right is for a panel on the bottom row)

3.2.10.3 Commercialization

From a commercialization perspective, GE Ventures managed to close a licensing deal with SPARQ Systems Inc., where the residential PV technologies have been licensed and technology transfer activities are underway.

4. Future Work

With the transition of the technology to SPARQ Systems, the residential PV and ACPV technologies developed throughout this program will be commercialized as part of SPARQ's product portfolio. GE will work with SPARQ to shape business opportunities and support their efforts in the development of the ACPV panels along with panel manufacturers, such as SolarWorld, Canadian Solar.. etc.
Current activities include working with National Grid and Buffalo Niagara Medical Center to shape a program to study the impact of smart grid ready micro-inverters on the distribution grid and study economic models of the residential PV systems. If funded, GE will work with SPARQ on delivering an ACPV panel for installation in this pilot project.

On the technical side, more work needs to be done to improve the micro-inverter controller to increase its robustness to parameter variations (e.g. sensor drifts) and also to better tune the control for more consistent operation in high voltage and grid environments.

Future activities also include extending the developed circuit technologies to build string inverters using wide bandgap SiC devices

5. Patents

Eight patent applications were filed: three on the micro-inverter topology and control and two on the AC and DC connectors for inverter/panel integration. One additional disclosure expanding the scope of partial power dc-micro-converter architectures has been started and in preparation for submission

a) Docket # 260357: "Transformerless Photovoltaic Inverter with Volt/Var Support," filed March 2012

b) Docket # 268366: “Interleaved Converter for PV Micro-inverter Application,” filed Nov. 2013

c) Docket # 268764: “PV Resonant converter system,” filed Nov. 2013

d) Docket # 268409-1: “Solar Micro-Inverter Panel Mounting and DC connector Design,” filed Oct. 2013

e) Docket 268409-2: “Solar Micro-Inverter Panel Mounting and AC connector Design,” filed Oct. 2013

f) Docket # 278828: “Rotating micro-inverter mounting system,” filed May 2015.

g) Docket # 278831: “Universal micro-inverter mounting bracket,” filed May 2015.

h) Docket # 278851: “System and method for soft switching power inversion,” filed May 2015.

6. External Publications:

Four published papers

[1] “A Soft Switching Interleaved Inverter Topology,” accepted for publication and to appear on proceedings of IEEE Applied Power Electronics Conference (APEC 2016)

[2] “Impact of Micro-inverter Reactive Power Support Capability in High Penetration Residential PV Networks,” Proceedings of IEEE Photovoltais Specialists Conference (PVSC 2015)

[3] “A High Efficiency PV Micro-Inverter with Grid Support Functions,” Proceedings of IEEE Energy Conversion Conference & Expo (ECCE 2014).

[4] “A Multi-Objective Study for Down Selection of A Micro-Inverter Topology for Residential Applications,” Proceedings of IEEE Photovoltais Specialists Conference (PVSC 2014)

One paper in preparation:

[5] “Micro-inverter Topology with Grid Support Functions,” in preparation for submission to IEEE Transactions on Sustainable Energy

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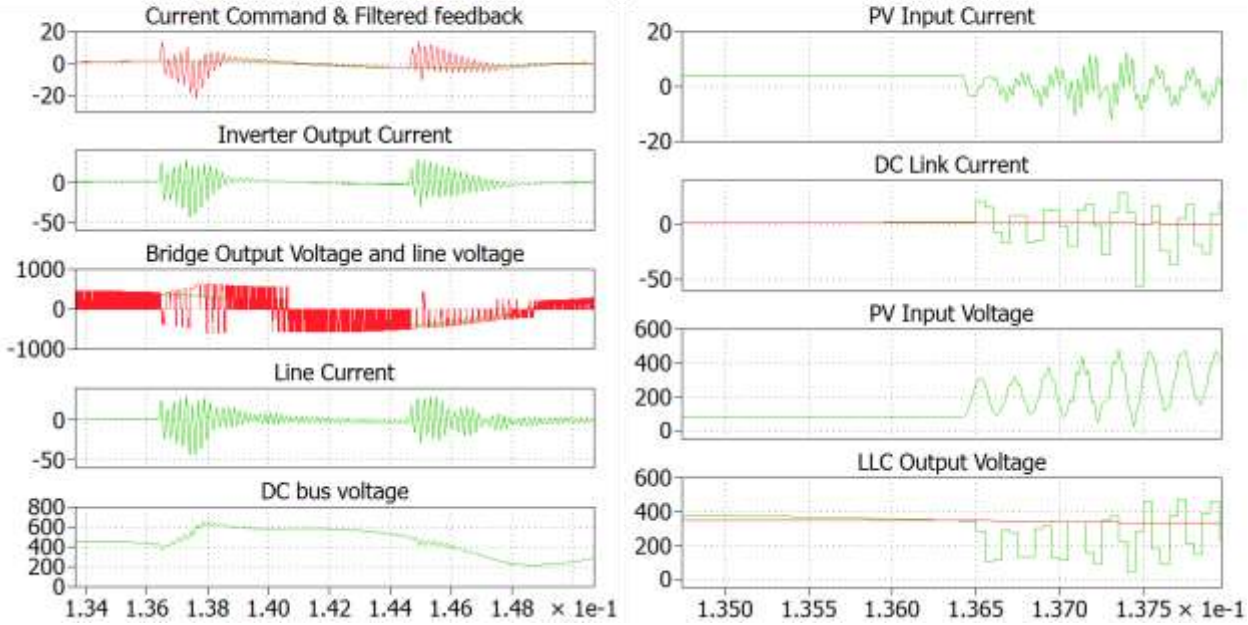
[31] http://ftp1.digi.com/support/documentation/90000982_R.pdf
[32] Digi International: www.digi.com
[33] X-CTU software: http://www.digi.com/products/wireless-wired-embedded-solutions/zigbee-rf-modules/xctu

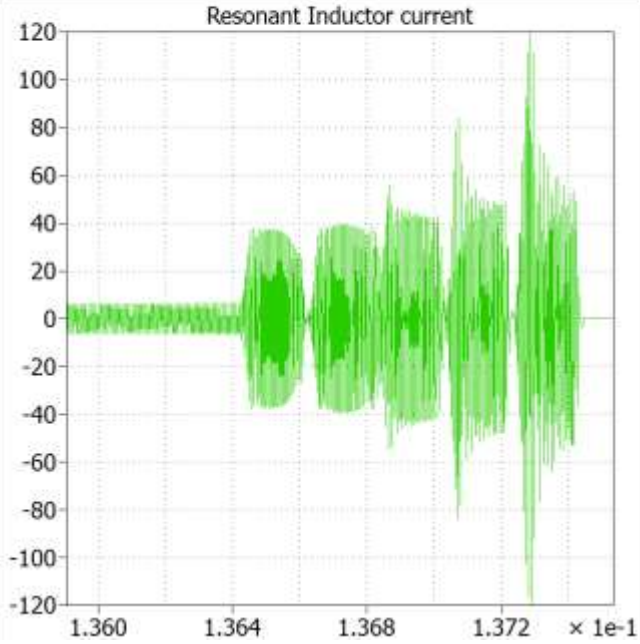
8. Appendix A: Simulations for System Safety

No control no relay

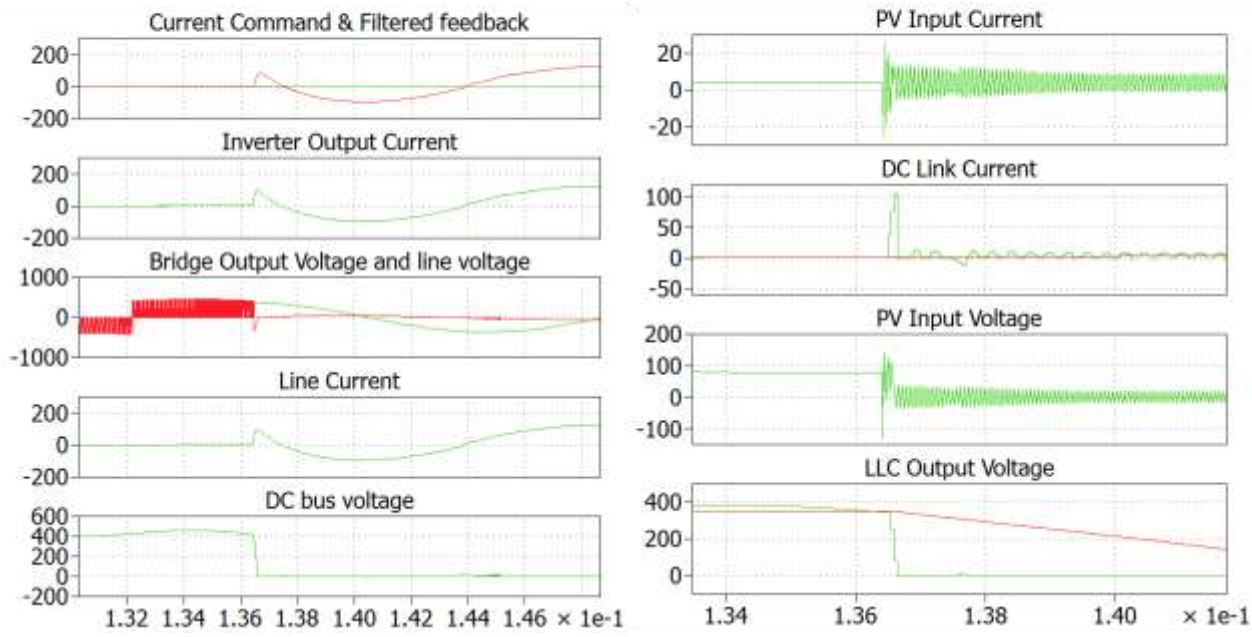
1. PV plus to ground:



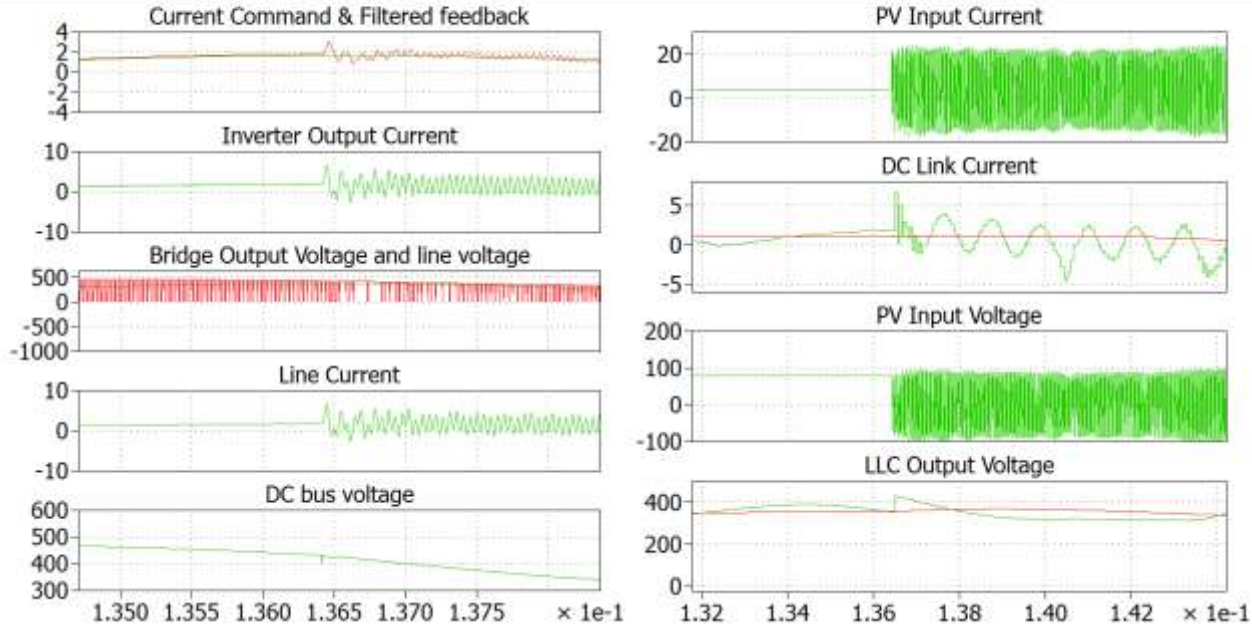
1. PV plus to ground:



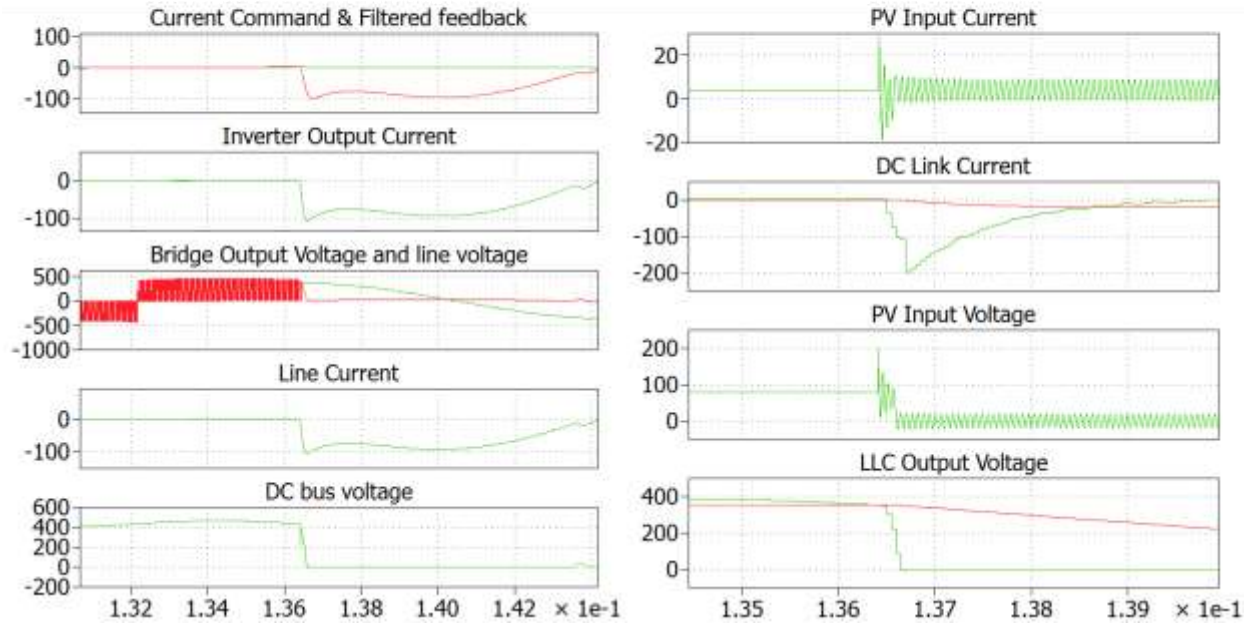
2. PV minus to ground:



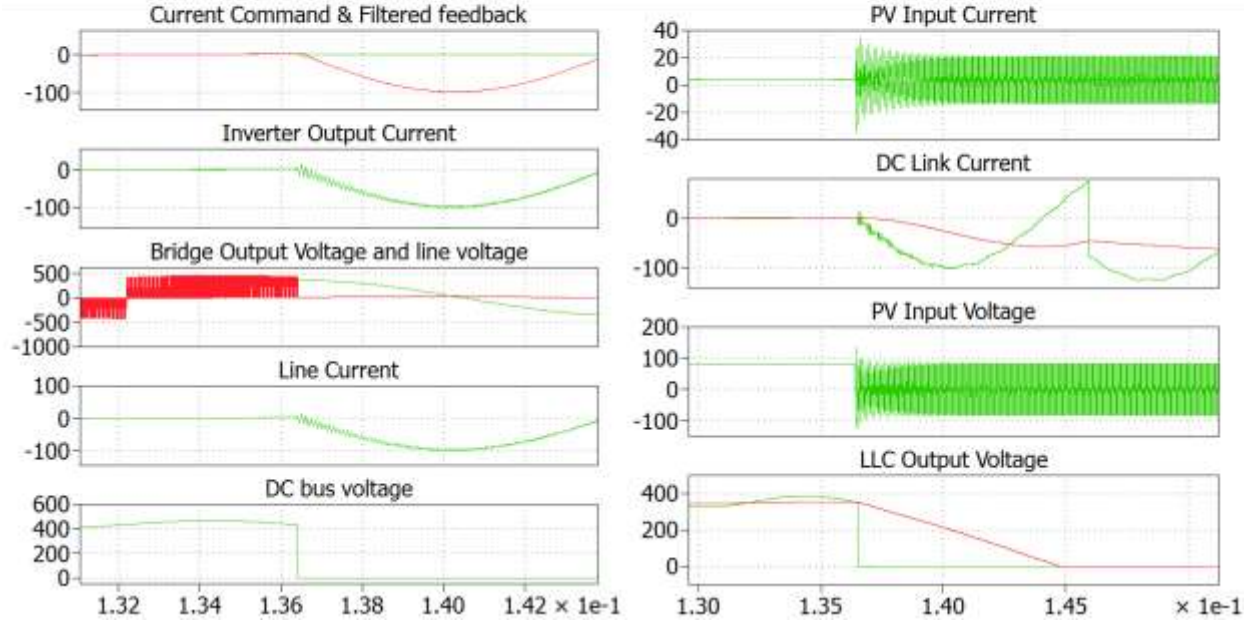
3. PV plus to minus:



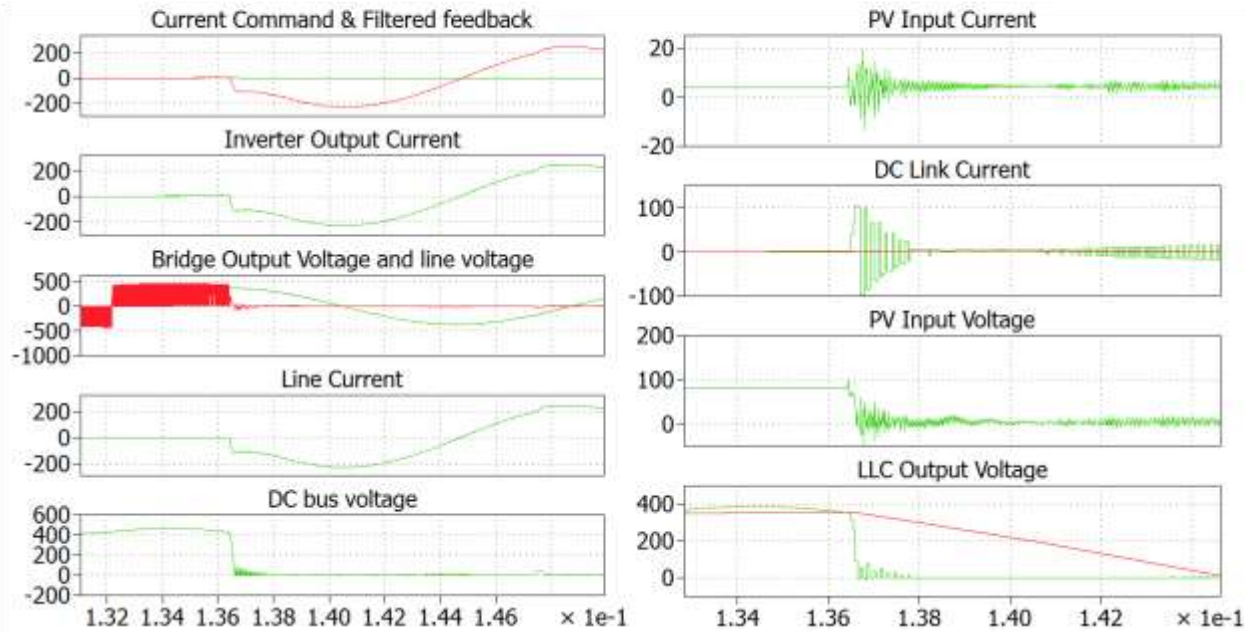
4. DC bus to ground:



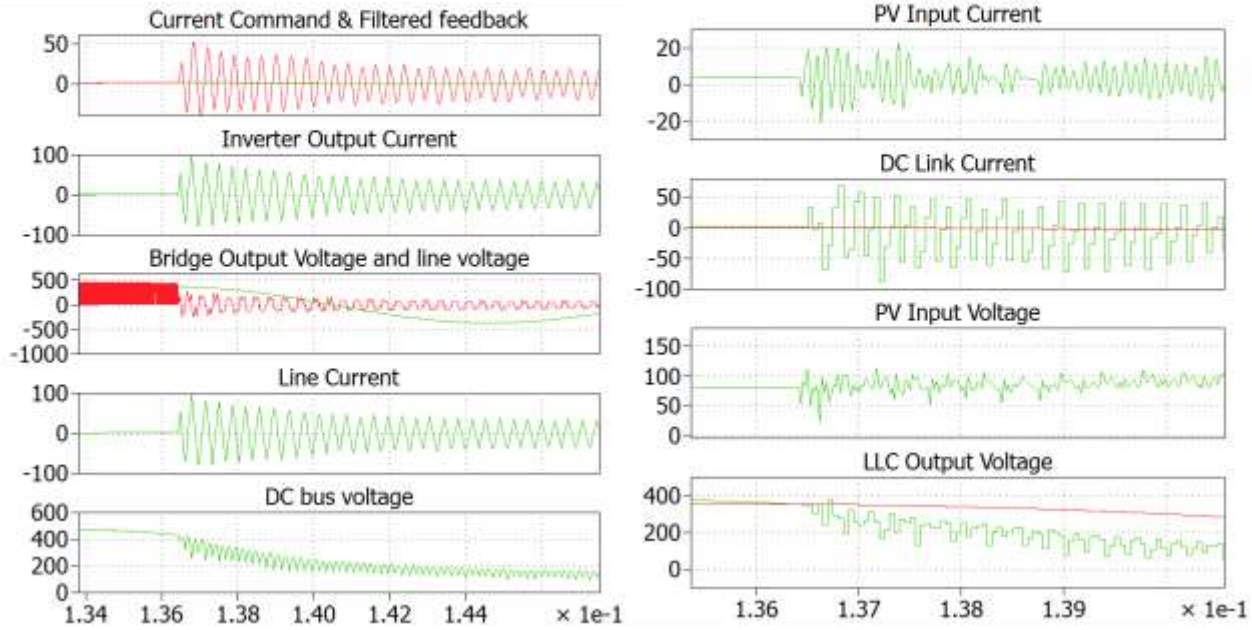
5. DC bus to DC minus:



6. Bridge output – point A to ground

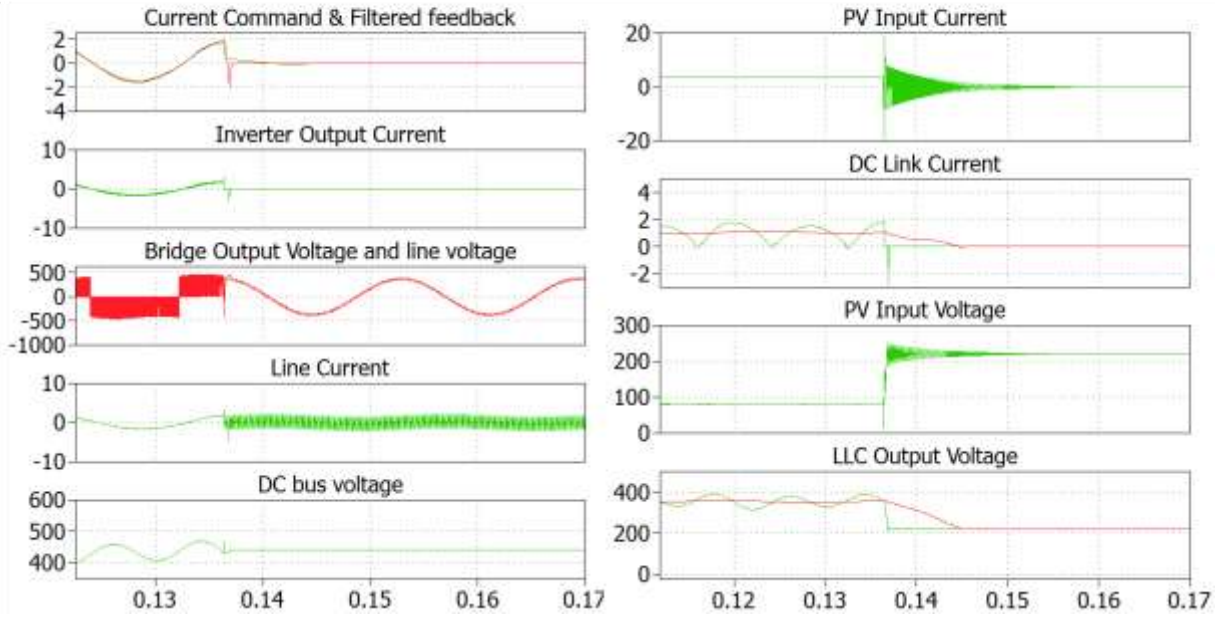


7. Bridge output – point B to ground

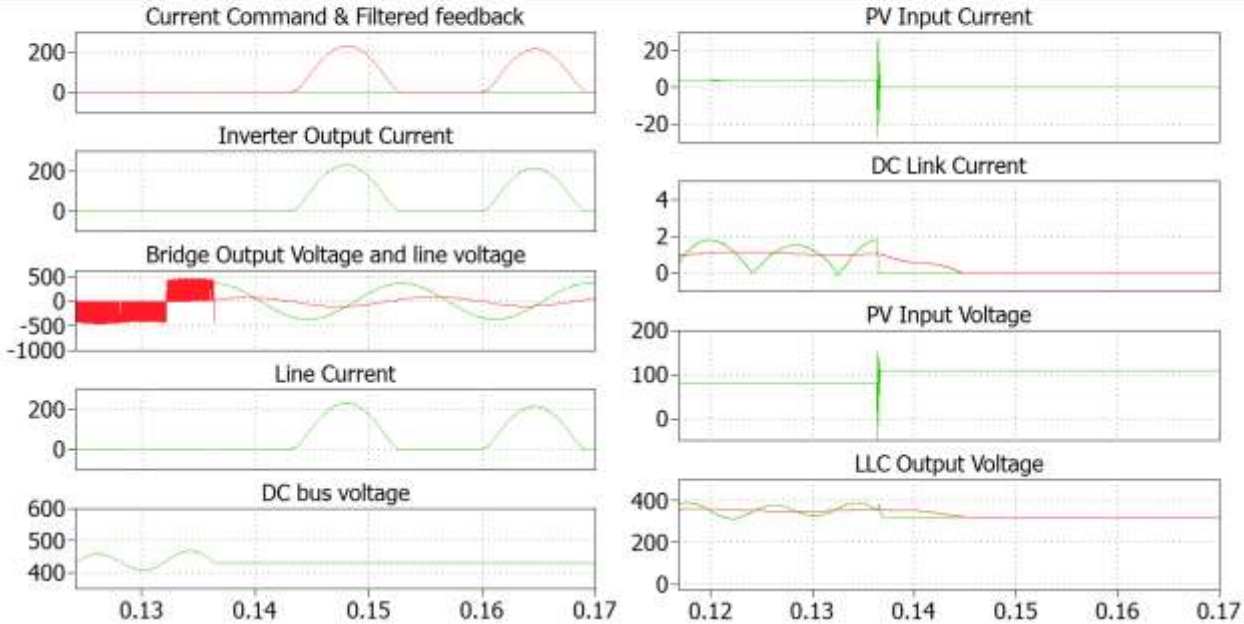


Control interrupt no relay

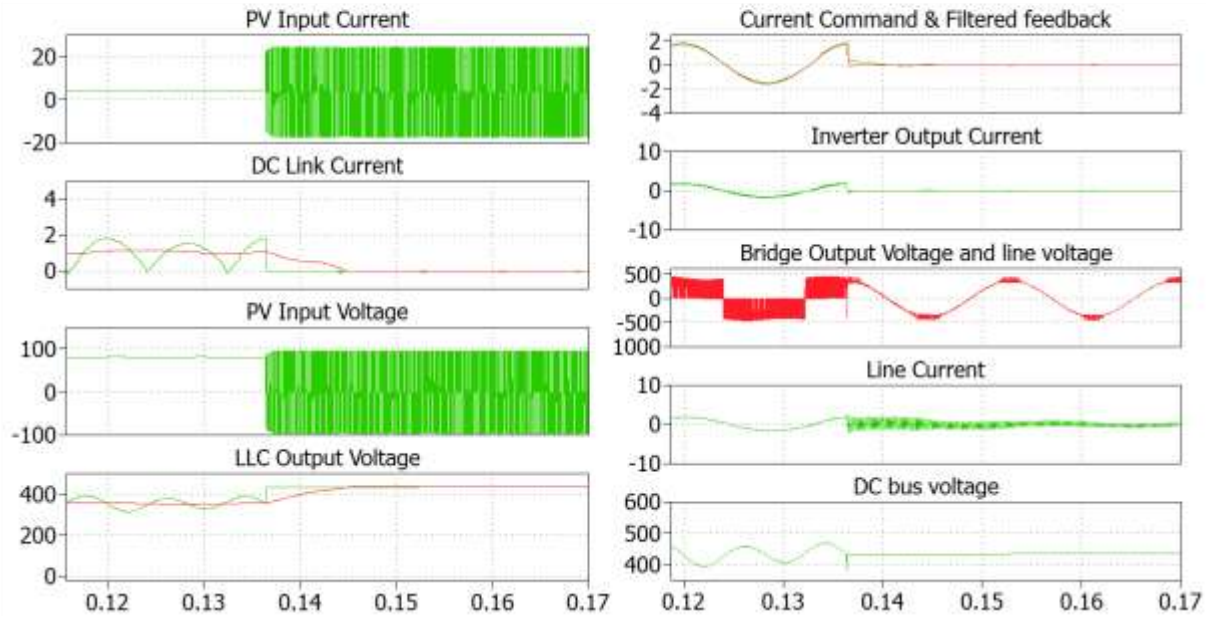
1. PV plus to ground:



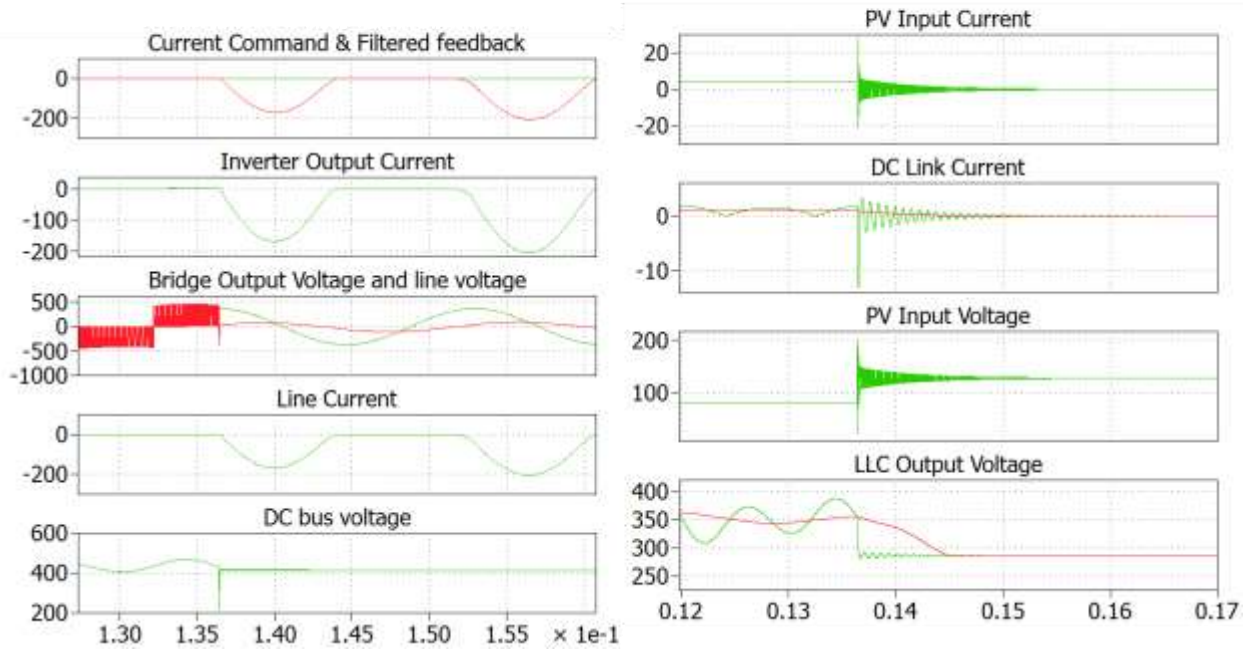
2. PV minus to ground:



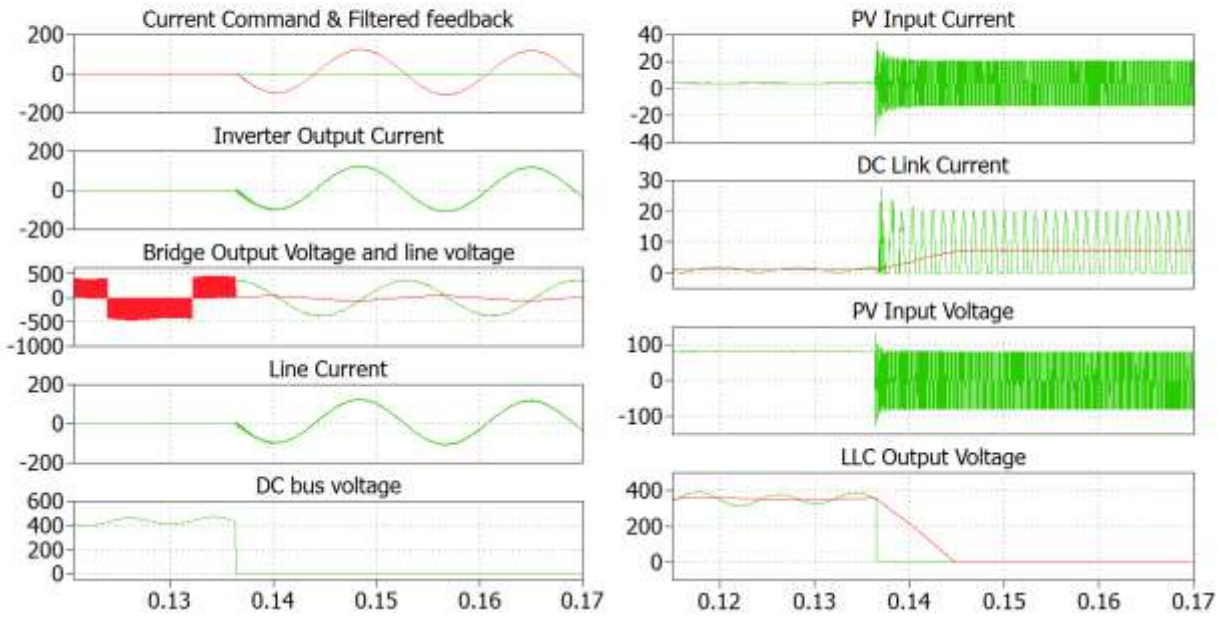
3. PV plus to minus:



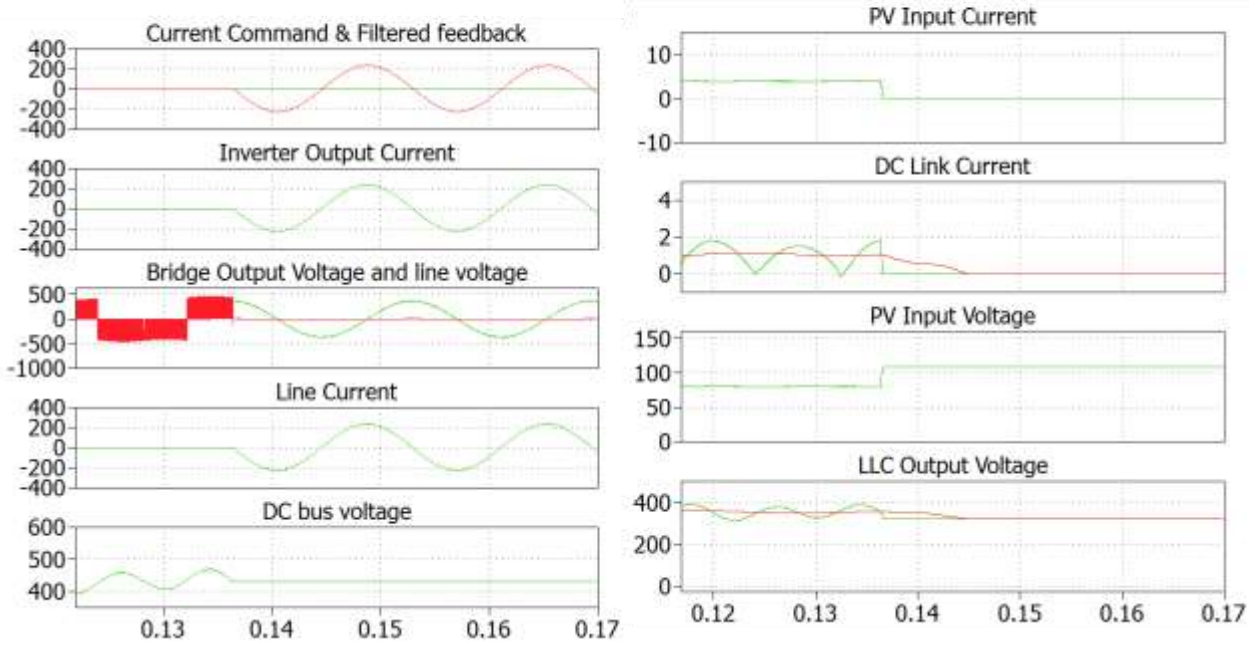
4. DC bus to ground:



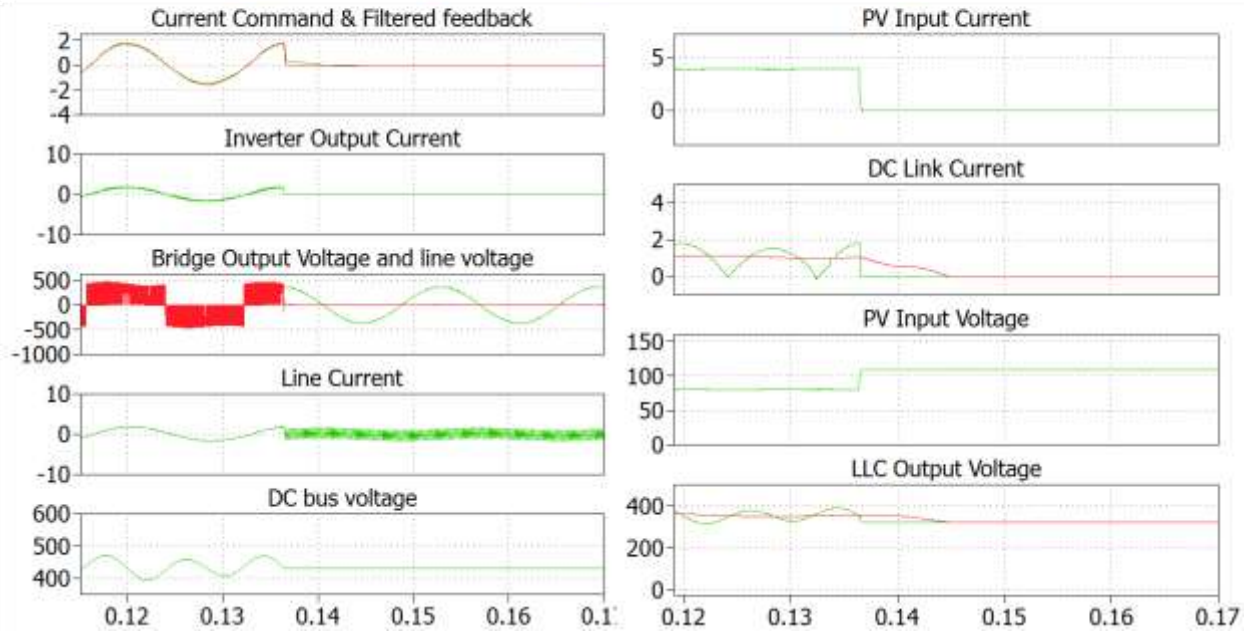
5. DC bus to DC minus:



6. Bridge output – point A to ground

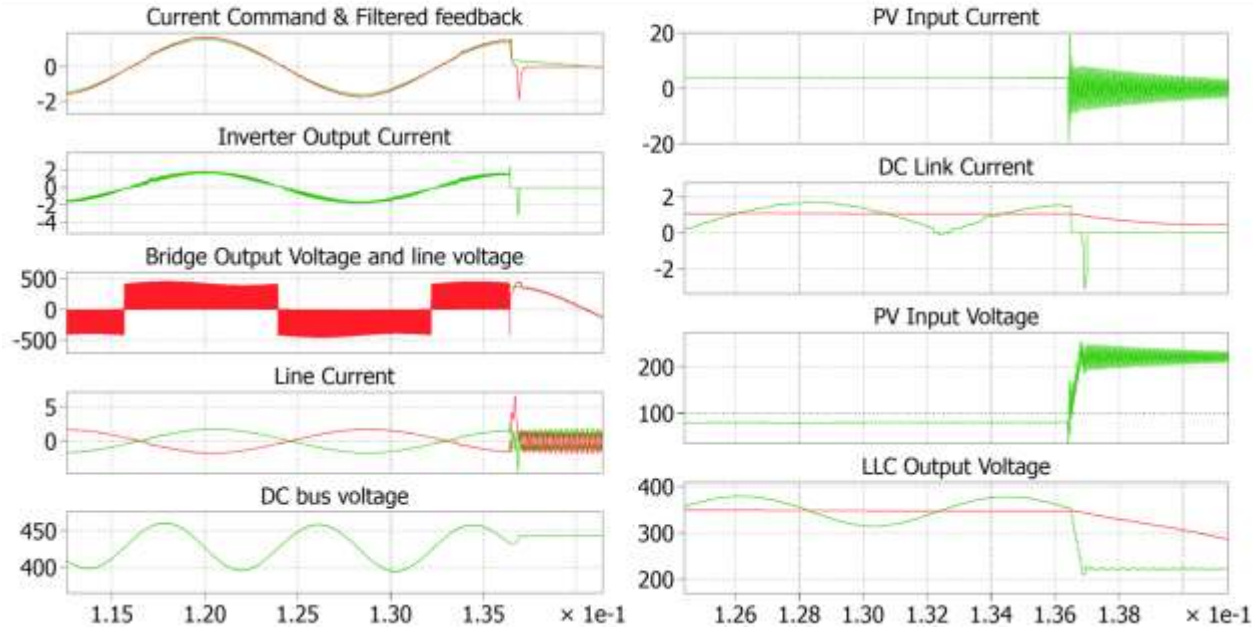


7. Bridge output – point B to ground

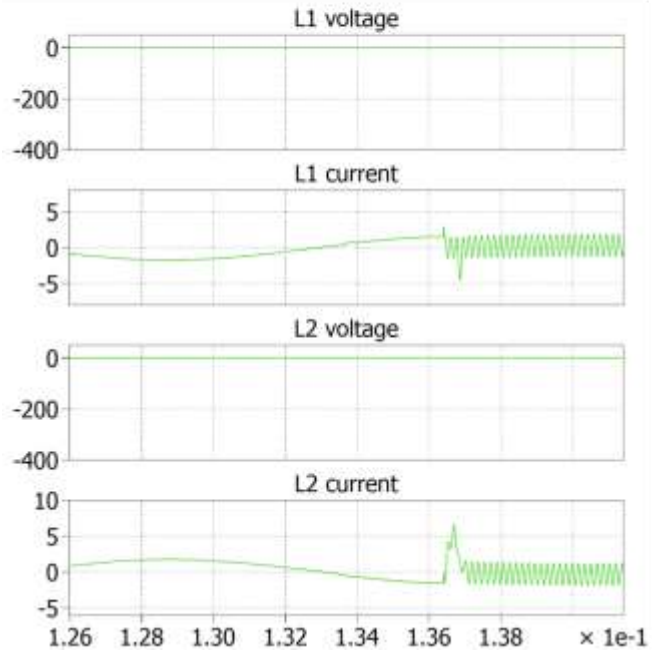


Control interrupt and relay (Trip Zone protection in 100 ns and relay opens in 5 ms, after fault):

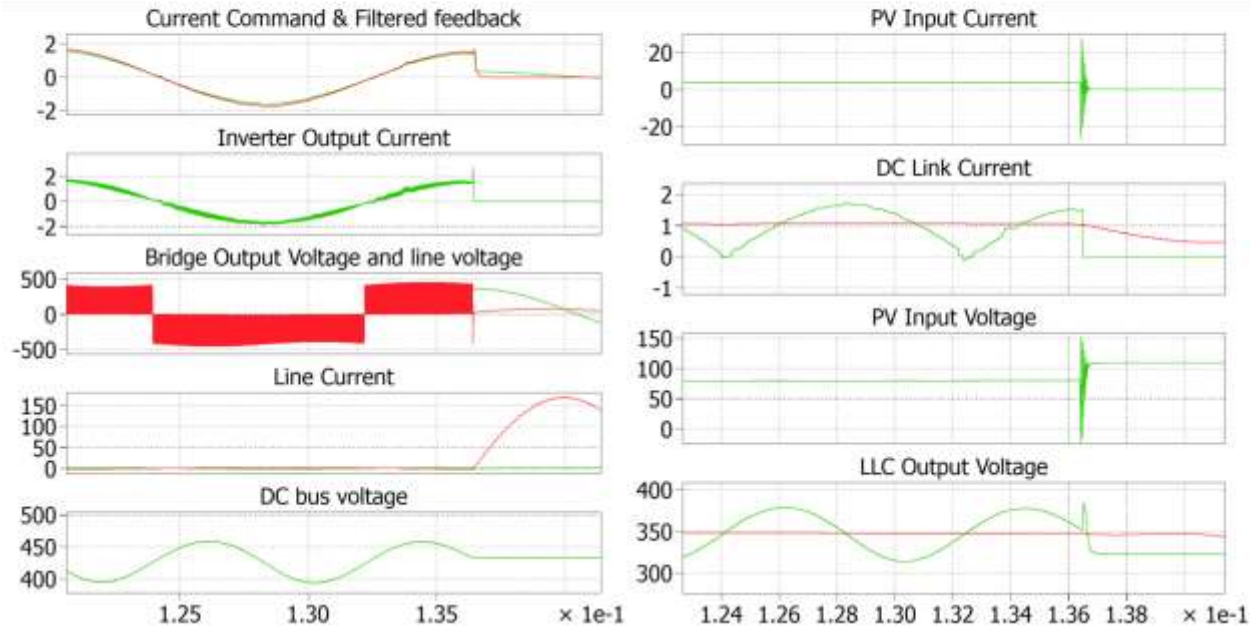
1. PV plus to ground:



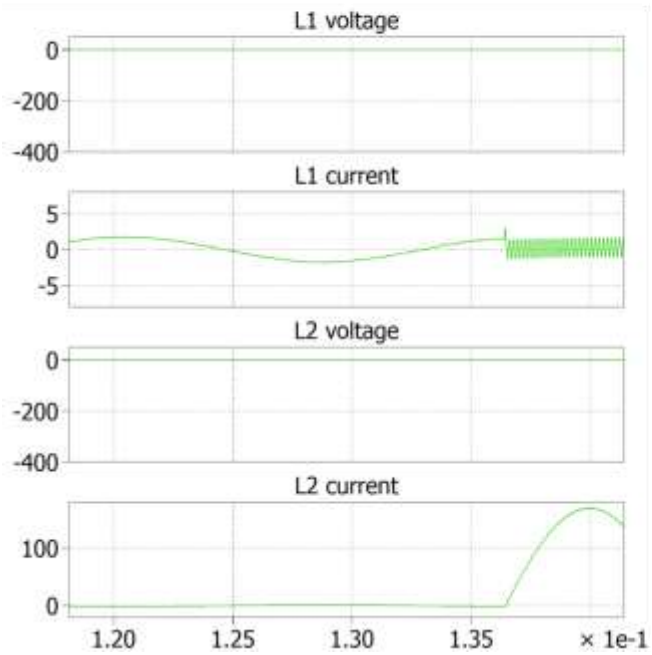
1. PV plus to ground:



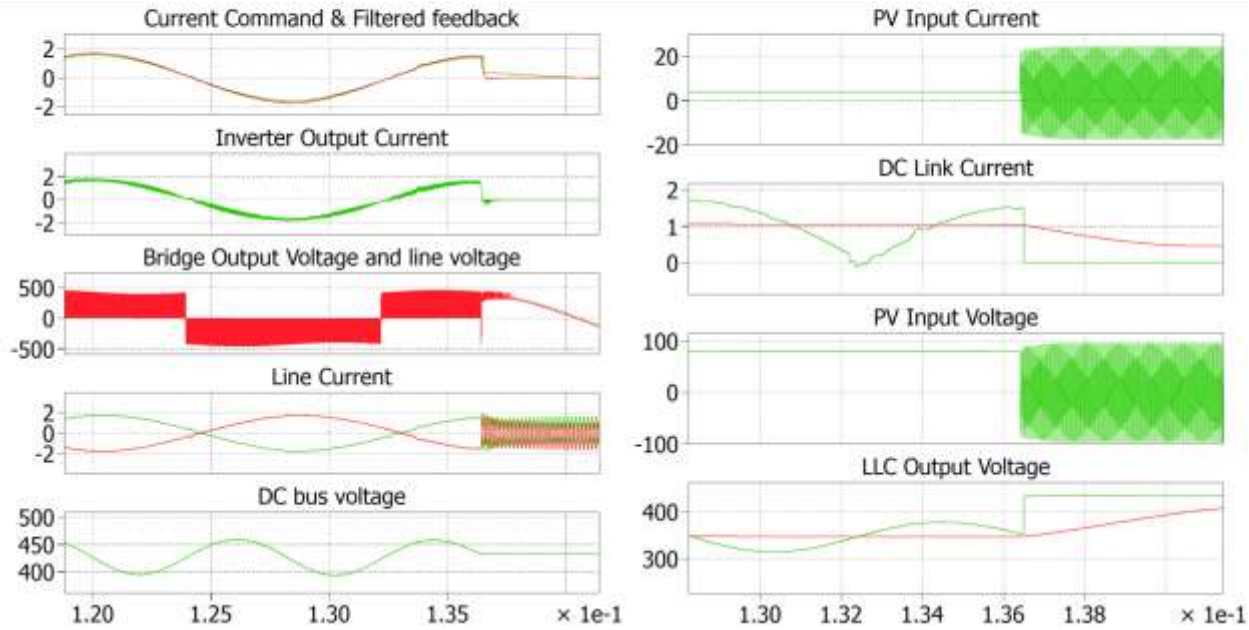
2. PV minus to ground:



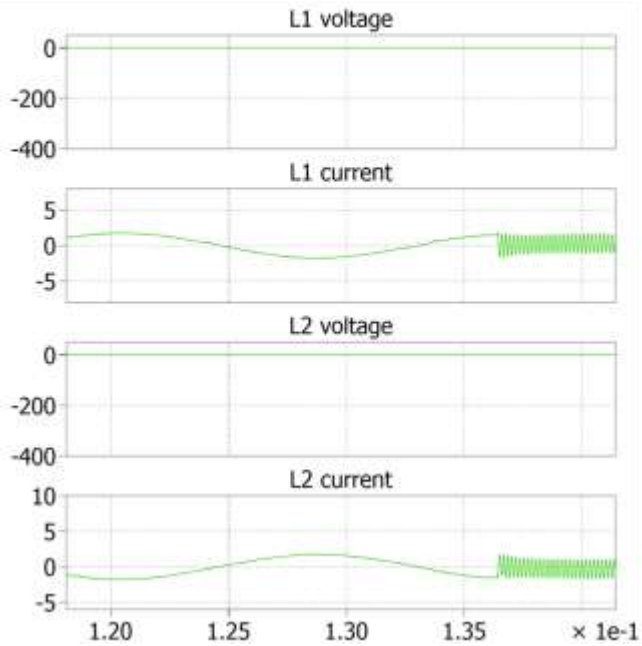
2. PV minus to ground:



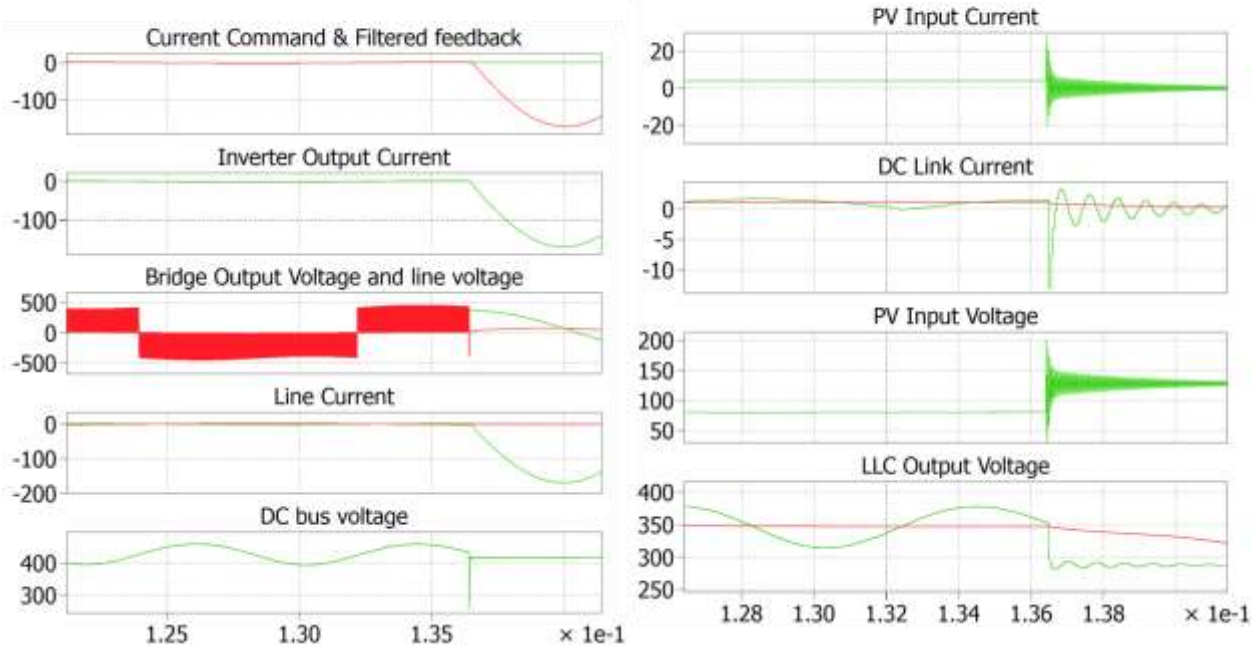
3. PV plus to minus:



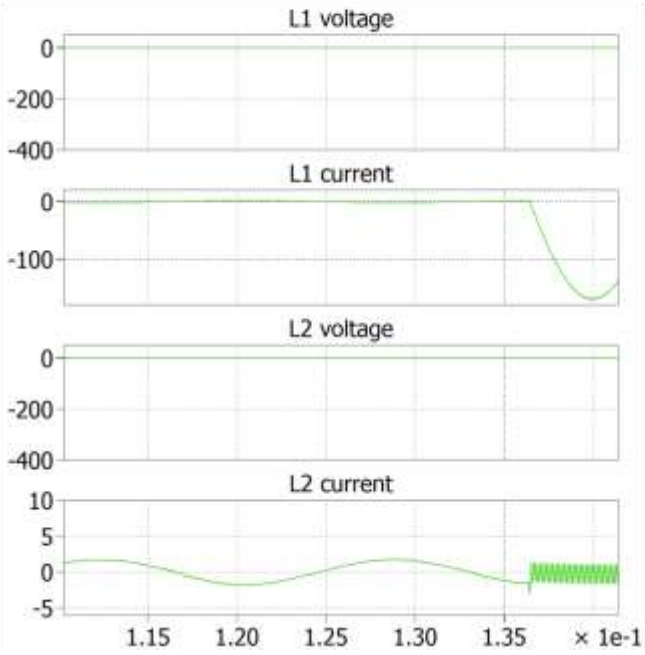
3. PV plus to minus:



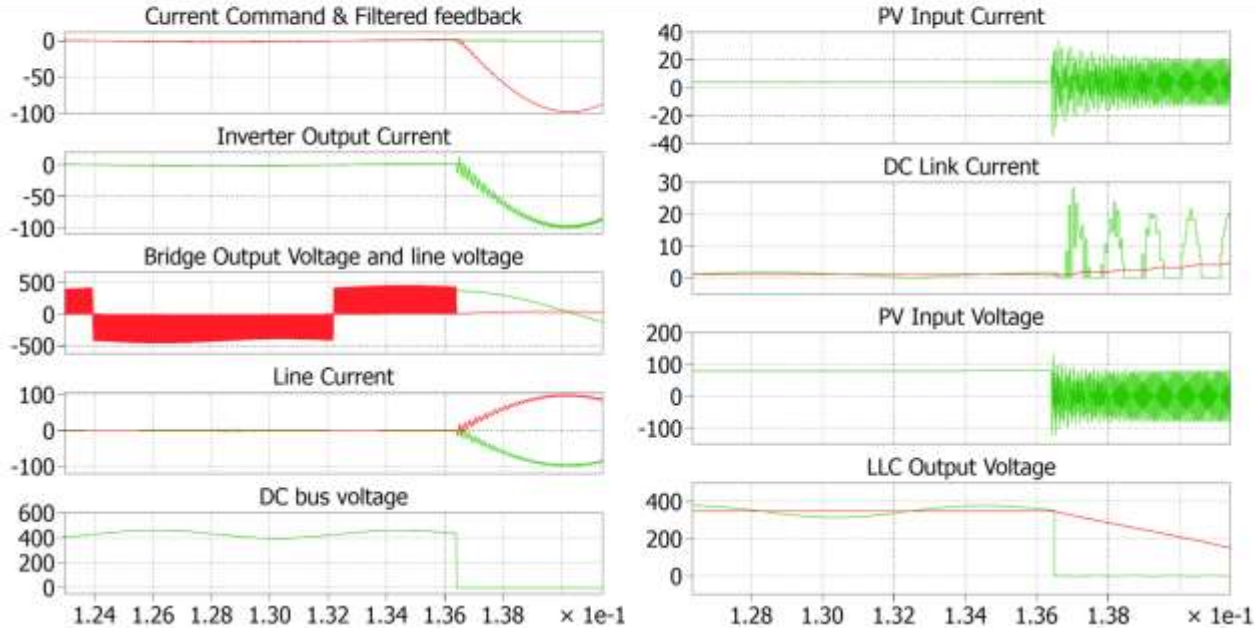
4. DC bus to ground:



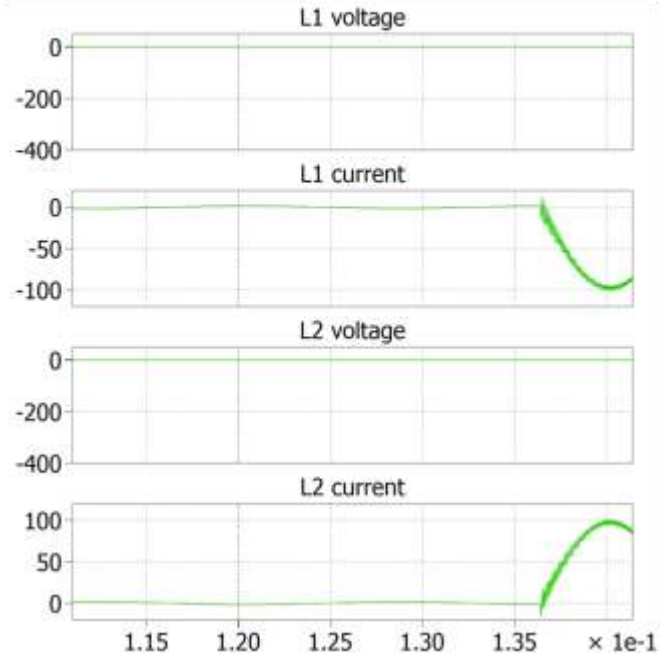
4. DC bus to ground:



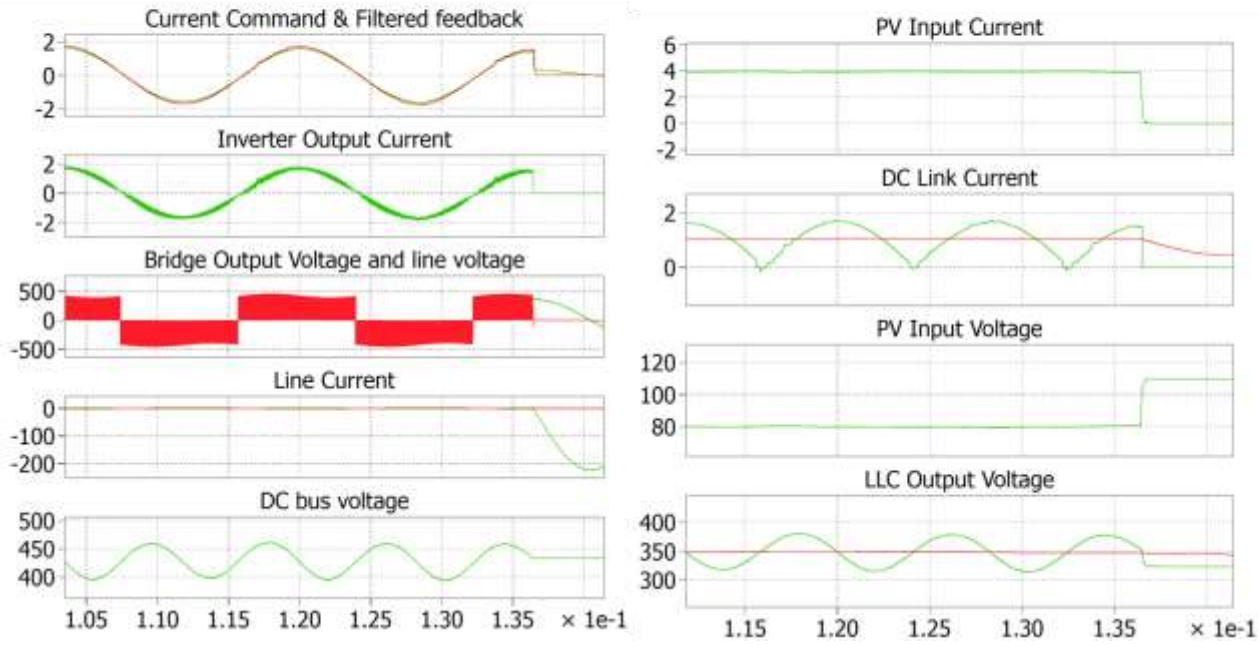
5. DC bus to DC minus:



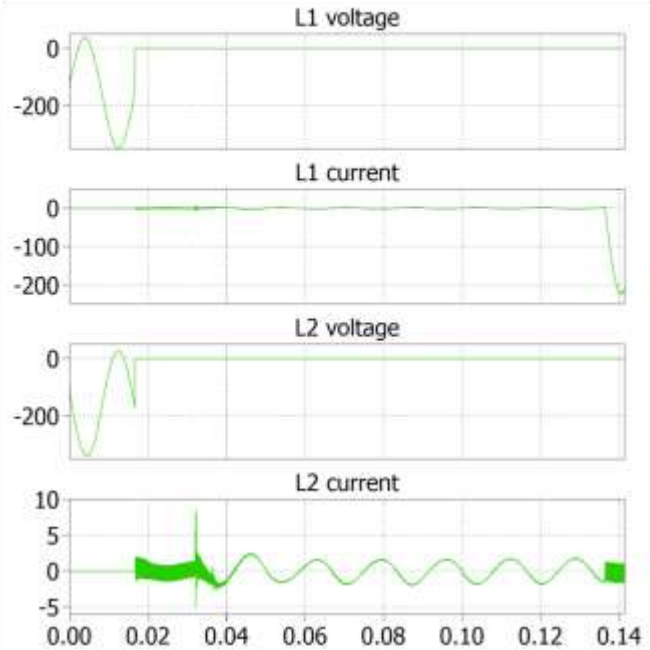
5. DC bus to DC minus:



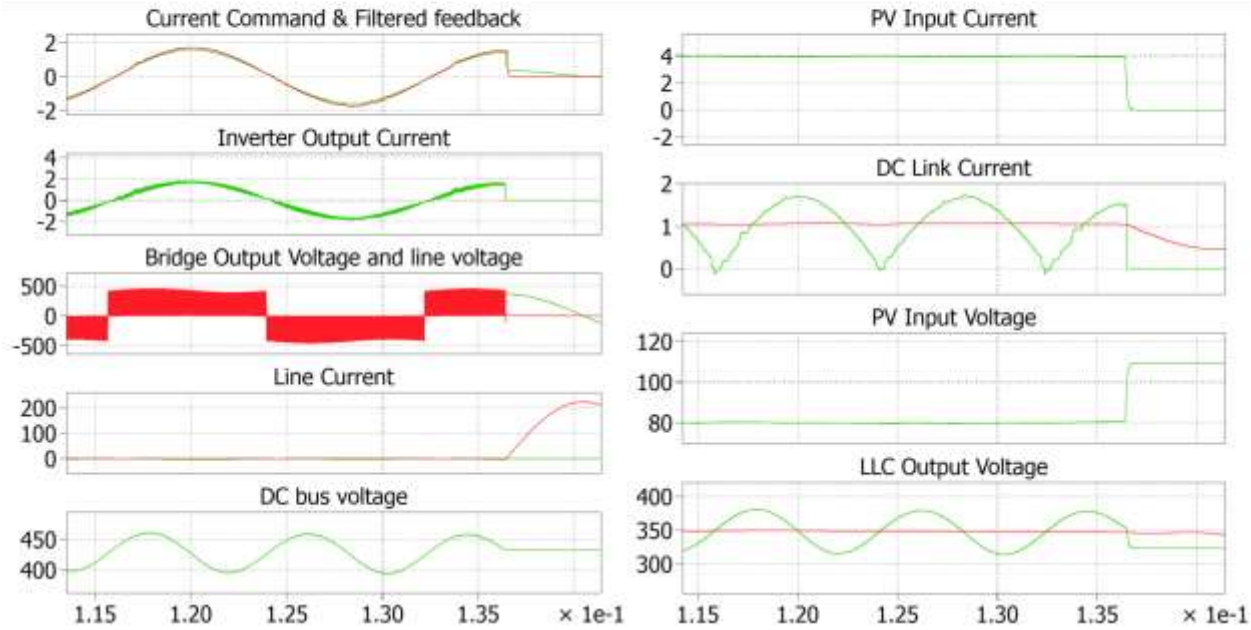
6. Bridge output – point A to ground



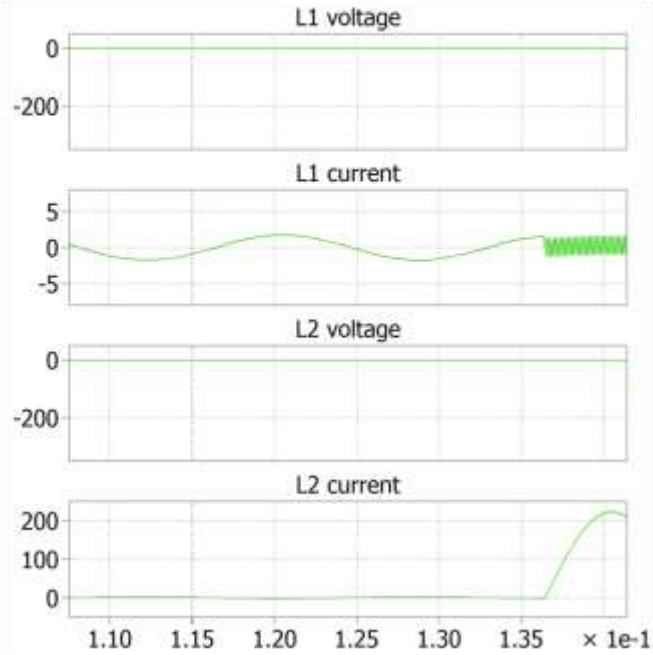
6. Bridge output – point A to ground



7. Bridge output – point B to ground



7. Bridge output – point B to ground



9. Appendix B: IEEE 1547 Tests

Voltage Test

Loading options:

a) 10% load
b) 100% loaf PF=1
c) 100% loaf PF=0.95
d) 100% loaf PF=-0.95

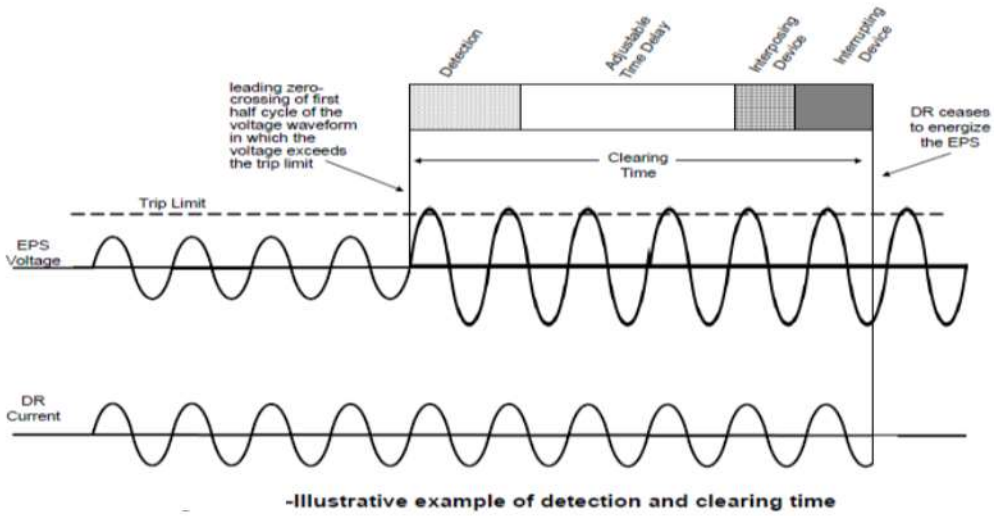
For each loading option test voltage magnitude and trip time:

1) Overvoltage 1 (110%Vnom =264V) magnitude
2) Overvoltage 1 (110%Vnom =264V) trip time
3) Overvoltage 2 (120%Vnom =288V) magnitude
4) Overvoltage 2 (120%Vnom =288V) trip time
5 Undervoltage 1 (88%Vnom =211V) magnitude
6) Undervoltage 1 (88%Vnom =211V) trip time
7) Undervoltage 2 (50%Vnom =120V) magnitude
8) Undervoltage 2 (50%Vnom =120V) trip time

Total 32 tests.

Abnormal Voltage

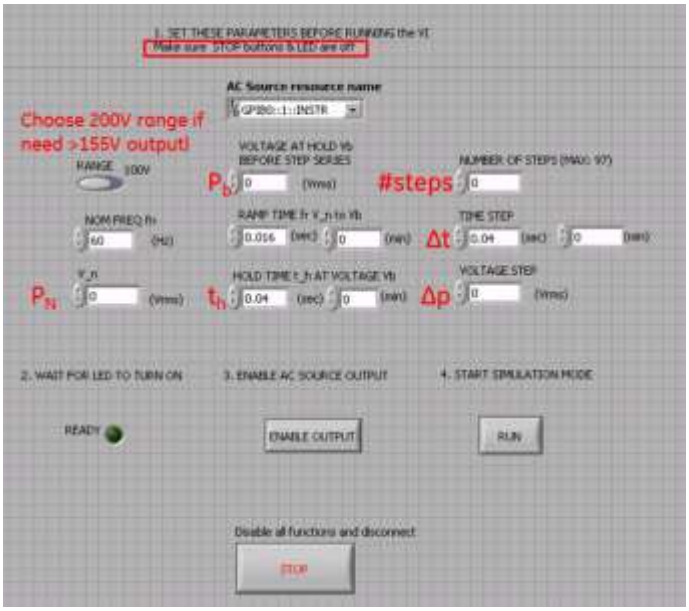
detection time: The minimum length of time from the inception of the abnormal condition to the change in state of the ICS's output dedicated to controlling the interrupting device. This is often on the order of 8 to 16 ms. *Syn:* processing time.
adjustable time delay: The intentional time added to the detection time in order to provide the desired clearing time. This may be adjustable from zero to several seconds.
interposing device time: The delay introduced in systems that include an auxiliary interface device, often an electromechanical hinged-armature relay. This is often on the order of 8 to 16 ms.
interrupting device time: Typically, the solenoid-initiated (trip) movement of the spring-loaded mechanism of the main current-carrying contacts of a circuit breaker plus any power arc interruption time (nonvacuum) that is dependant on the time to the next current zero-crossing. Interrupting device time varies widely from one half cycle to several cycles. For inverters, this would be the time needed to stop the bridge firing function and to cease energy outflow, which may be essentially zero time.
clearing time: The sum of the detection time, the adjustable time delay, the interposing devices time (if used), and the interrupting device time.
trip time: The interval that begins at the leading zero-crossing of the first half cycle of the voltage waveform in which the measured parameter (e.g., frequency, voltage, power) exceeds the trip limit and ends when the EUT responds as required. The trip time includes any time delay(s) used in conjunction with the ICS's protection functions. Depending on the EUT, the trip time can be a component of or equivalent to the clearing time.



-Illustrative example of detection and clearing time

VoltageMagnitudeTest.vi

- Change parameters on step 1
- Click arrow button on top left corner to start
- Follow instructions on front panel from 2 to 4
- Stop button can be pressed anytime when vi is running to disable output. If it's pressed when step 4 has not been reached, need to stop the vi use stop button
- The GPIB close function seems buggy. If wants to totally disconnect AC source from GPIB connect, have to exit LabView



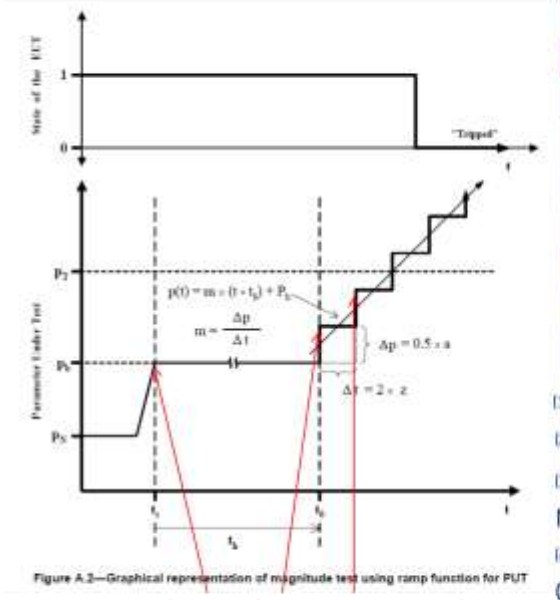


Figure A.2—Graphical representation of magnitude test using ramp function for PUT

At each step change, an active-low pulse is generated at SEQ TRI OUT port on the back of AC source

Setup values in LabView

	OV1	OV2	UV1	UV2
Pb (V)	125	130	110	108
Pt (V)	132	144	105.6	60
PN (V)	120 [1]	120	120	120
th (ms)	40 [2]	40	40	40
#steps	70+	70+	44+	96
Δt (ms)	40 [3]	40	40	40
Δp (V)	0.1 [4]	0.2 [5]	-0.1	-0.5

[1] =240/2 because of 1:2 transformer

[2] ≥ 2*(relay & sensing delay)

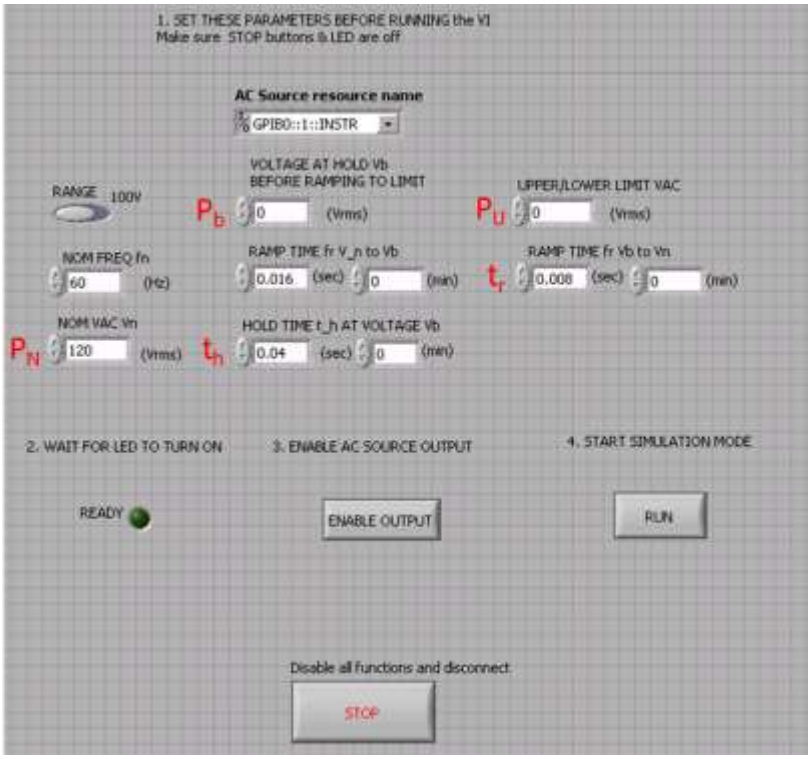
[3] =2*(relay & sensing delay)=2*(12+8)
Microcontroller detects Vpeak, not Vrms

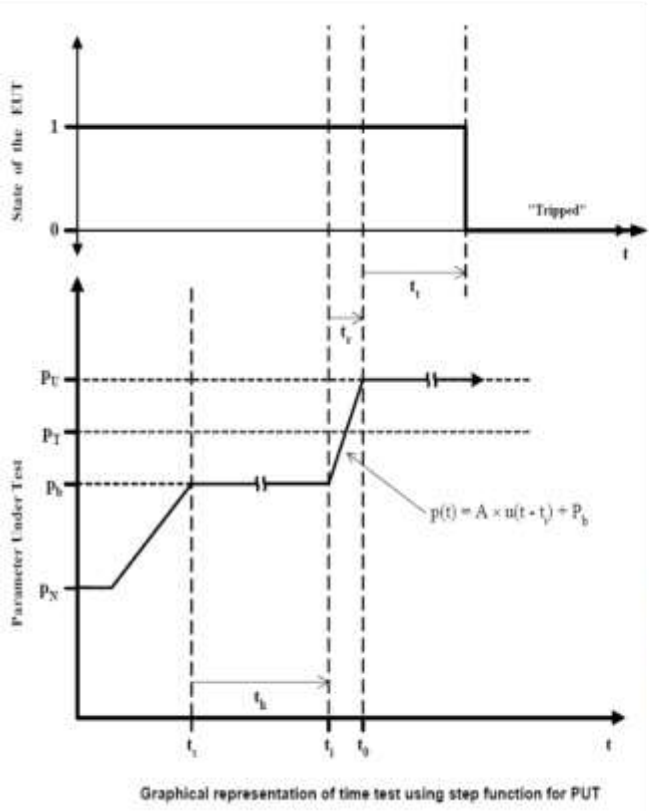
[4] Sensor resolution is 0.25V, but 0.1V is the resolution of AC source

[5] Can't use 0.1 because max #step is limited to 97

VoltageTripTimeTest.vi

- Instead of running voltage magnitude test, set AC source to output Pt (OV or UV value), then measure reading from micro-controller and use that value as trip point in the codes
- Then move on to voltage trip time test



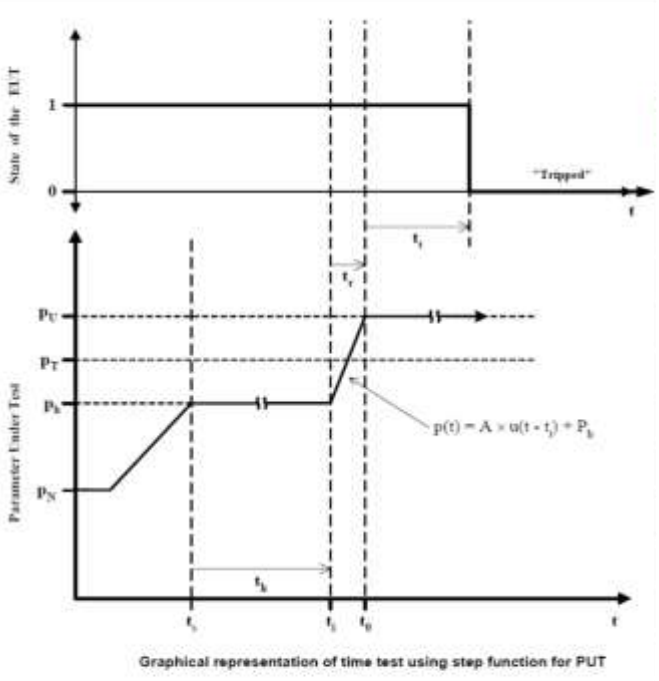


Graphical representation of time test using step function for PUT

Setup values in LabView

	OV1	OV2	UV1	UV2
Pb (V)	125	130	110	108
Pt (V)	132	144	105.6	60
PN (V)	120	120	120	120
PU (V)	132.5	144.5	105	59.5
th (ms)	40	40	40	40
tr (ms) [1]	8	8	8	8

[1] < larger of 1 cycle or 1% of the time-delay setting of the parameter under test (PUT)

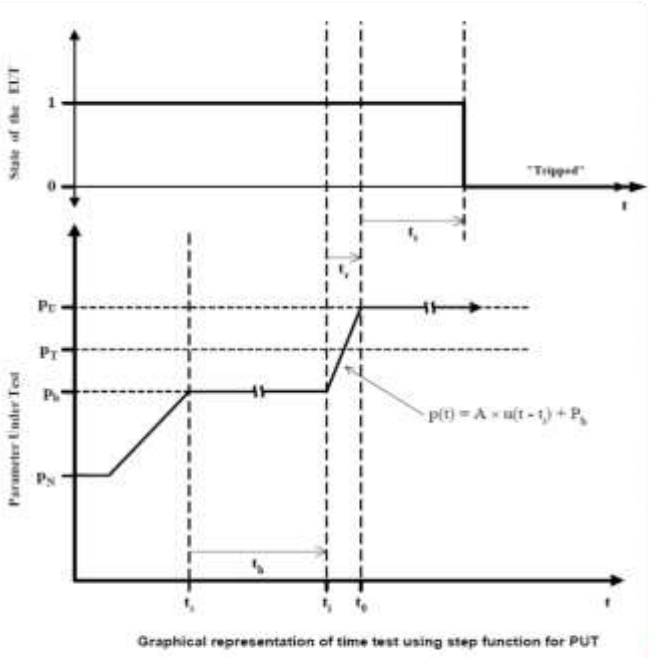


Graphical representation of time test using step function for PUT

Recorded values
100% load, pf = 1

	OV1	OV2	UV1	UV2
Pb (V)	231	141	204	200
Pt (V)	245	267	196	111
PN (V)	223	223	223	223
PU (V)	245	267	194	110
ts (ms)	0	0	0	0
ti (ms)	40	40	40	40
t0 (ms)	48	48	48	48
th (ms)	40	40	40	40
tr (ms)	8	8	8	8
tt (ms)	**8.4**	**28**	**20.8**	**15.2**

Meet standard requirement

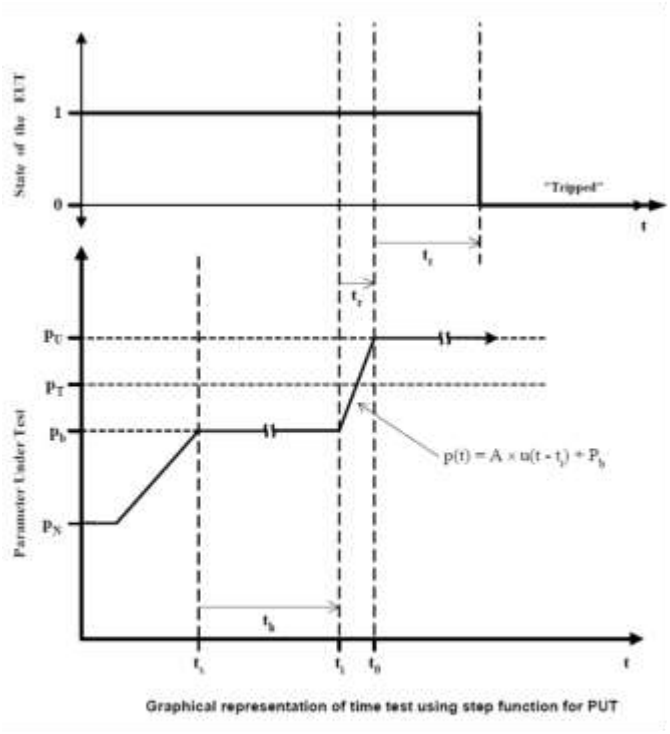


Graphical representation of time test using step function for PUT

Recorded values
100% load, pf =-0.95

	OV1	OV2	UV1	UV2
Pb (V)	231	141	204	200
Pt (V)	245	267	196	111
PN (V)	223	223	223	223
PU (V)	245	267	192	109
ts (ms)	0	0	0	0
ti (ms)	40	40	40	40
t0 (ms)	48	48	48	48
th (ms)	40	40	40	40
tr (ms)	8	8	8	8
tt (ms)	**10.8**	**20**	**18.4**	**13.6**

Meet standard requirement

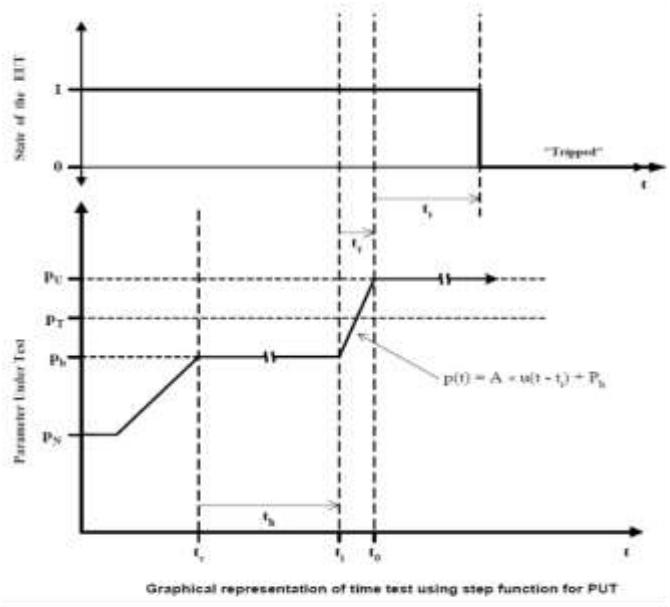


Graphical representation of time test using step function for PUT

Recorded values
100% load, pf = 0.95

	OV1	OV2	UV1	UV2
Pb (V)	231	141	204	200
Pt (V)	245	267	196	111
PN (V)	223	223	223	223
PU (V)	245	267	192	109
ts (ms)	0	0	0	0
ti (ms)	40	40	40	40
t0 (ms)	48	48	48	48
th (ms)	40	40	40	40
tr (ms)	8	8	8	8
tt (ms)	**19.2**	**17.2**	**24**	**9.6**

Meet standard requirement



Graphical representation of time test using step function for PUT

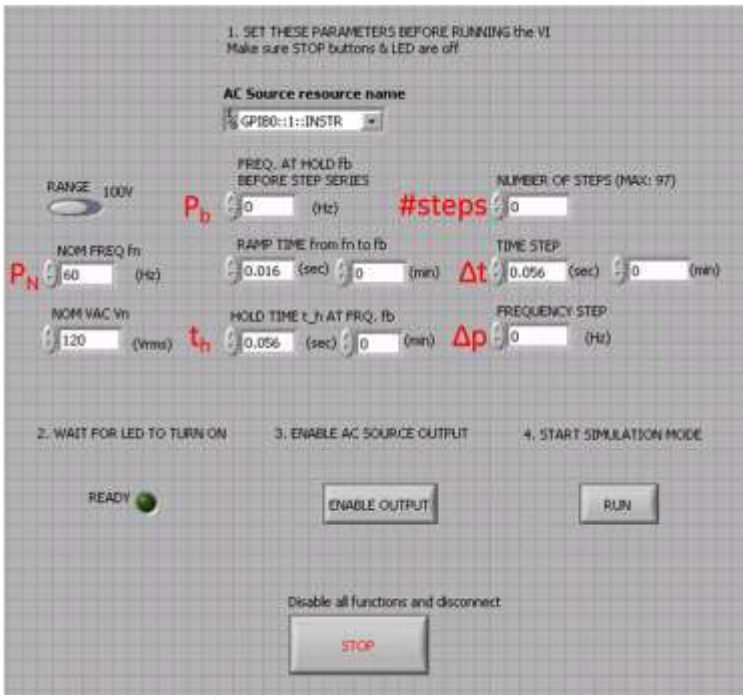
Recorded values
10% load, pf = 1

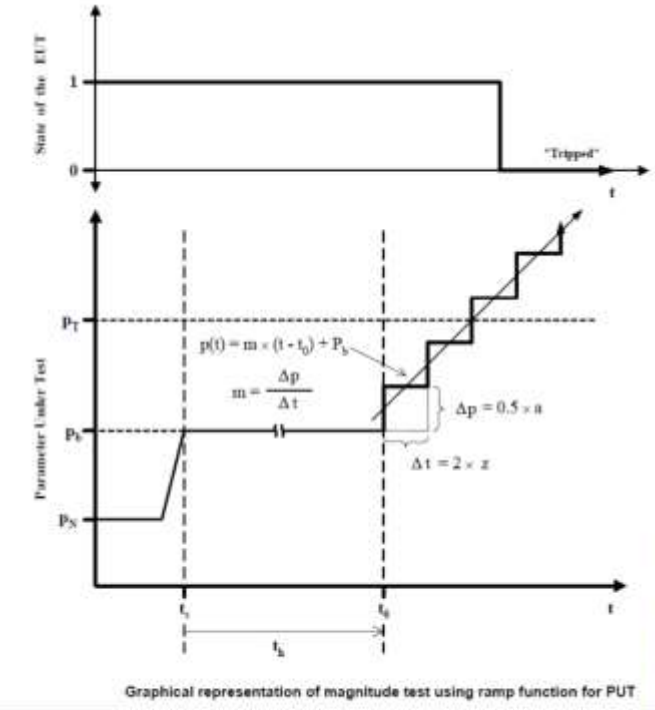
	OV1	OV2	UV1	UV2
Pb (V)	231	141	204	200
Pt (V)	245	267	196	111
PN (V)	223	223	223	223
PU (V)	245	267	192	109
ts (ms)	0	0	0	0
ti (ms)	40	40	40	40
t0 (ms)	48	48	48	48
th (ms)	40	40	40	40
tr (ms)	8	8	8	8
tt (ms)	**25.2**	**31.2**	**19.2**	**12.8**

Meet standard requirement

FrequencyMagnitudeTest.vi

- Instead of running this test, set AC source to output Pt (OF or UF value), then measure reading from micro-controller and use that value as trip point in the codes
- Then move on to frequency trip time test





Graphical representation of magnitude test using ramp function for PUT

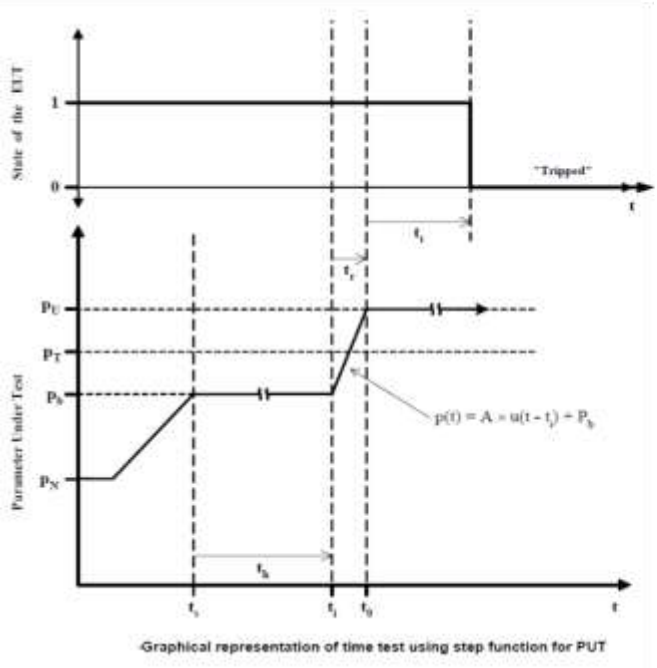
Setup values in LabView

	OF	UF
Pb (Hz)	60.2	59.6
Pt (Hz)	60.5	59.3
PN (Hz)	60	60
th (ms)	56	56
#steps	30+	30+
Δt (ms) [1]	56	56
Δp (Hz) [2]	0.01	-0.01

[1] =2*(relay & sensing delay)=2*(12+16)

[2] Supposed to be half of resolution of microcontroller's frequency calculation (executed every 16.7ms), but not sure how to determine the resolution. Use AC source resolution instead

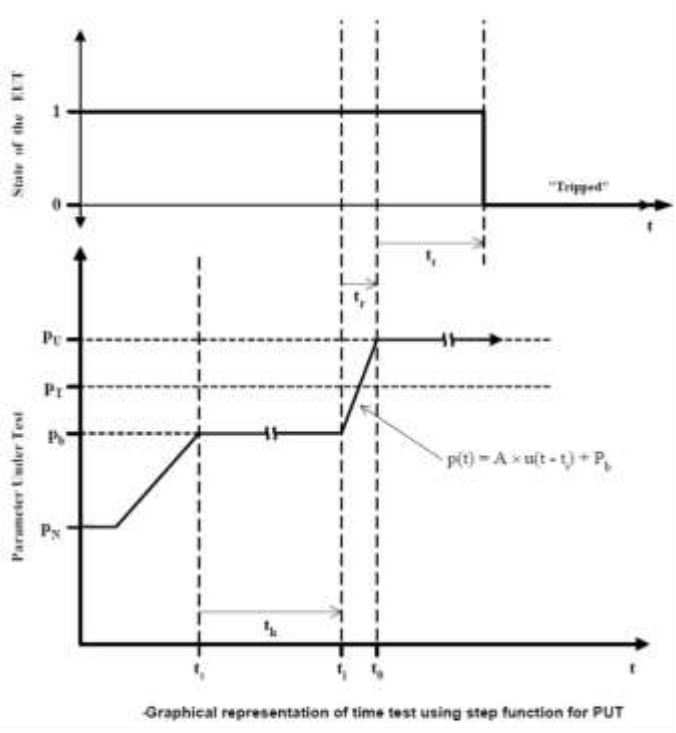
Frequency Trip Time



Graphical representation of time test using step function for PUT

Setup values in LabView

	OF	UF
Pb (Hz)	60.2	59.6
PN (Hz)	60	60
PU (Hz)	60.51	59.29
th (ms)	56	56
tr (ms)	10	10



Graphical representation of time test using step function for PUT

Recorded values

	OF	UF
Pb (Hz)	60.2	59.6
Pt (Hz)	60.5	59.3
PN (Hz)	60.0	60.0
PU (Hz)	60.51	59.29
ts (ms)	0	0
ti (ms)	56	56
t0 (ms)	64	64
th (ms)	56	56
tr (ms)	8	8
tt (ms)	**34.8**	**42.4**

Meet standard requirement