Final Report

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1. Executive Summary

The project focused on the development of high aspect ratio silicon heterojunction (HARSH) solar cells. The solar cells developed in this study consisted of high density vertical arrays of radial junction silicon microwires/pillars formed on Si substrates. Prior studies have demonstrated that vertical Si wire/pillar arrays enable reduced reflectivity and improved light trapping characteristics compared to planar solar cells. In addition, the radial junction structure offers the possibility of increased carrier collection in solar cells fabricated using material with short carrier diffusion lengths. However, the high junction and surface area of radial junction Si wire/pillar array devices can be problematic and lead to increased diode leakage and enhanced surface recombination. This study investigated the use of amorphous hydrogenated Si in the form of a heterojunction-intrinsic-thin layer (HIT) structure as a junction formation method for these devices. The HIT layer structure has widely been employed to reduce surface recombination in planar crystalline Si solar cells. Consequently, it was anticipated that it would also provide significant benefits to the performance of radial junction Si wire/pillar array devices.

The overall goals of the project were to demonstrate a HARSH cell with a HIT-type structure in the radial junction Si wire/pillar array configuration and to develop potentially low cost pathways to fabricate these devices. Our studies demonstrated that the HIT structure lead to significant improvements in the open circuit voltage (V_{oc}>0.5) of radial junction Si pillar array devices compared to devices fabricated using junctions formed by thermal diffusion or low pressure chemical vapor deposition (LPCVD). In addition, our work experimentally demonstrated that the radial junction structure lead to improvements in efficiency compared to comparable planar devices for devices fabricated using heavily doped Si that had reduced carrier diffusion lengths. Furthermore, we made significant advances in employing the bottom-up vapor-liquid-solid (VLS) growth technique for the fabrication of the Si wire arrays. Our work elucidated the effects of growth conditions and substrate pattern geometry on the growth of large area Si microwire arrays grown with $SiCl_4$. In addition, we also developed a process to grow p-type Si nanowire arrays using aluminum as the catalyst metal instead of gold. Finally, our work demonstrated the feasibility of growing vertical arrays of Si wires on non-crystalline glass substrates using polycrystalline Si template layers. The accomplishments demonstrated in this project will pave the way for future advances in radial junction wire array solar cells.

2. Comparison of Goals and Accomplishment

The project was high risk/high reward and required the development of a number of new processing and device fabrication schemes in order to achieve the planned tasks and milestones. Nevertheless, the majority of tasks were fully completed and the main goal of the project – the demonstration of a HARSH cell in the radial junction configuration – was realized. The task and milestone description from the original proposal is included in Table 1 along with a comparison of the project accomplishments. A brief description of the problems encountered is also included for tasks and milestones that were unable to be completed during the duration of the project.

Table 1. Summary of project tasks and milestones and accomplishments/problems.

Task	Description	Accomplishments/Problems Encountered
1	**Device design and modeling**	**Fully completed**
1.1	Numerical simulation of HARSH cell	COMSOL model of radial p-n junction solar cell developed
2	**Si wire array growth**	**Fully completed**
2.1	Si wire growth on patterned (111)Si	Extensive studies of Si wire growth on (111)Si were carried out
2.2	Si wire growth on patterned glass	Si wire array growth on poly-Si templated glass substrates demonstrated
2.3	Alternative catalyst development	Si wire array growth with Cu, In and Al demonstrated
3	**Si-liquid junction studies**	**Fully completed**
3.1	Surface passivation development	Not required since amorphous Si was found to be an effective passivant.
3.2	Interface state characterization	Liquid junction devices used to evaluate VLS-grown Si wire arrays.
4	**Radial p-n junction development**	**Fully completed**
4.1	PECVD of intrinsic/doped a-Si:H shell	Detailed studies of PECVD shell layers carried out.
4.2	LPCVD of epitaxial doped Si shell	Detailed studies of LPCVD shell layers carried out.
5	**TEM Characterization**	**Fully completed**
5.1	Structural characterization of Si wires	Extensive TEM characterization of Si wire arrays carried out.
5.2	a-Si/c-Si and c-Si/c-Si interface studies	High resolution TEM images of a-Si/c-Si and c-Si/c-Si interfaces obtained.
6	**Electrical Characterization**	**Partially completed**
6.1	Top contact fabrication and packaging	TCO top contact developed for solar cells
6.2	Diode characterization	All planned solar cell devices were fully characterized except a-Si/c-Si heterojunctions formed on VLS grown Si wire arrays and solar cells on glass substrates. This was due to unexpected shorting problems encountered on VLS grown Si wire arrays that could not be resolved within the timeframe of the project.
6.3	Solar cell testing	
Milestones		
1	Demonstration of 10% efficiency HARSH cell on Si substrate	HARSH cell with 9.8% efficiency demonstrated on Si substrate
2	Demonstration of 15% efficiency HARSH cell on Si substrate	High series resistance in HARSH cell prevented further efficiency improvements
3	Demonstration of 15% efficiency HARSH solar cell on glass	Problems with shorting of VLS grown Si wire arrays prevented HARSH solar cell demonstration on glass

3. Summary of Project Activities

The main project activities were divided into three main categories: 1) Si wire array growth; 2) radial p-n junction fabrication and 3) solar cell fabrication and testing. A summary of the accomplishments and problems encountered in each of the topics is included below.

3.1 Si Wire Array Growth

Extensive studies of the vapor-liquid-solid growth of Si microwires and nanowires arrays were carried out in this project. The studies focused on three primary topics: 1) VLS growth and intentional doping of Si microwire arrays on gold patterned Si substrates using a high temperature $SiCl_4$ growth process; 2) Investigation of alternative catalysts to gold for VLS growth of Si nanowires and 3) VLS growth of Si nanowires on polycrystalline Si templates on glass formed by aluminum-induced crystallization. A summary of the significant accomplishments in each of these topics is provided below.

3.1.1 VLS growth and doping of Si microwire arrays

The VLS growth of Si microwire arrays on gold patterned Si substrates using $SiCl_4$ was investigated for the formation of the Si wire array cores that were used for the fabrication of radial p-n junction solar cells. The effect of pattern size and density on the growth rate of Si microwires was initially investigated. For large diameter (>1 μm) Si microwires, it was found that the growth rate decreased with increasing wire diameter and also for higher packing densities.[1] This decrease in growth rate was explained as arising from the increased time required to supersaturate the large gold liquid droplets with Si and competition for the Si source gas as the packing density increased. The results of this work lead to the development of growth conditions which enabled the fabrication of large area arrays of Si microwires (Figure 1) that were suitable for device fabrication.

Intentional p-type doping of Si micro/nanowires grown using $SiCl_4$ was also investigated. This work utilized trimethylboron (TMB) as the boron dopant source. The electrical properties of the boron-doped Si nanowires were extensively characterized to evaluate the uniformity of doping along the axial and radial directions of the nanowires. Prior studies of B-doped Si nanowires grown with SiH_4 had demonstrated significant dopant variation along the wire length and radius due to sidewall doping that occurred during nanowire growth.[2] Our studies revealed that the uniformity of B-doping in the Si nanowires was significantly improved in both the axial and radial directions for wires grown with $SiCl_4$ and TMB.[3] The improved doping uniformity is believed to arise as a result of the significantly reduced vapor-solid deposition on the nanowire sidewalls with $SiCl_4$-based growth

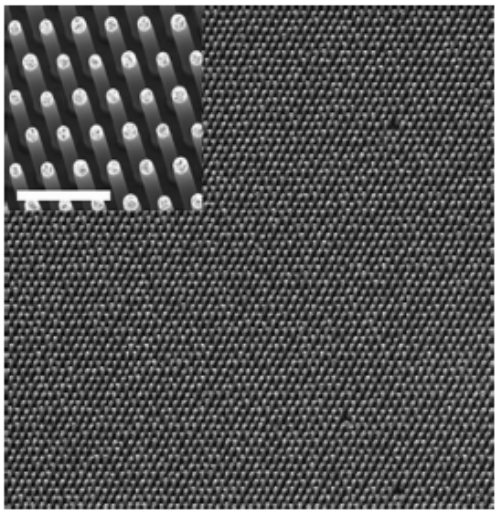

Figure 1. SEM image of Si microwire array (400 μm x 400 μm area). Inset is a higher magnification image of the microwires. Scale bar of inset is 20 μm

[1] C.E. Kendrick and J.M. Redwing, J. Crystal Growth 337, 1 (2011).
[2] R.A. Schlitz, D.E. Perea, J.L. Lensch-Falk, E.R. Hemesath and L.J. Lauhon, Appl. Phys. Lett. 95, 162101-3 (2009).
[3] M.W. Kuo, C.E. Kendrick, J.M. Redwing and T.S. Mayer, manuscript in preparation.

chemistry. The results suggest that the $SiCl_4$-based growth process may be preferred for the growth of micro/nanowire arrays for solar cells due to the ability to achieve high doping uniformity in the wires.

3.1.2 Investigation of alternative catalysts to gold for VLS growth of Si nanowires

It is well known that gold introduced deep level states within the bandgap of Si that lead to reduced minority carrier lifetimes. Consequently, there is significant interest in identifying alternative catalysts for VLS growth. Prior studies have demonstrated the use of Cu for Si microwire array growth and solar cell fabrication. However, Cu also forms deep levels in Si. Our studies therefore focused on investigating the use of Al as the catalyst for Si nanowire growth. Al is a shallow acceptor in Si and therefore was expected to auto-dope the Si nanowires during growth. Our initial work demonstrated the growth of Si nanowires using Al in a low pressure CVD (LPCVD) system using SiH_4 as the source gas.[4] This work revealed that high SiH_4 and H_2 partial pressures were needed in order to initiate and sustain nanowire growth. In addition, the Si nanowires were found to be heavily doped with Al during the growth process. Subsequent chemical analysis of the Al-catalyzed Si nanowires by local electrode atom probe tomography demonstrated that Al was present at levels much higher (>10^{19} cm^{-3}) than expected from solid solubility considerations.[5] Single wire radial p-n diodes were

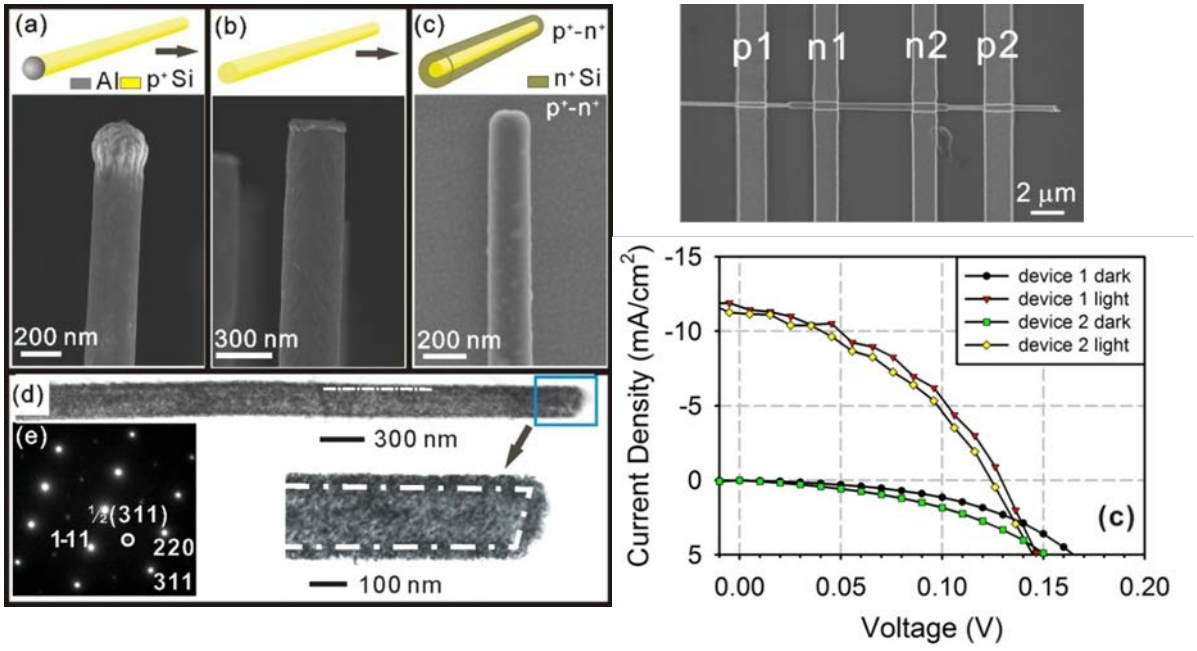

Figure 2. Radial p+/n+ junction single wire solar cell fabricated using Al-catalyzed Si nanowires. SEM images of Si nanowires (a) as-grown, (b) after Al tip etch, (c) after n-type shell layer deposition. (d) TEM images and (e) electron diffraction pattern indicate that the shell layer is oriented with respect to the Si nanowire core but is highly defective. (f) SEM image of fabricated single nanowire diode showing contacts to the n-type Si shell and p-type Si core. (g) Dark and light I-V data obtained from two single wire diodes.

[4] Y. Ke, X.J. Weng, J.M. Redwing, C.M. Eichfeld, T.R. Swisher, S.E. Mohney and Y.M. Habib, Nano Lett. 9, 4494 (2009).
[5] C.M. Eichfeld, S.S.A. Gerstl, T. Prosa, Y. Ke, J.M. Redwing and S.E. Mohney, Nanotechnol. 23, 215205 (2012).

fabricated using the Al-catalyzed Si nanowires as the core and a polycrystalline n-type Si layer deposited by LPCVD as the shell (Figure 2).[6] Short circuit current densities of~11.7 mA cm^{-2} were measured under 1-sun AM1.5G illumination, showing enhanced optical absorption. The power conversion efficiencies were limited to <1% by the low open circuit voltage and fill factor of the devices, which was attributed to junction shunt leakage promoted by the high p+/n+ doping. This demonstration of a radial junction device represents an important advance in the use of Al-catalyzed Si nanowire growth for low cost photovoltaics.

3.1.3 VLS growth of Si nanowires on Si templates formed on glass

The final goal of this project was to demonstrate a HARSH radial junction Si wire array solar cell on low cost glass substrates. The growth of vertical Si nanowire arrays on glass requires the development of crystalline template layers that can serve to epitaxially orient the Si nanowires which prefer to grow in the <111> direction. To achieve vertical nanowire growth, we investigated the use of aluminum-induced crystallization (AIC) of amorphous Si on glass. This process has previously been demonstrated to yield <111> oriented poly-Si layers with large grain size on glass substrates.[7] The AIC process involves the deposition of thin (<100 nm) Al and a-Si layers on glass followed by thermal annealing at temperatures below the Al-Si eutectic temperature (<~575°C). The a-Si diffuses through the Al and crystallizes resulting in layer exchange of Al and Si. The Al layer can then be etched off the top surface providing a poly-Si template layer on glass.

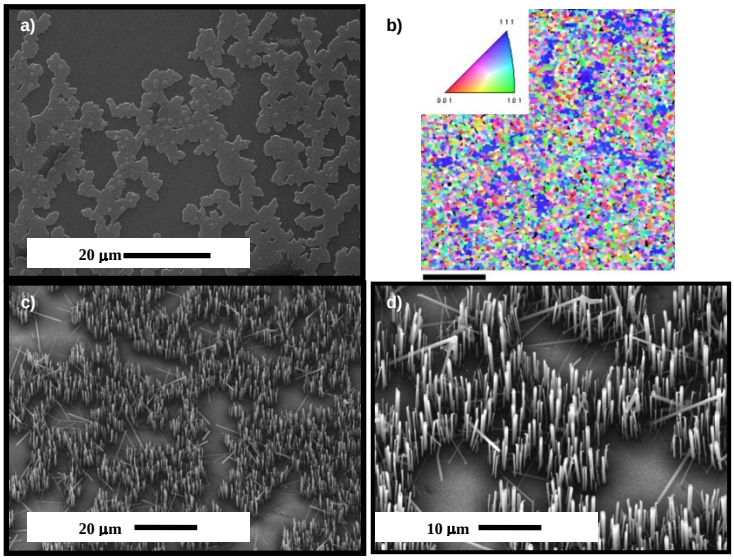

Figure 3. a) Plan-view SEM image and b) Orientation imaging map of AIC poly-Si layer on quartz showing dendritic grains with (111) orientation. c) and d) Tilted plan-view SEM images of surface showing vertical Si nanowire growth off of AIC poly-Si grains.

We carried out initial studies investigating layer deposition and annealing conditions required to produce <111> oriented poly-Si layers on fused quartz. The poly-Si templates were then used as substrates for the VLS growth of Si nanowires using $SiCl_4$ and gold as the catalyst. As shown in Figure 3, vertical Si nanowire growth was observed on the <111> oriented poly-Si regions formed by AIC on quartz.[8] These results demonstrate the possibility of producing vertical Si micro/nanowire arrays on non-crystalline substrates using poly-Si templates produced by the AIC process.

[6] Y. Ke, X. Wang, X.J. Weng, C.E. Kendrick, Y.A. Yu, S.M. Eichfeld, H.P. Yoon, J.M. Redwing, T.S. Mayer and Y.M. Habib, Nanotechnol. 22, 445401 (2011).
[7] M. Kurosawa, N. Kawabata, T. Sadoh and M. Miyao, Appl. Phys. Lett. 95, 132103 (2009).
[8] C.E. Kendrick, C. Bomberger, N. Dawley, J. Georgiev, H. Shen and J.M. Redwing, submitted to Phys. Stat. Solidi A.

3.2 Radial Junction Development

Three approaches were investigated for the formation of the radial p-n junction in the Si wire array devices fabricated in this project. These include thermal diffusion, LPCVD deposition of polycrystalline Si and single crystal Si shell layers and plasma enhanced CVD of amorphous hydrogenated Si (a-Si:H). One of the problems encountered in this project involved the cleanliness of surfaces of Si micro/nanowires grown by VLS growth. It was found that residual amounts of the catalyst metal (gold or aluminum) remain on the surface and therefore must be removed prior to radial junction fabrication.[9] This is particularly problematic for radial junction devices fabricated using shell layer deposition methods such as LPCVD or PECVD since the junction interface is located at the micro/nanowire surface in this design. Further details on the devices fabricated using the different radial junction fabrication methods are included in section 3.3.

3.3 Solar Cell Devices

The initial radial junction solar cell devices produced in this project were fabricated using thermal diffusion of n-type dopants into p-type Si pillars/microwires formed by either deep reactive ion etching (DRIE) of Si wafers or VLS growth of Si microwires on Si substrates. The use of thermal diffusion yielded solar cells with good open-circuit voltages (V_{oc}>0.40), however, thermal diffusion requires the use of high temperatures (>900^{o}C) and is generally incompatible with the long term goal of demonstrating devices on glass substrates. As a result, LPCVD was investigated as a method to deposit n-type Si shell layers at reduced temperatures (~650^{o}C). The final work in the project focused on the use of PECVD for the deposition of a-Si:H shell layers at low temperatures (<300^{o}C) to demonstrate a HARSH radial junction solar cell. The results obtained in each of these areas are summarized below.

3.3.1 Radial p-n junction Si pillar/wire array solar cells formed by thermal diffusion

Radial p-n junction Si pillar array solar cells were fabricated for an initial study into the effect of Si pillar dopant concentration on the performance of radial versus planar solar cells. In this study, Si pillar arrays were fabricated by deep reaction ion etching (DRIE) of highly doped Si wafers ($p=5x10^{18}$ cm^{-3} and $p=7x10^{19}$ cm^{-3}). The high doping concentration leads to a reduction in the minority carrier diffusion length, consequently, these samples were used to evaluate the potential of radial p-n junction devices compared to planar p-n junctions. The devices consisted of Si pillars that were 8 μm in diameter, 25 μm long and were spaced 10 μm apart. As shown in Figure 4, the open-circuit voltage of the pillar array devices decreased slightly compared to the planar devices as a result of the increased junction area. However, the short-circuit current density was significantly increased in the radial junction devices as a result of the improved collection of photogenerated carriers that is enabled in the radial junction devices.

[9] C.E. Kendrick, H.P. Yoon, Y.A. Yuwen, G.D. Barber, H.T. Shen, T.E. Mallouk, E.C. Dickey, T.S. Mayer and J.M. Redwing, Appl. Phys. Lett. 97, 143108 (2010).

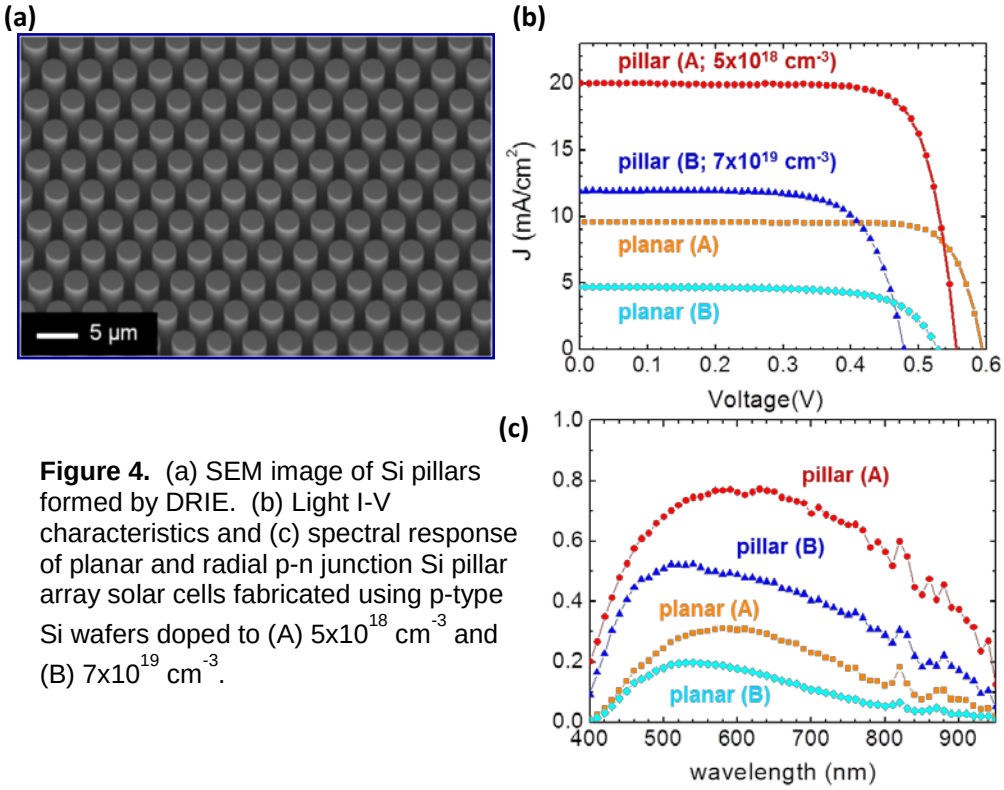

Figure 4. (a) SEM image of Si pillars formed by DRIE. (b) Light I-V characteristics and (c) spectral response of planar and radial p-n junction Si pillar array solar cells fabricated using p-type Si wafers doped to (A) $5x10^{18}$ cm^{-3} and (B) $7x10^{19}$ cm^{-3}.

Radial p-n junction devices were also fabricated using Si wire arrays formed by VLS growth. The Si wires were 2.5 μm in diameter, 50 μm long and were spaced 7 μm apart. Significant difficulties were encountered in processing devices using VLS-grown Si wire arrays. The VLS-grown Si wire array devices frequently exhibited shorting or high reverse leakage currents that negatively impacted the quality of the p-n diode. It was found that part of this difficulty arose from residual gold that remained on the tips or sidewalls of the Si wires after wet etching. An oxidation/strip procedure was developed to more effectively remove the residual gold. This reduced the shorting problem and enabled the first demonstration of a radial p-n junction Si microwire array solar cells fabricated using gold-catalyzed VLS wires.[10] It was also found that the shorting became even more problematic when the VLS-grown Si microwires were intentionally doped p-type. Subsequent liquid junction studies identified the shorting as arising from the region near the base of the Si microwires on the substrate. It is believed that residual gold is retained at the base of the Si microwires and that this dramatically increases the leakage current of the p-n junction particularly when the wire core is heavily doped p-type. A number of attempts were made to isolate the base region of the Si microwires using an infiltrating PDMS layer, however, it was not possible to successfully fabricate solar cell devices with intentionally doped VLS-grown Si microwires using this approach.

[10] C.E. Kendrick, H.P. Yoon, Y.A. Yuwen, G.D. Barber, H.T. Shen, T.E. Mallouk, E.C. Dickey, T.S. Mayer and J.M. Redwing, Appl. Phys. Lett. 97, 143108 (2010).

3.3.2 Single wire radial p-n junction solar cells formed by LPCVD

As a result of the difficulties that were encountered in fabricating large area VLS-grown Si wire array devices, we decided instead to utilize single wire devices in order to study the diode and photovoltaic properties of radial p^+-n^+ junction devices. Single wire array devices enable the diode properties to be directly studied without the additional parasitic resistances and problems with contacts that arise in wire array devices. In this study, the effects of LPCVD growth conditions on the morphology of the n-type Si shell layers and the radial p-n diode characteristics were examined. Core-shell nanowire structures were prepared by depositing heavily doped n-type Si layers by LPCVD (n~10^{19} cm^{-3}), approximately 50 nm thick, on p-type Si nanowires (p~$5x10^{18}$ cm^{-3}) grown by gold-catalyzed VLS. The growth temperature of the n-type Si shell layer was varied from 650ºC to 950ºC in order to study the effect of shell layer morphology on the diode characteristics. A sample was also prepared in which the p-type Si nanowire was heated to 950ºC in H_2 to clean the surface and then the growth temperature was lowered to 650ºC for shell layer deposition.

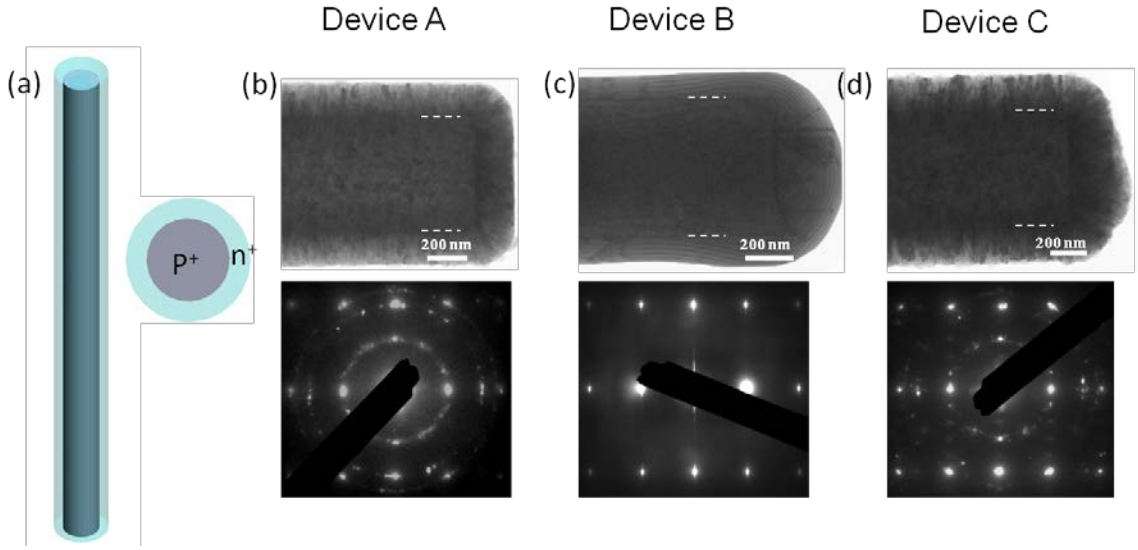

Figure 5. (a) Schematic and TEM images of radial p-n silicon nanowires with n-type shell layer grown at (b) 650°C, (c) 950°C and (d) 650°C with a 950°C pre-anneal.

The n-type Si shell layers deposited at 650ºC were polycrystalline while single crystal growth was obtained at 950ºC as shown in Figure 5. The n-type Si shell layer deposited at 650ºC after a 950ºC pre-anneal exhibited more oriented growth but contained a high density of defects. The shell layer morphology and growth conditions were found to have a significant impact on the diode and photovoltaic properties of the junction. Single wire radial p-n diodes that were fabricated with shell layers deposited at 650ºC exhibited linear I-V characteristics. Current rectification was observed in the single wire diodes fabricated with the 950ºC shell layer and the 950ºC anneal/650ºC growth shell layer. As shown in Table 1, devices fabricated with the 950ºC shell layer exhibited a lower reverse leakage current than those fabricated at 650ºC with a 950ºC. anneal. The lower reverse leakage current in the 950ºC shell layer devices resulted in a higher V_{oc}, J_{sc} and efficiency compared to devices fabricated with the 650ºC

growth/950^{o}C anneal conditions. The results demonstrate that the highest quality radial p-n junctions are obtained via epitaxial re-growth of the n-type Si shell layer. However, significant improvements in junction quality can be obtained through the development of strategies to reduce impurities and defects on the Si nanowire surface prior to the deposition of the shell layer at lower temperatures.

Table 1. Diode and photovoltaic properties of single wire radial p-n junction solar cells fabricated with n-type Si shell layers deposited under different processing conditions.

TYPE	Illuminated area (1×10^{-8}cm^2)	J_0 (1×10^{-7} A/cm^2)	Jsc (mA/cm^2)	Voc (V)	FF	Efficiency η
Device B (950^{o}C)	4.04	2.59	7.8	0.34	0.59	1.60%
	4.04	6.96	8.2	0.34	0.59	1.64%
Device C (650^{o}C w/ 950^{o}C anneal)	4.18	629	2.4	0.33	0.49	0.39%
	4.70	327	3.8	0.17	0.42	0.27%

3.3.3 HARSH radial junction solar cells

The proposed HARSH solar cells utilize thin a-Si:H layer in a heterojunction-intrinsic-thin layer (HIT) structure. In order to realize these devices, the a-Si:H must conformally coat the high aspect ratio Si pillar/wire structures without significant variations in thickness along the wire sidewalls. Consequently, we initially had to develop methods to achieve highly conformal, thin (<15 nm) a-Si:H on Si pillar/wire sidewalls by PECVD. The initial studies therefore investigated the effects of PECVD deposition conditions on the layer uniformity and also developed processes to deposit intentionally doped a-Si:H layers. It was difficult to achieve low resistivity p-type a-Si:H using the PECVD tool available at Penn State, consequently, the studies utilized n-type a-Si:H for the formation of intrinsic/*n*-type layers on the p-type Si pillar/wire cores.

The HIT structure was employed to form radial intrinsic/*n*-type *a*-Si:H junctions on *p*-type *c*-Si pillar arrays formed by deep reactive ion etching (DRIE). Hexagonally packed Si pillar arrays were etched into *p*-type *c*-Si wafers with resistivities of 0.3-0.5 Ω-cm, 0.067-0.08 Ω-cm and 0.01-0.02 Ω-cm which correspond to hole concentrations of approximately 5×10^{16} cm^{-3}, 7×10^{17} cm^{-3} and 5×10^{18} cm^{-3}, respectively. The minority carrier diffusion length is expected to vary from L_n~200 μm (5×10^{16} cm^{-3}) to L_n~10 μm (5×10^{18} cm^{-3}) in the Si wafers. The Si wafers were patterned and pillar arrays were fabricated by Bosch DRIE followed by two successive thermal oxidation and strip cycles to reduce sidewall roughness and damage. The pillar diameter was 8 μm and the pillar

length was 10 μm. The center-to-center distance between the pillars was 14 μm resulting in a filling ratio of approximately 0.3. Following a standard wet cleaning to remove residual contamination and oxide from the surface, the pillar array and planar samples were loaded into a PECVD chamber (Applied Materials P-5000) for the deposition of *a*-Si:H thin films. Intrinsic and *n*-type *a*-Si:H layers were then deposited sequentially using a total pressure of 5 Torr and a substrate temperature of 200 ^{o}C. The intrinsic *a*-Si:H layer was deposited using 30 sccm silane (SiH_4) and 300 sccm H_2 at a plasma power density 0.2 watt/cm^2. The *n*-type *a*-Si:H layer was deposited using 50 sccm phosphine (2% PH_3 in H_2), 75 sccm SiH_4 and 700 sccm H_2 at a plasma power density 0.8 watt/cm^2. The thicknesses of the intrinsic and *n*-type *a*-Si:H layers were estimated to be 15 nm and 50 nm, respectively, as determined by ellipsometry measurements carried out on the planar samples.

A thin (150 nm) Al-doped ZnO layer, deposited by atomic layer deposition, was used to form a conformal top transparent contact to the Si pillars. Photolithography and dry etching were then used to remove the ZnO and *a*-Si:H layers in the region outside of the device area. Metal layers consisting of 40 nm Ti/60 nm Au were deposited by thermal evaporation and patterned on the top surface of the samples to serve as both an electrical contact and a light aperture. The backside contact to the *p*-type Si wafer consisted of 40 nm Pd /200 nm Al also deposited by thermal evaporation. A schematic of the layer structure and a scanning electron micrograph (SEM) of a fabricated device are shown in Figure 6. The dark and light *I-V* characteristics of the planar and pillar array devices were measured using a probe station and solar simulator with an Air Mass (AM) 1.5G light source.

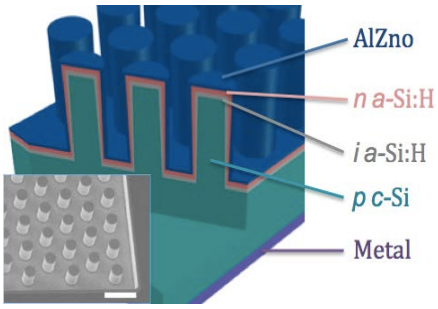

Figure 6: Schematic of HIT Si pillar array device. A 30^{o} tilted top-view SEM image of a fabricated device is included in the inset (scale bar is 10 μm).

The dark I-V measurement results showed that the leakage current densities under reverse bias were higher on the pillar array devices than that on planar ones as expected, because of the larger junction area. For both the dark and the light I-V, the current density was defined as current divided by the light aperture area (~0.3 mm^2) in order to compare the performance of planar and pillar array devices. A minimum of four devices were measured for each sample type and the properties of representative devices are included in Table 2. When the doping density of the *c*-Si wafer was lower than 10^{18} cm^{-3}, linear fitting of the semi-log plotted *J-V* curves under 0.3 - 0.5 V forward bias gave ideality factors (*n*) of 1.5 – 1.7 on the planar devices and 1.7 - 1.9 on the radial junction devices. The saturation current density (J_0) of the planar devices was also significantly lower than that of the radial junction devices. The differences in the measured J_o between devices fabricated with different doping density can be explained as arising from differences in the built-in potential (V_{bi}) of the junction. The Fermi level in 7×10^{17} cm^{-3} *p*-type *c*-Si is lower than that in 5×10^{16} cm^{-3} *p*-type *c*-Si which leads to a higher V_{bi} and lower J_0 in the 7×10^{17} cm^{-3} devices. The ideality factor was larger than 2

in devices fabricated with the highest *c*-Si wafer doping density ($5x10^{18}$ cm^{-3}) indicating more non-radiative recombination in the junction. In the 5×10^{18} cm^{-3} devices, recombination played a more important role than the higher V_{bi} hence J_0 was two orders of magnitude higher than that on devices fabricated from *c*-Si with a lower doping density.

Doping (cm^{-3})	n	J_0 nA/cm^2	V_{oc} (V)	J_{sc} mA/cm^2	FF (%)	Eff. (%)
Radial_5×10^{16}	1.7	66	0.55	23.6	75.4	9.8
Planar_5×10^{16}	1.5	3.9	0.58	26.3	75.1	12.1
Radial_7×10^{17}	1.7	13	0.59	19.9	65.7	9.1
Planar_7×10^{17}	1.6	1.8	0.59	18.1	64.8	7.3
Radial_5×10^{18}	2.4	1487	0.57	16.7	65.8	6.3
Planar_5×10^{18}	1.9	53	0.59	12.7	65.6	5.2

Table 2: Diode parameters and photovoltaic properties of the radial junction and planar solar cells as a function of the substrate doping density

The light *I-V* characteristics of the radial junction and the planar devices are shown in Figure 7. The open circuit voltages (V_{oc}), short circuit current densities (J_{sc}), fill factors and efficiencies (η) of solar cells from different doping density *c*-Si wafers are listed in Table 1. Benefitting from the HIT structure, the V_{oc} of all devices were over 550 mV even without a p^+ back surface-field. Although V_{bi} increases with the doping density of *c*-Si which is helpful to obtain a higher V_{oc}, the lower shunt resistance, higher J_0 and shorter L_n of the 5×10^{18} cm^{-3} devices compensated this effect. The trade-off thus results in the highest V_{oc} on the devices fabricated from 7×10^{17} cm^{-3} *c*-Si.

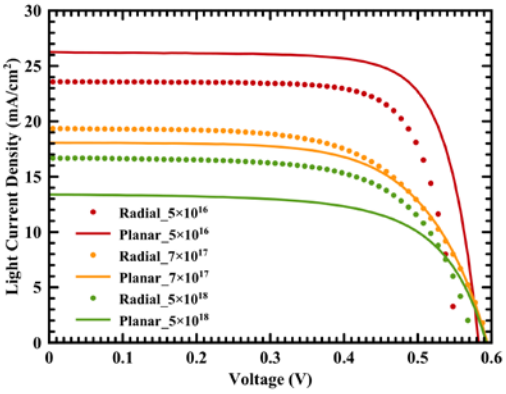

Figure 7. Light *J-V* curves of the radial junction and the planar solar cells as a function of the substrate doping density measured under AM 1.5G illumination.

For the lightly doped samples (5×10^{16} cm^{-3}), the J_{sc} of the planar device was higher than that collected from the radial junction device. This can be explained by a combination of the large L_n (~200 μm) which limits the carrier collection benefits of the radial junction and the effect of the higher J_0 of the radial junction devices. As the doping density increased and L_n was reduced, the J_{sc} of the radial junction devices became higher than that of the planar devices due to enhanced carrier collection. Specifically, on the planar devices, J_{sc} decreased by 49.4% with increasing doping density of *c*-Si, from 26.1 mA/cm^2 on the 5×10^{16} cm^{-3} device (L_n~ 200 μm) to 13.2 mA/cm^2 on the 5×10^{18} cm^{-3} device (L_n~ 10 μm). However, on the radial junction devices, the decrease in J_{sc} with increasing doping density was significantly reduced by the improved carrier collection. The J_{sc} was 23.6 mA/cm^2 on the 5×10^{16} cm^{-3} device (L_n~ 200 μm) and 16.8 mA/cm^2 on 5×10^{18} cm^{-3} device (L_n~ 10 μm) - a reduction of 28.8%. The conversion efficiency likewise tracked the trends in doping density. The radial junction device efficiency was lower than the planar device efficiency (9.84% compared to 12.14%) for the 5×10^{16} cm^{-3} devices but was higher than the planar device efficiency (6.32% compared to 5.2%) for

the 5×10^{18} cm^{-3} devices. The results demonstrate that the *a*-Si:H HIT structure provides an effective, low temperature route for junction formation and surface passivation in high aspect ratio wire/pillar array devices.

4. Products

4.1 Published Papers

1. C.M. Eichfeld, S.S.A. Gerstl, T. Prosa, Y. Ke, J.M. Redwing and S.E. Mohney, "Local electrode atom probe analysis of silicon nanowires grown with an aluminum catalyst," Nanotechnol. 23, 215205 (2012).
2. C.E. Kendrick and J.M. Redwing, "The effect of pattern density and wire diameter on the growth rate of micron diameter silicon nanowires," J. Crystal Growth 337, 1 (2011).
3. H.P. Yoon, Y.A. Yuwen, H. Shen, N.J. Podraza, T.E. Mallouk, E.C. Dickey, J. Redwing, C.R. Wronski and T.S. Mayer, "Parametric study of micropillar array solar cells," Proceed. of 37th IEEE Photovoltaics Specialists Conference (PVSC), 303 (2011).
4. Y. Ke, X. Wang, X.J. Weng, C.E. Kendrick, Y.A. Yu, S.M. Eichfeld, H.P. Yoon, J.M. Redwing, T.S. Mayer and Y.M. Habib, "Single wire radial junction photovoltaic devices fabricated using aluminum catalyzed silicon nanowires," Nanotechnol. 22, 445401 (2011).
5. S.M. Eichfeld, H.T. Shen, C.M. Eichfeld, S.E. Mohney, E.C. Dickey and J.M. Redwing, "Gas phase equilibrium limitations on the vapor-liquid-solid growth of epitaxial silicon nanowires using $SiCl_4$," J. Mater. Res. 26, 2207 (2011).
6. V. Ganapati, D.P. Fenning, M.I. Bertoni, C.E. Kendrick, A.E. Fecych, J.M. Redwing and T. Buonassisi, "Seeding of silicon wire growth by out-diffused metal precipitates," Small 7, 563 (2011).
7. C.E. Kendrick, H.P. Yoon, Y.A. Yuwen, G.D. Barber, H.T. Shen, T.E. Mallouk, E.C. Dickey, T.S. Mayer and J.M. Redwing, "Radial junction silicon wire array solar cells fabricated by gold-catalyzed vapor-liquid-solid growth," Appl. Phys. Lett. 97, 143108 (2010).
8. H.P. Yoon, Y.A. Yuwen, C.E. Kendrick, G.D. Barber, N.J. Podraza, J.M. Redwing, T.E. Mallouk, C.R. Wronski and T.S. Mayer, " Appl. Phys. Lett. 96, 213503 (2010).
9. C.E. Kendrick, S.M. Eichfeld, Y. Ke, X.J. Weng, X. Wang, T.S. Mayer and J.M. Redwing, "Epitaxial regrowth of silicon for the fabrication of radial junction nanowire solar cells," Proceed. Of SPIE 7768, 776801 (2010).
10. Y. Ke, X.J. Weng, J.M. Redwing, C.M. Eichfeld, T.R. Swisher, S.E. Mohney and Y.M. Habib, Nano Lett. 9, 4494 (2009).

4.2 Manuscripts Submitted

1. C.E. Kendrick, C. Bomberger, N. Dawley, J. Georgiev, H. Shen and J.M. Redwing, "Silicon nanowire growth on poly-silicon-on-quartz substrates formed by aluminum-induced crystallization," submitted to Phys. Stat. Solidi A.
2. H. Shen, Y. Yuwen, X. Wang, J.I Ramirez, Y.Y. Li, Y. Ke, C.E. Kendrick, N.J. Podraza, T.N. Jackson, E.C. Dickey, T.S. Mayer and J.M. Redwing, "Effect of c-Si doping density on heterojunction with intrinsic thin layer (HIT) radial junction solar cells," submitted to 2013 Photovoltaics Specialists Conference.

4.3 Manuscripts in Preparation

1. X. Wang, Y. Ke, C.E. Kendrick, X.J. Weng, H. Shen, Y.A. Yuwen, J.M. Redwing and T.S. Mayer, "Effects of shell layer morphology on the properties of radial p+/n+ silicon nanowire single-wire solar cells."
2. Y. Ke, D.J. Won, X.J. Weng, D. Kohen, S.M. Eichfeld and J.M. Redwing, "Influence of carrier gas on the nucleation and growth of Al-catalyzed Si nanowires."
3. M.W. Kuo, C.E. Kendrick, J.M. Redwing and T.S. Mayer, "Axial and radial doping uniformity of p-type Si nanowires grown with $SiCl_4$."

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