

# A Silicon Photonics Platform for Government Applications



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# Acknowledgements

- Christopher T. DeRose
- Paul S. Davids
- Nicolas J. D. Martinez
- William A. Zortman
- Jonathan A. Cox
- Adam Jones
- Douglas C. Trotter
- Andrew T. Pomerene
- Andrew L. Starbuck
- Daniel J. Savignon
- Todd Bauer
- Michael Wiwi
- Patrick B. Chu
- F. B. McCormick
- G. Keeler
- A. Vawter
- External Collaboration and/or former Sandians
- M. W. Watts (MIT)
- S. Mookherjea (UCSD)

# Applications for Silicon Photonics

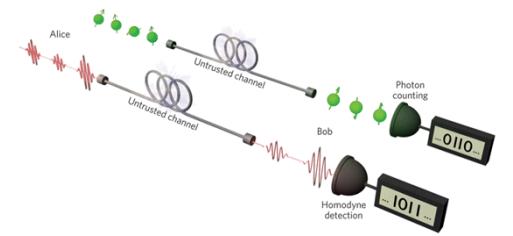
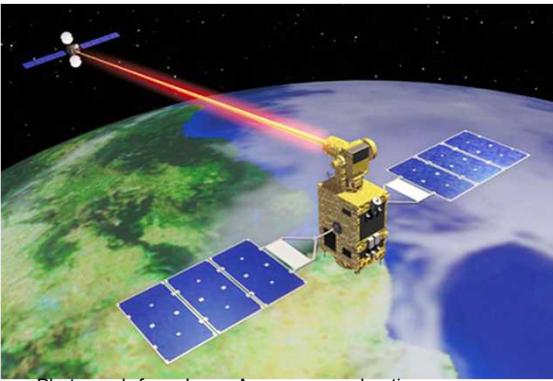
## Communications

Satellite networks

Avionics

Secure terrestrial networks

Commercial networks



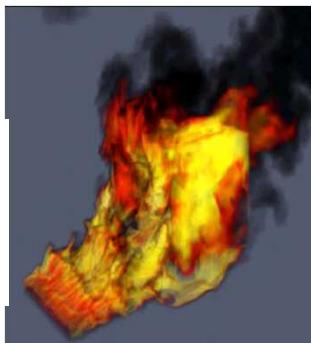
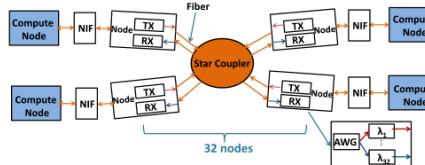
P. K. Lam and T. C. Ralph, "Quantum Cryptography: Continuous improvement", *Nature Photonics* 7, 350–352 (2013)

## Computing (interconnect)

High performance computing

Data centers

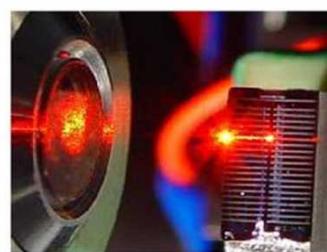
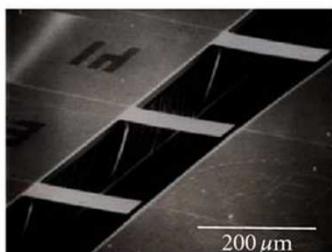
Q. Li et. al., "Scaling star-coupler based optical networks for avionics applications", *Optical Communications Networks*, Vol 5 pp 945-956 (2013)



## Electronic Warfare

High frequency agile processing

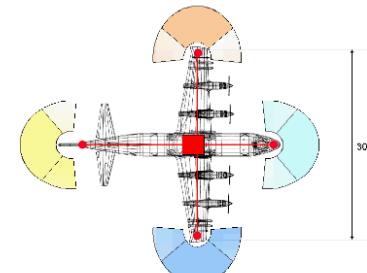
Kirill Zinoviev et. al., "Silicon Photonic Biosensors for Lab-on-a-Chip Applications," *Advances in Optical Technologies*, vol. 2008, Article ID 383927, 2008.



## Sensing

Sensing networks

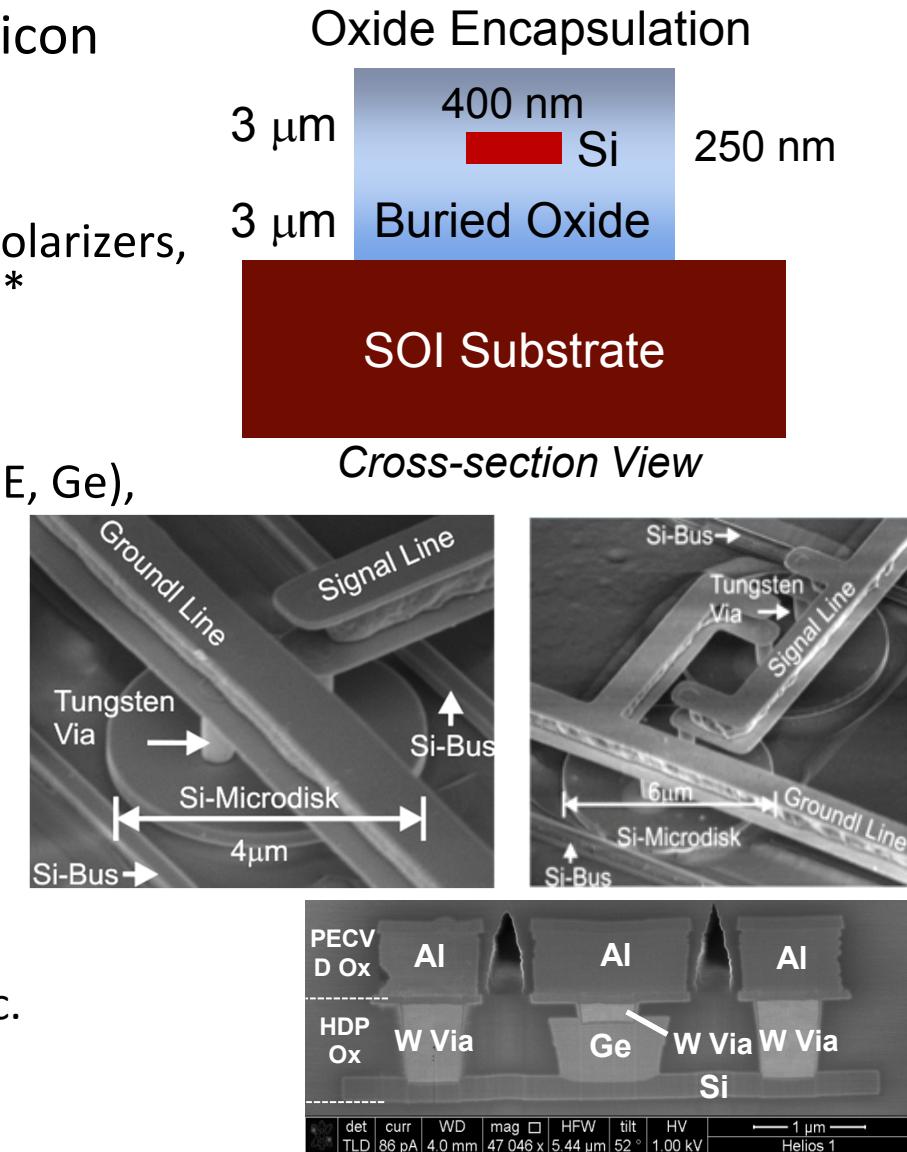
Bio/chemical sensors



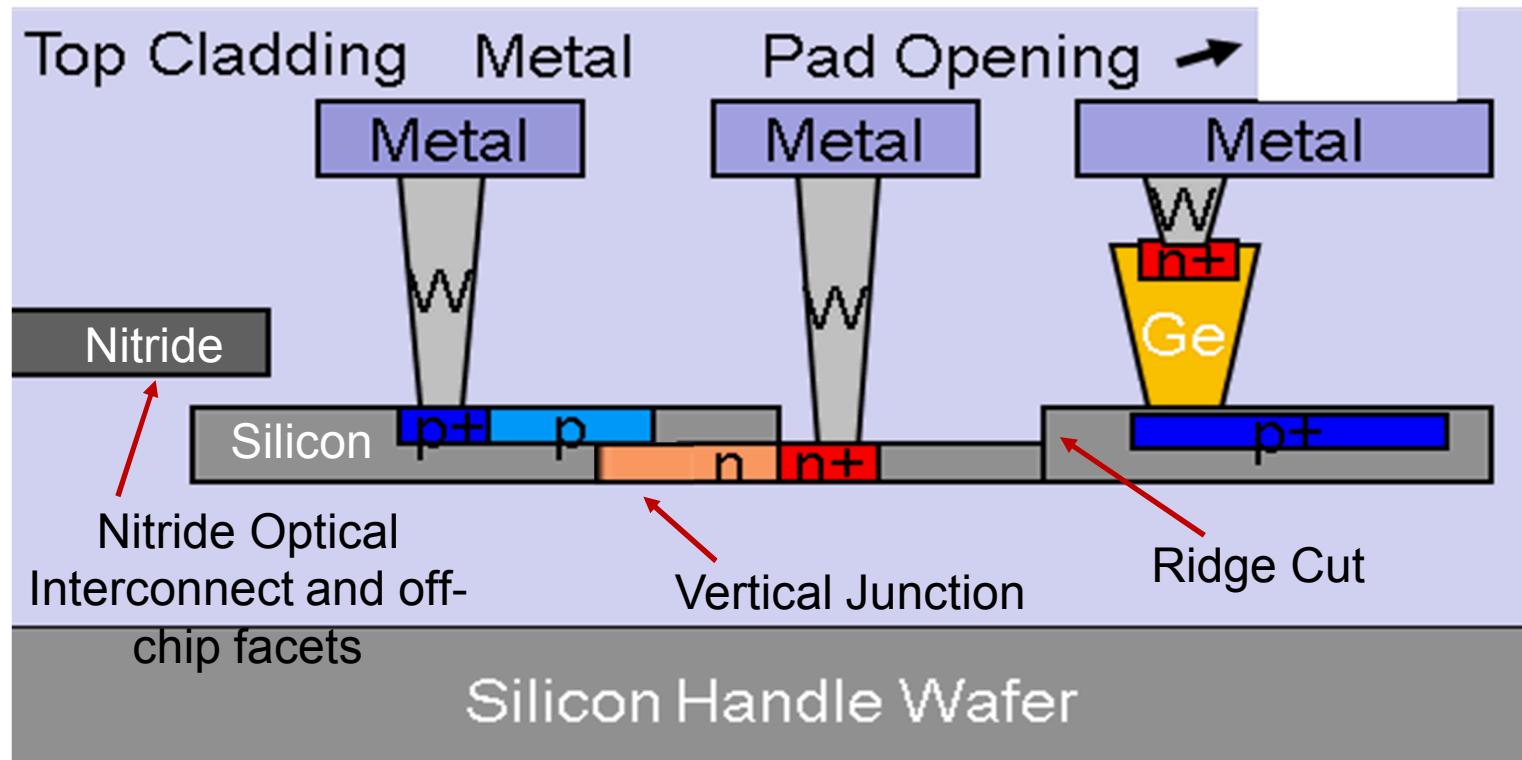
M. E. Manka "Microwave photonics for electronic warfare applications", *Proc. IEEE MWPI'08 Conf.*, pp.175 -178 2008

# What is Silicon Photonics?

- Active and Passive Photonics on/in Silicon
- Passive:
  - Waveguides, spectral filters, splitters, polarizers, polarization rotators, gratings, isolators\*
- Active
  - Modulators(EO), switches, detectors (OE, Ge), lasers\*
    - Thermal Shift of index
    - Electro-refraction
    - Electro-absorption (SiGe)
- Most applications require intimate integration with CMOS Electronics
  - Heterogeneous integration
    - Flip-chip bonding, Wafer bonding, etc.
  - Monolithic integration



# Silicon Photonics Layer Structure



# Microsystems and Engineering Sciences Applications (MESA): 400,000 Sq-ft Complex with >650 Employees in Secure Facility



- Trusted Digital, Analog, Mixed Signal & RF Integrated Circuits Design & Fabrication
- Custom IC Design
  - Secure microcontrollers
  - Sensor Readout ICs
  - Analog/Digital/RF
  - IBM Trusted Foundry
  - Tamper Resistant
- Micromachining
- RAD Effects and Assurance
- Failure Analysis, Reliability Physics
- Test & Validation
- 3-D Integration Features

- Advanced Computation
- Modeling & Simulation
- COTS Qualification
- Advanced Packaging
- Custom Electronic Components
- System Design & Test



**Compound  
Semiconductor  
Fabrication**

Si

III-V

**Materials  
Research**

- Compound Semiconductor Epitaxial Growth (UV-THz)
- Photonics: Si & III-V
- MEMS, VCSELs, Plasmonics
- Specialized Sensors, FPAs
- Materials Science, Graphene
- Nanotechnology, Chem/Bio
- Heterogeneous-Technology Integration & Processing
- III-V Semiconductor Devices
  - Rad-Hard mElectronics
  - Rad-hard Optical Links
  - Solid-State RF Devices
  - GaN Power Electronics

***MESA is an FFRDC-based development and production facility for any microsystem component or technology that cannot or should not be obtained commercially.***

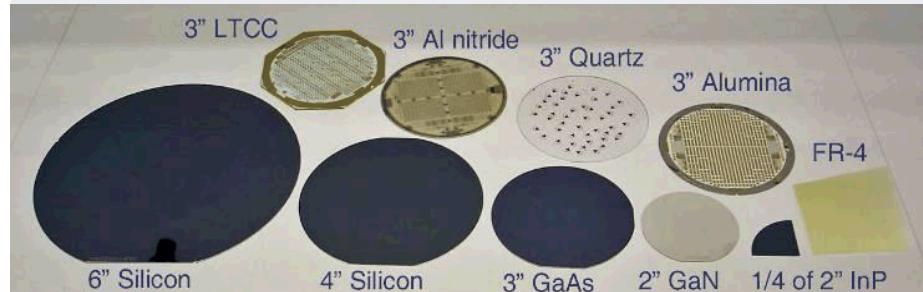
# Microsystems and Engineering Sciences Applications (MESA) Fabrication Facilities

## Silicon Fabrication Facility



- Total clean room area 33,000 ft<sup>2</sup> (12,500 ft<sup>2</sup> Class 1)
- 22 Separate laminar flow clean room bays
- 5V Bulk & 3.3V SOI Rad Hard CMOS in production
- In-house microelectronics technology & facility to deliver specialized IC products
- Primary supplier of custom Rad-Hard ICs for weapon life extension programs and Satellite Systems
- Supports silicon bulk *and* silicon surface micromachining
- DOD Defense Microelectronics Activity (DMEA) accredited Microelectronics Trusted Supplier (design and foundry services)

## Microfabrication Facility



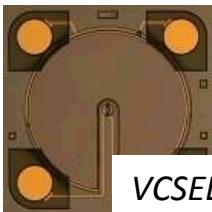
- Clean room area 89,000 ft<sup>2</sup> (16,640 ft<sup>2</sup> Class 10/100)
- Reconfigurable tools from wafer pieces to 6" wafers
- 6" silicon post-processing facility to support hybrid substrates and 3D integration (8" compatible)
- Compound Semiconductor Epitaxial Growth
- Compound Semiconductor Discretes, IC's and MEMS
- Silicon MEMS / photonics / optoelectronics / VCSELs
- Mixed-Technology Integration and Processing
- 3D Integration; Packaging
- Materials Characterization
- Failure Analysis

# III-V Photonics

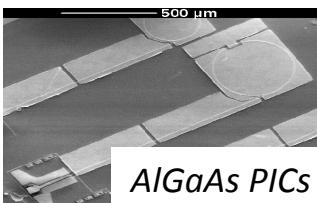
2010s



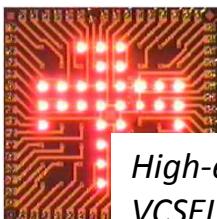
InGaAsP PICs



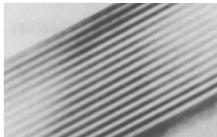
VCSEL+ PD



AlGaAs PICs



High-efficiency  
VCSELs

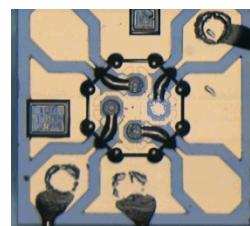


Strained-layer  
superlattices

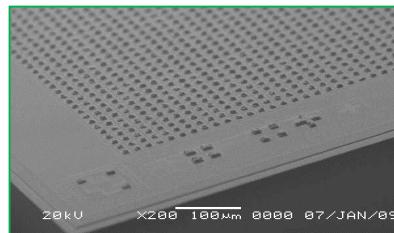
1980s



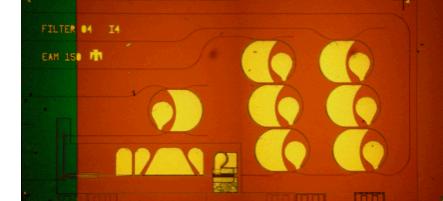
On-Chip Injection Locking  
Enhanced Modulation > 50 GHz, C-Band



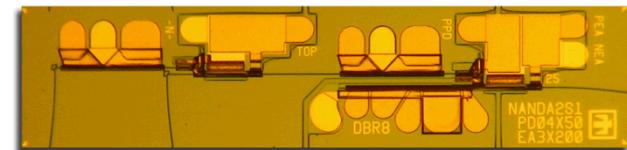
Single-Frequency Tunable VCSELs,  
For atomic spectroscopy and sensors



nBn FPAs in the SWIR, MWIR and LWIR,  
leveraging novel III-P and III-Sb materials



RF-Optical Channelizing Filter  
1-20 GHz RF on C-Band Light

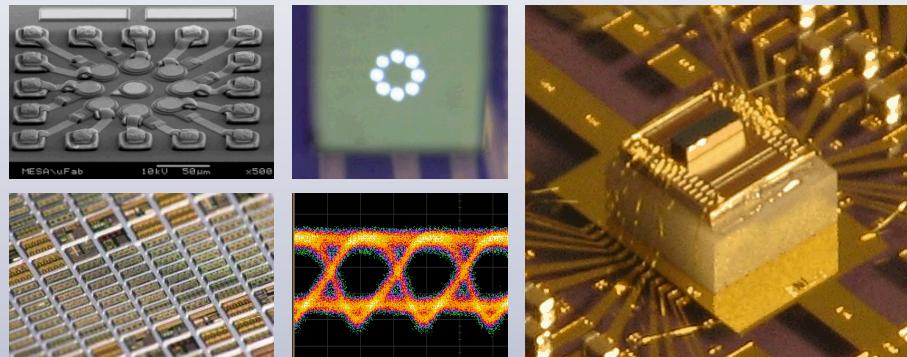


All-Optical Logic at >40 Gb/s, C-Band

- **Foundational Capabilities**
  - III-V compound semiconductor epitaxy, microfabrication, integration
  - Device physics, modeling, simulation
  - Microelectronics/optoelectronics, and complex mono/hetero-circuits
- **Prove, Advance Technology Readiness Level, Productize**
  - TRL1-6+: create, develop, prototype
  - NNSA QMS/QC-1-10; trusted
- **Trusted, low-volume, high-reliability products for harsh environments**

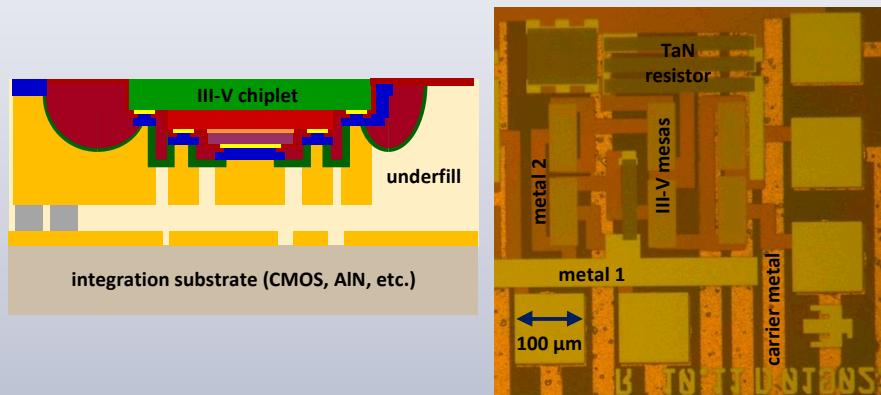
# Trusted Advanced Pathfinder Products: Heterogeneous Integration

## Optical Data Communications



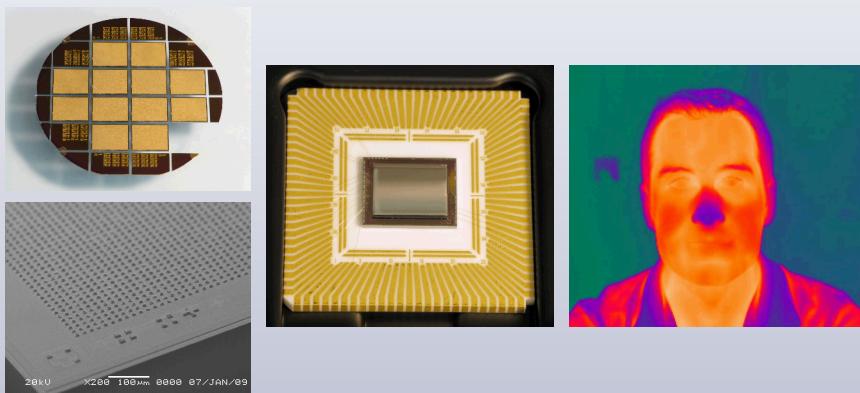
- GaAs- and InP-based devices: VCSELs, modulators, photodiodes
- dense integration onto 32-nm and 45-nm CMOS

## Heterogeneous III-V/CMOS Microelectronics



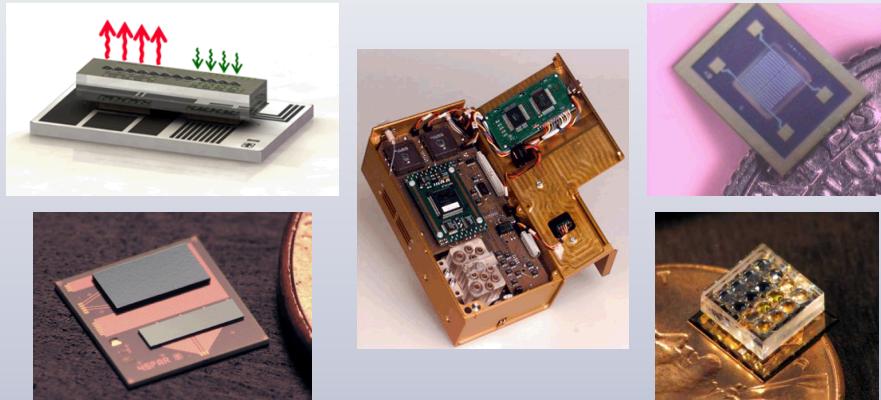
- complementary integration of GaAs and InP microelectronics
- III-V microelectronics circuitry on CMOS ASICs

## IR Imagers for Remote Sensing



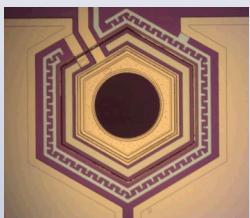
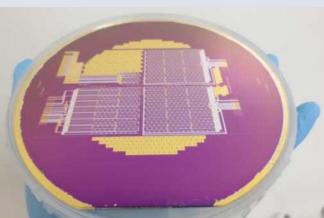
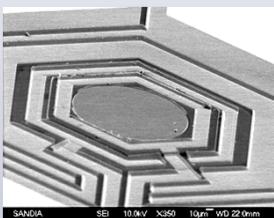
- nBn InAs/GaSb MWIR/LWIR detector arrays for large-format FPAs
- 10 μm indium bump bonding, underfill, thinning, AR coating
- hybridization to silicon ROICs with >99.99% interconnect yield

## Optical and MEMS-based Microsensors



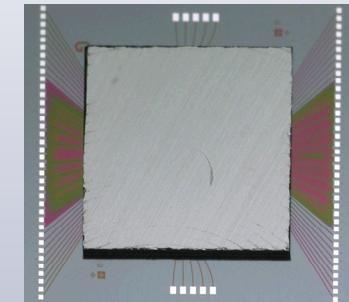
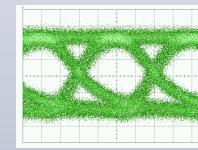
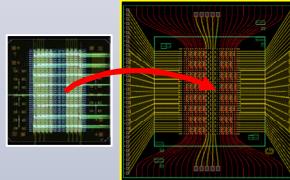
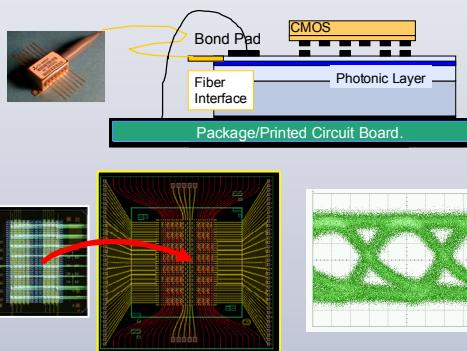
- chemical and bio sensors using MEMS and SAW devices
- g-hard optical microsensors with in-house photonics
- hybrid device integration with custom micro-optics

## Microsystem-Enabled Photovoltaics



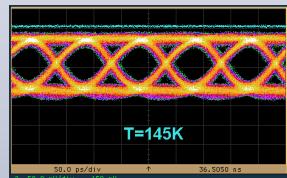
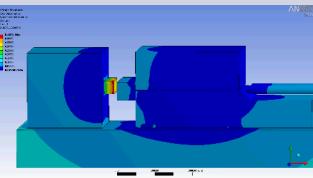
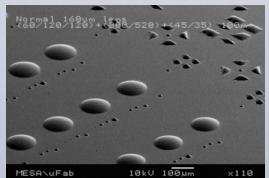
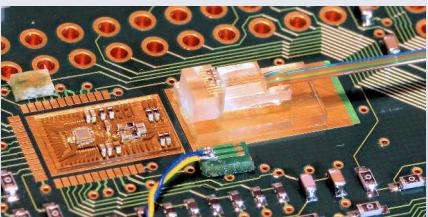
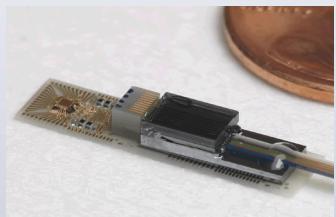
- wafer-level bonding for multi-junction solar cells
- InGaAsP/InP and InGaP/GaAs devices on silicon
- dielectric interfaces with III-V substrate removal
- integration with collection optics

## High Performance Computing



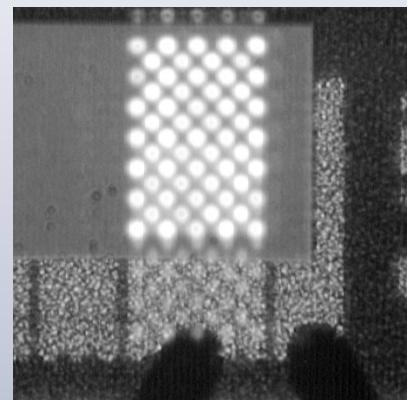
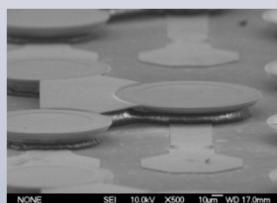
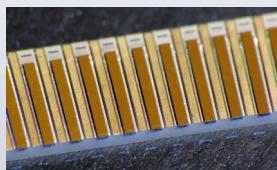
- silicon photonics on high-speed silicon ASIC
- independent optimization of electronics & photonics

## Extreme Environment Applications



- custom photonics, optics, electronics for cryogenic interconnects
- advanced optoelectronics and integration for radiation hardness

## High Performance Photonics

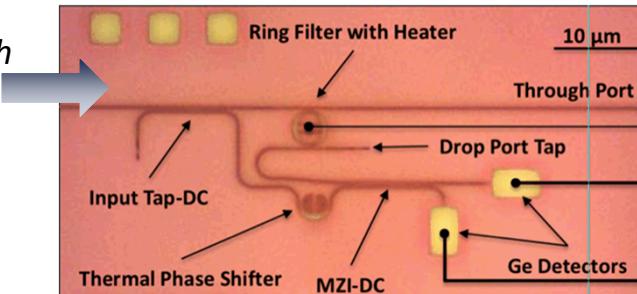


- high-power emitters on AlN and diamond
- RF packaging for high-speed test and measurement

# Silicon Photonics

2014

*balanced homodyne  
resonant wavelength  
stabilization > 55C*



2013

*Si Photonics MPW  
(CIAN NSF ERC)*

2012

*24 GHz Si TW MZM*

2011

*45 GHz Ge Detector*

2010

*3 fJ/bit resonator  
modulator, 1V-cm  
MZM  
wavelength tunable  
rings over 35 nm*

2008

*2.4 ns Wavelength  
selective switch*

2007

*MicroDisk resonator  
infrared detector*

2005

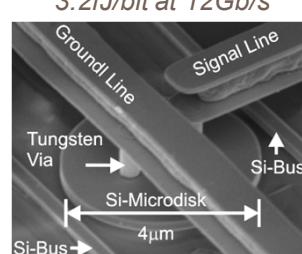
*$Si_3N_4$  low-loss  
waveguides*

2000

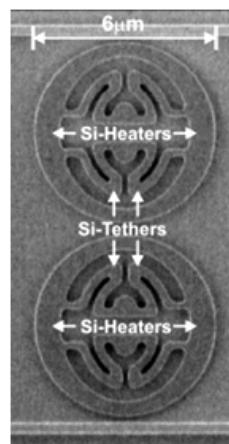
*$SiON$  /  $SiO_2$   
(Clarendon Photonics)*

1990s

*$Si$  PhC & Optical MEMS*

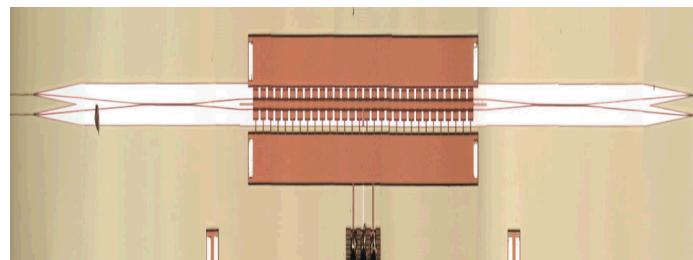


**Resonant Optical  
Modulator/Filter**

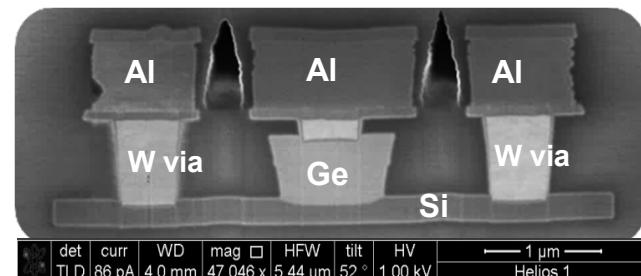


**Tunable Resonant  
Filter**

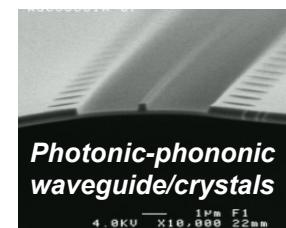
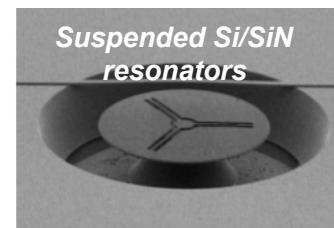
**MEMS process  
for additional  
capability**



**24 GHz 0.7V-cm Travelling  
Wave MZI Modulator**

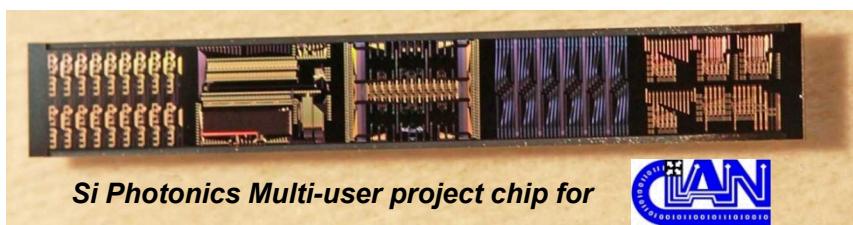
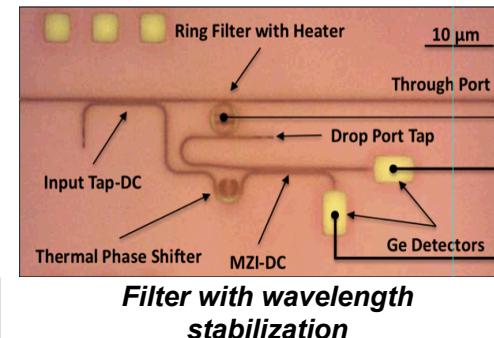
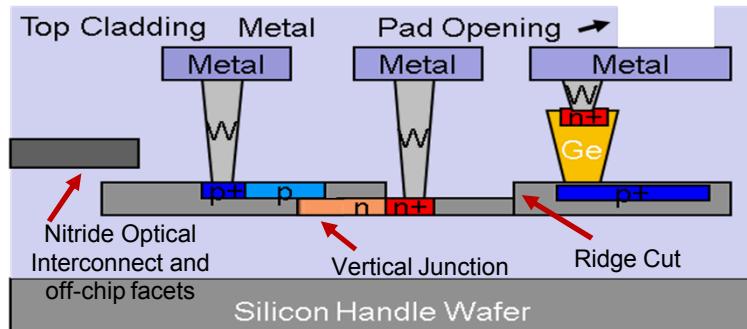
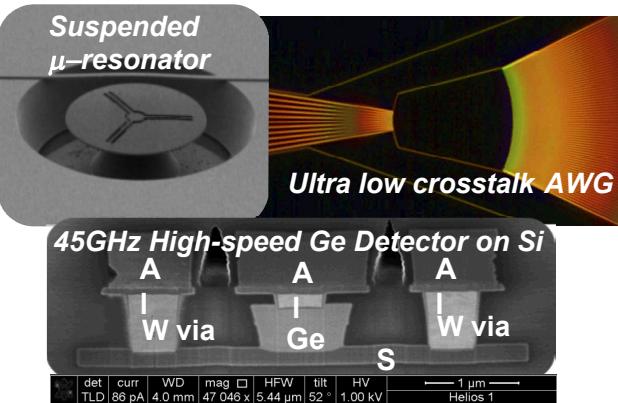


**45 GHz High-speed Ge Detector  
on Silicon**



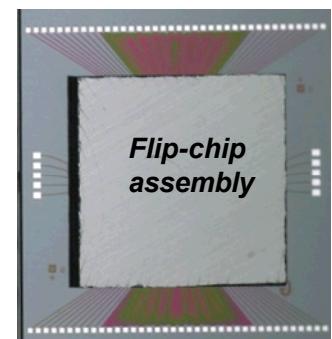
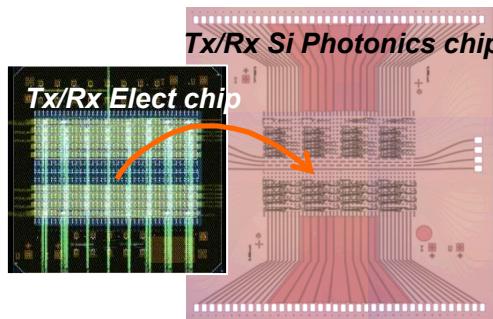
**Photonic-phononic  
waveguide/crystals**

# Sandia Si Photonics Integrated Circuits



## Silicon-based Integrated Devices

- **Active Components:** Linear and digital Mach-Zehnder modulators, ring and disk ultra-low energy modulators with/without integral micro-heaters for resonant wavelength stabilization, high-freq. and high power integrated germanium detectors, integration with rad-hard CMOS, 2 x 2 wavelength selective switches and broad-band switches, and tunable filters
- **Passive Components:** wavelength division multiplexers using resonant filters and arrayed grating routers, surface normal and in-plane polarization beam splitters, polarization rotators, polarization mode filters, directional couplers and splitters, integral SiN second photonics routing layer, Sagnac interferometers, AWG RF channelizers
- **Demonstrated Circuits:** transmitters, receivers, on-chip links, resonant wavelength stabilization circuits for both modulators and filters, optical active beam steering, optical logic (matrix multiply), low noise oscillators, optical network add-drop node (CIAN), optical channel monitor (spectrum analyzer) (CIAN)



# Sandia Silicon Photonics MPW



- Sandia's Role
  - Not to compete with Industry
    - Focus on what you cannot get elsewhere
    - Collaborative research best
    - Custom work possible within MPW framework or separate program
  - 2-3 offerings per year
- Process features
  - Silicon passives (silicon rib, ridge guides, silicon nitride guides)
  - Silicon actives (modulators, switches, efficient tuning devices)
  - Germanium detectors
- Design tools and features
  - Design guide
  - Library (gds/scripted)
  - Working with vendor on design environment

#### 4. TECHNOLOGY OVERVIEW

Sandia National Laboratories (SNL) has developed a Microsystems and Engineering Sciences Applications (MESA) facility located in a limited classified area. Trusted custom fabrication of silicon and radiation-hardened process technologies for digital, analog and mixed signal ICs is currently available through MESA, which delivers production micro-electronics components to support special DOE and DOD programs. The MESA Complex is designed to integrate the numerous scientific disciplines necessary to produce functional, robust, integrated [microsystems](#) and represents the center of SNL's investment in [microsystems](#) research, development, and prototyping systems. This suite of facilities encompasses approximately 400,000 square feet and includes [cleanroom](#) facilities, laboratories and offices.

ISSUE DETAILS

process flow of are described in Table 5-1. The base process can be broken

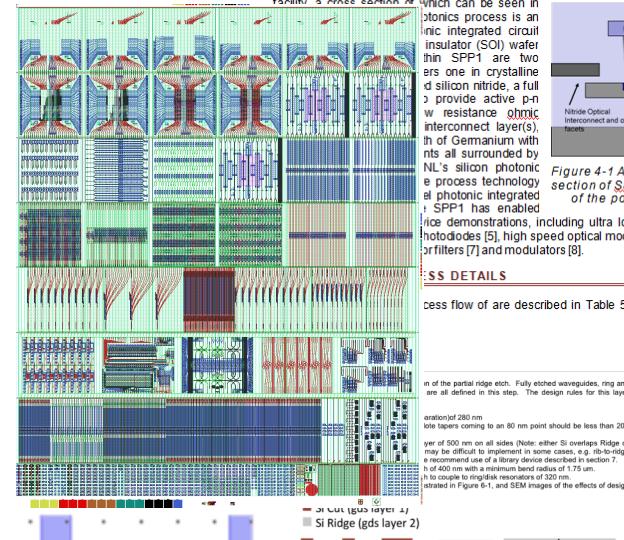
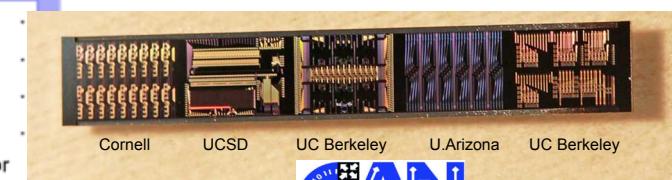


Figure 6-1 Illustration of Si cut layer design rule.



C. T. DeRose et. al., OIC 2014

# SNL Si Photonics Design Manual

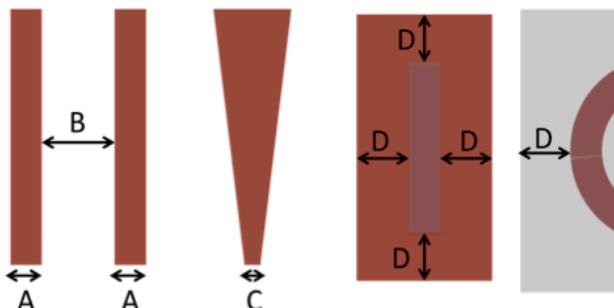
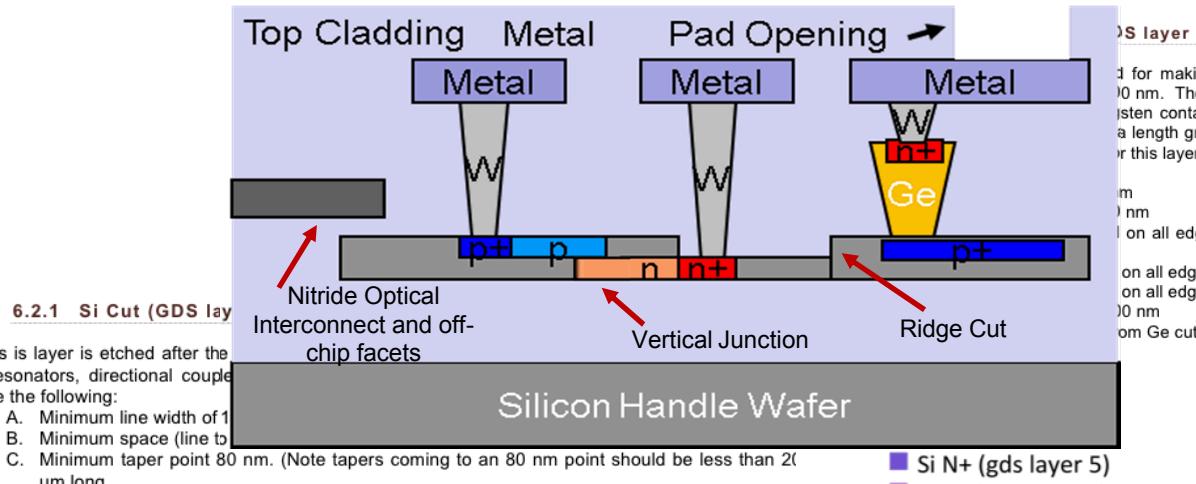


Figure 6-1 Illustration of Si cut layer design rules

## OS layer 15)

for making ohmic electrical contacts to P+ and N+ doped Si. The contact width is specified in order to guarantee proper filling of the trench contact. For trench type contacts a rectangular shape should be used with a length greater than 500 nm. For point type contacts, circular contacts are specified below.

m

nm

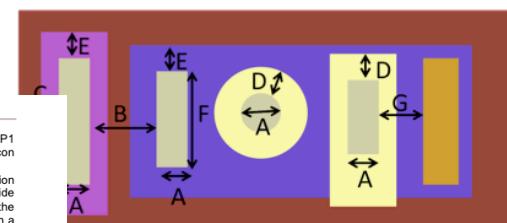
on all edges by a minimum of 150 nm of Ge cut, Recommended 400 nm

on all edges by a minimum of 150 nm of Metal 1

on all edges by a minimum of 100 nm of P+ or N+ Ge

nm

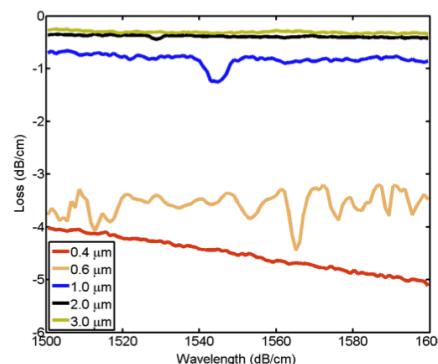
from Ge cut is 1 um



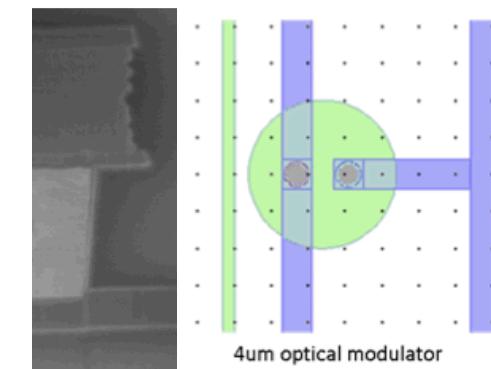
## 9.1 Silicon Waveguide

The silicon waveguide is the most basic element used in optoelectronic device layouts in the SPP1 platform. Since the thickness of the SOI is determined by the starting wafer selection, the silicon waveguide effectively has one parameter: its width.

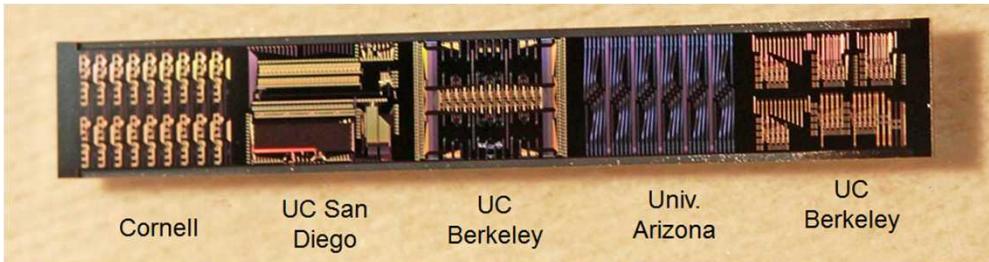
Although the width of the waveguide is the only critical parameter, it determines the propagation losses. The waveguide group velocity, dielectric constant, and bend radius of the waveguide. The waveguide propagation losses in the silicon waveguide are dominated by scattering from roughness at the waveguide sidewalls. Currently for our process, the rms value of the sidewall roughness is 1.2 nm with a correlation length of 100 nm and an exponential autocorrelation function. Losses for a single mode 400 nm wide waveguide are between 4 and 5 dB/cm for the TE polarization. Increasing the waveguide width results in a reduction in propagation losses but as the guide becomes multimode, coupling between the modes is induced by the line edge roughness. The losses for guides of various widths can be seen in Figure 9-1. Typically bend radii of greater than 6 micron can be used for a 400 nm wide waveguide for the TE polarization.



9-1 Propagation loss for the TE polarization for si waveguides of various widths. Multimode phenomena is observed in the wider waveguides.

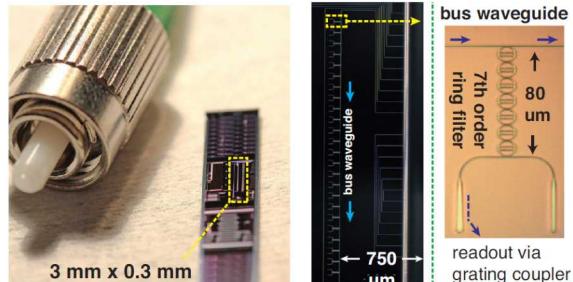


# CIAN Silicon Photonics Multi-Project Wafer (MPW)



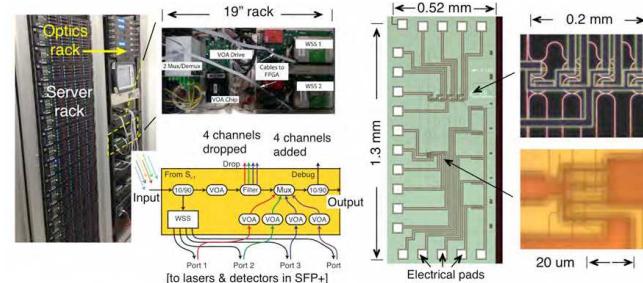
CIAN (center for integrated access networks)  
Si Photonics MPW Highlights

- Five university participants
- 1/7<sup>th</sup> wafer from internally funded program (XGC LDRD grand challenge)
- Sandia has delivered 100+ chips
- 6 conf. & journal papers so far



Optical Spectrum Analyzer

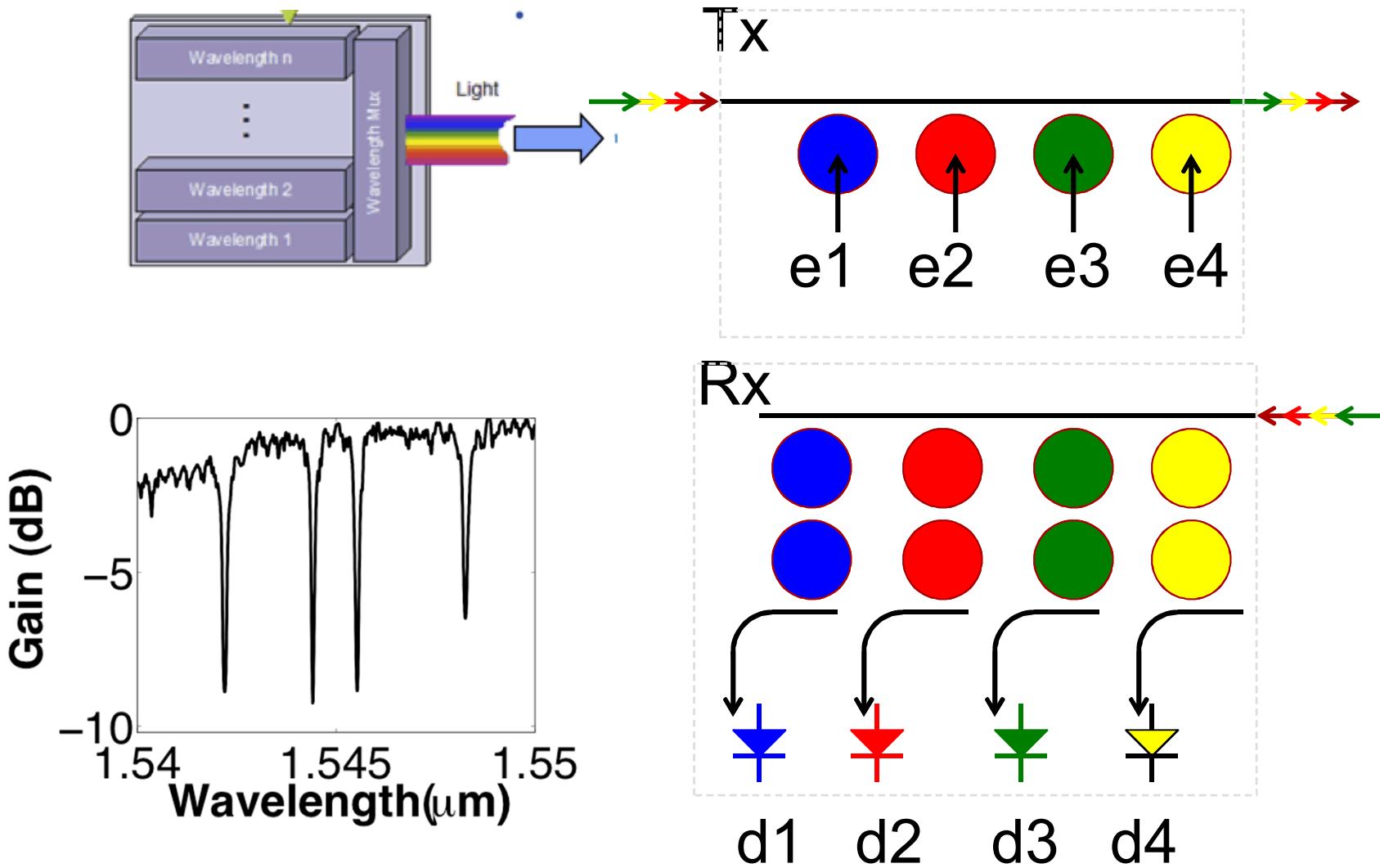
R. Aguinaldo et. al. OIC 2014



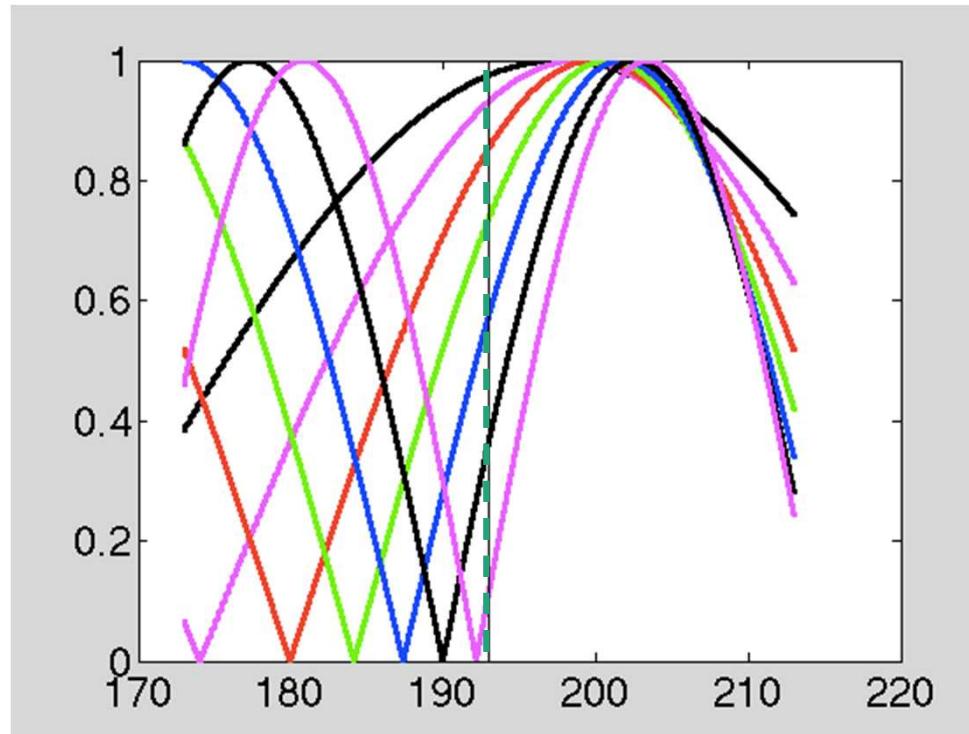
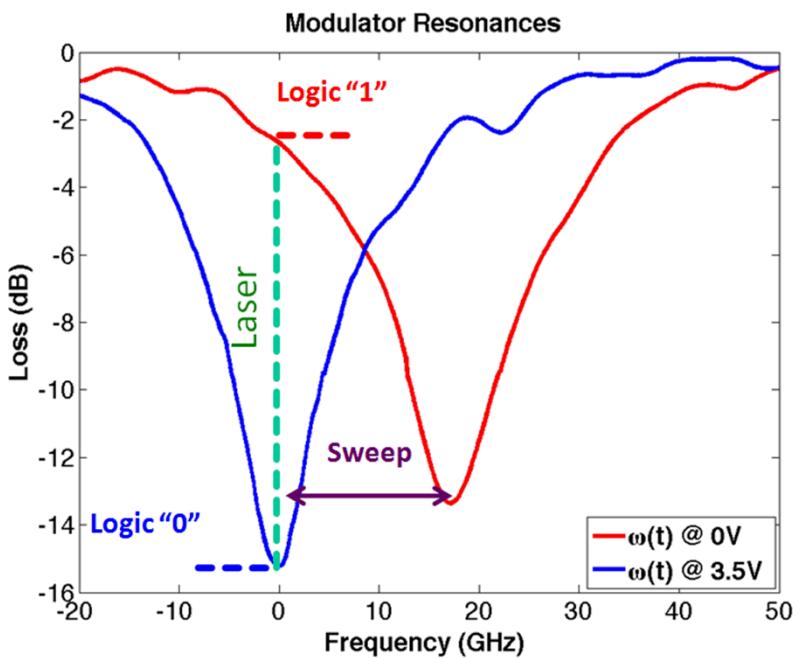
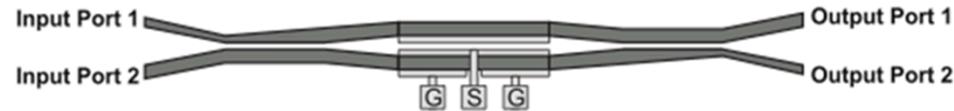
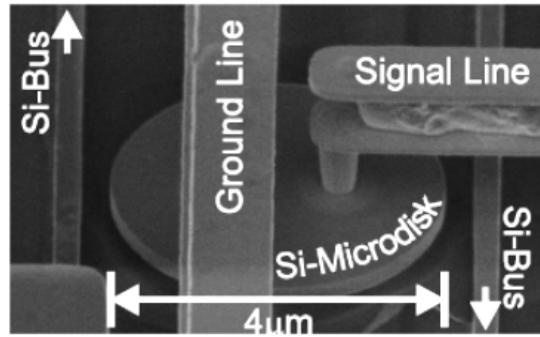
Network Node on a Chip

R. Aguinaldo et. el. IPC 2014

# Si Photonics for On-chip DWDM



# Si Photonics for Modulators



Photograph from: M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine, Group IV photonics 4-6 (2008)

# Resonant Silicon Micro-Photonics

- Why resonant silicon photonics?

- Small size (<4  $\mu$ m dia.)
  - Resonant frequency  $\rightarrow$  DWDM modulators & mux/demux

- Benefits

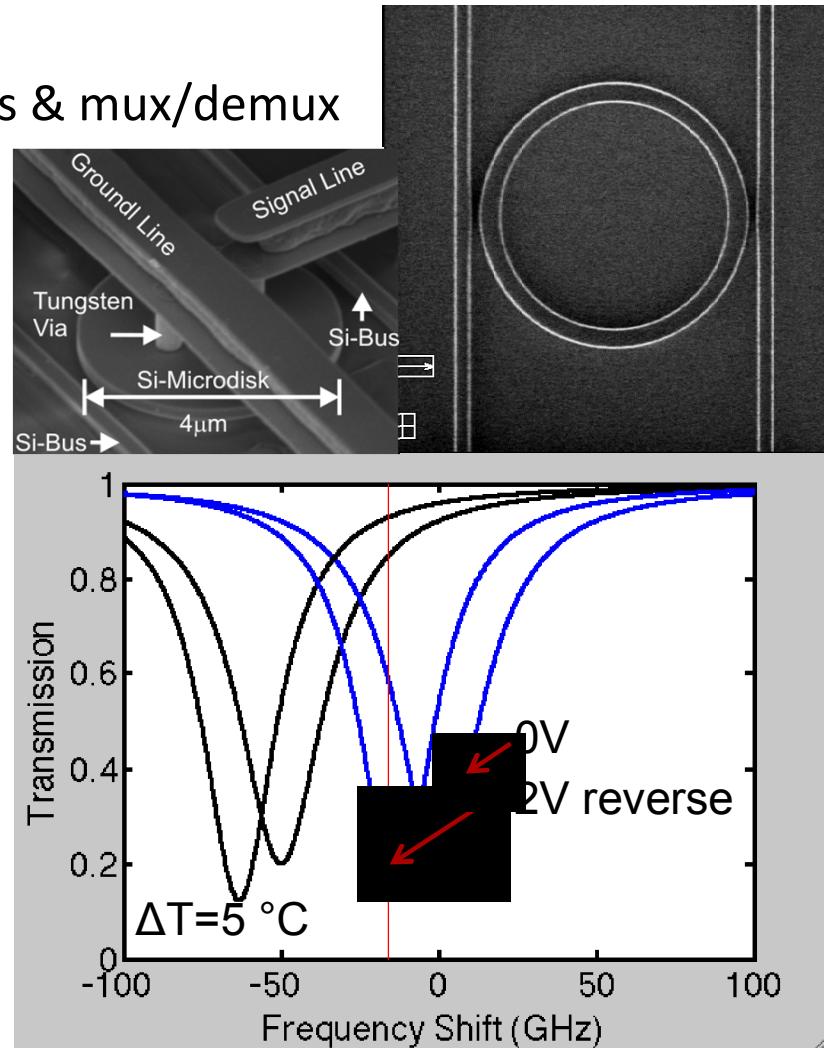
- Low energy
  - High bandwidth density

- Resonant Variations

- Manufacturing Variations
  - Temperature Variations
  - Optical Power (1s density)
  - Aging?

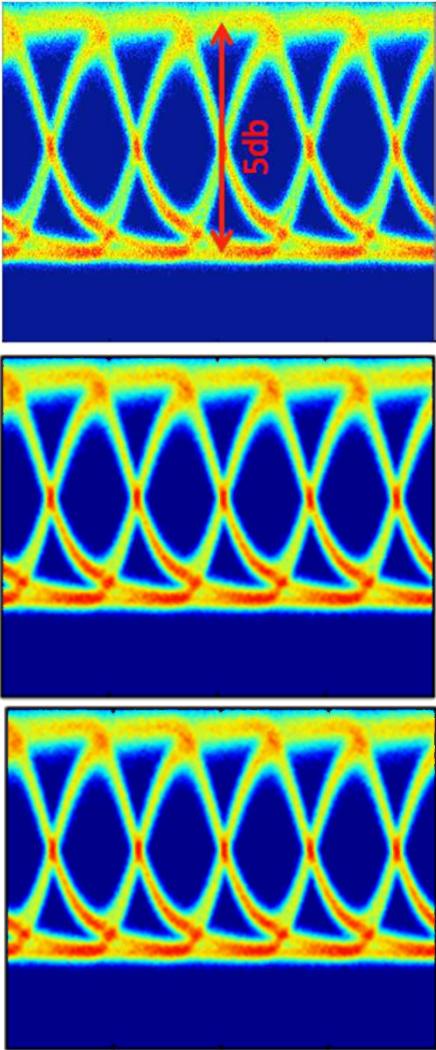
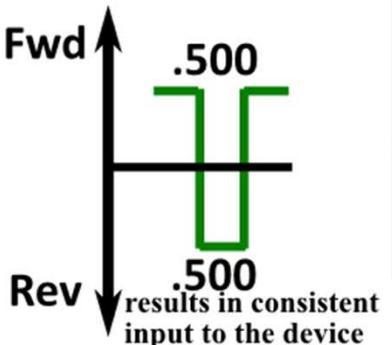
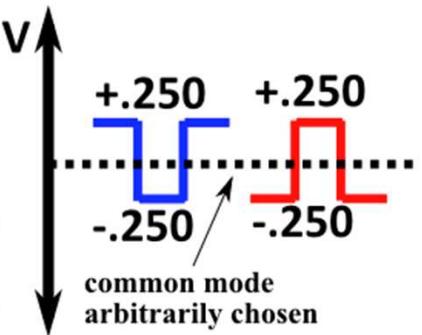
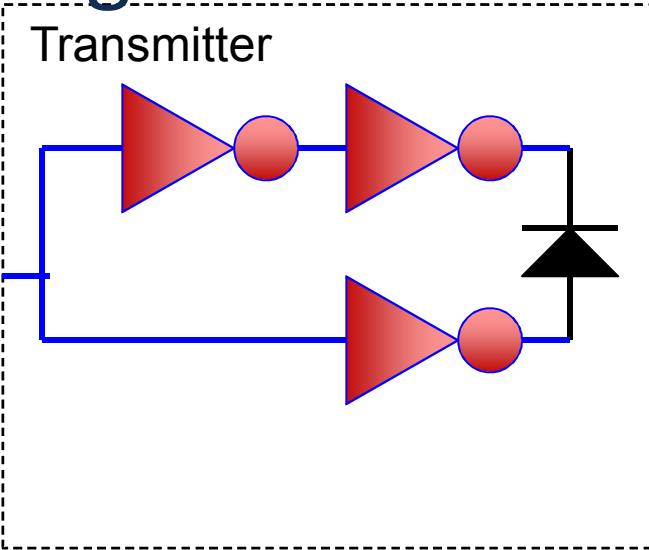
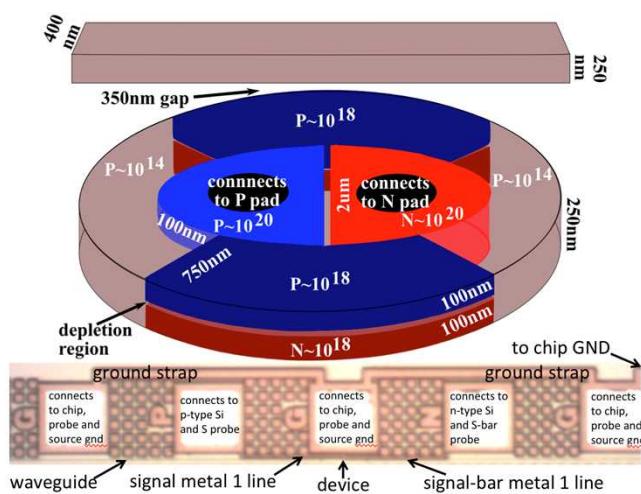
- Requirements:

- Resolution:  $\pm 0.25^\circ \text{C}$  (depending)
  - Range:  $10 - 85^\circ \text{C}$  (depending)



# Simple Modulator Driver: Differential Signaling

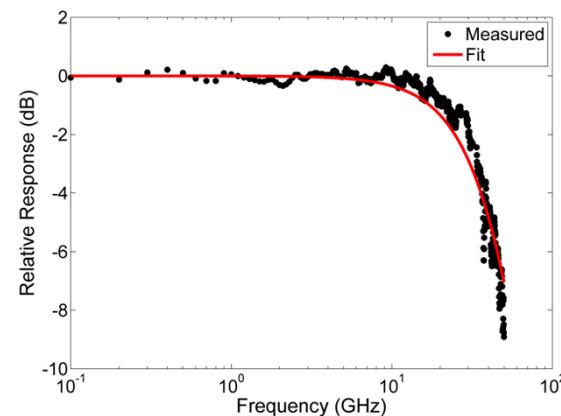
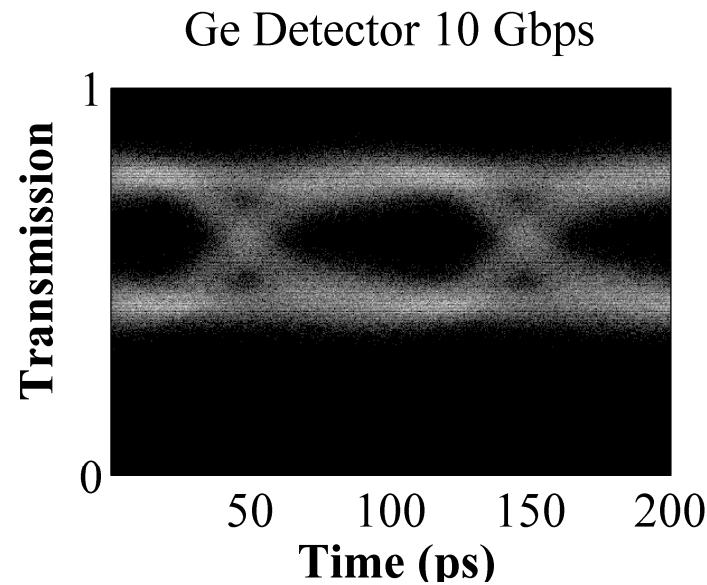
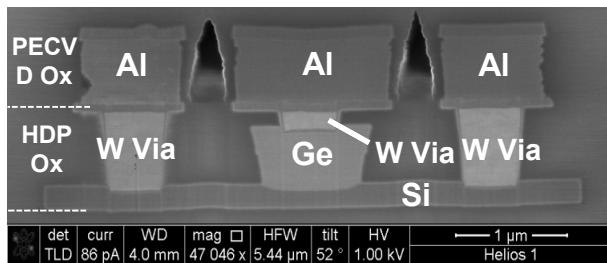
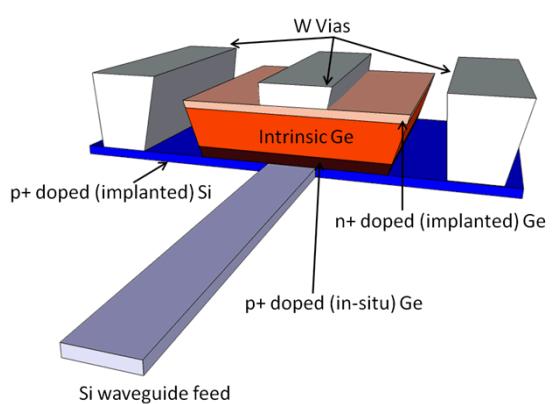
- No pre-emphasis
- No AC coupling
- No high voltages
- CMOS logic levels



- **10 Gb/s**
- **Common Mode:**
- **.25V, .8V, 1.2V**
- **3 fJ/bit**

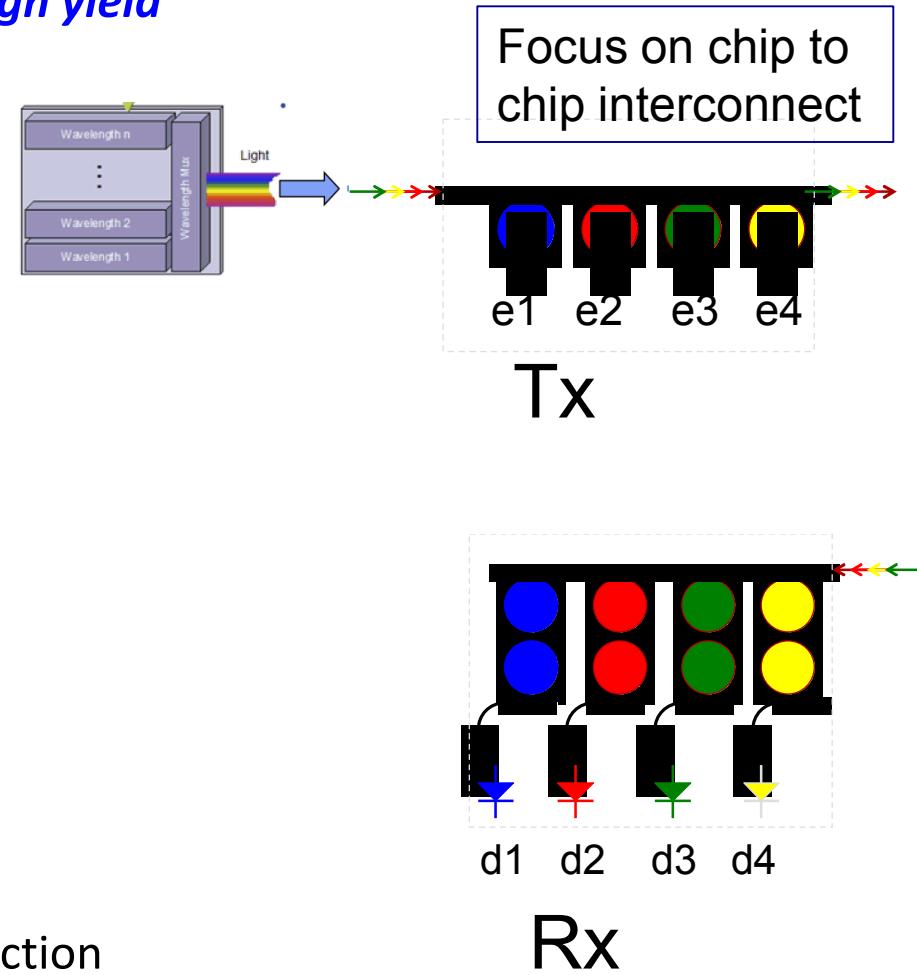
# Integrated Germanium Detectors

- Operation at 10 Gbps
  - equipment limited
- Frequency response  $\sim 45$  GHz
- $\sim 1$  A/W responsivity at 1500 nm
- $< 100$  nA dark current at 1 V



# Technology Gaps

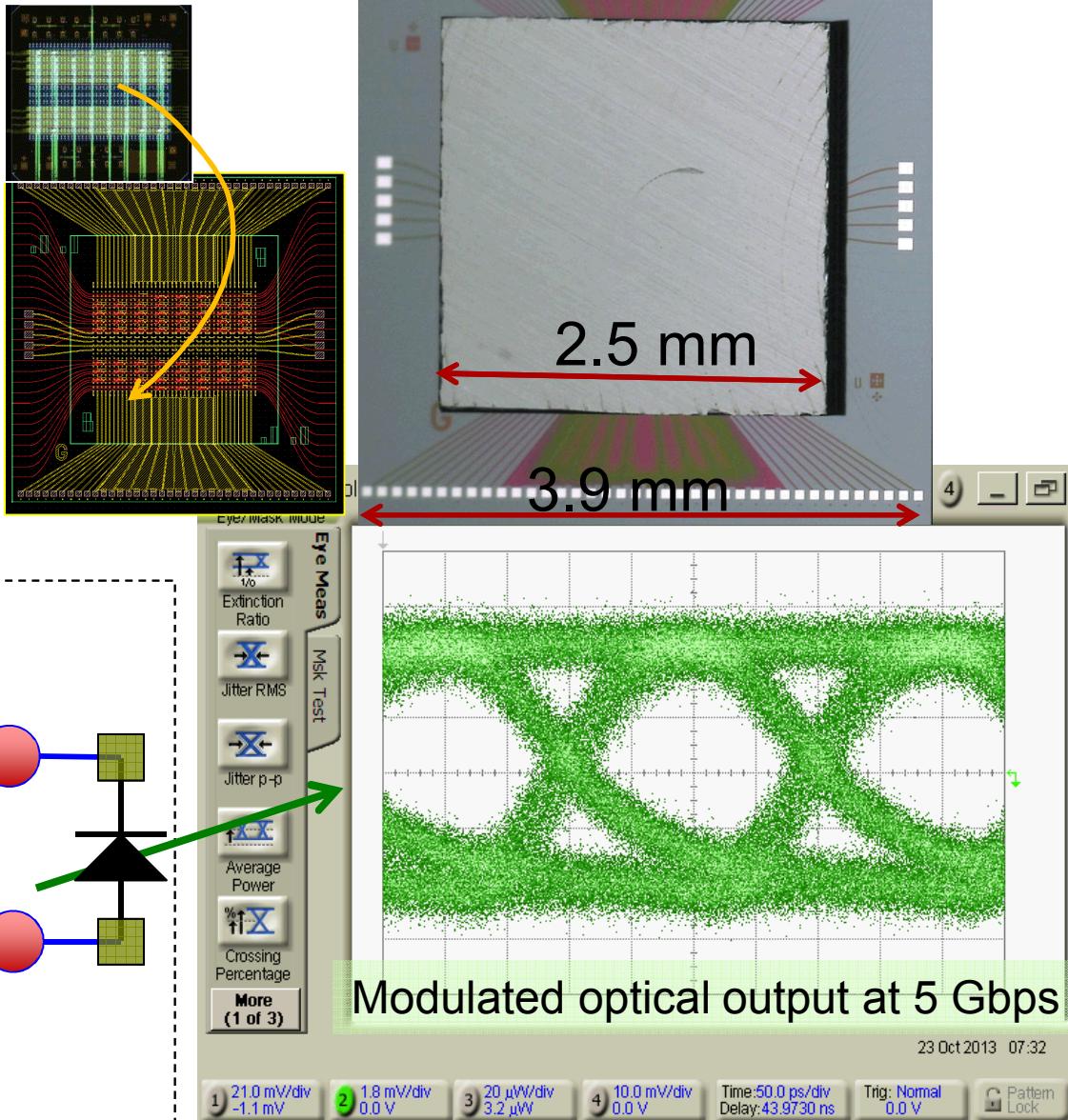
- Integration
  - *Silicon photonics integration with state of the art CMOS with low capacitance and high yield*
  - Cost effective, reliable packaging
- Silicon Photonics
  - *Low energy receivers*
  - *Modulator and optical filter resonant wavelength stability and uniformity*
  - *Fiber coupling and waveguide losses*
  - Efficient Laser source
- Interface Electronics
  - *Efficient clock and data recovery*
  - Data TDM multiplexing (SERDES)
  - Efficient Data encoding and error correction



# First flip chip bonded SiP at Sandia

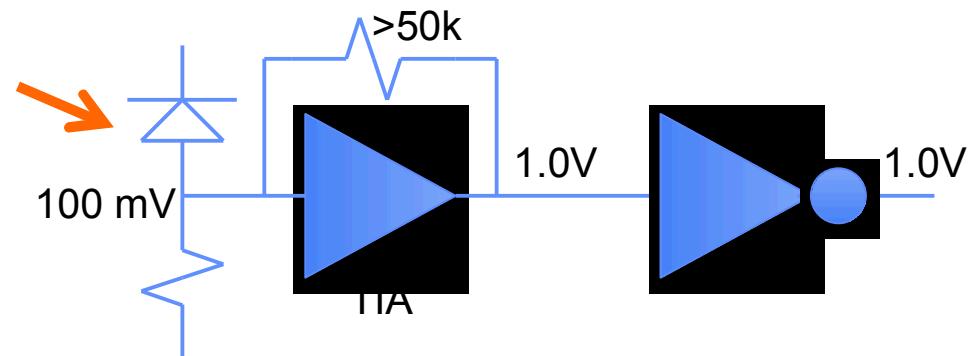
- Modulator drivers, receivers, and combinations
- IBM 45 nm CMOS
- Sandia Silicon Photonics
- 10  $\mu$ m bumps/14  $\mu$ m pads
  - Test coupons 2  $\mu$ m x 5  $\mu$ m
- 1120 connections

- 400  $\mu$ A dynamic current draw at 1V  
 - 80 fJ/bit at 5 Gbps - high bond series R

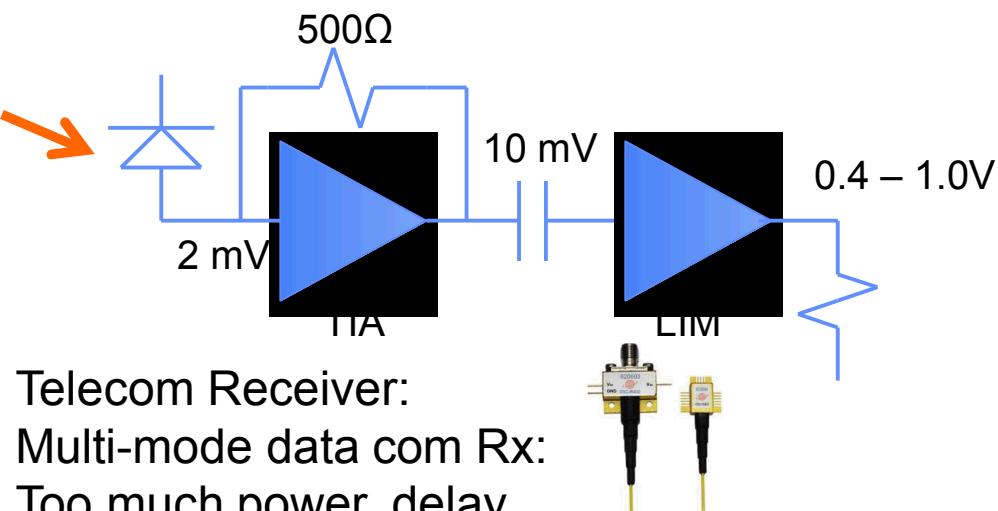


# High Transimpedance Receivers

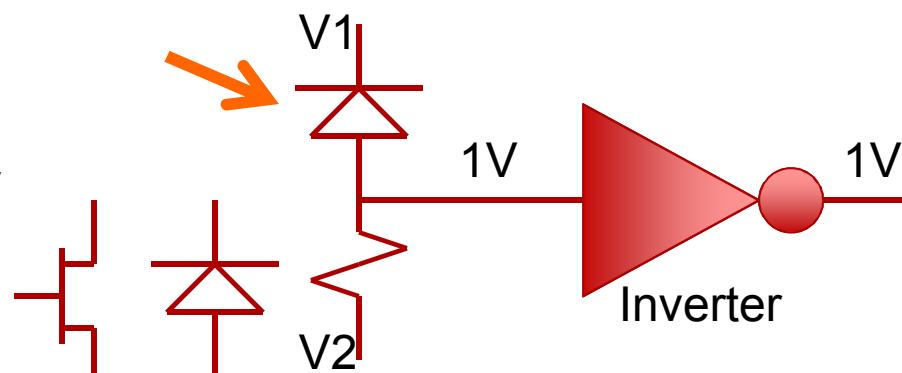
- No AC coupling
- No data encoding
- Low input capacitance
- High trans-impedance
- Low delay



Low capacitance, high transimpedance gain  
Lower noise floor, good sensitivity  
Might be DC offset limited vs. noise limited



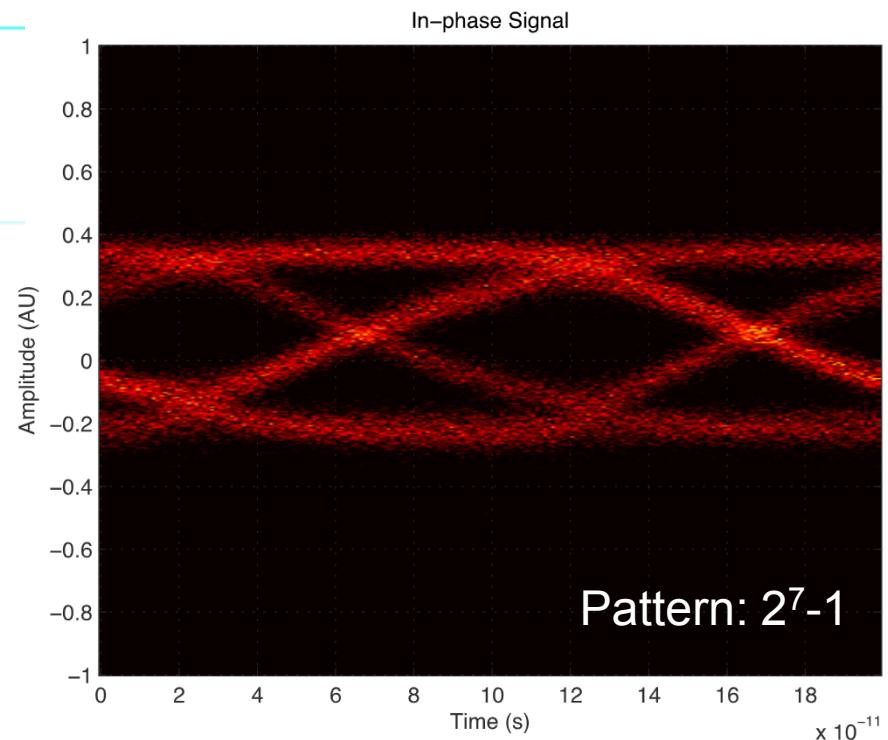
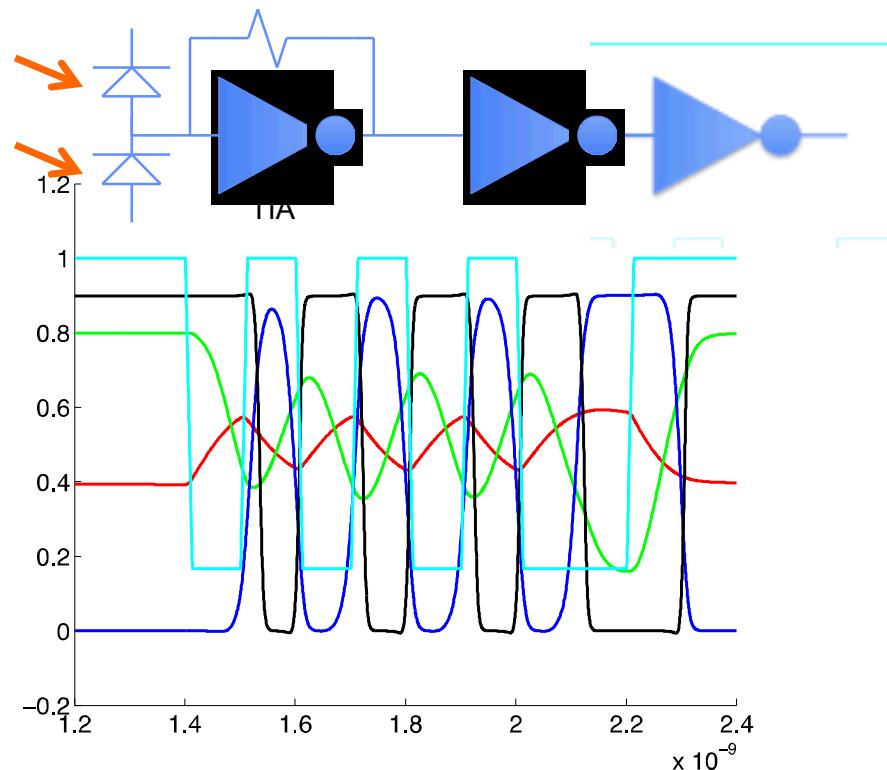
Telecom Receiver:  
Multi-mode data com Rx:  
Too much power, delay



Very low energy, poor sensitivity

D. A. B. Miller et. al., PTL 1989  
L. M. F. Chirovsky et. al., IEEE Int. Opt. (1994)  
C. Debaes, et. al., in IEEE JSTQE (2003)

# Receiver Energies (Simulation)

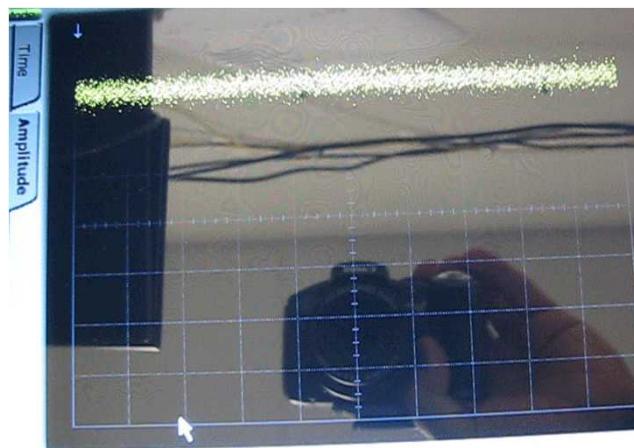
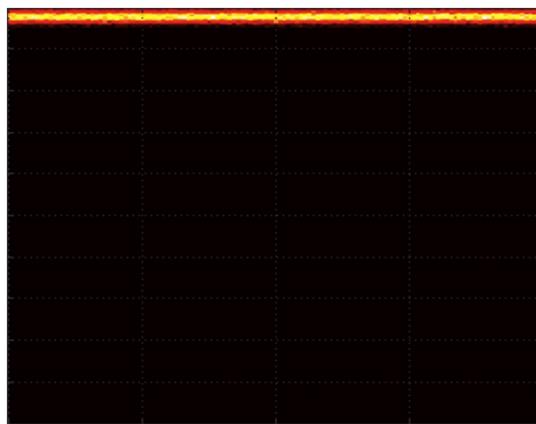
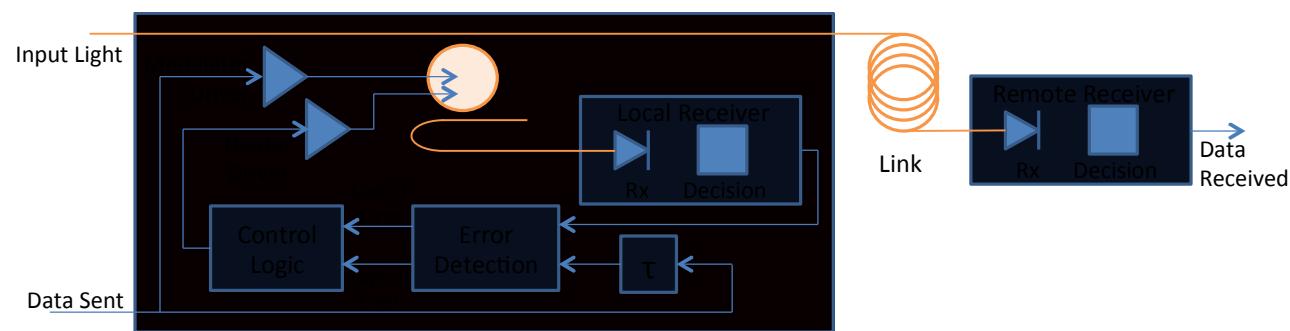
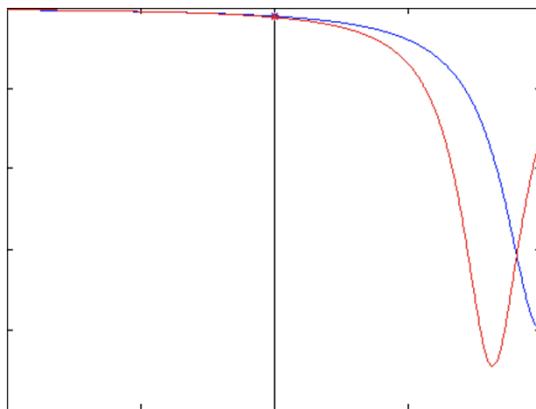


Bit Rate = 10.00Gbps, *Energy per bit* = 2.74fJ

- 45 nm technology node,
- optimum sample delay = 109 ps, total margin= 70ps,
- BER = 0.000000e+00,

# Modulator wavelength stabilization

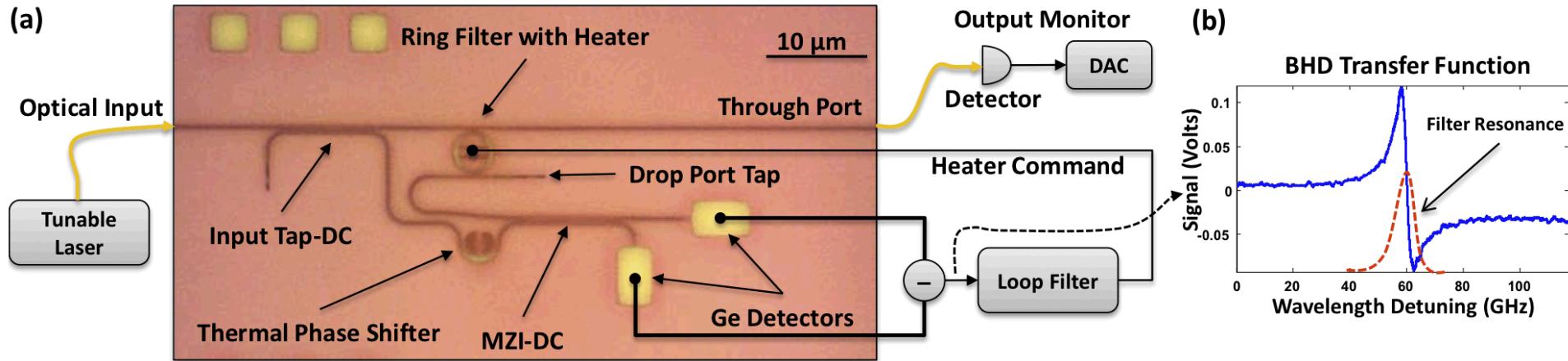
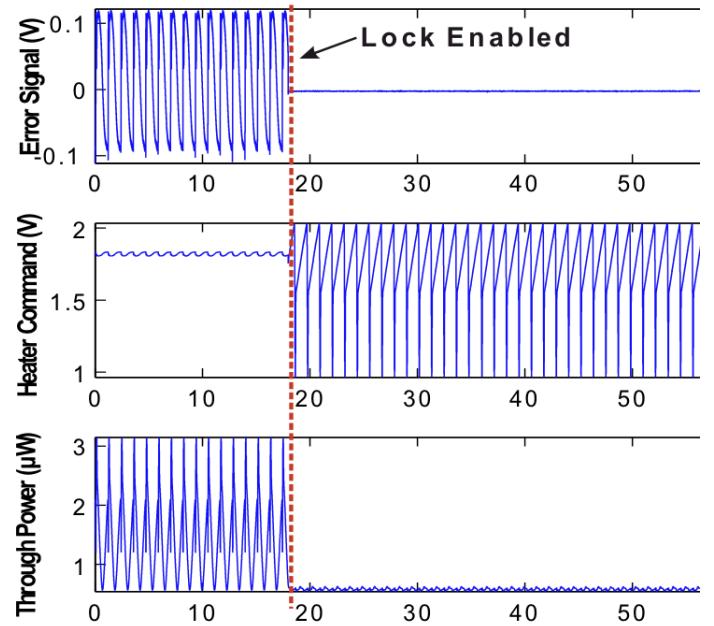
- Local receiver detects 1s and 0s errors
- Shift of the resonator generates asymmetric errors.
  - Simple relation sets operating point



W. A. Zortman et. al., IEEE Micro (2012)

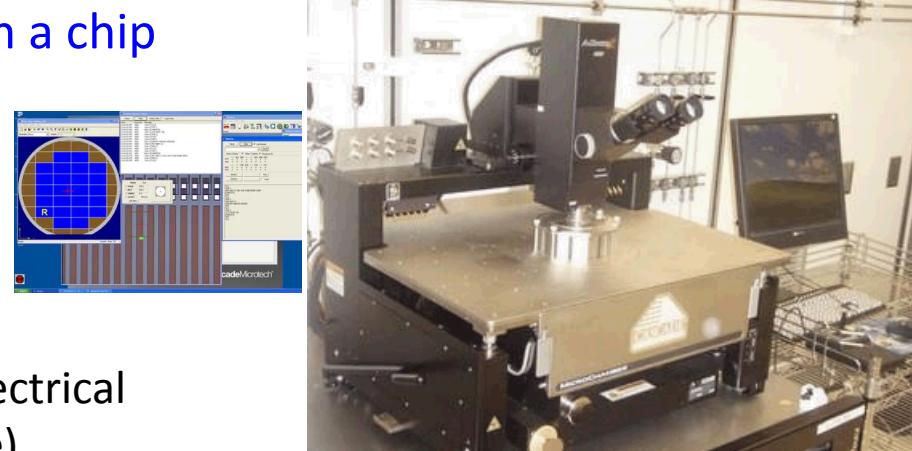
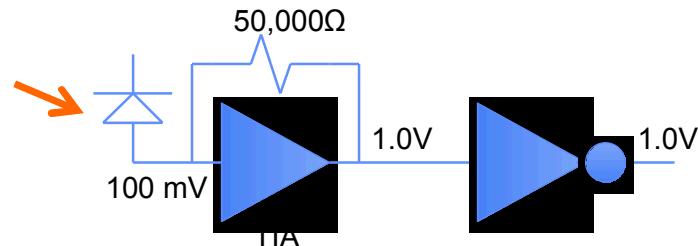
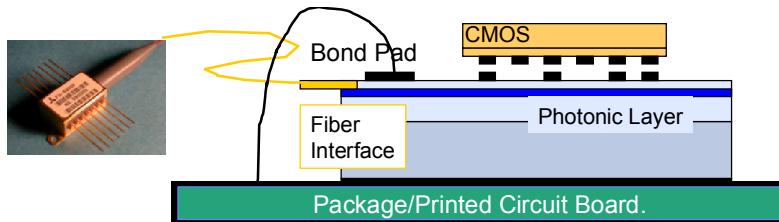
# Resonant locking of a DWDM filter

- Problem: locking on minimum power level does not lend itself to a simple control loop
- Solution: Homodyne detection with balanced detection gives optimal locking solution



# Silicon Photonics Challenges

- Integration with State of the art electronics
  - VERY Low capacitance
  - VERY High yield
- Power reduction of photonics connections
  - Rx designs that reduce system energies
  - Resonant device wavelength stabilization
  - Minimize associated Electronics (CDR, Serdes)
- Laser Source
  - Significant reductions in cost & power
- Scaling to 100,000s of photonic devices on a chip
  - Batch automated testing of photonics
  - Manufacturing (wavelength) variations
  - High Yield
- Design methodology
  - Optical interconnects as comfortable as electrical interconnects to IC designers (design guide)



# Questions?

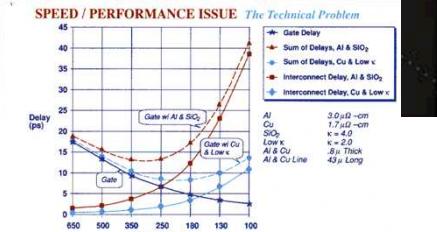
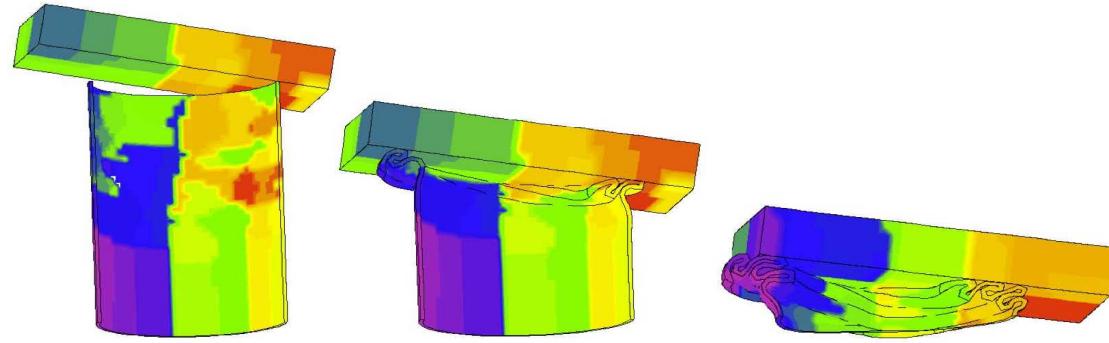


**Anthony L. Lentine**  
**Sandia National Laboratories, Albuquerque NM**  
[alentine@sandia.gov](mailto:alentine@sandia.gov)

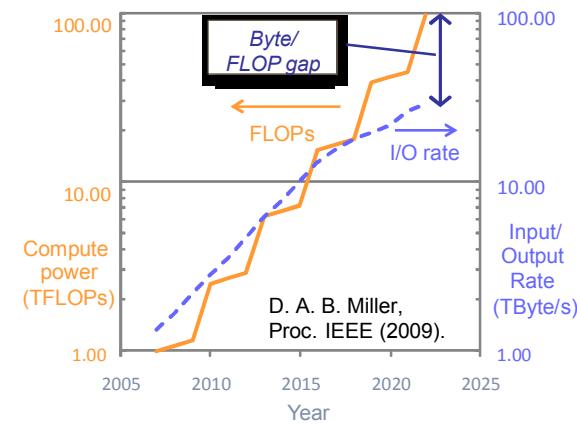
# High performance computing: National Security

## Finite Element Model (FEM) of a Crushed Can

Courtesy of Sandia CSRI

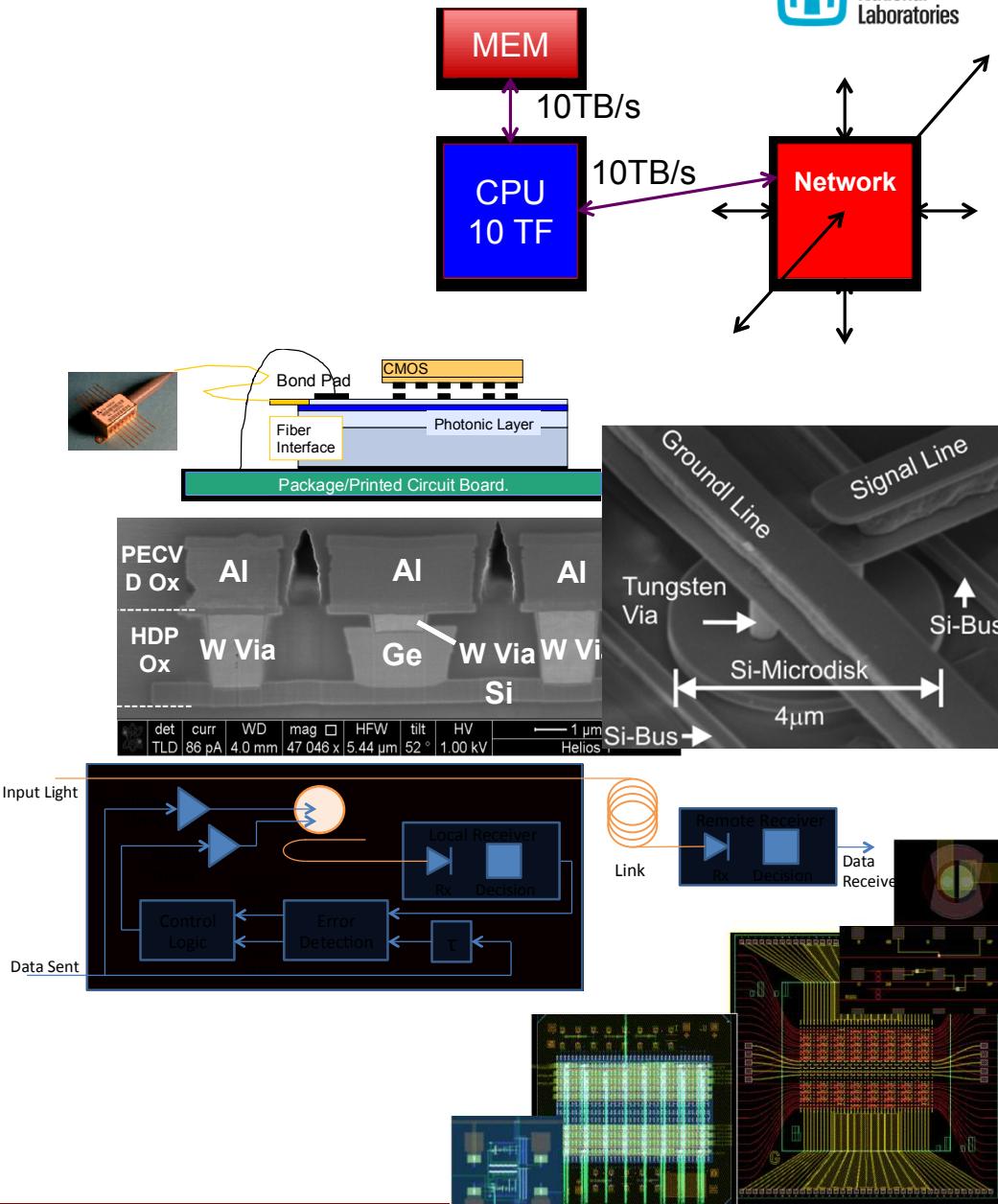


- Physics simulations
- Data analysis
- Future computing scaling limited by interconnect
  - Performance (frequency) not scaling (RC, power)
  - Power dissipation not scaling ( $CV^2f$ )
  - Off-chip interconnect bandwidth not keeping up
  - Result is highly parallel computing (even more so)



# Approach

- Instead of ... Evolutionary architecture approach:
  - Design around limited (network and memory) interconnect bandwidth (<< 1 bit per second/flop)
- Pursue ... Revolutionary approach:
  - Small silicon micro-photonic devices intimately integrated with network and processor ICs
  - Chip-scale **>100Tbps per second IO**
  - **<100 femtojoule/bit** → <10W IO
- Identify and solve critical technology gaps
- Identify fundamental/practical limits
- Develop models for co-design for link energy and bandwidth capability based on experimentally demonstrated key technological innovations, particularly in receivers and resonant wavelength control.



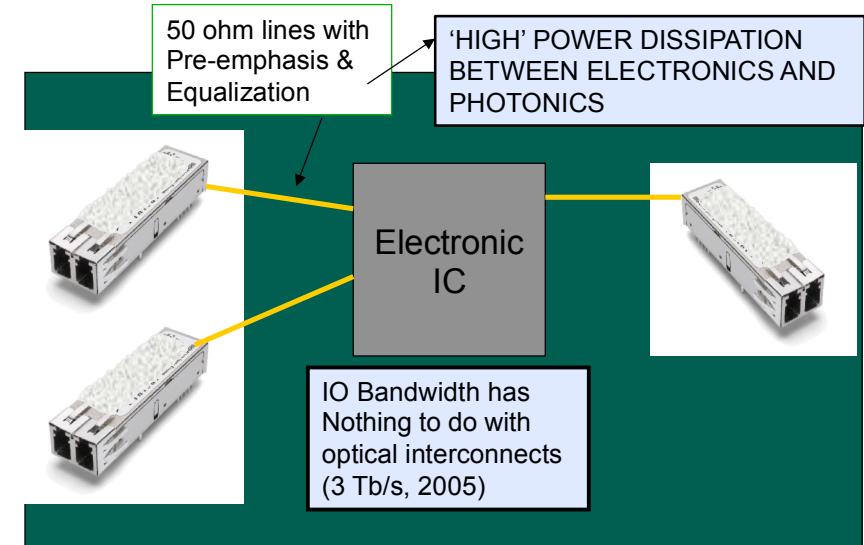
# Optical Interconnects

## ■ Evolutionary (Modules)

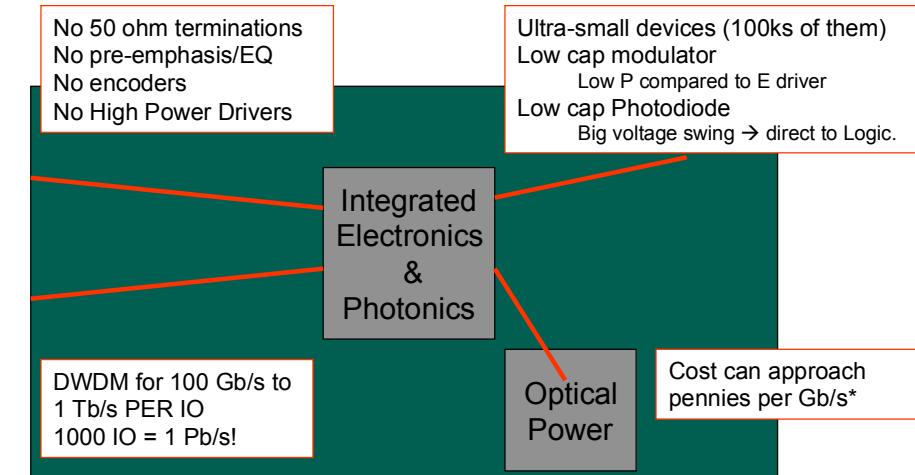
- 10Gb/s Products are low cost
- 100 Gbps modules available
  - Expensive, big, power hungry
- TbE modules on the horizon

## • Revolutionary (3DI)

- Higher bandwidth density
- Drastic potential power reduction
  - No  $50 \Omega$  lines, pre-emphasis or equalization
  - Receiver has high transimpedance, low number of gain stages
  - Shared CDR (less delay variation and jitter)
  - Laser Power (more sensitive receiver)



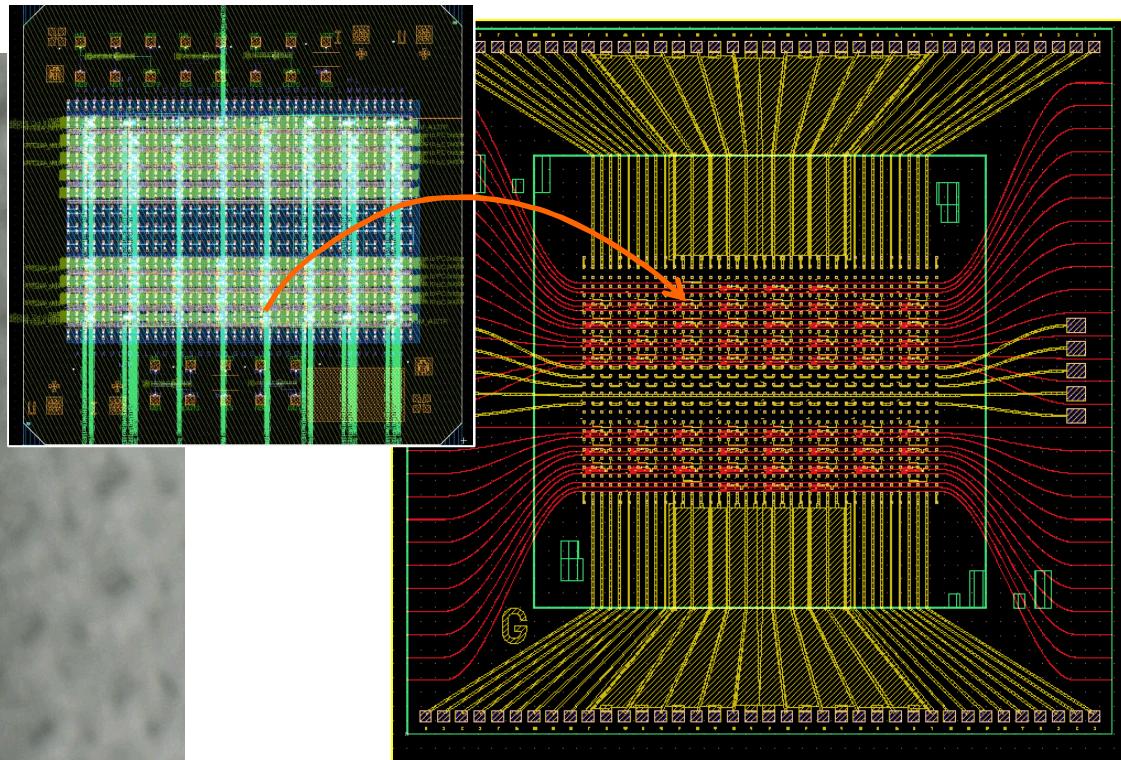
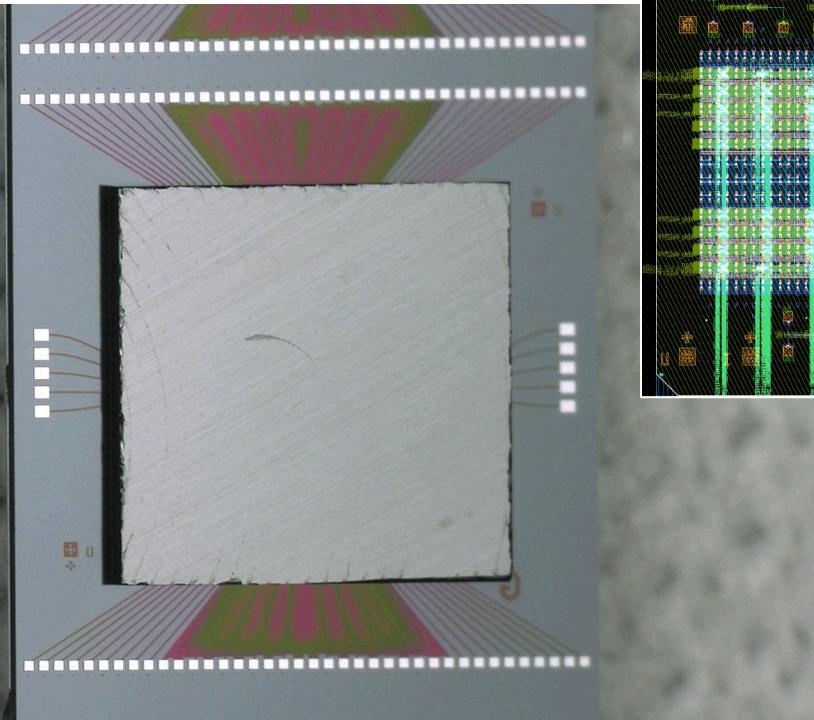
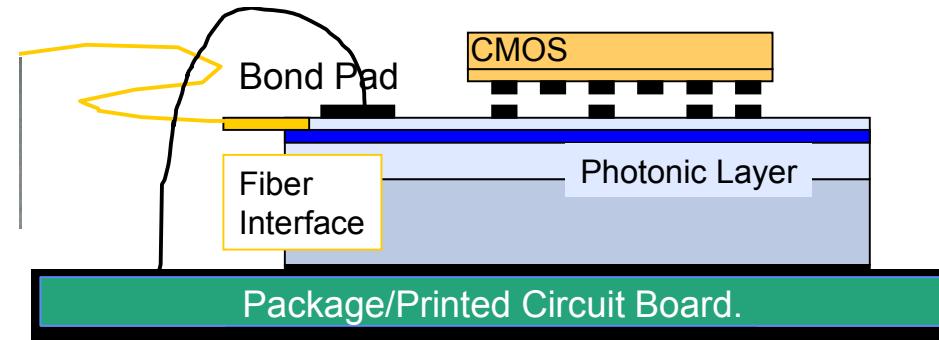
## OPTICS FOR DISTANCE



## OPTICS FOR LOW POWER, HIGH BANDWIDTH DENSITY, COST, SIZE, WEIGHT, DISTANCE

# Electronic-Photonics Integration

- Heterogeneous integration
  - Independent optimization of electronics & photonics
  - Need very high yields and small size



# Lack of scaling in Moore's Law is an interconnect problem

- Gate delay (transistor performance) speeds are scaling
- On-chip RC lines are not scaling
  - Capacitance is nearly constant (fringing)
  - $R$  is increasing as line widths narrow
  - Increased repeaters for long lines
- $\text{Power} = \text{CV}^2f$  (C dominated by interconnect)
  - Capacitance is not scaling (fringing)
  - Voltage also not scaling (transistor)
- Off-chip (electrical)
  - Looming divergent capacity compared to on-chip processing capability

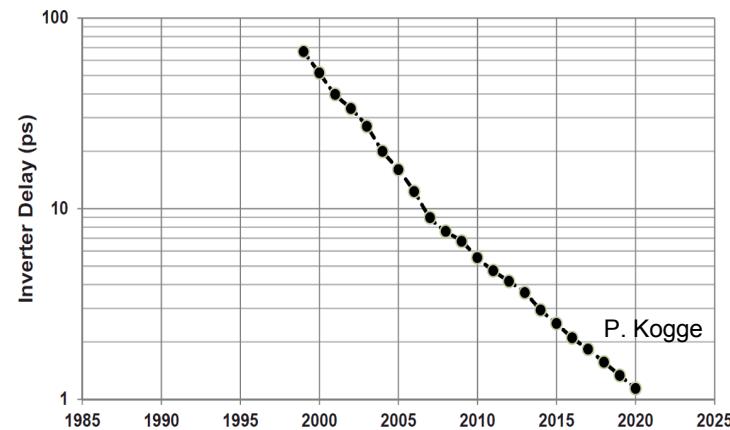
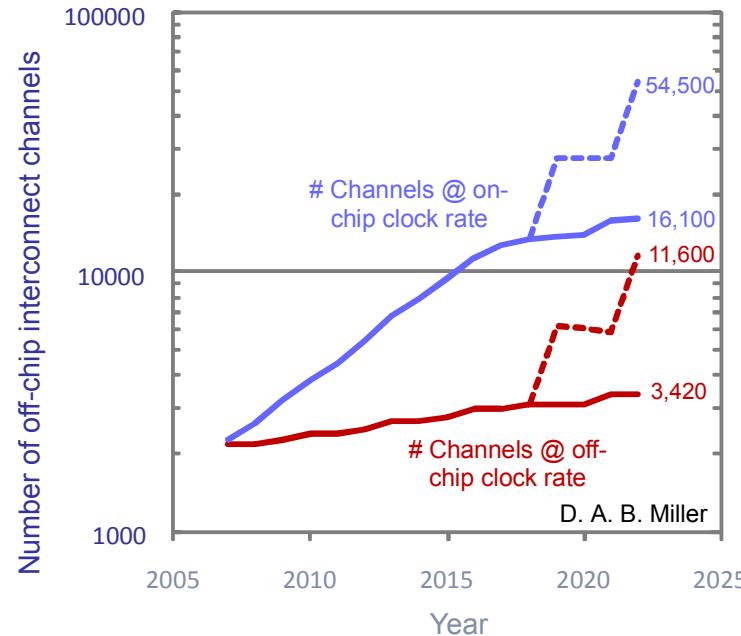
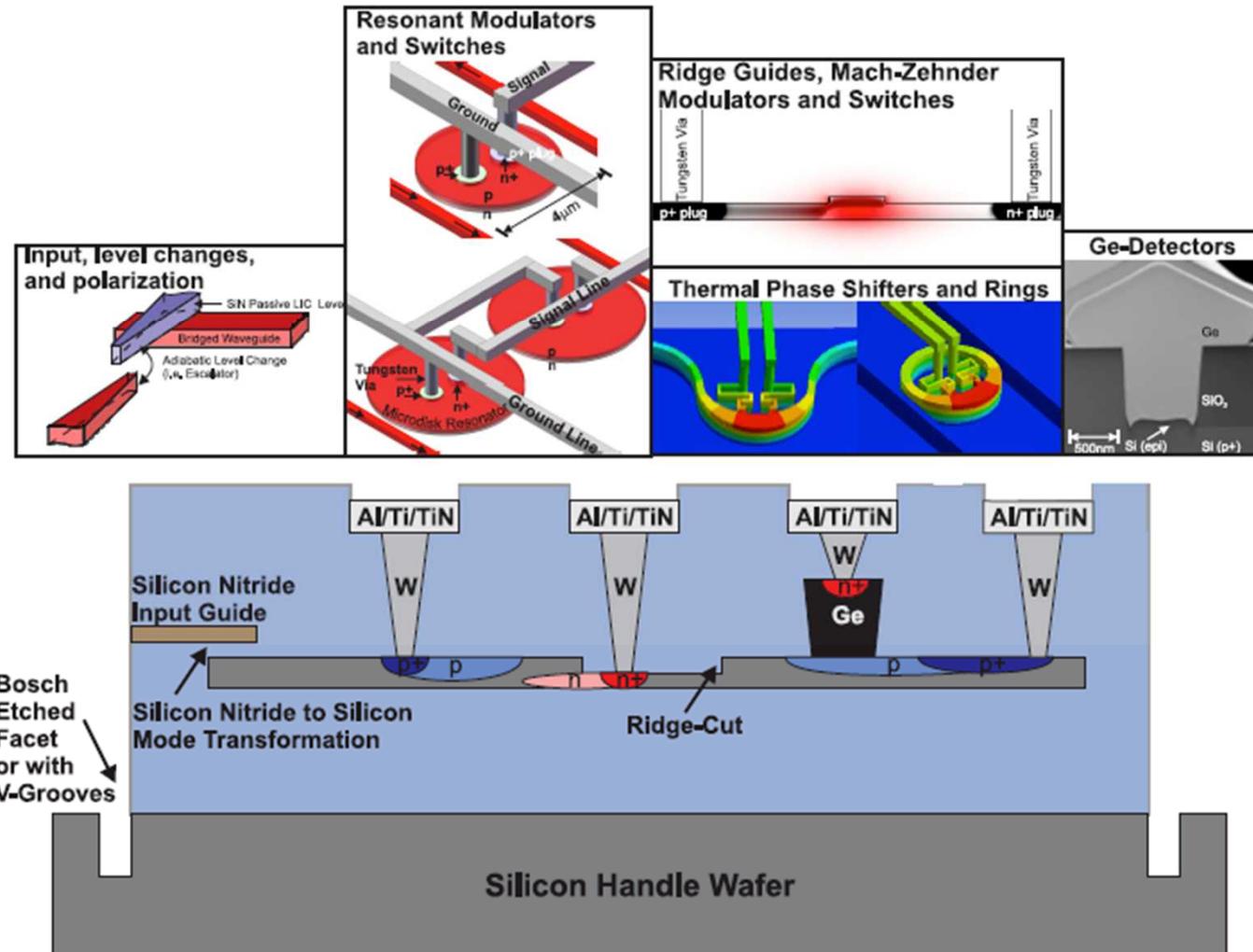


Figure 2.2: Inverter Delay as Derived from ITRS.



# SNL Si Photonics Platform



# Beyond Optical Interconnect

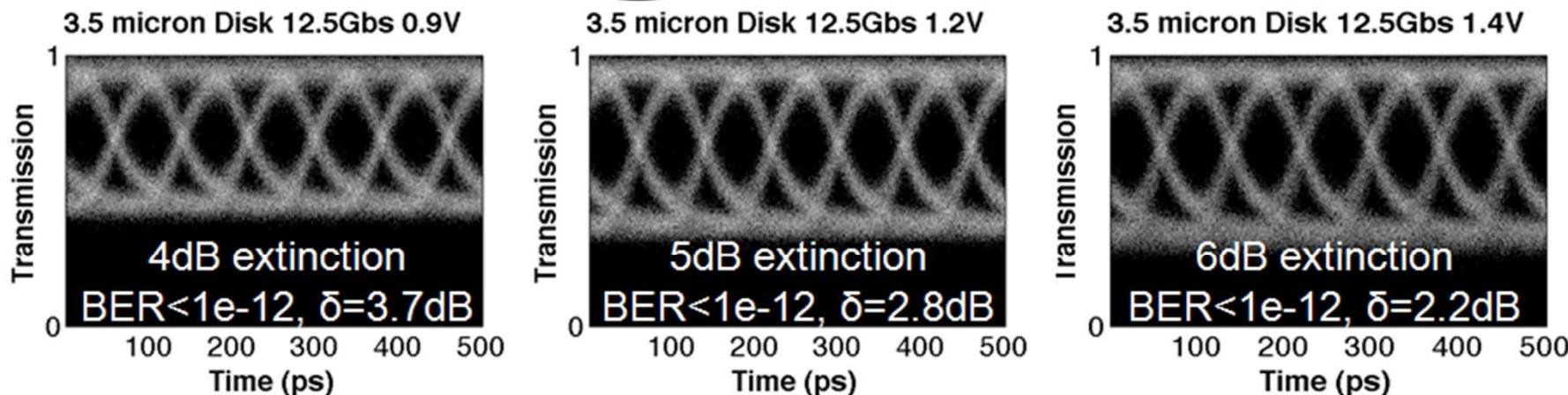
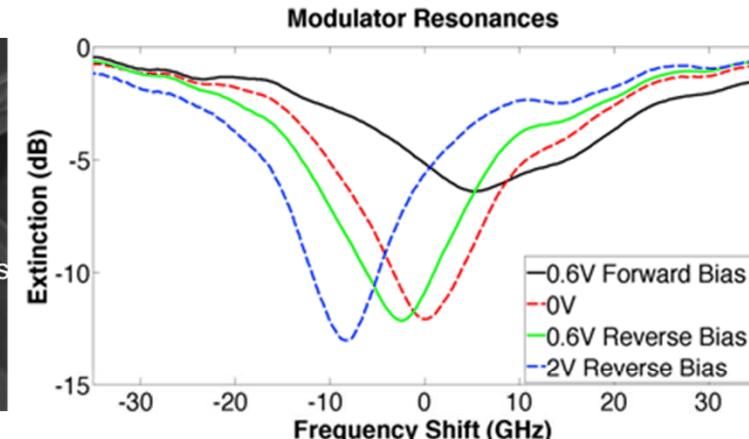
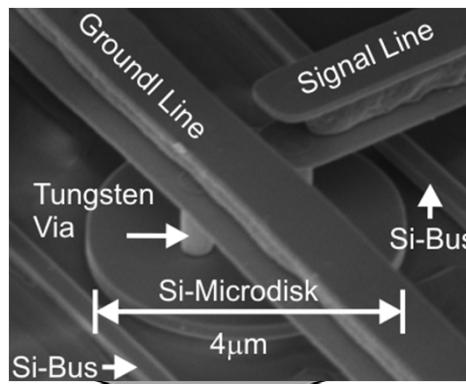
- Various technologies exist for optical transceivers
  - Silicon Photonics, VCSELs & III-V integrated optoelectronics
- Intimate integration with high-value electronics
  - Lower power and higher bandwidth density, lower cost?

---

- From a networking perspective, optical interconnects aren't that interesting
- More interesting are routing functions
  - Passive routing (wavelength intermixing)
  - Active provisioning (not reconfigured often)
  - 'Flow' or packet routing (reconfigured every ps/ns/us)

# Low Energy Optical Modulators

- Very small device
- Limit doping in ring
- Slight drive into forward bias for reduce voltage



Energy/bit: 0.9V

Analysis: 3.8fJ/bit

Measured: 3.2fJ/bit@1V

1.2V

6.8fJ/bit

1.4V

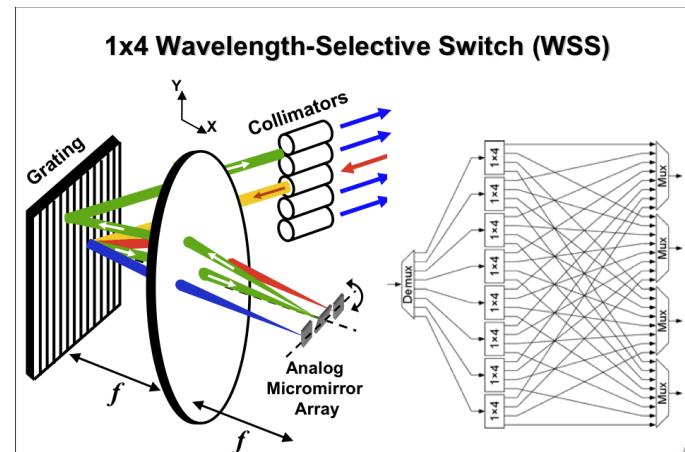
10.6fJ/bit

10.1fJ/bit@1.5V

W. A. Zortman, M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine,  
'Low power, high speed silicon microdisk modulators,' CLEO 2010

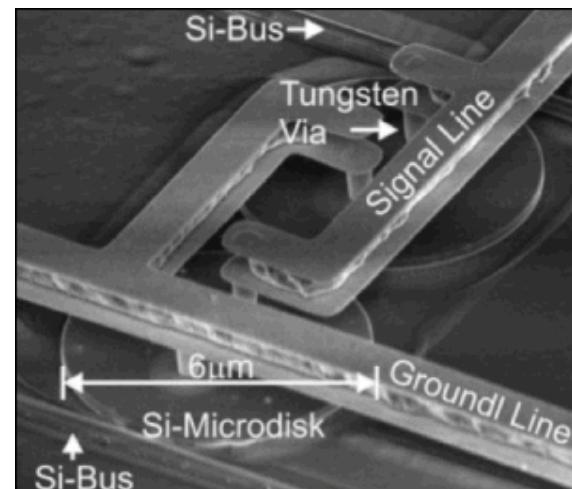
# Active switching technology choices

- MEMs, Liquid Crystal (WSS)
  - 1:N (good!) or 2 x 2 (bad)
  - Slow (1 us – 1 ms)
  - Often free-space (grating for WSS) {expensive}
  - Fairly scalable to large sizes?
    - $80 \lambda \times 1 \times 9$
  - Flex bandwidth
  - Products
- Integrated Optics (Silicon Photonics, III-V)
  - 2 x 2 (bad)
  - Slow (1 us) or very fast (<100ps)
  - Scalable (with more maturation)
  - Flex bandwidth
  - Research



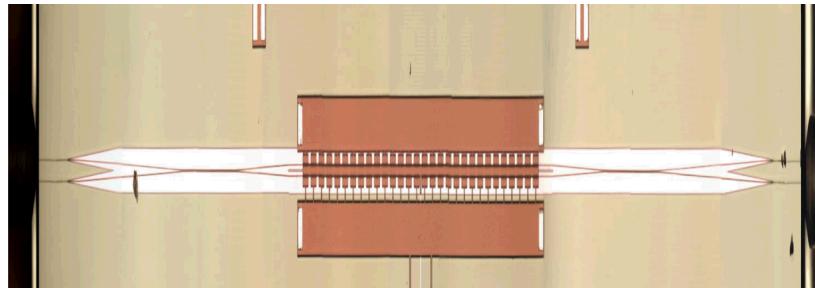
Ming Wu, EE233 class notes  
Dan Marom et. al., OFC 2002

BSAC

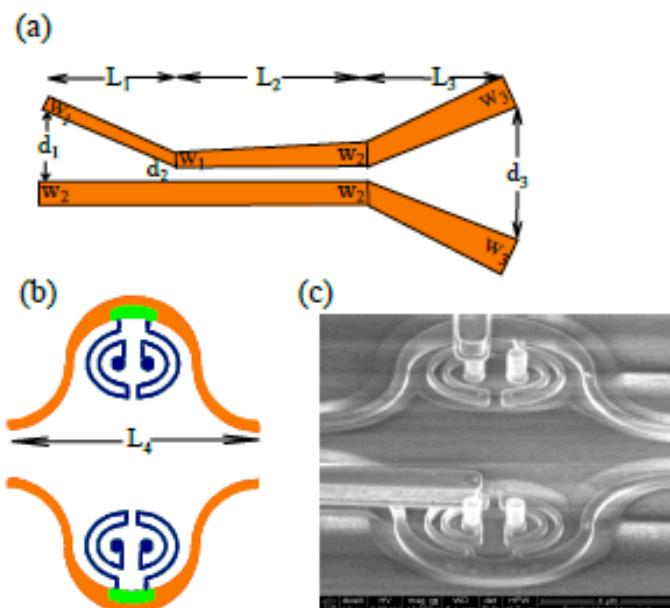


M. Watts et. al., Group IV Photonics 2008

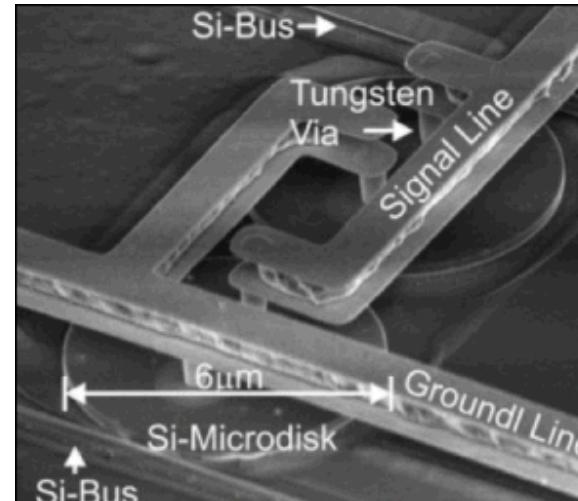
# Sandia 2 x 2 silicon photonics switches



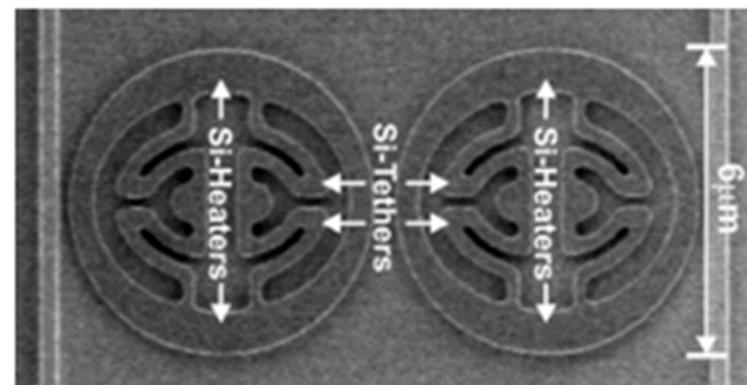
## MZ – free carrier effect



## MZ – thermo-optic



## MR – free carrier effect

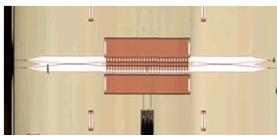


## MR – thermo-optic

# Sandia 2 x 2 silicon photonics switches

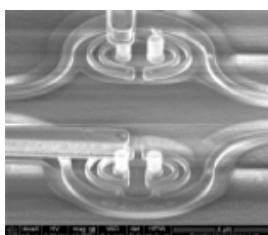


- Fast (< 100ps)
- Broadband
- 1pJ/switching event
- No static power
- 1 mm size



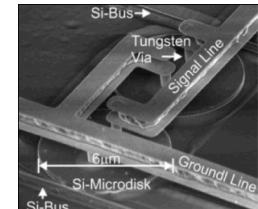
## MZ – free carrier effect

- Slow (10 us)
- Broadband
- $\sim 15 \text{ mW}/2\pi$
- Static power in one state
- < 10 um size + coupler



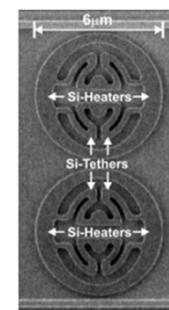
## MZ – thermo-optic

- Fast (< 100ps)
- Wavelength selective\*
- 1fJ/switching event
- No static power
- < 10 um size



## Ring – free carrier effect

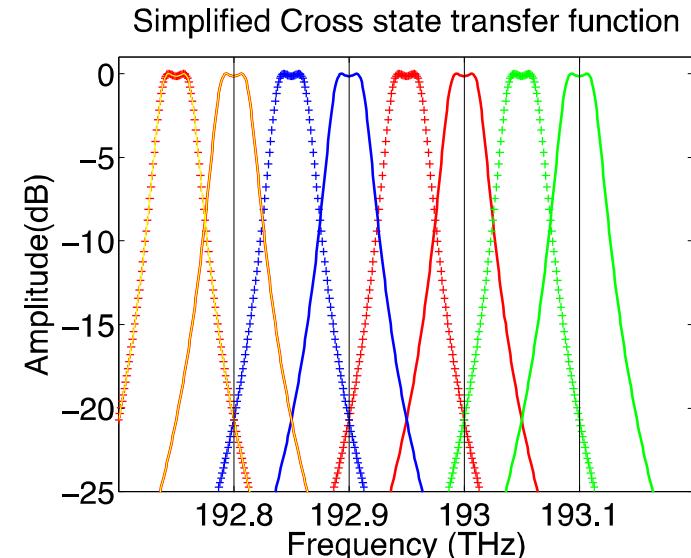
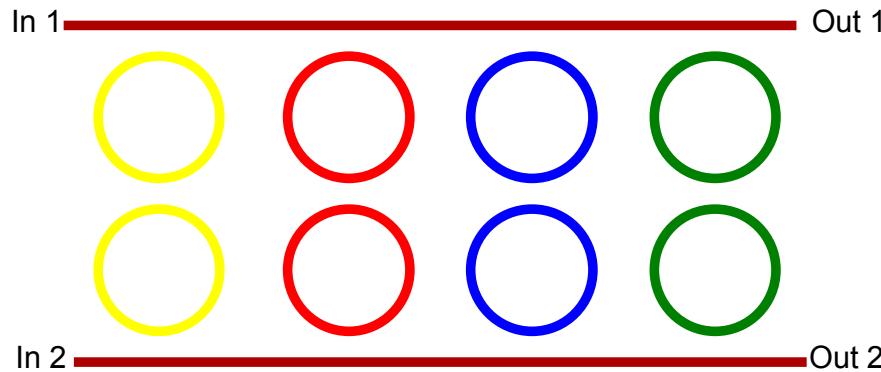
- Slow (10 us)
- Wavelength selective
- $\sim 4 \text{ uW}/\text{GHz}$  (200uW)
- Static power in one state
- < 10 um size



## Ring – thermo-optic

\*Can also switch all channels at once if free spectral range = channel spacing

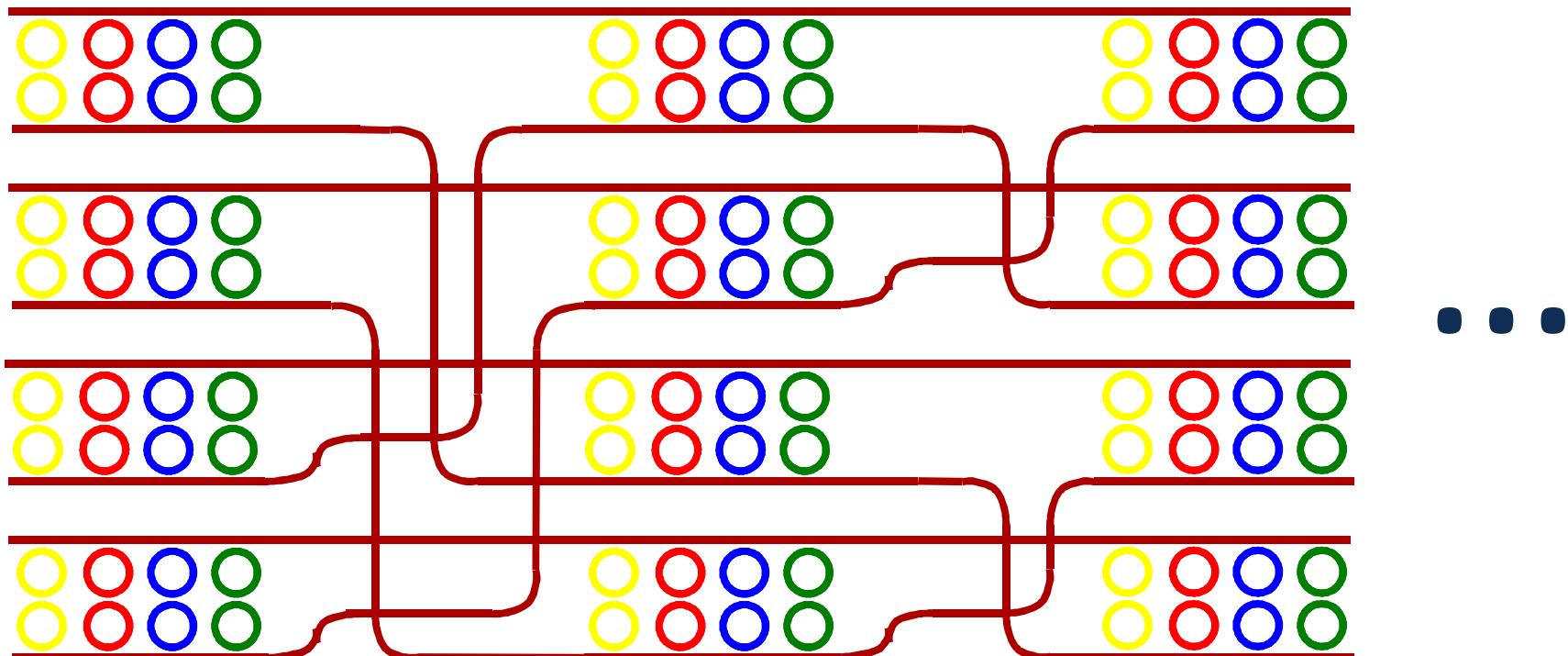
# Si Photonics 2 x 2 WSS



## LONG TERM (IDEAL) SPECS:

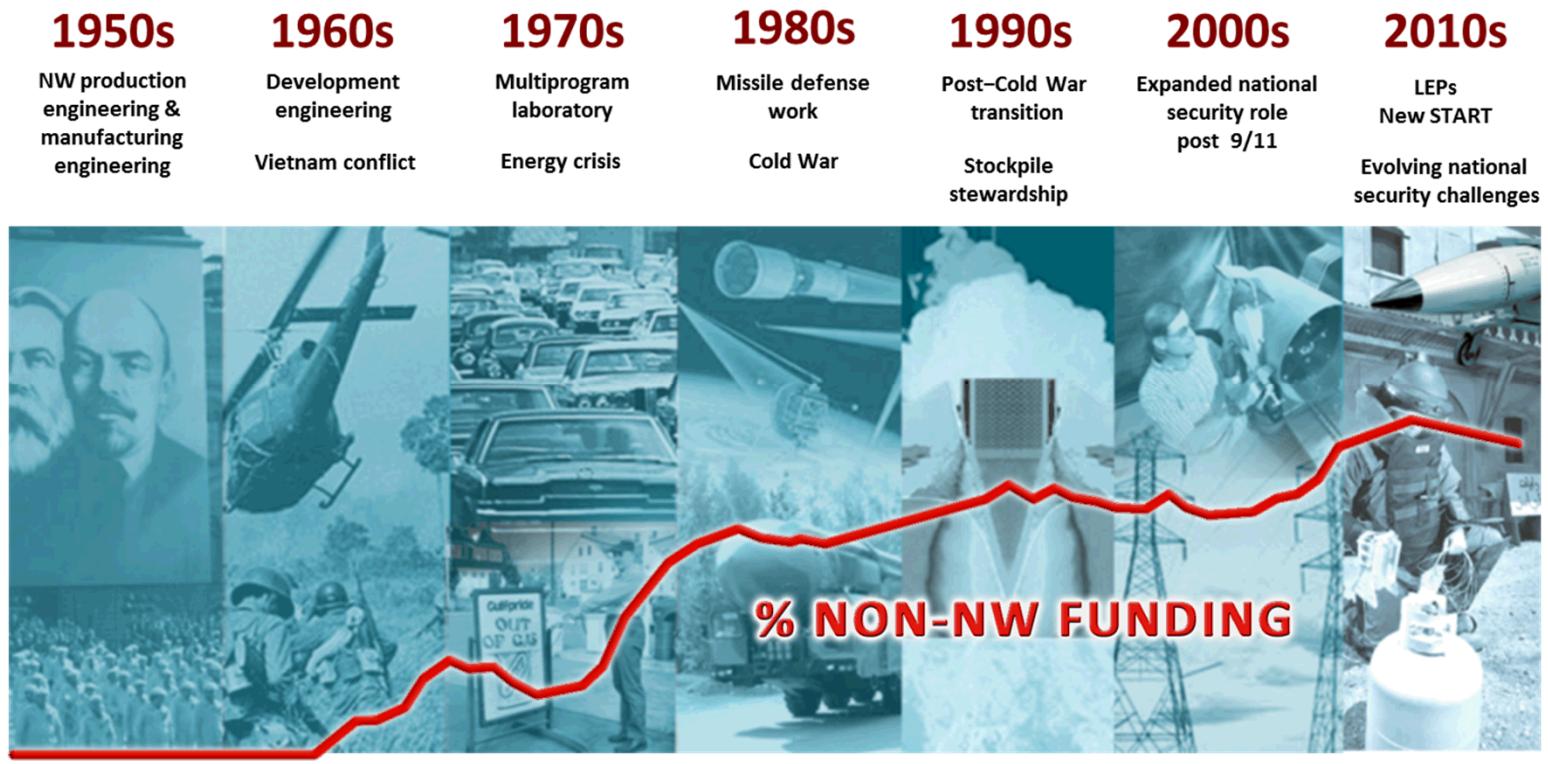
- Ultimate Switch time < 25 ps
- Loss (cross state) 1 – 2 dB
- Loss (bar state) < 0.2 dB
- Crosstalk (15 – 30+ dB)
- Resonant wavelength stabilization
- Ring Size  $\sim$  4 - 6  $\mu\text{m}$
- Coupling gaps  $\sim$  200 - 500 nm
- Ring to ring spacing  $\sim$  4 – 6  $\mu\text{m}$ \*
- Size < 12  $\mu\text{m}$   $\times$   $\lambda$   $\times$  10  $\mu\text{m}$ .

# WSS Networks ...



- Variety of networks from  $2 \times 2$ s
  - Squaring of crosstalk (EGS, Dilated Benes)
  - Tradeoff between initial fan-out and number of stages (EGS)
- Interconnects require planar crossings or two level optics
  - Nitride, Polysilicon: crosstalk can be very good, careful of loss

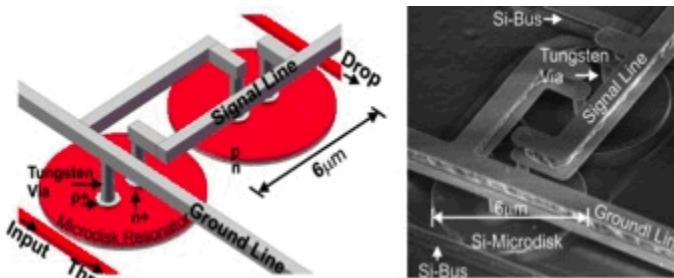
# What is Sandia National Lab?



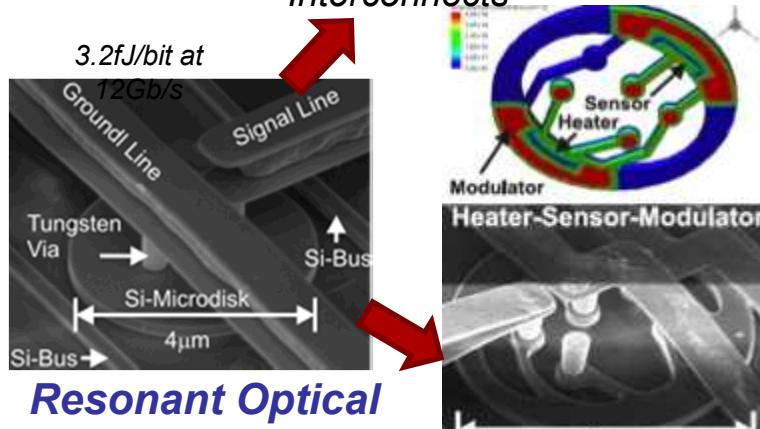
- DOE FFRDC: Initially Z-division of Manhattan Project (Non-nuclear Components, Weaponization of NEP)
- **National security tech transition:** Gov't Agencies (&/or Academia) → SNL → Industry
- DOE supports our “Strategic Partnership Projects” (with Industry & other gov’t agencies (OGAs))
- Our Big 3: **Non-compete with Industry, Fairness of Opportunity, No Organizational Conflict of Interest**
- Managed by LMC, but see OCI above
- **CRADAs with many Defense Contractors, Many STTRs & SBIRs, BAA response teaming**
- **Experience handling sensitive & proprietary information**

# Silicon Photonics At Sandia

## Free-carrier Effect (high-speed)



## Fast Reconfigurable Interconnects



## Resonant Optical Modulator/Filter

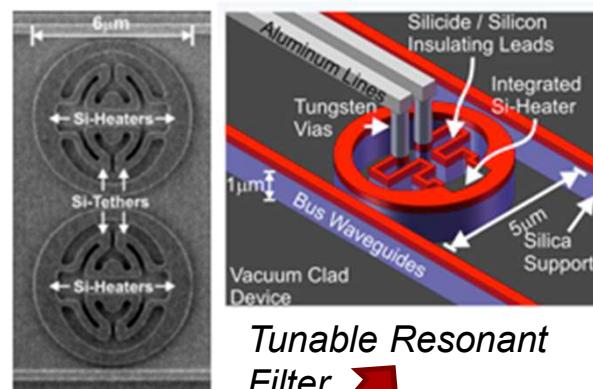
Thermally stabilized modulator

## Broadband Mach-Zehnder Filter/Switch

< 1V-cm at 10 Gb/s



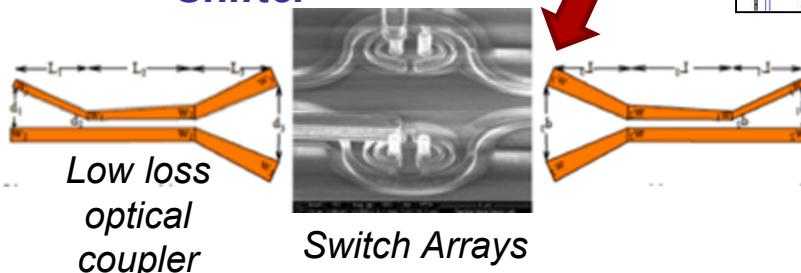
## Thermal Optic Effect (wide-band)



## Tunable Resonant Filter

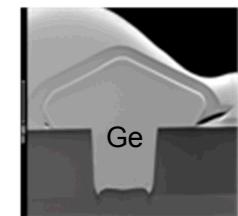


## Thermo-optic Phase Shifter



## Switch Arrays

## High-speed Ge Detector in Si Photonics-CMOS Integration



## Si Photonics-CMOS Integration

