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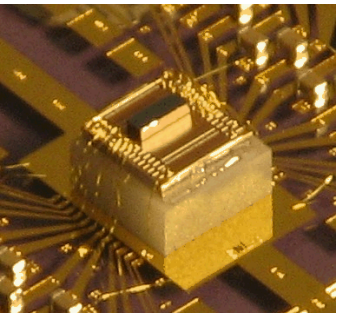
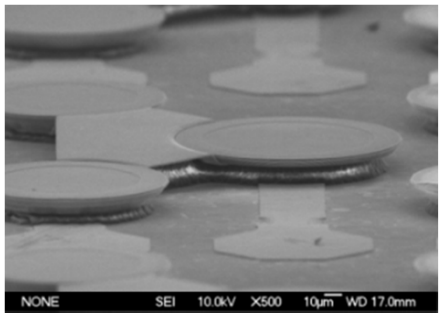

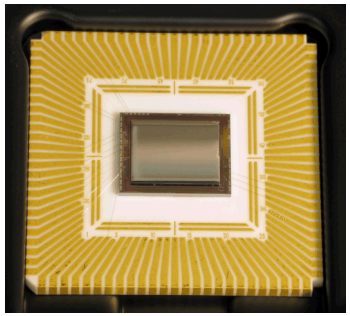
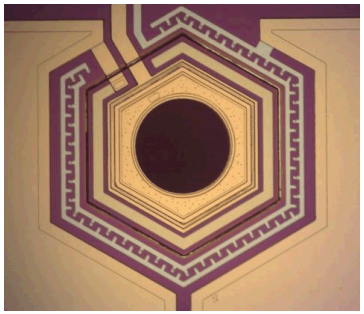
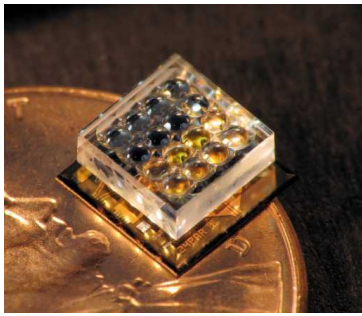

Heterogeneous Integration of III-V Photonics and Silicon Electronics for Advanced Optical Microsystems

Gordon A. Keeler, Kent M. Geib, Darwin K. Serkland, Gregory M. Peake, Mark E. Overberg, Jeffrey G. Cederberg, Thomas M. Gurrieri, Jin K. Kim, and Charles T. Sullivan

Sandia National Laboratories

U.S. DEPARTMENT OF ENERGY | NNSA National Nuclear Security Administration

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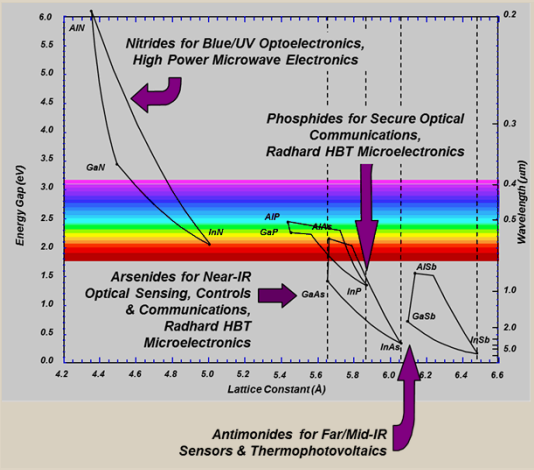
Heterogeneous Integration of Photonics at Sandia

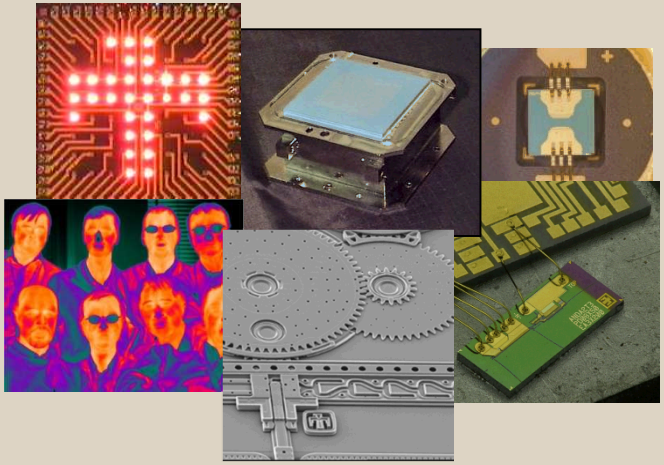
microsystems capability

SiFab: 11,900 ft² Class 1
MicroFab: 14,230 ft² Class 10/100

compound semiconductors



advanced photonics



Rationale for integration

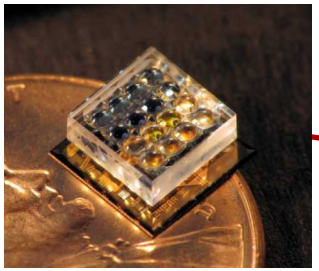
- **SWAP-C:** size, weight, and power; cost
- **performance:** combine technologies, improve interconnect
- **diverse functionality:** optical, RF, MEMS, analog, chem, bio
- **agility & turn time:** prototyping and low-volume
- **trust:** secure microsystems

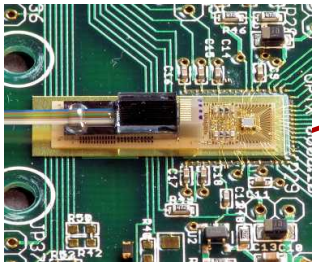
} low volume, high value

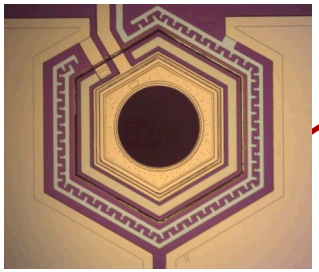
Approaches to integration

- in-package
- this talk → die-to-die: flip-chip bonding, micro-optics, etc.
- talk 17.2, next → wafer-level: interconnect bonding (3D DBI)
- wafer-level: epitaxy bonding (dielectric interfaces)
- common at Sandia → monolithic integration

Outline







Overview of Si/III-V heterogeneous integration

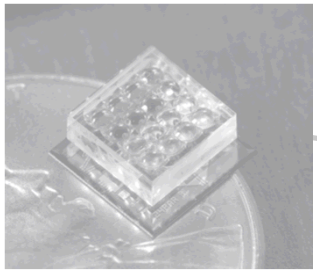
- rationale and methods

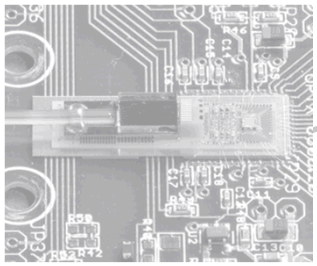
Selected photonics programs leveraging integration

- imaging sensor development
  - nBn detector arrays based on GaSb
  - indium-based flip-chip to silicon ROICs
- optical microsensor prototyping
  - photonic proximity fuzing
  - high-power lasers, detectors, micro-optics
- low-power data communications R&D
  - high-performance computing & cryogenic satellite applications
  - 32-nm CMOS, dense VCSEL & photodiodes, micro-optics, multi-core fibers
- pathfinder technologies
  - microsystem-enabled photovoltaics
  - III-V/CMOS microelectronics
  - high-performance & extreme environment applications

Outlook and Summary

Outline





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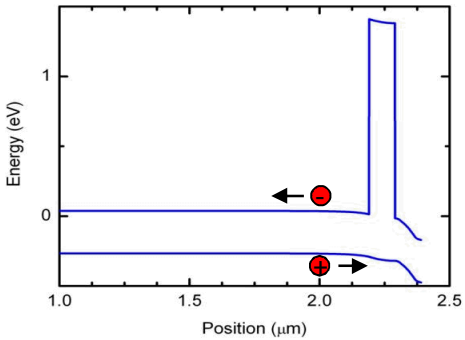
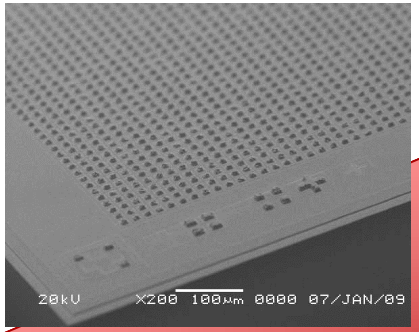
Outlook and Summary

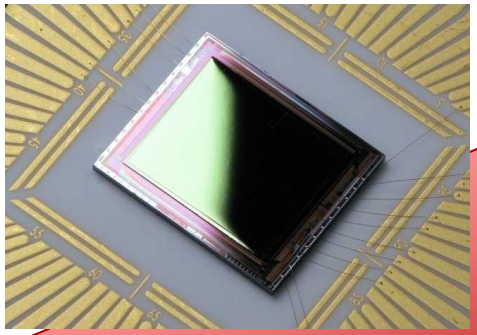
MWIR/LWIR nBn Focal Plane Arrays



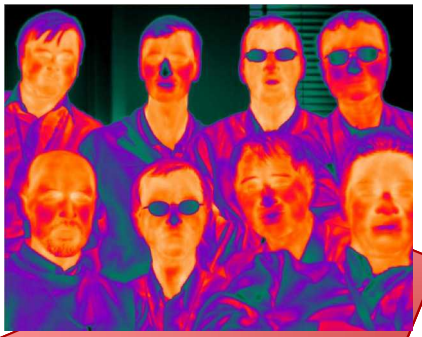
nBn band diagram



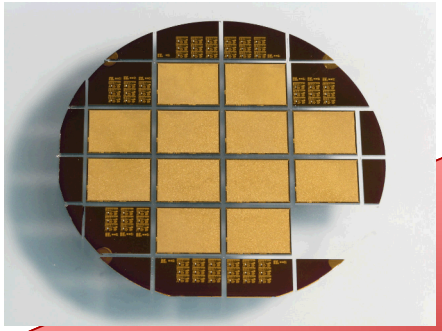
nBn array with indium bumps



hybridized nBn FPA prototype



MWIR still frame, 160K

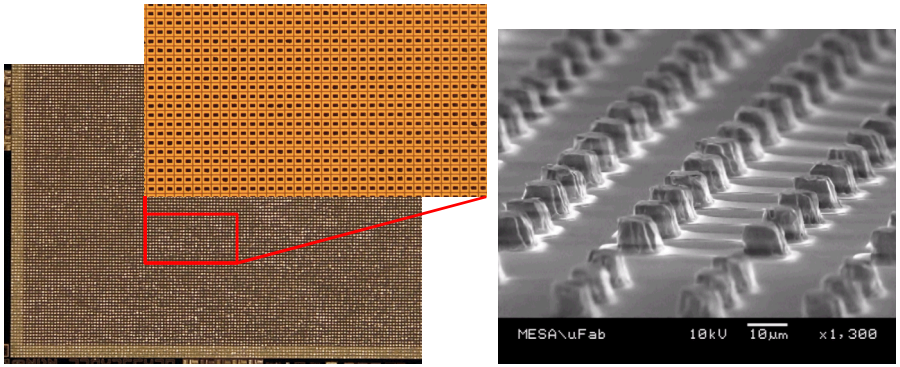


GaSb detector epitaxy

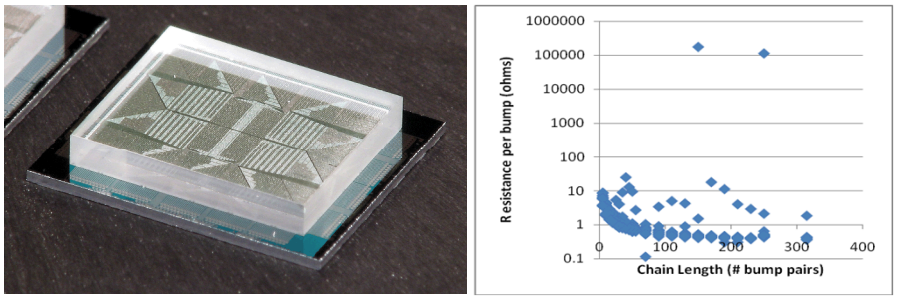
- **nBn rapidly approaching MCT sensor performance**
- **In-house development of nBn detector technology includes growth, fabrication, integration, and device/system testing**
- **Requires hybridization of large (≤1MP) GaSb detectors to CMOS ROICs**

FPA Integration Process Overview 1

- **ROIC hybridization after back-end fabrication & detector testing**
  - **solder dam, underbump metallization**
  - **indium solder bumps (electroplating or evaporation)**
  - **singulation**
  - **flip-chip bonding**



pixels with indium bumps (~8µm)



bonded test chips to assess yield (>0.9999)

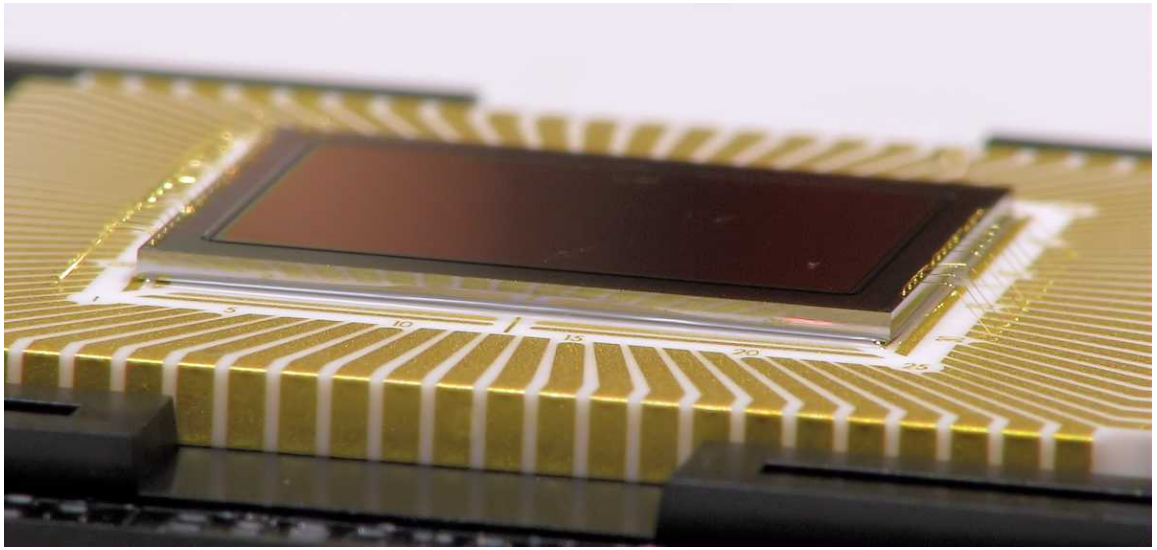
semi-automated flip-chip bonder

Capabilities:

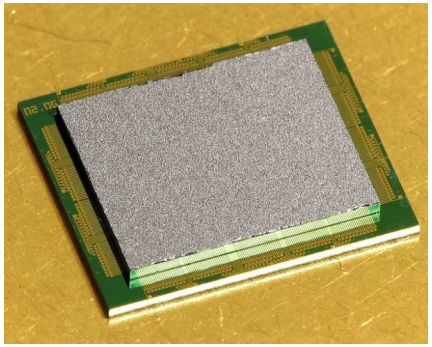
- +/- 1 micron xyz accuracy, excellent planarity
- 400x imaging, alignments at >450C
- thermocompression bonding up to 100 kg
- flip-chip, die attach, UV-curing, fiber alignment, replication
- “dry flux” vapor removes oxides to improve bonds

FPA Integration Process Overview 2

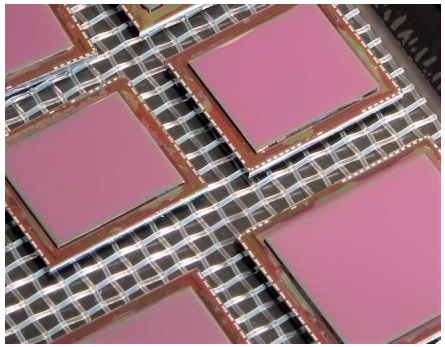
- **Post flip-chip processes**
  - epoxy underfill
  - backside grinding & polishing
  - precision optical coatings
  - packaging
  - cryo testing



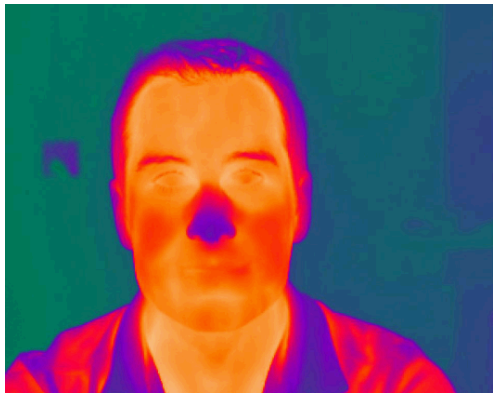
FPA packaged for cryo testing



full thickness hybridized chips

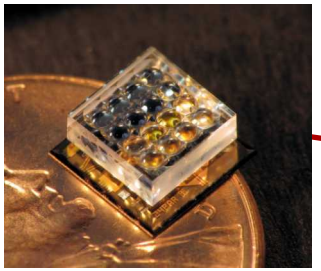


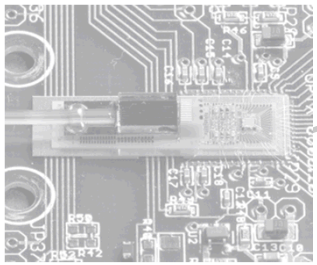
FPAs after thinning and AR coat



MWIR imaging with nBn sensor

Outline





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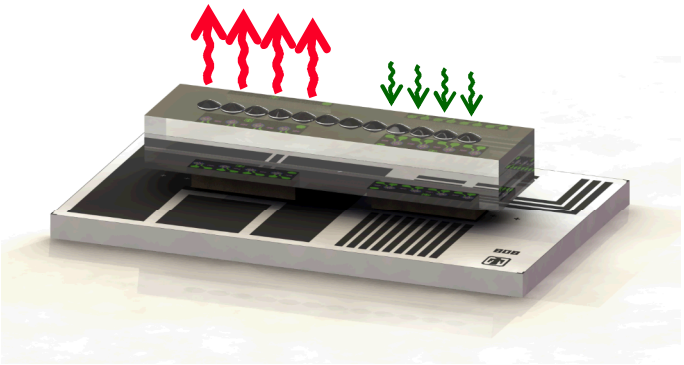
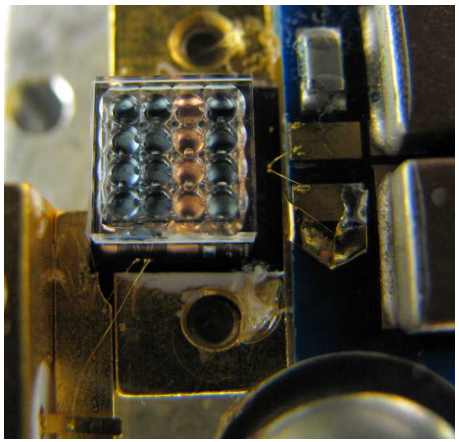
Outlook and Summary

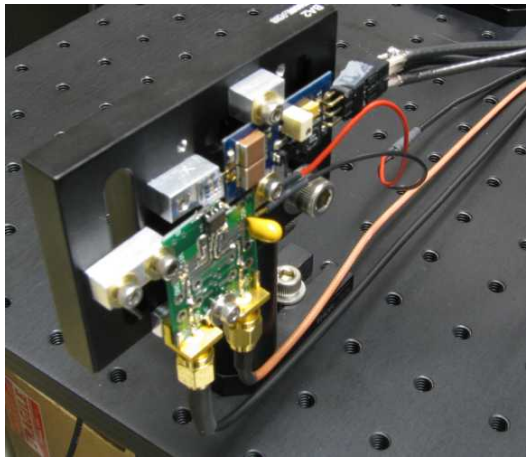
Microscale Optical Sensors

- **Robust photonic proximity fuzes employ flip-chip optoelectronics and micro-optics**
  - **very compact, g-hard; high sensitivity; narrow FOV; immunity to RF jamming**
  - **requires high-power VCSELs; fast photodiodes at 980nm; micro-optics**
  - **flip-chip integration of optoelectronics on AlN or diamond heat spreaders**

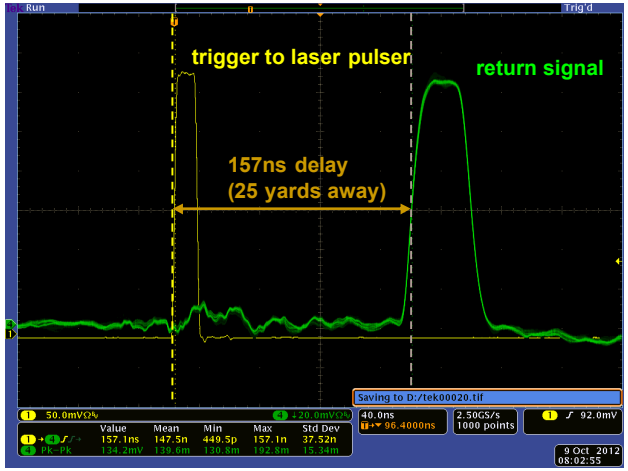




time-of-flight optical range sensor



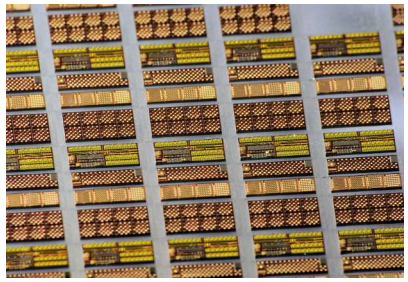
microfuze with support electronics



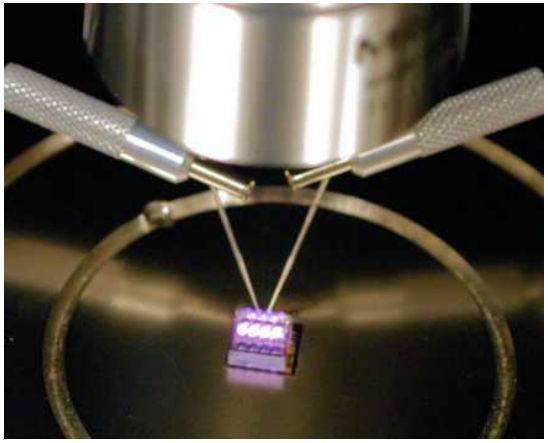
photonic fuzing demo with micro-optics and VCSEL transmitter array

Optical Microsystem Integration

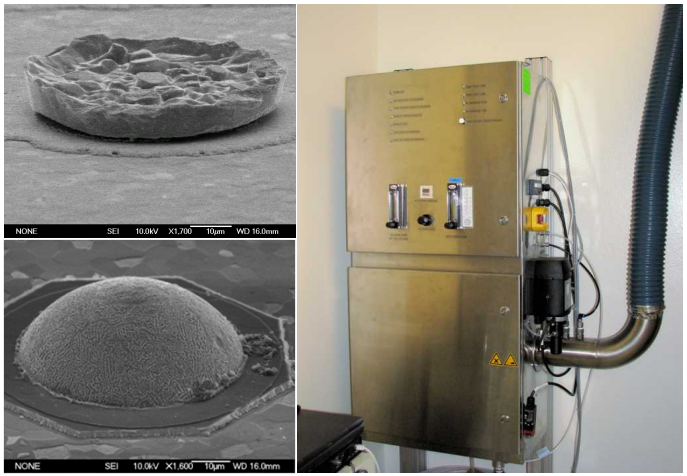
- **Processes combined into photonics fabrication**
  - solder dam, underbump metallization, solder bump
  - thinning and AR coatings
  - singulation (scribe and break)
  - flip-chip attach
- **Micro-optics fab & align**
  - diamond turning
  - molding in optical plastics
  - active alignment
  - UV epoxy attach



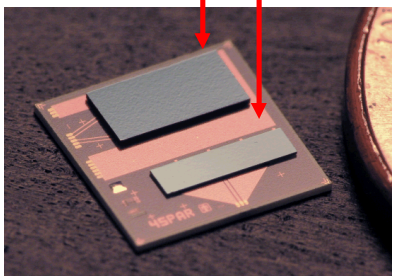
photodiode and VCSEL arrays



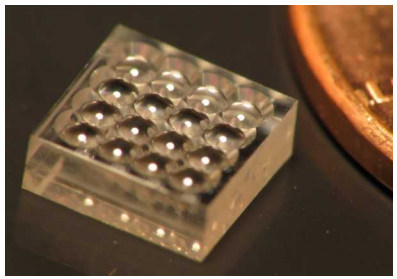
integrated component testing



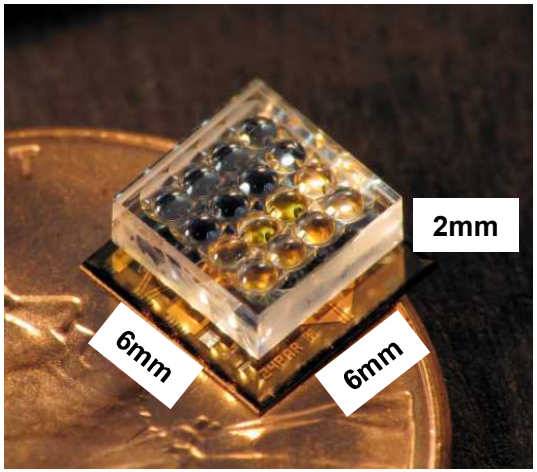
indium solder reflow for thermal transfer



populated fuse submount

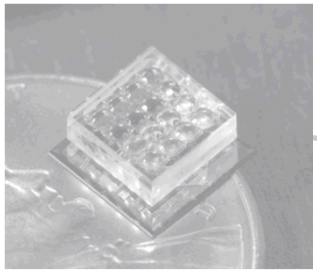


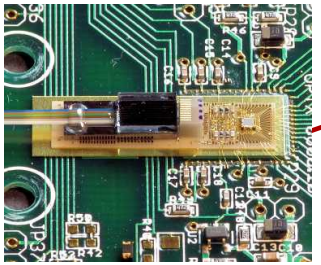
microlens array



high-power optical proximity sensor

Outline





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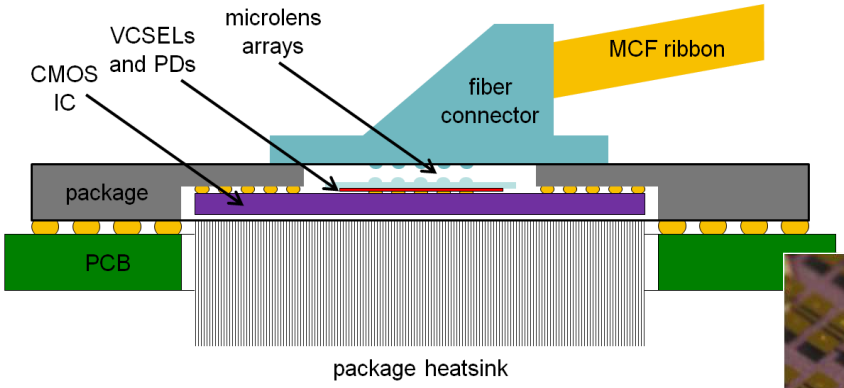
  - 32-nm CMOS, dense VCSEL & photodiodes, micro-optics, multi-core fibers
- pathfinder technologies
  - microsystem-enabled photovoltaics
  - III-V/CMOS microelectronics
  - high-performance & extreme environment applications

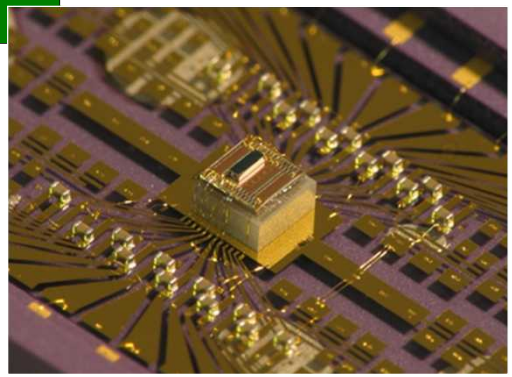
Outlook and Summary

Optical Interconnects for High Performance Computing

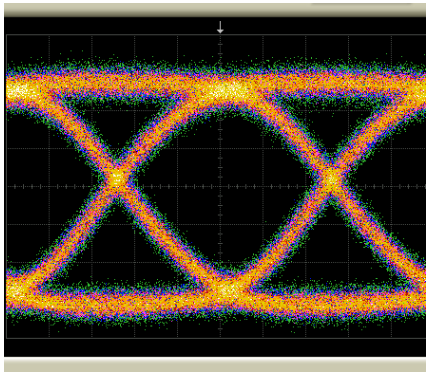
- **Dense integration of photonics and CMOS for advanced interconnect technologies**
  - **hybrid integration for very high density and low electrical parasitics**
  - **targets <1 pJ/bit and >1 Tbps/mm^2**
- **Development of circuits, photonics, optics and integration techniques**
  - **transmit/receive circuits in 32-nm and 45-nm CMOS (TAPO)**
  - **combines VCSEL and photodiode arrays, micro-optics, custom fiber**

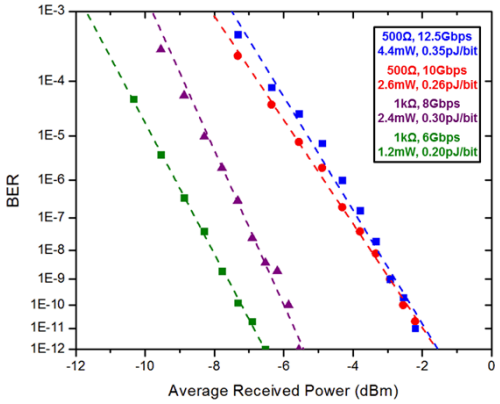


multichannel interconnect concept



packaged CMOS/VCSEL assembly

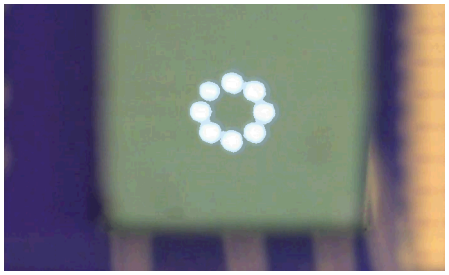


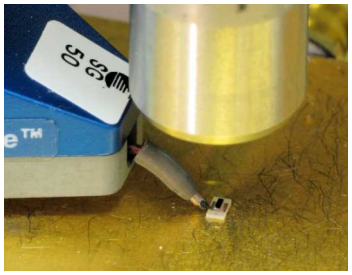


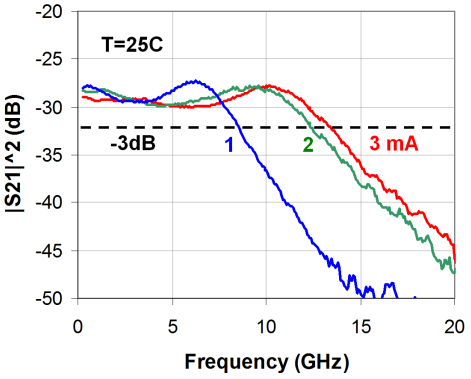
system link testing

Interconnect Components

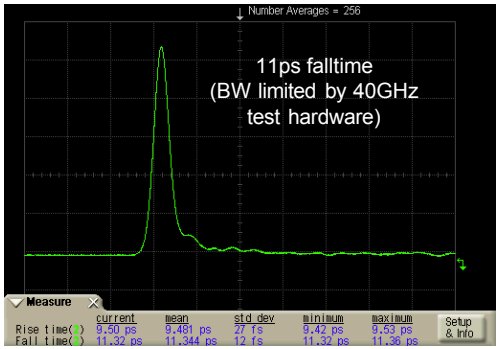
- development of high-density optoelectronics arrays
  - low-power VCSELs designed for high BW at low drive current
  - photodiodes >40Gb/s with very low capacitance through flip-chip integration
- Micro-optics designed for coupling to multicore fibers
  - custom micro-optics developed for multicore fiber links



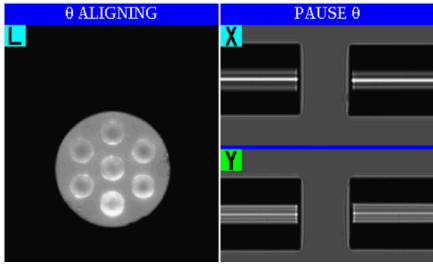


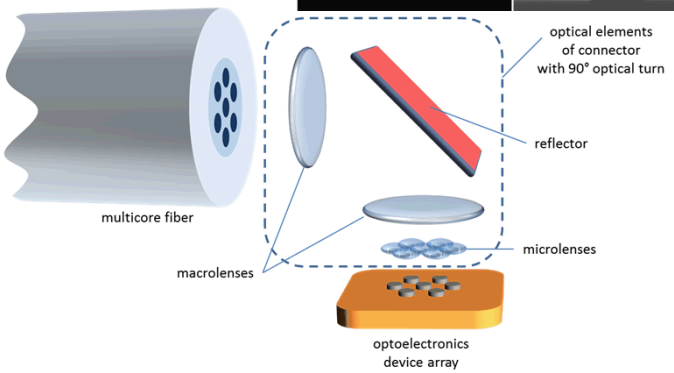


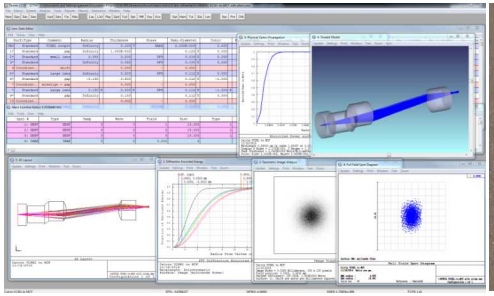
VCSEL performance

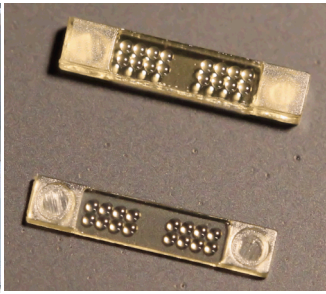


InGaAs photodiode performance





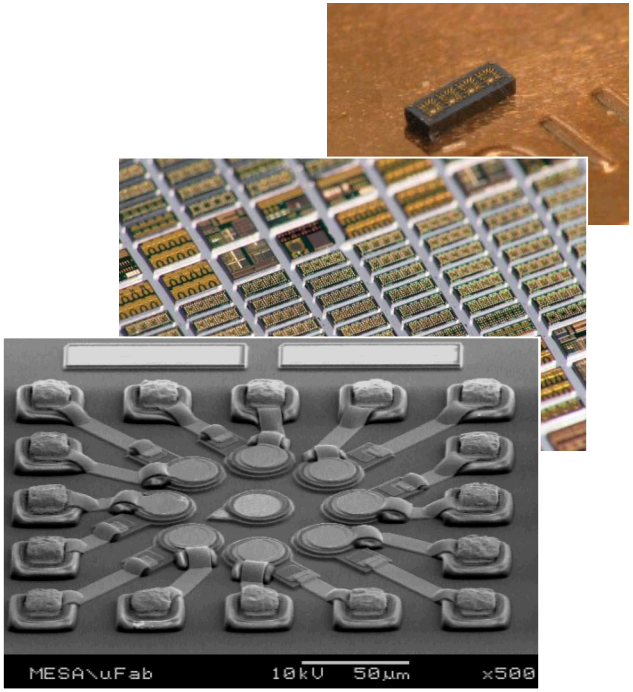




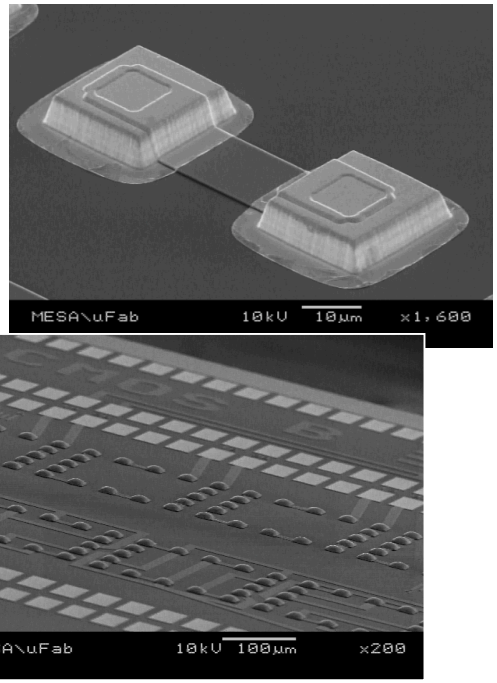
micro-optics and multicore fibers

Interconnect Heterogeneous Integration

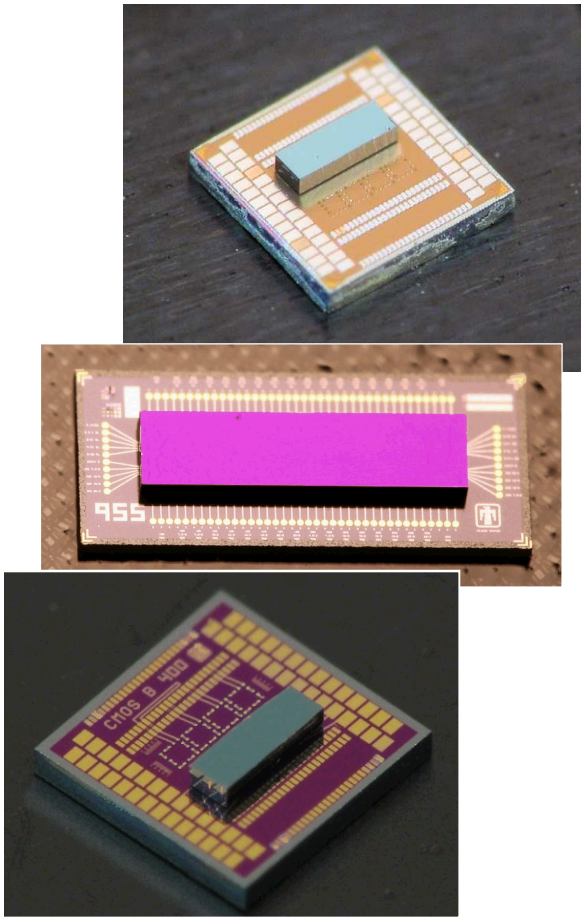
- **III-V processes combined into photonics fabrication**
  - **AuSn bumps, 100µm substrate thinning, AR coating, scribe and break**
- **CMOS processed in die form**
  - **plated underbump and bumps**
- **Flip-chip integration**



VCSEL and PD arrays
on GaAs and InP



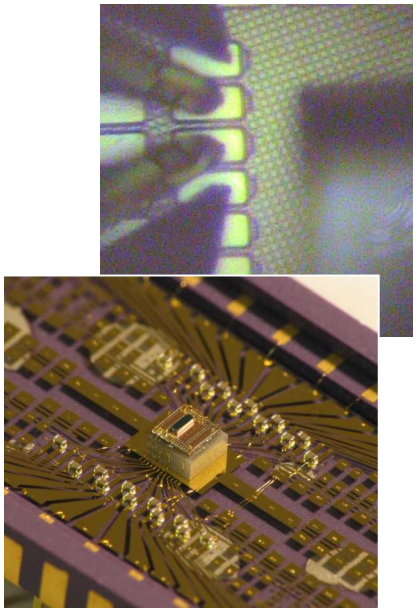
CMOS IC prior to flip-chip
50µm bump pitch (AuSn, SAC…)



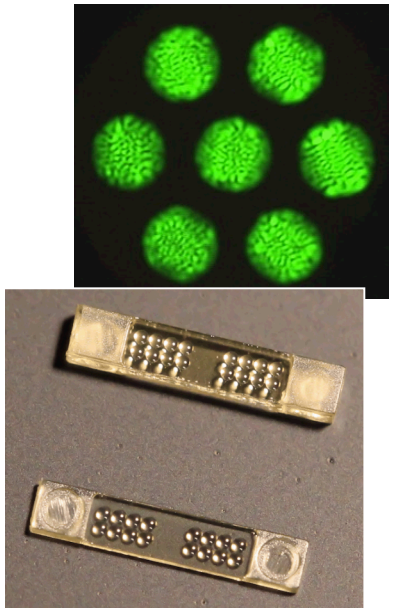
CMOS IC with III-V optoelectronics

Interconnect Testing

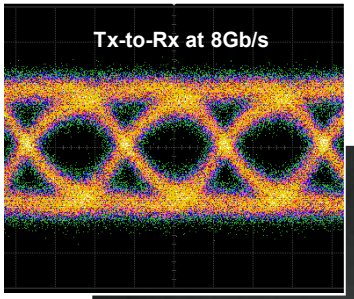
- **Hybridized parts packaged for high-speed opto-electronic testing**
  - **DC wirebonding, RF probing**
  - **active fiber alignment**
- **Single channel links demonstrated using 45-nm CMOS**
  - **10Gbps at 1.7 pJ/bit**
- **Ongoing characterization of new link and components**
  - **test & attach multicore fiber, micro-optics, and 32-nm IC**

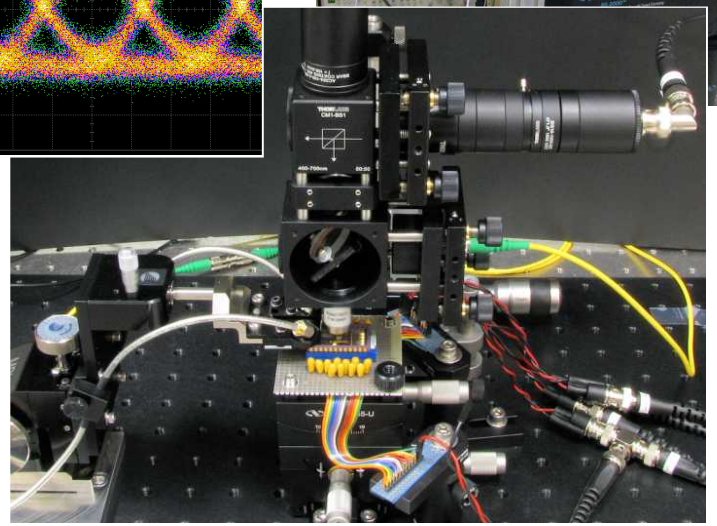


packaged CMOS/III-V photonics



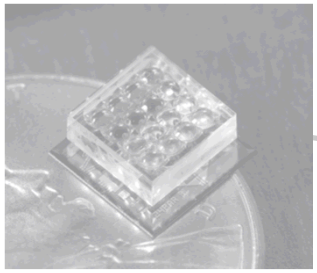
multicore fiber and molded microlens arrays

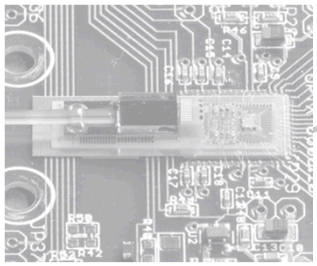


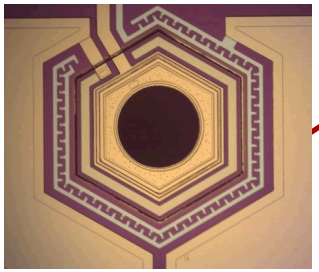


system link testing

Outline







Overview of Si/III-V heterogeneous integration

- rationale and methods

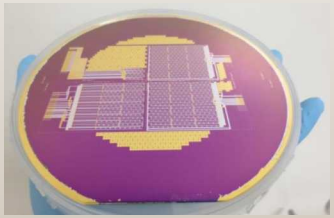
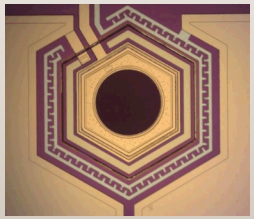
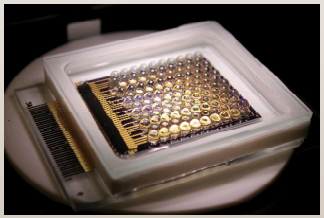
Selected photonics programs leveraging integration

- imaging sensor development
  - nBn detector arrays based on GaSb
  - indium-based flip-chip to silicon ROICs
- optical microsensor prototyping
  - photonic proximity fuzing
  - high-power lasers, detectors, micro-optics
- low-power data communications R&D
  - high-performance computing & cryogenic satellite applications
  - 32-nm CMOS, dense VCSEL & photodiodes, micro-optics, multi-core fibers
- pathfinder technologies
  - microsystem-enabled photovoltaics
  - III-V/CMOS microelectronics
  - high-performance & extreme environment applications

Outlook and Summary

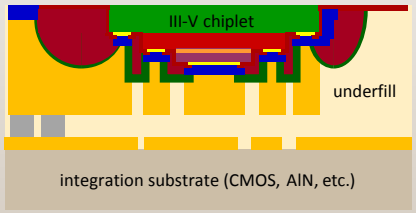
Pathfinder Technologies

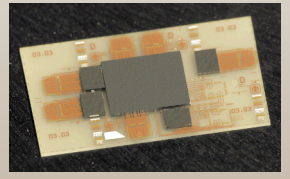
Microsystem-Enabled Photovoltaics

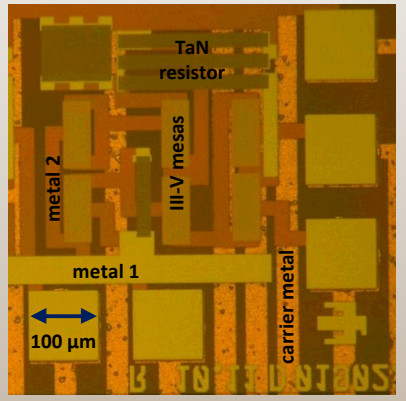




- wafer-level oxide bonding for multi-junction solar cells
- InGaAsP/InP and InGaP/GaAs devices on silicon
- dielectric interfaces with III-V substrate removal
- integration with collection optics

Heterogeneous III-V/CMOS Microelectronics

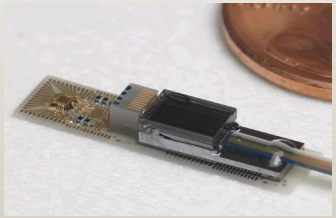
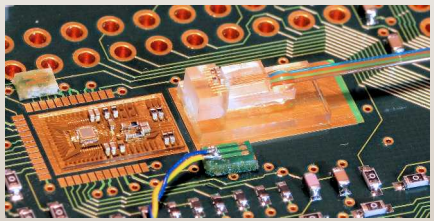
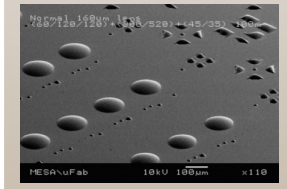
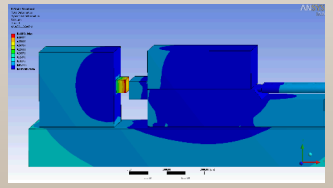
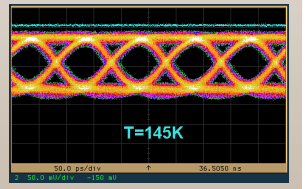






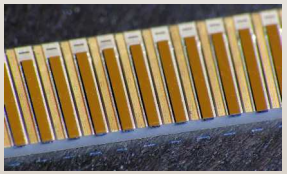
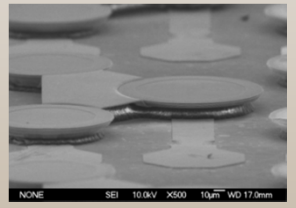
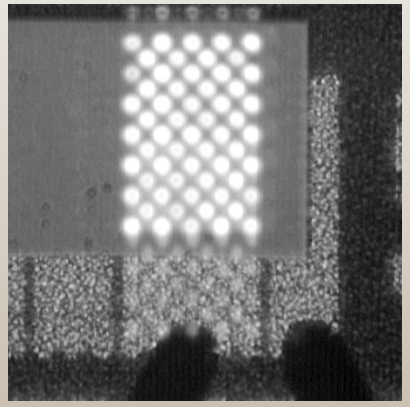
- complementary integration of GaAs and InP microelectronics
- III-V microelectronics circuitry on CMOS ASICs

Extreme Environment Applications

- custom photonics, optics, electronics for cryogenic interconnects
- advanced optoelectronics and integration for radiation hardness

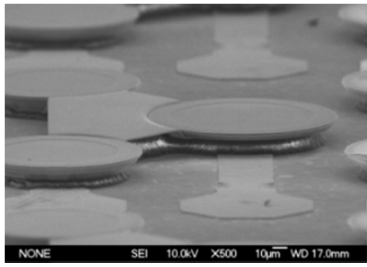
High Performance Photonics

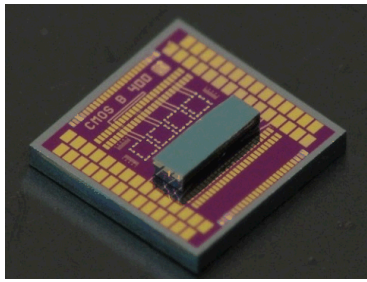




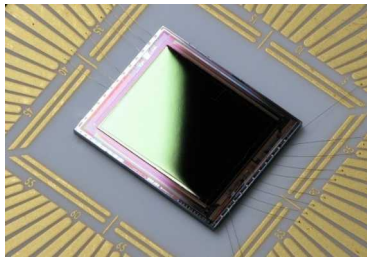
- high-power edge & surface emitters on AlN and diamond
- RF packaging for high-speed test and measurement

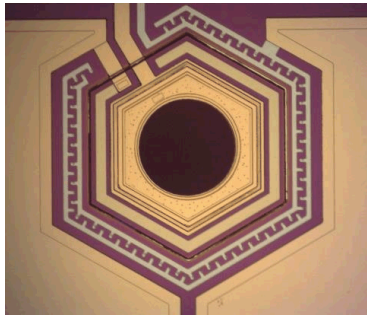
Summary

- **Heterogeneous integration of III-V photonics**
  - provides high performance and more-than-Moore functionality
  - "best" approach depends on the application
    - package and wirebond, flip-chip, wafer-scale oxide bonding, DBI, …
- **Optical microsystem integration**
  - leveraging extensive III-V capabilities
  - trusted microelectronics design/fabrication
  - heterogeneous integration as part of the fabrication process
- **Numerous applications at Sandia**
  - advanced FPAs (infrared/vis/UV/x-ray)
  - microscale optical sensors
  - optical communications for HPC and satellites
  - high power lasers
  - telecommunications
  - photovoltaics









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  Jin Kim
  Jeffrey Cederberg
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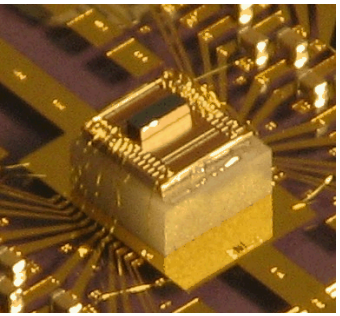
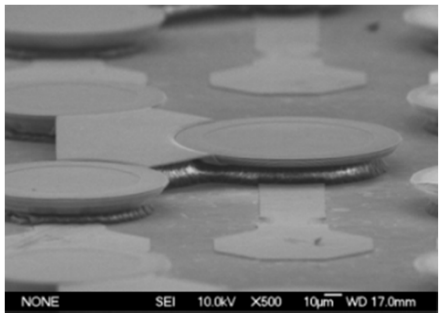
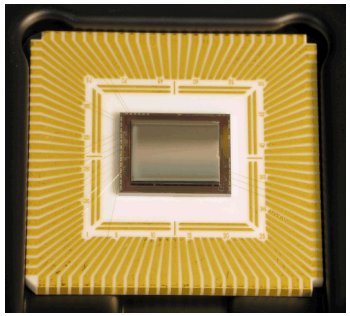
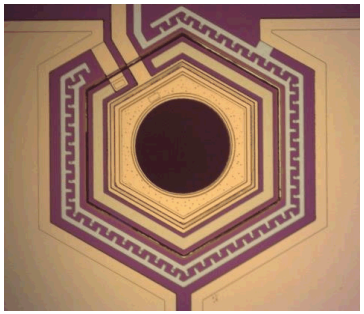
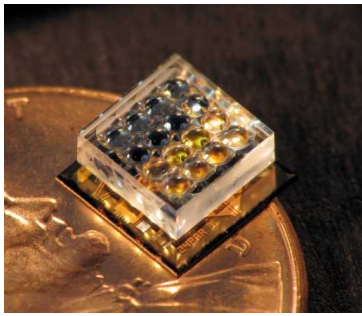
Exceptional service in the national interest

Sandia National Laboratories

Heterogeneous Integration of III-V Photonics and Silicon Electronics for Advanced Optical Microsystems

Gordon A. Keeler, Kent M. Geib, Darwin K. Serkland, Gregory M. Peake, Mark E. Overberg, Jeffrey G. Cederberg, Thomas M. Gurrieri, Jin K. Kim, and Charles T. Sullivan

Additional Slides

U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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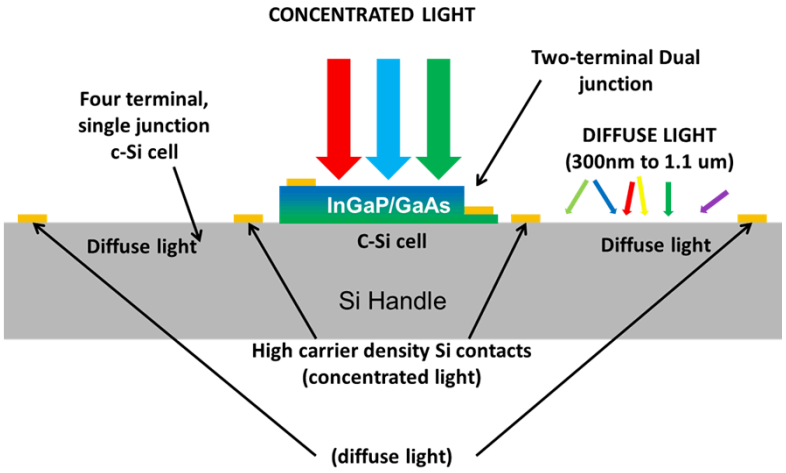
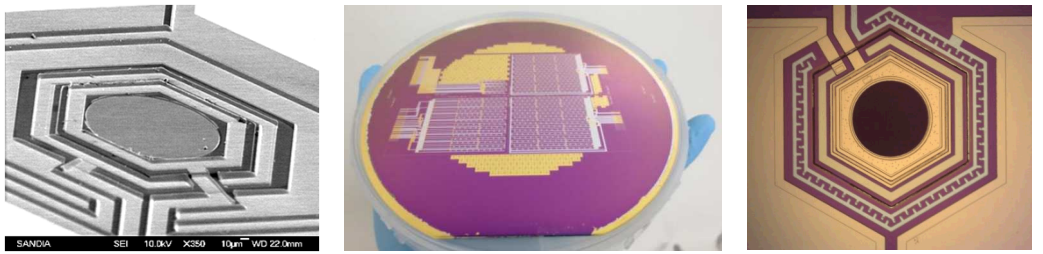
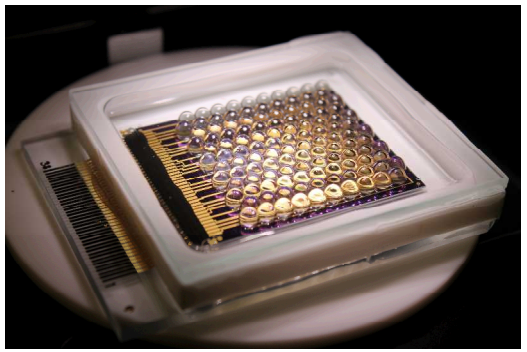
Microsystem-Enabled Photovoltaics (MEPV)

- **Wafer-level bonding for microscale multi-junction solar cells**
  - **InGaAsP/InP and InGaP/GaAs devices on silicon**
- **Dielectric interfaces with III-V substrate removal**
  - **re-use of substrates to reduce ultimate cost**
- **Photonic microsystem prototyping**
  - **integration with collection optics**





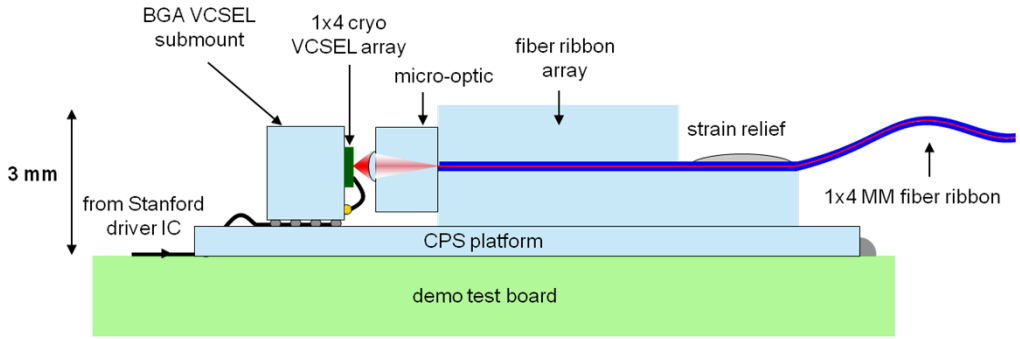
wafer-level integration of III-V and silicon cells

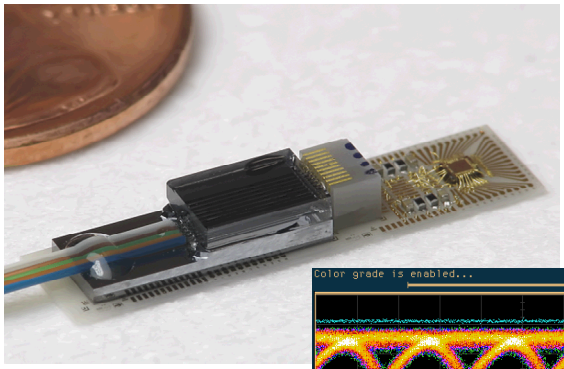


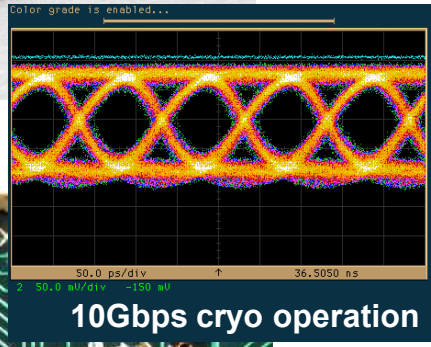
MEPV packaged module

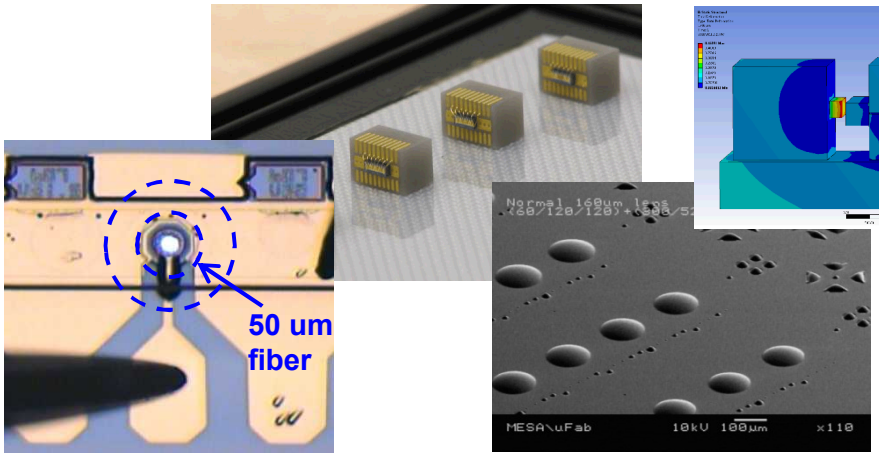
Cryogenic Optical Transceivers

- **Integration of custom low-power cryogenic VCSELs, custom CMOS driver IC, passives, microlenses, and optical fiber array for satellite communications**

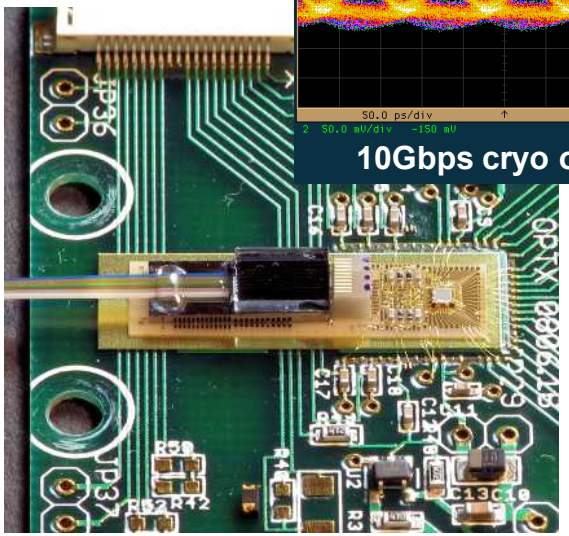








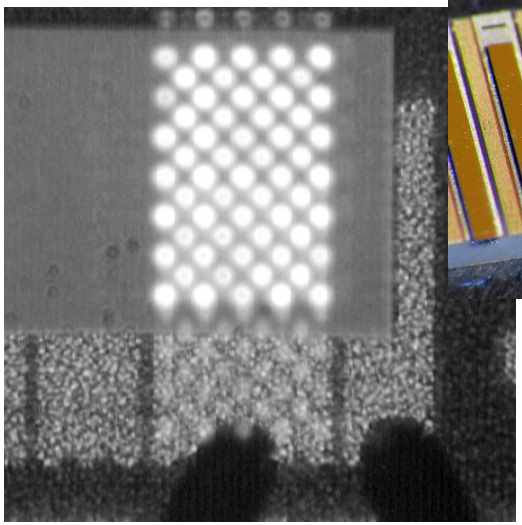
microfabrication, modeling, and assembly of transceiver elements



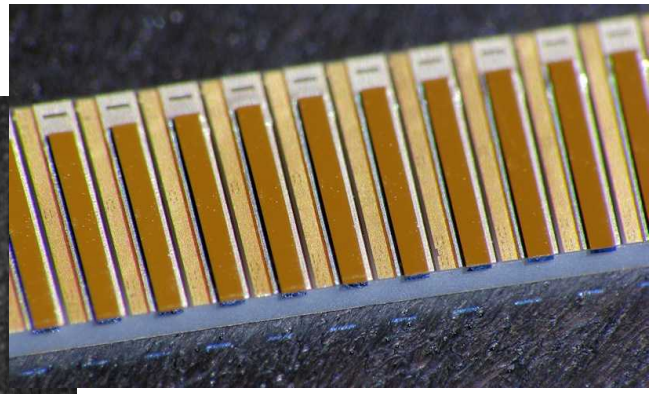
prototype assembled for cryo testing with FPA

High-Power Laser Arrays

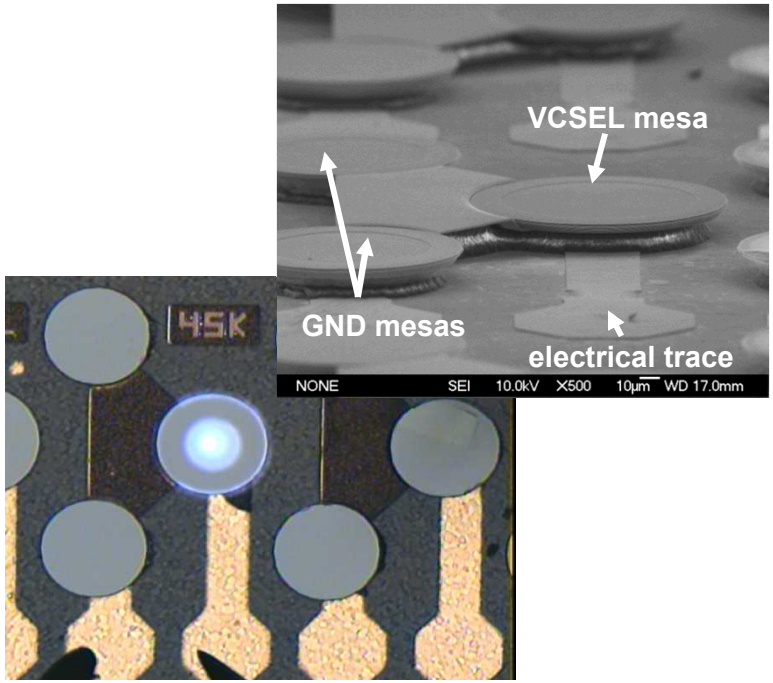
- **Multiple programs have require custom high-power laser arrays**
  - **integration enables high density & efficient coupling to AlN heatsinks**
- **Various approaches exploited**
  - **serial attachment of discrete devices with AuSn solder**
  - **high-density 980nm VCSEL arrays with In solder**
  - **850nm VECSELs with substrate removal for reduced optical absorption**



10W VCSEL array



high-power laser bars on heatsink



high-power 850nm VCSELs on AlN