Total Ionizing Dose Effects on Strained Ge pMOS FinFETs on Bulk Si

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***Abstract*— We have characterized the total ionizing dose response of strained Ge *p*MOS FinFETs built on bulk Si using a fin replacement process. Devices irradiated to 1.0 Mrad(SiO_2) show minimal transconductance degradation (less than 5%), very small V_{th} shifts (less than 40 mV in magnitude) and very little ON/OFF current ratio degradation (<5%), and only modest variation in radiation response with transistor geometry (typically less than normal part-to-part variation). Both before and after irradiation, the performance of these strained Ge *p*MOS FinFETs is far superior to that of past generations of planar Ge *p*MOS devices. These improved properties result from significant improvements in processing technology, as well as the enhanced gate control provided by the strained Ge FinFET technology.**

***Index Terms*— 10 keV X-ray, geometry dependence, germanium FinFETs, total ionizing dose.**

I. Introduction

GERMANIUM-based *p*MOS FinFETs integrate material and structural advantages to optimize several key device operating properties that support their use in sub-14 nm CMOS technologies. Benefits over Si *p*MOS FinFETs include higher hole mobility, reduced short-channel effects, and reduced bias-temperature instabilities, while maintaining compatibility with conventional Si integration processes [1]–[3]. The radiation responses of planar Ge *p*MOSFETs [4]–[7] and SiGe FinFETs [8] have previously been evaluated. For Ge planar *p*MOSFETs, relatively low ON/OFF ratios were observed [4]–[7], and device response was sensitive to process conditions, e.g., the thickness of the Si capping layer that separated the Ge and dielectric layers, and/or halo implantation [5]. For SiGe FinFETs, a combination of bias-stress and radiation-induced charge trapping effects was observed [8]. As a result, these earlier-generation planar Ge *p*MOS transistors and SiGe *p*MOS FinFETs were not suitable for use in high-volume commercial or space environments.

As processing technologies have improved, knowledge from previous studies has been employed to continually improve the performance and reliability of Ge-based technologies. In this work, we provide a detailed evaluation of the radiation response of strained Ge *p*MOS FinFETs with different geometries under different bias conditions. We find that ON/OFF ratios are improved significantly before and after irradiation, compared to planar Ge *p*MOSFETs, and that charge trapping effects due to both bias-stress and irradiation are reduced in these Ge FinFETs, compared with SiGe FinFETs evaluated in 2014 [8]. These results indicate that strained Ge *p*MOS FinFETs are excellent candidates for integration into next-generation radiation-tolerant CMOS IC technologies.

II. Experimental Details

The Ge *p*MOS FinFETs evaluated in this work were fabricated at imec on 300 mm bulk Si (100) wafers. Transistor fabrication included a fin replacement process in which the original Si fin is replaced by a partially relaxed $Si_{0.25}Ge_{0.75}$ layer and Ge channel in a single step [1], [9]. For these devices, a thin Si cap was partially oxidized, yielding an unconsumed thin Si buffer layer to passivate the Ge surface and improve the interface quality. On top of the SiO_2 interfacial layer (IL), a ~1.5 nm HfO_2 layer and TiN metal gate were deposited. The effective oxide thickness (EOT) of the gate dielectric stack is ~1.9 nm. Because these are test structures intended to characterize the initial response of a developing process technology, the starting threshold voltage value was not optimized.

Fig. 1(a) shows a schematic diagram of the targeted-undoped, strained Ge Fin on $Si_{0.3}Ge_{0.7}$ strain-relaxed buffer built on 45 nm pitch spacer-defined Si fins on a (100)

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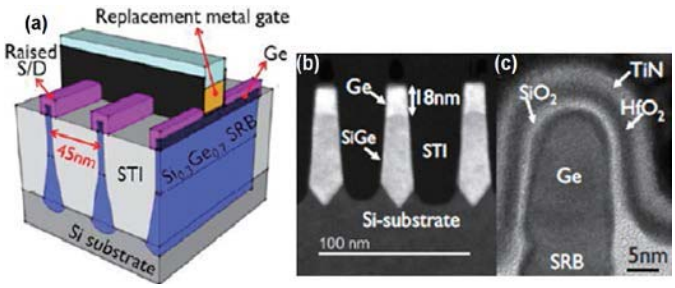

Fig. 1. (a) Schematic diagram of the targeted-undoped, strained Ge fin on $Si_{0.3}Ge_{0.7}$ strain-relaxed buffer, built on 45 nm pitch spacer-defined Si fins on a (100) Si substrate, (b) HAADF XTEM after replacement channel deposition, and (c) zoom into Ge channel at the end of processing. The final Ge fin is 13 nm wide and 18 nm tall.

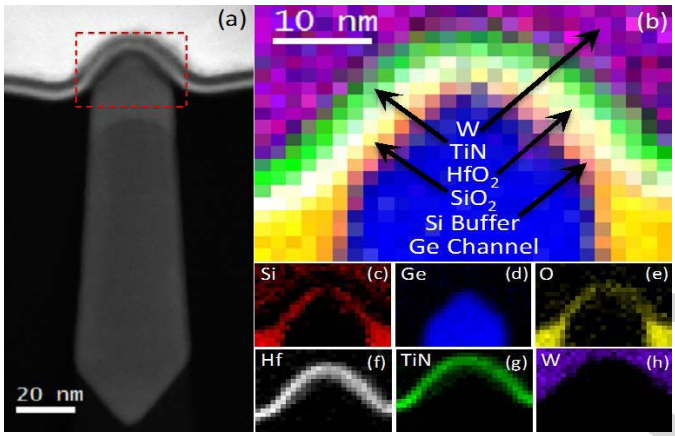

Fig. 2. (a) STEM image of bulk Ge FinFET. (b) Chemical composition map of different structure layers from EELS. (c)-(h) Individual maps of elements/compounds found in device.

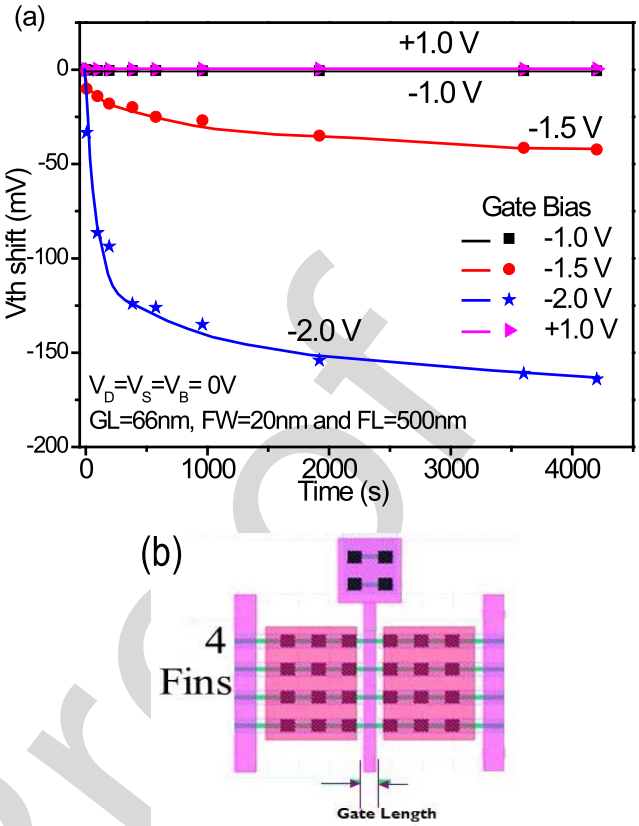

Fig. 3. (a) Threshold voltage shifts as functions of time and gate bias for Ge pMOS FinFETs. A schematic illustration of the test structures is shown in (b). The devices include 4 fins in parallel. All dimensions are as-designed. The printed value after trimming the "66 nm" gate is around 36 nm, for example.

Si substrate; Fig. 1(b) shows a high-angle annular dark field (HAADF) cross-sectional transmission-electron-microscopy XTEM image after replacement channel deposition; and Fig. 1(c) shows a zoomed image of the Ge channel at the end of processing. These images show that the final Ge fin is 13 nm wide and 18 nm tall [9]. A scanning transmission electron microscope (STEM) image of the FinFET is shown in Fig. 2(a). To ascertain the chemical composition of the different layers in the STEM image, electron energy loss spectroscopy (EELS) is used to form spectral images of the elements in the device. A composite drawing showing the chemical composition of different layers is shown in Fig. 2(b), along with maps of the Si, Ge, O, Hf, TiN, and W (Figs. 2c–2h). The underlying strained Ge layer, Si cap (to enhance interface quality), thin SiO_2/HfO_2 gate dielectric, and TiN/W gate metallization are all clearly delineated.

Total ionizing dose (TID) irradiations were performed using a 10-keV ARACOR X-ray source at room temperature at a rate of 31.5 krad(SiO_2)/min. Three gate bias conditions ($V_G = -1$ V, $+1$ V, and all pins grounded) were applied during irradiation and/or bias stress. A semiconductor parameter analyzer, HP4156A, was used to supply DC bias during the experiment, as well as to perform the I-V characterization before and after each exposure. The dimensions of the tested devices vary in fin width from 16 nm to 100 nm, fin length from 500 nm to 12.5 μm, and gate length from 66 nm to 230 nm. The fin length (see Fig. 3) was varied as part of the process evaluation matrix, but the channels of individual transistors are defined by the gate length, fin width, and fin height, as shown in Fig. 1. At least three devices with the same dimensions were tested for each set of test results shown. Results of average devices are shown below, with error bars indicating the range of responses.

III. Results and Analysis

Fig. 3 shows (a) the threshold voltage V_{th} shift as a function of applied gate bias and stress time for devices with a gate length of 66 nm and fin width of 20 nm, and (b) a schematic illustration of the 4-fin test devices evaluated in this study. There are significant V_{th} shifts for negative gate biases of -2 V and -1.5 V, which are comparable to those observed previously for SiGe FinFETs [8]. However, these voltages are well beyond the expected operating limits of this technology. At room temperature and ± 1 V bias (approximately double the expected operating voltage of this technology), there is no detectable shift in V_{th} or significant increase in leakage current for any of the strained Ge pMOS FinFETs tested under voltage stress, for the times and biases of this study. These results demonstrate the relative stability of devices during irradiation under the bias conditions of this study. Moreover, these results

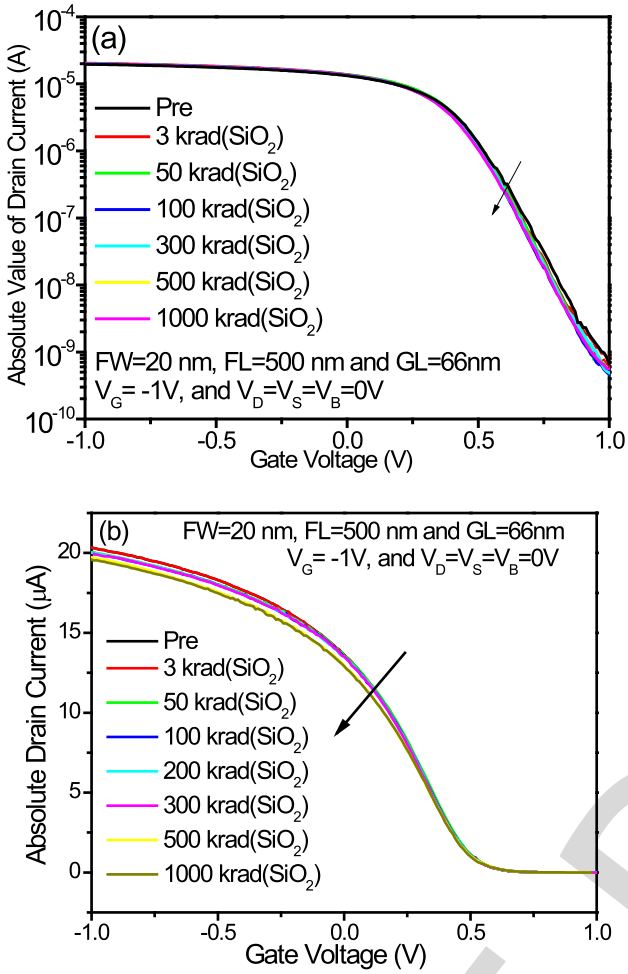

Fig. 4. I_D-V_G curves as functions of dose for a device with gate length of 66 nm, fin width of 20 nm, and fin length of 500 nm: (a) semi-log plot and (b) linear plot. $V_D = -0.1$ V during all I_D-V_G sweeps.

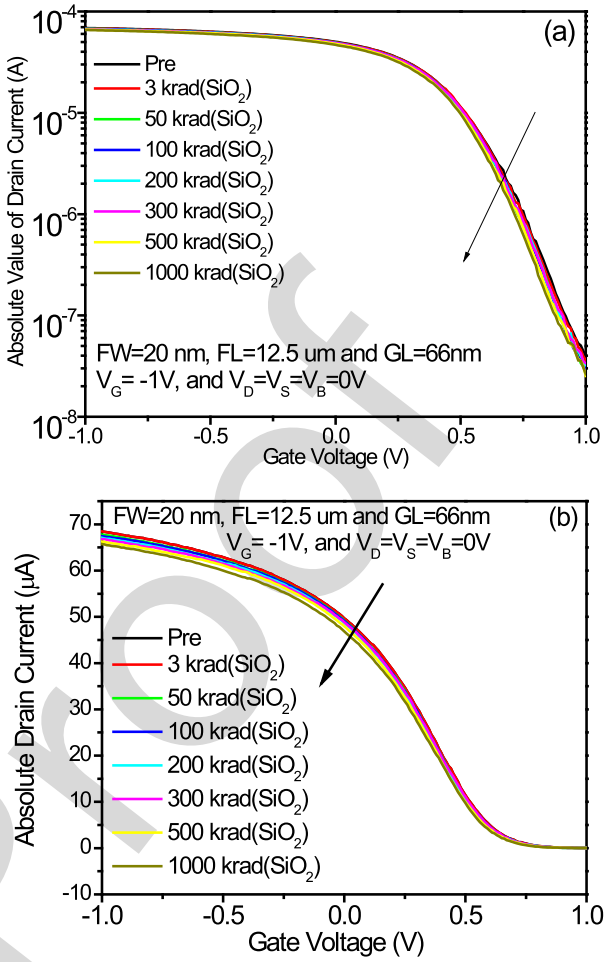

Fig. 5. I_D-V_G curves as functions of dose for a device with gate length of 66 nm, fin width of 20 nm, and fin length of 500 nm: (a) semi-log plot and (b) linear plot. $V_D = -0.1$ V during all I_D-V_G sweeps.

contrast with the responses of SiGe *p*MOS FinFETs in [8], for which shifts due to bias-induced charging during irradiation complicated the extraction of the "pure" TID response [8].

Figs. 4 and 5 show the I_D-V_G characteristics for TID tests on devices with gate length of 66 nm, fin width of 20 nm, and fin lengths of 500 nm and 12500 nm, respectively. In each case, the active transistor gate is much shorter than the lithographically defined fin, as shown in Fig. 3(b). Each device shows a small, negative V_{th} shift with increasing TID, consistent with a small amount of net hole trapping in the gate dielectric layers. Less than ~5% ON state current degradation is observed for either device. From these curves, the extrapolated V_{th} and $G_m = \Delta I_D/\Delta V_G$ were extracted using standard techniques in the linear mode of device operation, with $V_D = -0.1$ V. No adjustment to the gate-metal work function was performed to optimize the starting value of threshold voltage for these devices, so the OFF state current for these test structures is taken to be the current measured at $V_G = 1$ V. With this definition, the ON/OFF current ratio for the 500 nm fin length device in Fig. 4(a) is more than 10^5, which is comparable to that of the strained SiGe FinFETs in [8], and significantly higher than the ratios observed for (relaxed) planar Ge *p*MOS devices in [4]–[7]. The increased ON/OFF current ratios for these FinFETs are due to improvements in starting material quality as well as the improved gate control achievable in FinFETs, as compared to planar Ge devices, as we discuss below.

Fig. 6 shows threshold voltage shifts, changes in normalized transconductance, and measured ON/OFF current ratios as functions of irradiation and annealing time for devices irradiated at gate biases of ±1 V and 0 V, and annealed under negative bias. The largest V_{th} shifts occur for negative gate bias during irradiation, and correspond to net hole trapping in the gate dielectric layers during irradiation. Under positive irradiation bias, V_{th} shifts are small and positive, consistent with net radiation-induced electron trapping in the HfO_2 dielectric layer, as commonly observed [8], [10], [11]. TID-induced shifts are smaller in these strained Ge *p*MOS FinFETs than the SiGe FinFETs in [8], most likely because of the reduced gate bias used in this study, which is closer to anticipated device operating conditions, and/or lower defect densities in the dielectric layers of these devices. V_{th} shifts decrease or remain approximately constant during room-temperature, negative-bias annealing. The stability of

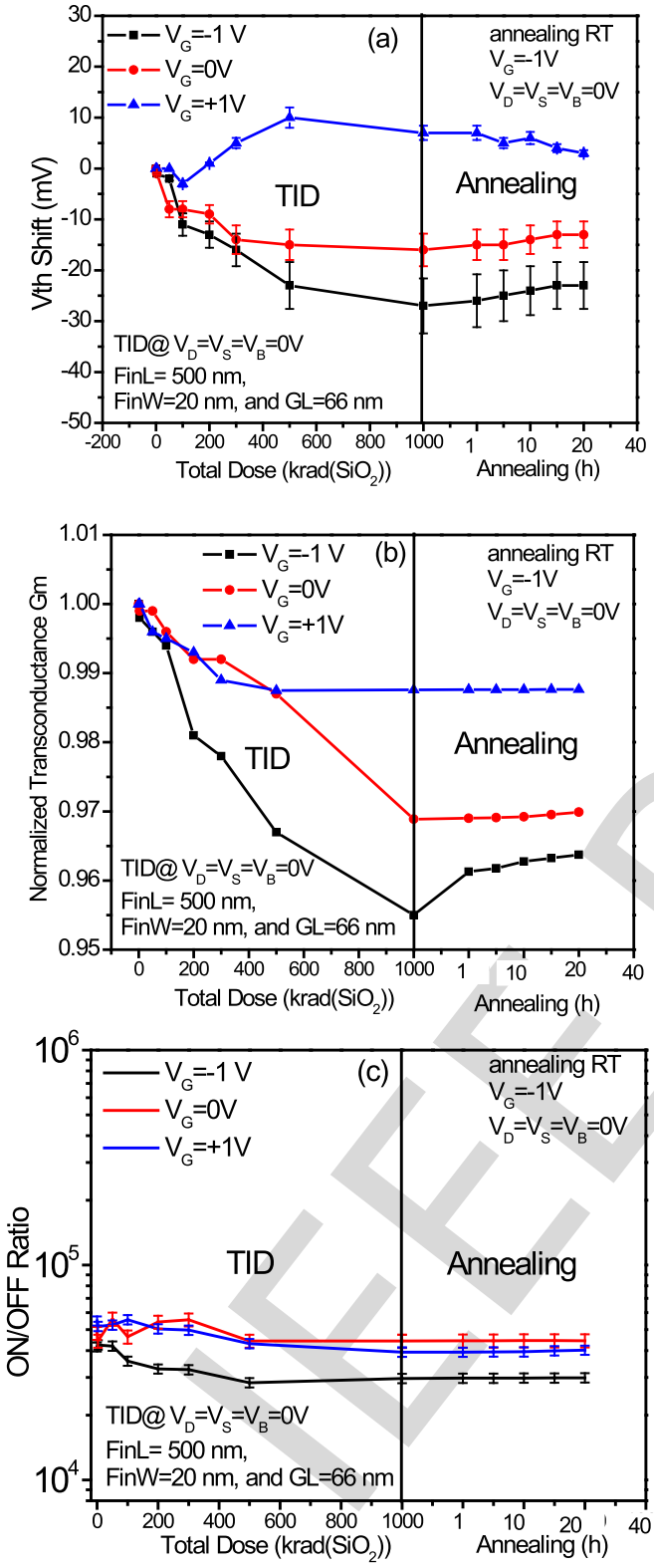

Fig. 6. (a) Threshold voltage shift, (b) normalized transconductance, and (c) ON/OFF current ratio as functions of total dose for gate biases $V_G = -1$ V, 0 V, and +1 V, and/or room temperature annealing time at $V_G = -1$ V, for devices with gate length of 66 nm, fin width of 20 nm, and fin length of 500 nm. Data points here are averages from at least three devices, and error bars show the full range of variation observed.

the devices during annealing further demonstrates that bias-induced charging is negligible during these irradiation and annealing tests. The transconductance G_m degradation (<5%),

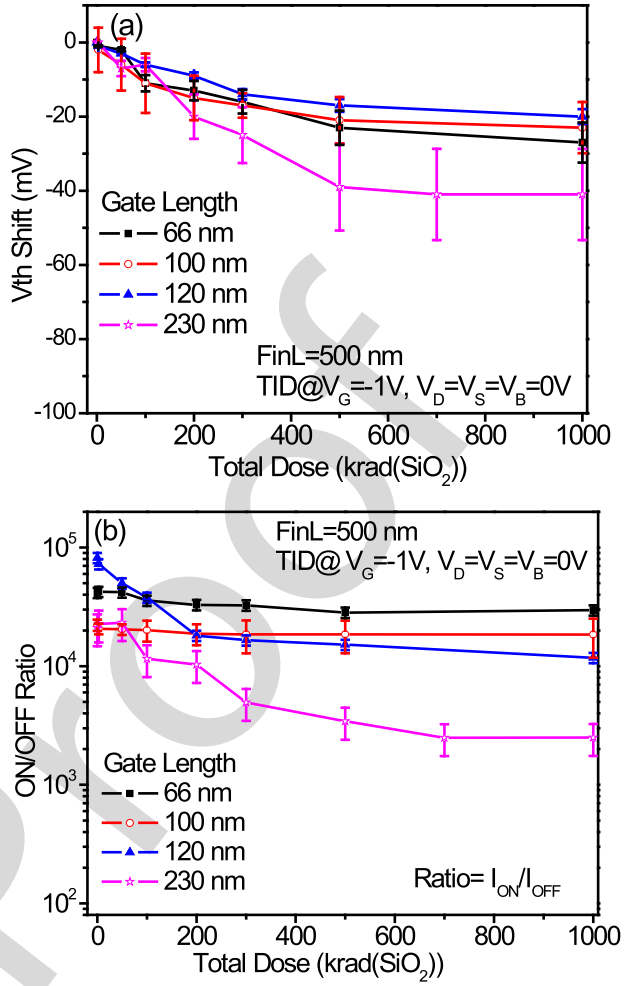

Fig. 7. (a) Threshold voltage shifts and (b) ON/OFF current ratios as functions of total dose and gate length for devices with fin width of 20 nm and fin length of 500 nm at a gate bias during irradiation of $V_G = -1$ V, and $V_D = V_S = V_B = 0$ V. Data points here are averages from at least three devices, and error bars show the full range of variation observed.

V_{th} shifts (<30 mV) and ON/OFF current ratio degradation (<5%) in these strained Ge pMOS FinFETs are far superior to the responses of relaxed, planar Ge pMOS devices in [4]–[7], again as a result of significant improvements in processing technology [1]–[3] and improved gate control.

Fig. 7 summarizes (a) V_{th} shifts and (b) ON/OFF current ratios as a function of TID for negative gate-bias irradiation of devices with fin width of 20 nm and gate lengths of 66 nm to 230 nm. All devices show V_{th} shifts smaller than 50 mV in magnitude. Devices with shorter gate lengths show smaller V_{th} shifts (-20 mV to -35 mV), increased ON/OFF ratios, and smaller variations in response compared to devices with 230 nm gate length. This likely occurs because shorter gate-length devices are less likely to be impacted by defects in the starting material, which can degrade junction and oxide quality before and after irradiation [5], [6]. That the ON/OFF current ratio before and after irradiation is greatest for shorter gate-length devices is encouraging, since the properties of smaller-dimension devices have more practical significance for future IC applications than properties of larger-dimension devices.

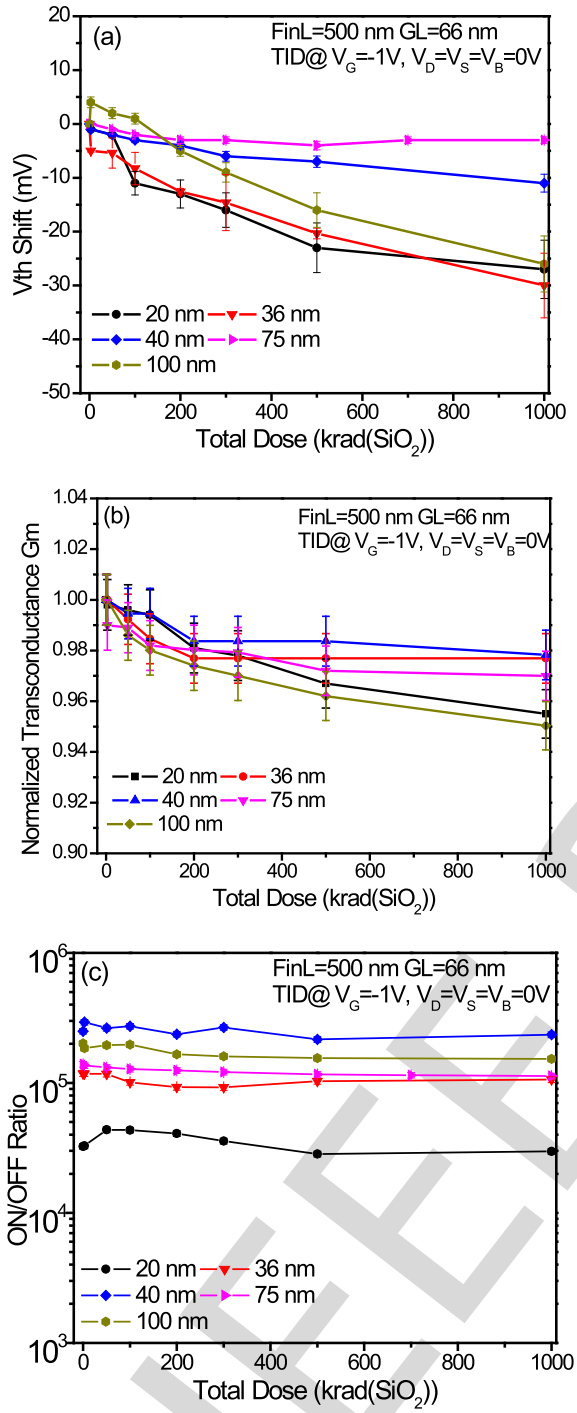

Fig. 8. (a) V_{th} shifts, (b) normalized transconductance, and (c) ON/OFF current ratios as functions of total dose for gate biases during irradiation of $V_G = -1$ V and $V_D = V_S = V_B = 0$ V for Ge pMOS FinFETs with gate length of 66 nm and fin widths of 20-100 nm. Data points here are averages from at least three devices, and error bars show the full range of variation observed.

We note that the results of Fig. 7 are the only case in our testing of these devices, to date, in which it appears that one geometrical split exhibits a statistically different response from other process splits, which should simplify IC design in this technology.

Fig. 8 shows (a) V_{th} shifts, (b) normalized transconductance, and (c) ON/OFF current ratios as functions of total dose for devices irradiated with $V_G = -1$ V and $V_D = V_S = V_B = 0$ V for Ge pMOS FinFETs with gate length of 66 nm and fin widths of 20- 100 nm. All devices show negative V_{th} shifts (-3 mV to -35 mV), decreases in transconductance (1 to 5%), and minimal changes in ON/OFF current ratio with increasing TID. No clear trends in radiation response are observed with varying fin width.

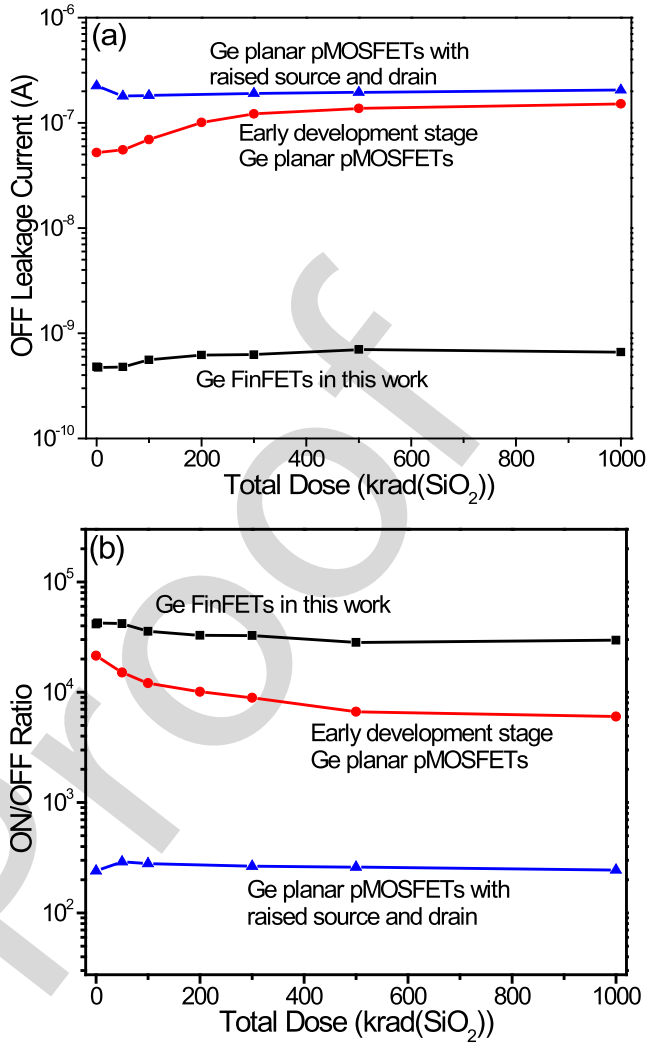

Fig. 9. (a) Leakage current, and (b) ON/OFF current ratios as functions of total dose with gate biases during irradiation of $V_G = -1$ V and $V_D = V_S = V_B = 0$ V for Ge pMOS transistors from three technology generations: 1) early development stage Ge planar pMOSFETs; 2) Ge planar pMOSFETs with raised source and drain; and 3) Ge pMOS FinFETs from this work.

IV. Discussion

The excellent radiation response of the strained Ge pMOS FinFETs and absence of fin-width dependence in this work contrasts strongly with previous results on earlier generation Si nMOS FinFETs on SOI wafers [12], [13], in which much larger V_{th} shifts and a strong fin width dependence were observed. These improvements in response for strained Ge pMOS FinFETs, relative to SOI FinFETs, result primarily from the absence of a buried oxide layer. In SOI devices, the buried oxide layer can strongly affect device response as a result of buried-oxide to top-gate electrostatic charge coupling

effects [12], [13], [20]–[22]. Instead, the relatively small V_{th} shifts in these bulk Ge pMOS FinFETs are due primarily to charge trapping in the gate dielectric (SiO_2/HfO_2) layers.

These strained Ge pMOS FinFETs also show far superior radiation response to recent-generation, bulk nMOS Si FinFETs, for which significant STI leakage is observed below $\sim$ 300 krad(SiO_2) [14]. This improvement in response is due primarily to three factors: (1) The thickness of the STI at the lower fin corner of the strained Ge pMOS FinFET (see Fig. 1(c)) is reduced in thickness, as compared with the STI of the bulk nMOS Si FinFETs in [14], leading to reduced STI charge trapping in the region closest to the active device channel [23]. (2) The QW structure effectively isolates conduction in the active device channel and associated parasitic structures from potential coupling effects that can be associated with charge trapping in the STI in some types of devices [24], [25]. (3) The nominally undoped Ge channel layer in these pMOS FinFETs has an effective n-type doping after processing, as a result of dopant diffusion out of the highly n-doped underlayer [9], [26]. Net positive trapped charge in the STI more strongly accumulates n-type surfaces [10], [23]. Consequently, no significant STI-related leakage is observed for these strained Ge pMOS FinFETs, up to at least 1 Mrad(SiO_2), under the conditions of this study.

The strained Ge pMOS FinFET structure illustrated in Figs. 1 and 2 also enables high performance transistors to be fabricated without the requirement for process steps that are necessary to include in planar Ge pMOS technologies. For example, the halo implant that is necessary in planar technology to control short channel effects [15] also leads to a radiation-induced reduction of ON/OFF ratio [5] and increase in low-frequency noise [6] for planar Ge pMOS technologies. With the enhanced gate control of FinFET technology, halo implantation is no longer required.

To illustrate the technology scaling trends in Ge pMOS technology, Fig. 9 compares (a) off-state drain leakage and (b) ON/OFF current ratios as functions of total dose for devices from three generations of imec Ge-based pMOSFETs built on silicon substrates: 1) early development stage Ge planar pMOSFETs with a Ge layer thickness of 2 μm and $W/L = 9.8$ μm/0.8 μm [6], [16]–[18]; 2) Ge planar pMOSFETs with Ge layer thickness of 200 nm, raised source and drain, and dimensions of $W/L = 1$ μm/0.47 μm [7], [19]; and 3) Ge pMOS FinFETs with strained Ge-fin height of 15 nm on a 100 nm-SiGe buffer layer [9] and gate length of 66 nm, fin length of 500 nm, and fin width of 20 nm from this work. As a result of the transition to FinFET technology, reductions in STI thickness in areas of relevance to transistor operation, and elimination of process steps leading to degradation in radiation response (e.g., halo implant), Fig. 9 shows clearly that the strained Ge pMOS FinFETs in this work show vastly superior leakage current and significantly improved ON/OFF current ratios than devices built in previous generations of Ge pMOS technology. The existing structures require only an adjustment to the starting V_{th} (e.g., by changing the gate metal to adjust the work function) to become viable candidates for insertion into next-generation, radiation-tolerant CMOS technology. We also note that initial single-event-effects results on test structures appear quite promising [27], but of course, the TID and single-event response of fully processed ICs would also need to be evaluated to assess the technology for potential space use.

V. Conclusions

We have evaluated the total-ionizing-dose response of strained Ge pMOS FinFETs varying in fin length, fin width, and gate length. Modest threshold-voltage shifts, small transconductance degradation, and minimal changes in ON/OFF current ratios are observed. These devices show superior performance to planar Ge pMOS devices because of improvements in material quality, device processing, and gate control, relative to previous technology generations. These improvements are due primarily to the transition to FinFET technology, reductions in STI thickness in areas of relevance to transistor operation, and elimination of process steps leading to degradation in radiation response (e.g., halo implant). These results demonstrate that strained Ge pMOS FinFETs are strong candidates for incorporation into near-future generations of CMOS ICs for space and other high-radiation, high-reliability applications.

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Total Ionizing Dose Effects on Strained Ge pMOS FinFETs on Bulk Si

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***Abstract*— We have characterized the total ionizing dose response of strained Ge *p*MOS FinFETs built on bulk Si using a fin replacement process. Devices irradiated to 1.0 Mrad(SiO_2) show minimal transconductance degradation (less than 5%), very small V_{th} shifts (less than 40 mV in magnitude) and very little ON/OFF current ratio degradation (<5%), and only modest variation in radiation response with transistor geometry (typically less than normal part-to-part variation). Both before and after irradiation, the performance of these strained Ge *p*MOS FinFETs is far superior to that of past generations of planar Ge *p*MOS devices. These improved properties result from significant improvements in processing technology, as well as the enhanced gate control provided by the strained Ge FinFET technology.**

***Index Terms*— 10 keV X-ray, geometry dependence, germanium FinFETs, total ionizing dose.**

I. Introduction

GERMANIUM-based *p*MOS FinFETs integrate material and structural advantages to optimize several key device operating properties that support their use in sub-14 nm CMOS technologies. Benefits over Si *p*MOS FinFETs include higher hole mobility, reduced short-channel effects, and reduced bias-temperature instabilities, while maintaining compatibility with conventional Si integration processes [1]–[3]. The radiation responses of planar Ge *p*MOSFETs [4]–[7] and SiGe FinFETs [8] have previously been evaluated. For Ge planar *p*MOSFETs, relatively low ON/OFF ratios were observed [4]–[7], and device response was sensitive to process conditions, e.g., the thickness of the Si capping layer that separated the Ge and dielectric layers, and/or halo implantation [5]. For SiGe FinFETs, a combination of bias-stress and radiation-induced charge trapping effects was observed [8]. As a result, these earlier-generation planar Ge *p*MOS transistors and SiGe *p*MOS FinFETs were not suitable for use in high-volume commercial or space environments.

As processing technologies have improved, knowledge from previous studies has been employed to continually improve the performance and reliability of Ge-based technologies. In this work, we provide a detailed evaluation of the radiation response of strained Ge *p*MOS FinFETs with different geometries under different bias conditions. We find that ON/OFF ratios are improved significantly before and after irradiation, compared to planar Ge *p*MOSFETs, and that charge trapping effects due to both bias-stress and irradiation are reduced in these Ge FinFETs, compared with SiGe FinFETs evaluated in 2014 [8]. These results indicate that strained Ge *p*MOS FinFETs are excellent candidates for integration into next-generation radiation-tolerant CMOS IC technologies.

II. Experimental Details

The Ge *p*MOS FinFETs evaluated in this work were fabricated at imec on 300 mm bulk Si (100) wafers. Transistor fabrication included a fin replacement process in which the original Si fin is replaced by a partially relaxed $Si_{0.25}Ge_{0.75}$ layer and Ge channel in a single step [1], [9]. For these devices, a thin Si cap was partially oxidized, yielding an unconsumed thin Si buffer layer to passivate the Ge surface and improve the interface quality. On top of the SiO_2 interfacial layer (IL), a ~1.5 nm HfO_2 layer and TiN metal gate were deposited. The effective oxide thickness (EOT) of the gate dielectric stack is ~1.9 nm. Because these are test structures intended to characterize the initial response of a developing process technology, the starting threshold voltage value was not optimized.

Fig. 1(a) shows a schematic diagram of the targeted-undoped, strained Ge Fin on $Si_{0.3}Ge_{0.7}$ strain-relaxed buffer built on 45 nm pitch spacer-defined Si fins on a (100)

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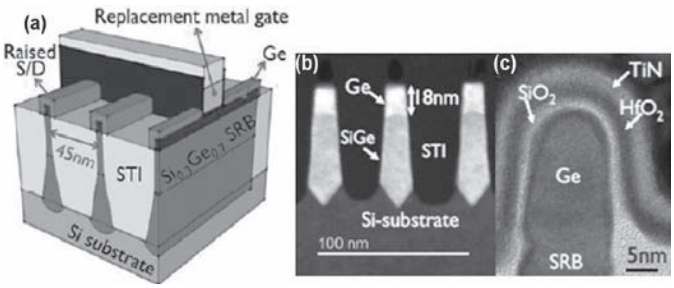

Fig. 1. (a) Schematic diagram of the targeted-undoped, strained Ge fin on $Si_{0.3}Ge_{0.7}$ strain-relaxed buffer, built on 45 nm pitch spacer-defined Si fins on a (100) Si substrate, (b) HAADF XTEM after replacement channel deposition, and (c) zoom into Ge channel at the end of processing. The final Ge fin is 13 nm wide and 18 nm tall.

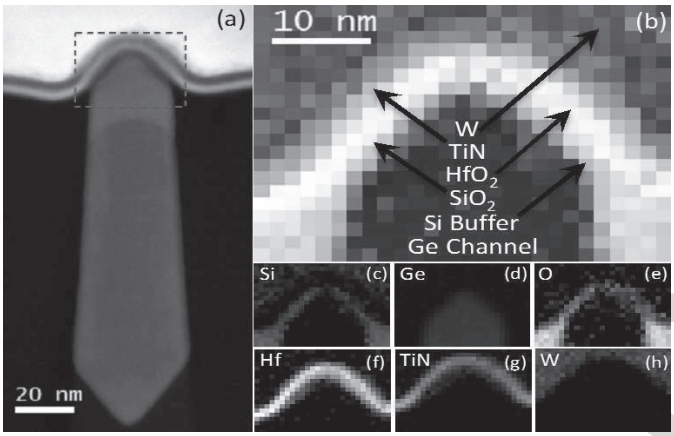

Fig. 2. (a) STEM image of bulk Ge FinFET. (b) Chemical composition map of different structure layers from EELS. (c)-(h) Individual maps of elements/compounds found in device.

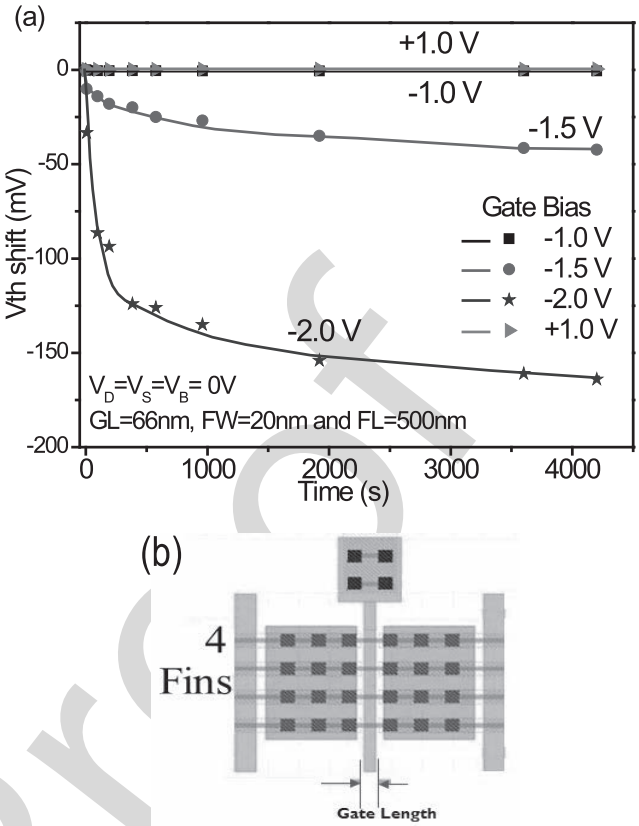

Fig. 3. (a) Threshold voltage shifts as functions of time and gate bias for Ge pMOS FinFETs. A schematic illustration of the test structures is shown in (b). The devices include 4 fins in parallel. All dimensions are as-designed. The printed value after trimming the "66 nm" gate is around 36 nm, for example.

Si substrate; Fig. 1(b) shows a high-angle annular dark field (HAADF) cross-sectional transmission-electron-microscopy XTEM image after replacement channel deposition; and Fig. 1(c) shows a zoomed image of the Ge channel at the end of processing. These images show that the final Ge fin is 13 nm wide and 18 nm tall [9]. A scanning transmission electron microscope (STEM) image of the FinFET is shown in Fig. 2(a). To ascertain the chemical composition of the different layers in the STEM image, electron energy loss spectroscopy (EELS) is used to form spectral images of the elements in the device. A composite drawing showing the chemical composition of different layers is shown in Fig. 2(b), along with maps of the Si, Ge, O, Hf, TiN, and W (Figs. 2c–2h). The underlying strained Ge layer, Si cap (to enhance interface quality), thin SiO_2/HfO_2 gate dielectric, and TiN/W gate metallization are all clearly delineated.

Total ionizing dose (TID) irradiations were performed using a 10-keV ARACOR X-ray source at room temperature at a rate of 31.5 krad(SiO_2)/min. Three gate bias conditions ($V_G = -1$ V, $+1$ V, and all pins grounded) were applied during irradiation and/or bias stress. A semiconductor parameter analyzer, HP4156A, was used to supply DC bias during the experiment, as well as to perform the *I-V* characterization before and after each exposure. The dimensions of the tested devices vary in fin width from 16 nm to 100 nm, fin length from 500 nm to 12.5 μm, and gate length from 66 nm to 230 nm. The fin length (see Fig. 3) was varied as part of the process evaluation matrix, but the channels of individual transistors are defined by the gate length, fin width, and fin height, as shown in Fig. 1. At least three devices with the same dimensions were tested for each set of test results shown. Results of average devices are shown below, with error bars indicating the range of responses.

III. Results and Analysis

Fig. 3 shows (a) the threshold voltage V_{th} shift as a function of applied gate bias and stress time for devices with a gate length of 66 nm and fin width of 20 nm, and (b) a schematic illustration of the 4-fin test devices evaluated in this study. There are significant V_{th} shifts for negative gate biases of -2 V and -1.5 V, which are comparable to those observed previously for SiGe FinFETs [8]. However, these voltages are well beyond the expected operating limits of this technology. At room temperature and ± 1 V bias (approximately double the expected operating voltage of this technology), there is no detectable shift in V_{th} or significant increase in leakage current for any of the strained Ge pMOS FinFETs tested under voltage stress, for the times and biases of this study. These results demonstrate the relative stability of devices during irradiation under the bias conditions of this study. Moreover, these results

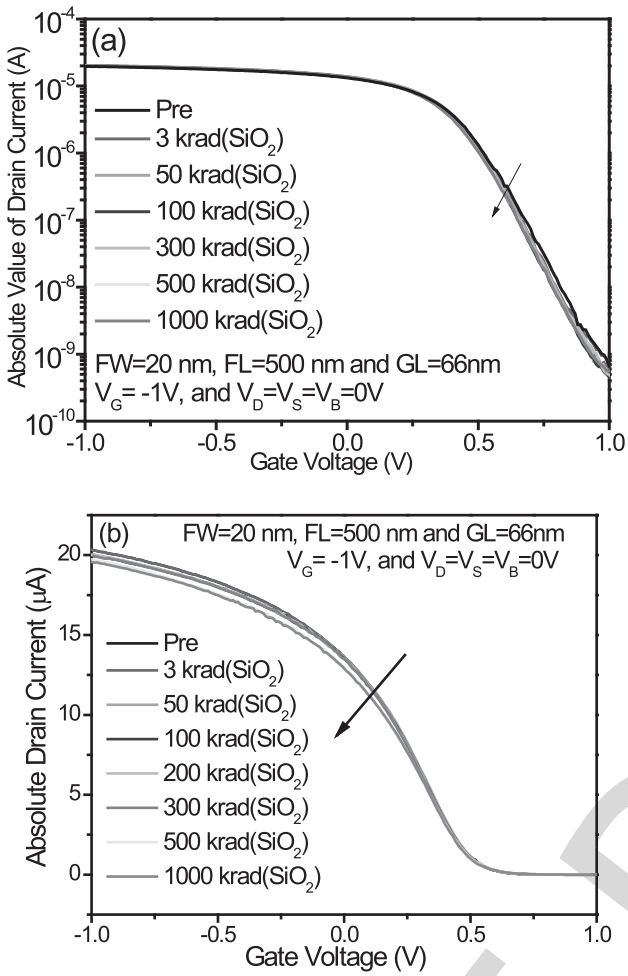

Fig. 4. I_D-V_G curves as functions of dose for a device with gate length of 66 nm, fin width of 20 nm, and fin length of 500 nm: (a) semi-log plot and (b) linear plot. $V_D = -0.1$ V during all I_D-V_G sweeps.

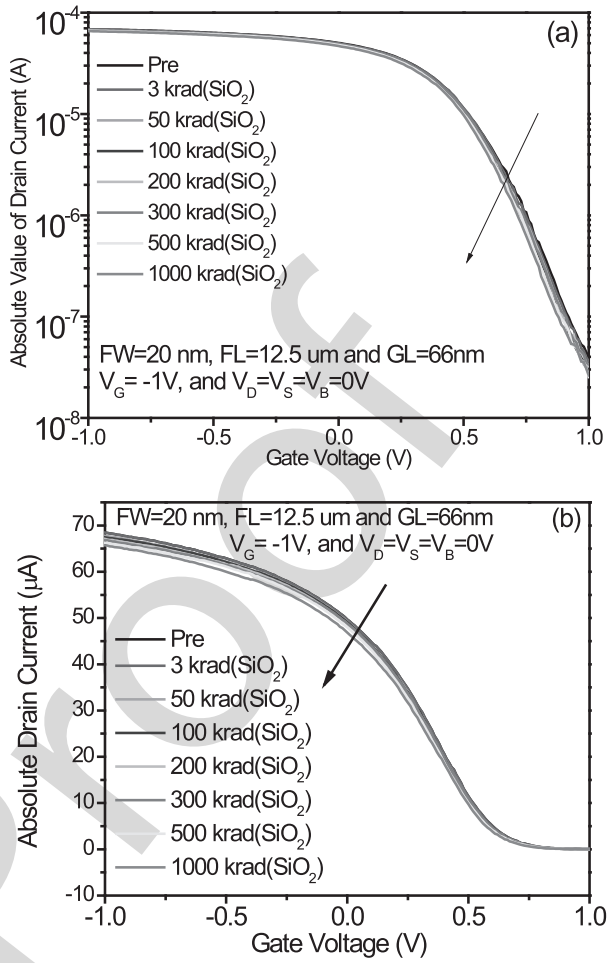

Fig. 5. I_D-V_G curves as functions of dose for a device with gate length of 66 nm, fin width of 20 nm, and fin length of 500 nm: (a) semi-log plot and (b) linear plot. $V_D = -0.1$ V during all I_D-V_G sweeps.

contrast with the responses of SiGe pMOS FinFETs in [8], for which shifts due to bias-induced charging during irradiation complicated the extraction of the "pure" TID response [8].

Figs. 4 and 5 show the I_D-V_G characteristics for TID tests on devices with gate length of 66 nm, fin width of 20 nm, and fin lengths of 500 nm and 12500 nm, respectively. In each case, the active transistor gate is much shorter than the lithographically defined fin, as shown in Fig. 3(b). Each device shows a small, negative V_{th} shift with increasing TID, consistent with a small amount of net hole trapping in the gate dielectric layers. Less than ~5% ON state current degradation is observed for either device. From these curves, the extrapolated V_{th} and $G_m = \Delta I_D / \Delta V_G$ were extracted using standard techniques in the linear mode of device operation, with $V_D = -0.1$ V. No adjustment to the gate-metal work function was performed to optimize the starting value of threshold voltage for these devices, so the OFF state current for these test structures is taken to be the current measured at $V_G = 1$ V. With this definition, the ON/OFF current ratio for the 500 nm fin length device in Fig. 4(a) is more than 10^5, which is comparable to that of the strained SiGe FinFETs in [8], and significantly higher than the ratios observed for (relaxed) planar Ge pMOS devices in [4]–[7]. The increased ON/OFF current ratios for these FinFETs are due to improvements in starting material quality as well as the improved gate control achievable in FinFETs, as compared to planar Ge devices, as we discuss below.

Fig. 6 shows threshold voltage shifts, changes in normalized transconductance, and measured ON/OFF current ratios as functions of irradiation and annealing time for devices irradiated at gate biases of ±1 V and 0 V, and annealed under negative bias. The largest V_{th} shifts occur for negative gate bias during irradiation, and correspond to net hole trapping in the gate dielectric layers during irradiation. Under positive irradiation bias, V_{th} shifts are small and positive, consistent with net radiation-induced electron trapping in the HfO_2 dielectric layer, as commonly observed [8], [10], [11]. TID-induced shifts are smaller in these strained Ge pMOS FinFETs than the SiGe FinFETs in [8], most likely because of the reduced gate bias used in this study, which is closer to anticipated device operating conditions, and/or lower defect densities in the dielectric layers of these devices. V_{th} shifts decrease or remain approximately constant during room-temperature, negative-bias annealing. The stability of

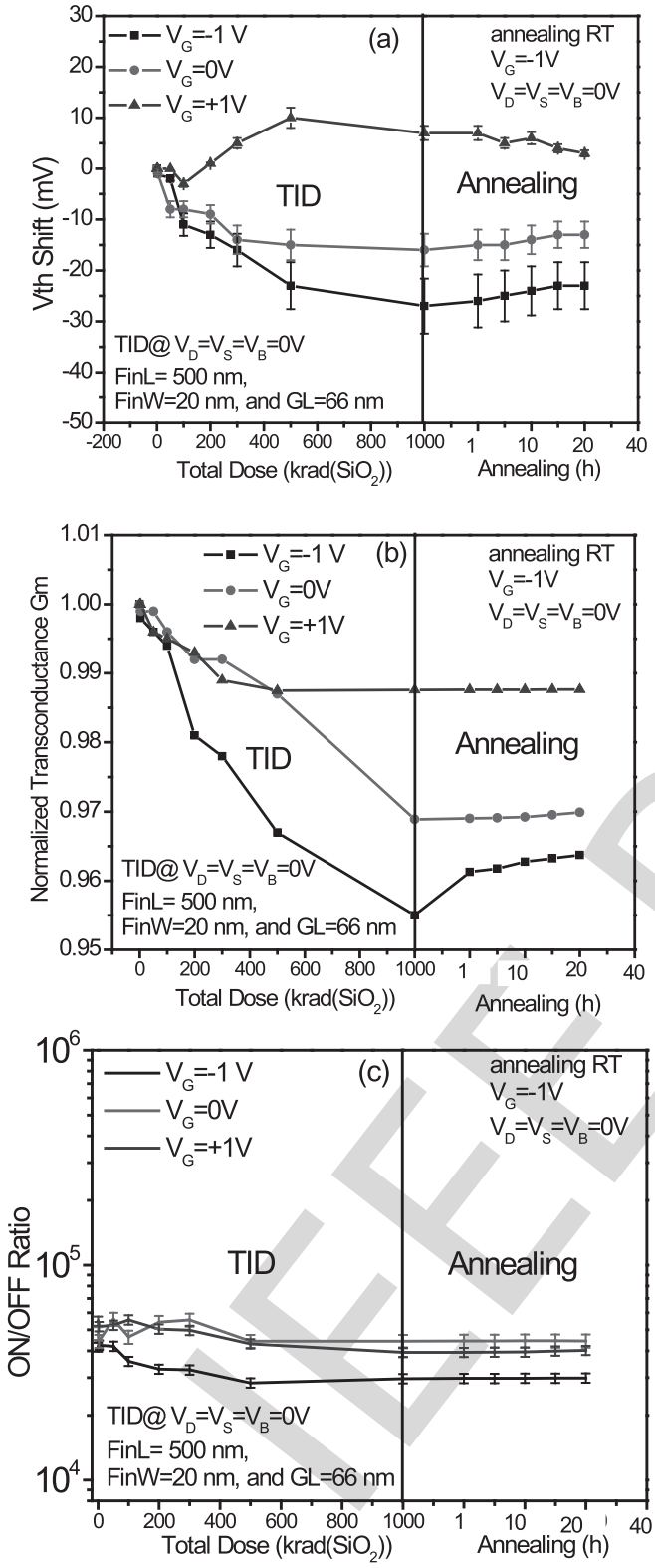

Fig. 6. (a) Threshold voltage shift, (b) normalized transconductance, and (c) ON/OFF current ratio as functions of total dose for gate biases $V_G = -1$ V, 0 V, and +1 V, and/or room temperature annealing time at $V_G = -1$ V, for devices with gate length of 66 nm, fin width of 20 nm, and fin length of 500 nm. Data points here are averages from at least three devices, and error bars show the full range of variation observed.

the devices during annealing further demonstrates that bias-induced charging is negligible during these irradiation and annealing tests. The transconductance G_m degradation (<5%),

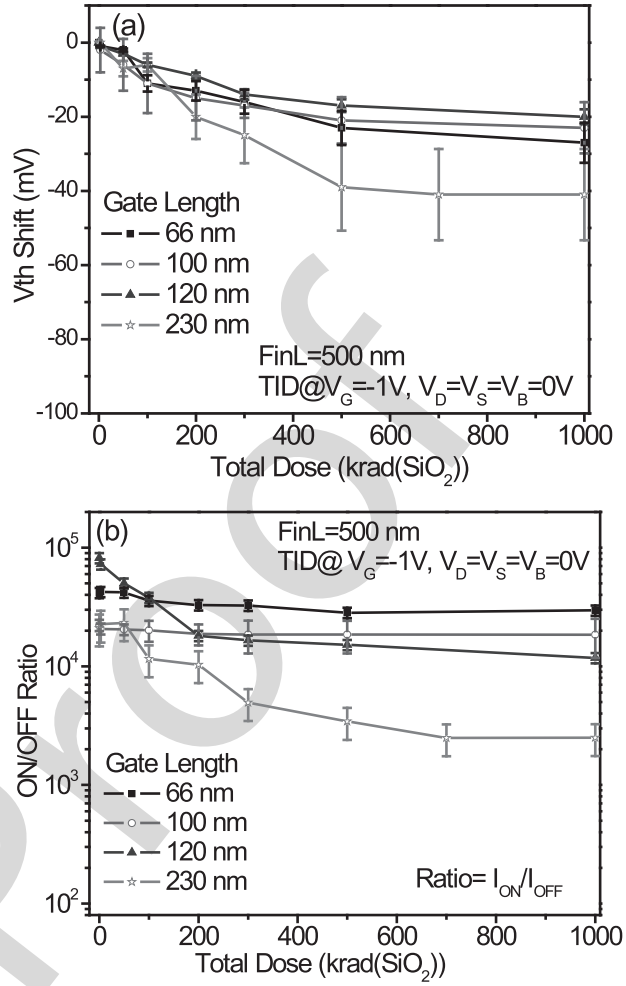

Fig. 7. (a) Threshold voltage shifts and (b) ON/OFF current ratios as functions of total dose and gate length for devices with fin width of 20 nm and fin length of 500 nm at a gate bias during irradiation of $V_G = -1$ V, and $V_D = V_S = V_B = 0$ V. Data points here are averages from at least three devices, and error bars show the full range of variation observed.

V_{th} shifts (<30 mV) and ON/OFF current ratio degradation (<5%) in these strained Ge pMOS FinFETs are far superior to the responses of relaxed, planar Ge pMOS devices in [4]–[7], again as a result of significant improvements in processing technology [1]–[3] and improved gate control.

Fig. 7 summarizes (a) V_{th} shifts and (b) ON/OFF current ratios as a function of TID for negative gate-bias irradiation of devices with fin width of 20 nm and gate lengths of 66 nm to 230 nm. All devices show V_{th} shifts smaller than 50 mV in magnitude. Devices with shorter gate lengths show smaller V_{th} shifts (-20 mV to -35 mV), increased ON/OFF ratios, and smaller variations in response compared to devices with 230 nm gate length. This likely occurs because shorter gate-length devices are less likely to be impacted by defects in the starting material, which can degrade junction and oxide quality before and after irradiation [5], [6]. That the ON/OFF current ratio before and after irradiation is greatest for shorter gate-length devices is encouraging, since the properties of smaller-dimension devices have more practical significance for future IC applications than properties of larger-dimension devices.

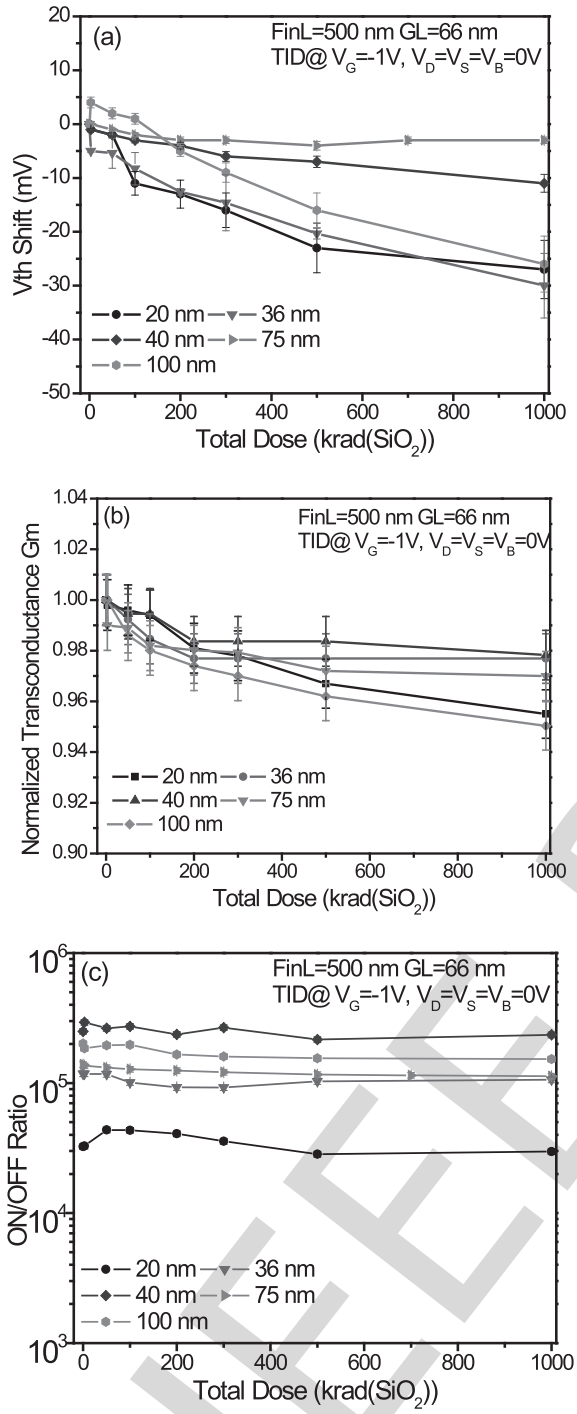

Fig. 8. (a) V_{th} shifts, (b) normalized transconductance, and (c) ON/OFF current ratios as functions of total dose for gate biases during irradiation of $V_G = -1$ V and $V_D = V_S = V_B = 0$ V for Ge pMOS FinFETs with gate length of 66 nm and fin widths of 20-100 nm. Data points here are averages from at least three devices, and error bars show the full range of variation observed.

We note that the results of Fig. 7 are the only case in our testing of these devices, to date, in which it appears that one geometrical split exhibits a statistically different response from other process splits, which should simplify IC design in this technology.

Fig. 8 shows (a) V_{th} shifts, (b) normalized transconductance, and (c) ON/OFF current ratios as functions of total dose for devices irradiated with $V_G = -1$ V and $V_D = V_S = V_B = 0$ V for Ge pMOS FinFETs with gate length of 66 nm and fin widths of 20- 100 nm. All devices show negative V_{th} shifts (-3 mV to -35 mV), decreases in transconductance (1 to 5%), and minimal changes in ON/OFF current ratio with increasing TID. No clear trends in radiation response are observed with varying fin width.

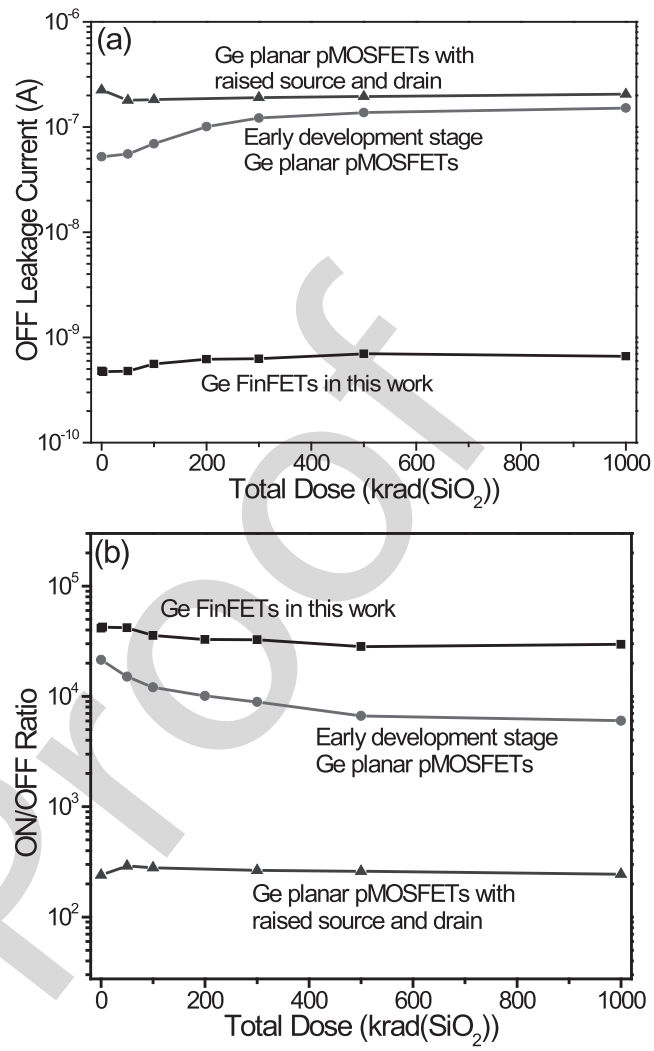

Fig. 9. (a) Leakage current, and (b) ON/OFF current ratios as functions of total dose with gate biases during irradiation of $V_G = -1$ V and $V_D = V_S = V_B = 0$ V for Ge pMOS transistors from three technology generations: 1) early development stage Ge planar pMOSFETs; 2) Ge planar pMOSFETs with raised source and drain; and 3) Ge pMOS FinFETs from this work.

IV. Discussion

The excellent radiation response of the strained Ge pMOS FinFETs and absence of fin-width dependence in this work contrasts strongly with previous results on earlier generation Si nMOS FinFETs on SOI wafers [12], [13], in which much larger V_{th} shifts and a strong fin width dependence were observed. These improvements in response for strained Ge pMOS FinFETs, relative to SOI FinFETs, result primarily from the absence of a buried oxide layer. In SOI devices, the buried oxide layer can strongly affect device response as a result of buried-oxide to top-gate electrostatic charge coupling

effects [12], [13], [20]–[22]. Instead, the relatively small V_{th} shifts in these bulk Ge pMOS FinFETs are due primarily to charge trapping in the gate dielectric (SiO_2/HfO_2) layers.

These strained Ge pMOS FinFETs also show far superior radiation response to recent-generation, bulk nMOS Si FinFETs, for which significant STI leakage is observed below $\sim$ 300 krad(SiO_2) [14]. This improvement in response is due primarily to three factors: (1) The thickness of the STI at the lower fin corner of the strained Ge pMOS FinFET (see Fig. 1(c)) is reduced in thickness, as compared with the STI of the bulk nMOS Si FinFETs in [14], leading to reduced STI charge trapping in the region closest to the active device channel [23]. (2) The QW structure effectively isolates conduction in the active device channel and associated parasitic structures from potential coupling effects that can be associated with charge trapping in the STI in some types of devices [24], [25]. (3) The nominally undoped Ge channel layer in these pMOS FinFETs has an effective n-type doping after processing, as a result of dopant diffusion out of the highly n-doped underlayer [9], [26]. Net positive trapped charge in the STI more strongly accumulates n-type surfaces [10], [23]. Consequently, no significant STI-related leakage is observed for these strained Ge pMOS FinFETs, up to at least 1 Mrad(SiO_2), under the conditions of this study.

The strained Ge pMOS FinFET structure illustrated in Figs. 1 and 2 also enables high performance transistors to be fabricated without the requirement for process steps that are necessary to include in planar Ge pMOS technologies. For example, the halo implant that is necessary in planar technology to control short channel effects [15] also leads to a radiation-induced reduction of ON/OFF ratio [5] and increase in low-frequency noise [6] for planar Ge pMOS technologies. With the enhanced gate control of FinFET technology, halo implantation is no longer required.

To illustrate the technology scaling trends in Ge pMOS technology, Fig. 9 compares (a) off-state drain leakage and (b) ON/OFF current ratios as functions of total dose for devices from three generations of imec Ge-based pMOSFETs built on silicon substrates: 1) early development stage Ge planar pMOSFETs with a Ge layer thickness of 2 μm and $W/L = 9.8$ μm/0.8 μm [6], [16]–[18]; 2) Ge planar pMOSFETs with Ge layer thickness of 200 nm, raised source and drain, and dimensions of $W/L = 1$ μm/0.47 μm [7], [19]; and 3) Ge pMOS FinFETs with strained Ge-fin height of 15 nm on a 100 nm-SiGe buffer layer [9] and gate length of 66 nm, fin length of 500 nm, and fin width of 20 nm from this work. As a result of the transition to FinFET technology, reductions in STI thickness in areas of relevance to transistor operation, and elimination of process steps leading to degradation in radiation response (e.g., halo implant), Fig. 9 shows clearly that the strained Ge pMOS FinFETs in this work show vastly superior leakage current and significantly improved ON/OFF current ratios than devices built in previous generations of Ge pMOS technology. The existing structures require only an adjustment to the starting V_{th} (e.g., by changing the gate metal to adjust the work function) to become viable candidates for insertion into next-generation, radiation-tolerant CMOS technology. We also note that initial single-event-effects results on test structures appear quite promising [27], but of course, the TID and single-event response of fully processed ICs would also need to be evaluated to assess the technology for potential space use.

V. Conclusions

We have evaluated the total-ionizing-dose response of strained Ge pMOS FinFETs varying in fin length, fin width, and gate length. Modest threshold-voltage shifts, small transconductance degradation, and minimal changes in ON/OFF current ratios are observed. These devices show superior performance to planar Ge pMOS devices because of improvements in material quality, device processing, and gate control, relative to previous technology generations. These improvements are due primarily to the transition to FinFET technology, reductions in STI thickness in areas of relevance to transistor operation, and elimination of process steps leading to degradation in radiation response (e.g., halo implant). These results demonstrate that strained Ge pMOS FinFETs are strong candidates for incorporation into near-future generations of CMOS ICs for space and other high-radiation, high-reliability applications.

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