

Department of Energy

Final Project Report for WIRELESS LINK AND MICROELECTRONICS DESIGN FOR RETINAL PROSTHESES

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This project focuses on delivering power and data to the artificial retinal implant inside the eye and the implant microstimulator electronics which delivers the current pulses to stimulate the retinal layer to elicit visual perception. Since the use of invasive means such as tethering wires to transmit power and data results in discomfort to the patients which could eventually cause infection due to the abrasion caused by the wire and contact of the internals of the eye to the external environment, a completely wireless approach is used to transfer both power and data. Power is required inside the eye for the microelectronic implant which uses a dual voltage supply scheme (positive and negative) to deliver biphasic (anodic and cathodic) current pulses. Data in the form of digital bits from the data transmitter external to the eye, carries information about the amplitude, phase width, interphase delay, stimulation sequence for each implant electrode. The data receiver unit decodes the digital stream and the microstimulator unit generates the appropriate current stimuli. Since the external unit consisting of the power transmitter can experience coupling a variation with the power receiver due to the patient's movements, a closed loop approach is used which varies the transmitted power dynamically to automatically compensate for such movements. This report presents the salient features of this research activities and results.

I. Power Link—A Multi-Voltage Rectifier

Inductive power has been a main source to supply biomedical implants which requires a reliable and efficient DC powering scheme. Modern implants rely on mixed-mode designs and inevitably requires multi-voltage in order to optimize the system power. Furthermore implants are usually operated under physics and regulatory service regulation on tissue absorption (e.g. SAR and field strength), which implies the constraints of frequency, power, and size. To generate multi-voltage at high efficiency for retinal prosthesis, we present an integrated rectifier using the multi-well structured HV CMOS process. The rectifier achieves an efficiency of 89.3% with a loading of 36mW.

Figure 1 shows a proposed multi-voltage rectifier (Timing Control Rectifier (TCR)), which utilizes both I/O (5V) and HV (32V) transistors with 0.8V and 1.2V threshold voltages, respectively. Two AC voltages, Coil_HV and Coil_LV, are induced by coils L_1 and L_2 (middle tapped) from an external coil. The rectifier simultaneously generates both low positive and negative voltages of VddL and VssL for digital and data telemetry circuits, as well as both high positive and negative voltages of VddH and VssH for stimulators. Our dual-HV scheme reduces the required induced voltage amplitude, which implies smaller

coil and also reduction of overall power dissipation. In Figure 1(a), when Coil_HV is larger than V_{ddH} and Coil_LV is larger than V_{ddL} , the corresponding control logic turns on the rectifying transistors at a short predefined interval. Similarly the control logic is applied when Coil_HV is smaller than V_{ssH} and Coil_LV is smaller than V_{ssL} . During this interval, the charge/discharge is carried out for C_{F1-F4} , which in turn drive the loads of R_{L1-L4} . By using a precise timing control, the reverse leakage currents are preventable if the rectifying transistors are turned off before the induced voltages drops below V_{ddH} and V_{ddL} .

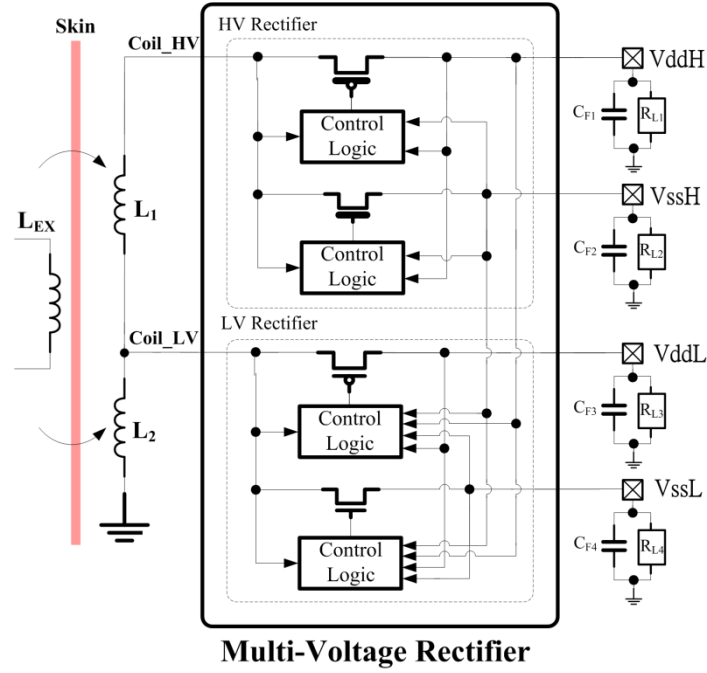


Figure 1. A multi-voltage rectifier architecture.

Figure 2 shows the start-up waveform of the proposed rectifier, in which four output voltages gradually stabilize after inductive power is turned on. Note that LV outputs are intentionally designed to reach the stable values earlier than the HVs. This start-up sequence has advantages of a) an early-stabilized LVs ensure the proper function of the telemetry and digital circuits before stimulation starts; b) it enables the implementation of the control logic of the HV rectifier with LV transistors to save both area and power.

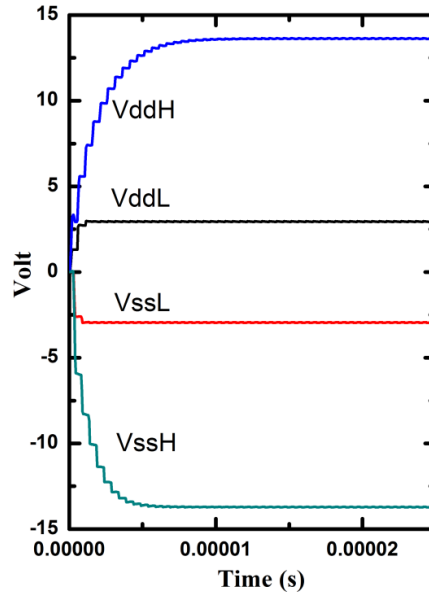
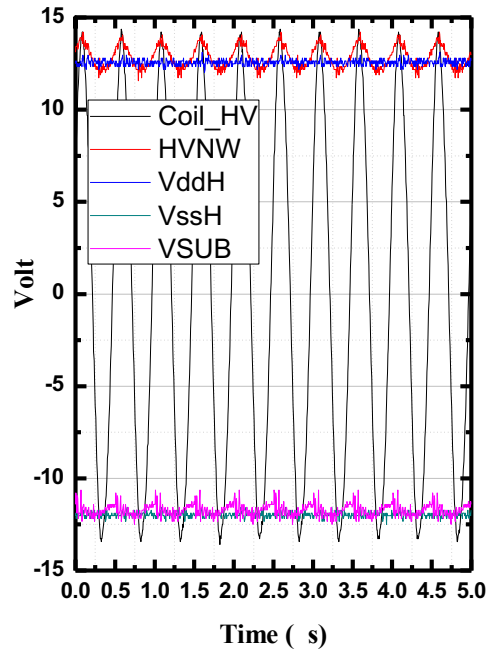


Figure 2. Output supplies voltages from a multi-voltage rectifier.

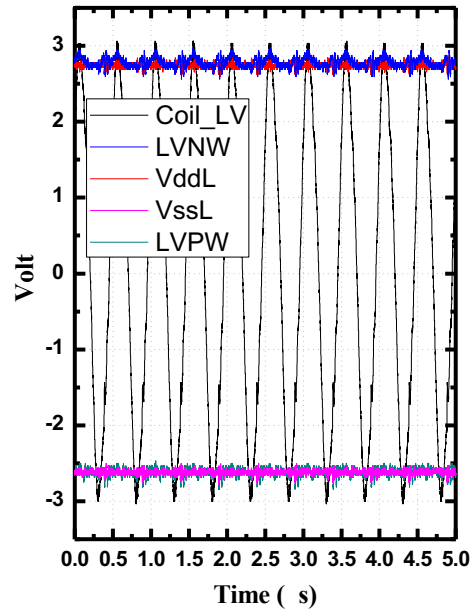
The rectifier receives the induced voltages, Coil_LV ($3V_{\text{amp}}$) and Coil_HV ($14V_{\text{amp}}$), at 2MHz. The static power of the rectifier is $150\mu\text{W}$. Four external filter capacitors of 100nF are placed at the rectifier outputs. The output voltages of the rectifier are $\pm 2.4\text{V}$ and $\pm 12.5\text{V}$ at the loading power of 10mW and 36mW. For the application of retina prosthesis, the HV rectifier has an efficiency of 89% at 3mA current. Figure 3(a) shows the measured waveforms of VddL, VssL, LVPW and LVNW (the bulk voltages of MP_{R1} and MN_{R1}), at the loading of 4.5mW. The measured results of VddH, VssH, HVNW and VSUB (the bulk voltages of MP_{R2} and MN_{R2}), at the loading of 48 mW are shown in Figure 3(b). Figure 4 shows the measured results of VddH-VssH versus induced peak-to-peak voltage of Coil_HV under a loading current of 2mA. Consequently, the rectifier has the flexibility of providing a wide range of compliance voltages and thus it is applicable to various biomedical applications.

At 2MHz, Figure 5 shows the measured rectifier efficiency versus the loading power. An increasing loading current leads to lower efficiency as a result of the increasing drain-to-source voltage of the rectifying transistor. The LV rectifier has an efficiency of 82% with $\pm 2.4\text{V}$ outputs under the loading of 10mW. HV rectifier has an efficiency $> 90\%$ when loading $< 15\text{mW}$. At the loading of 127mW, the efficiency is 80.7%. The working frequency of the rectifier is up-to 6 MHz, but efficiency is degraded if the frequency is increased.

In summary, our multi-voltage rectifier can provide multiple voltages for digital circuits and analog stimulators at the same times have a higher efficiency than previous works in the literatures.



(a)



(b)

Figure 3. Measured waveforms of rectifier outputs and corresponding bulk voltages of (a) HV rectifier at 48mW (b) LV rectifier at 4.5mW.

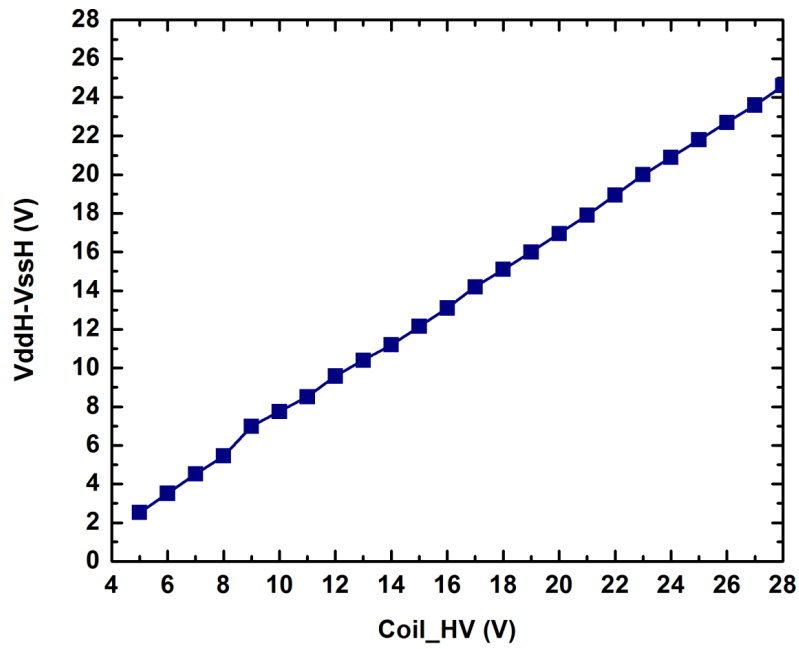


Figure 4. Measured VddH-VssH versus induced peak-to-peak voltage of Coil_HV at 2mA current loading.

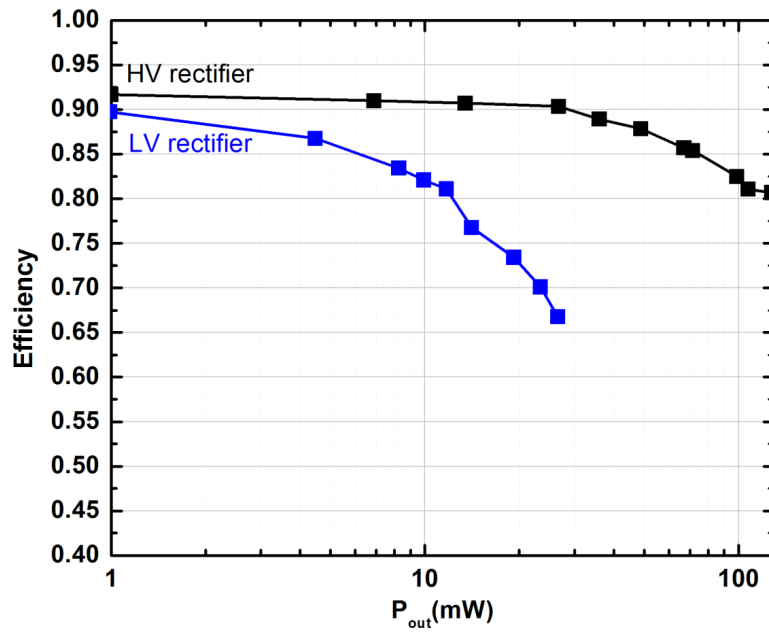


Figure 5. Measured efficiency of the rectifier at various loading. The efficiency is defined as peak-to-peak voltages of Coil_LV and Coil_HV versus $V_{ddL}-V_{ssL}$ and $V_{ddH}-V_{ssH}$ for LV and HV rectifiers, respectively.

The multi-voltage rectifier is designed and fabricated with TSMC 0.18 μm HV (32V) CMOS process. The chip microphotography is shown in Figure 6 with an active area of $900 \times 650\mu\text{m}^2$. HV and LV devices are separated far enough to prevent latch-ups.

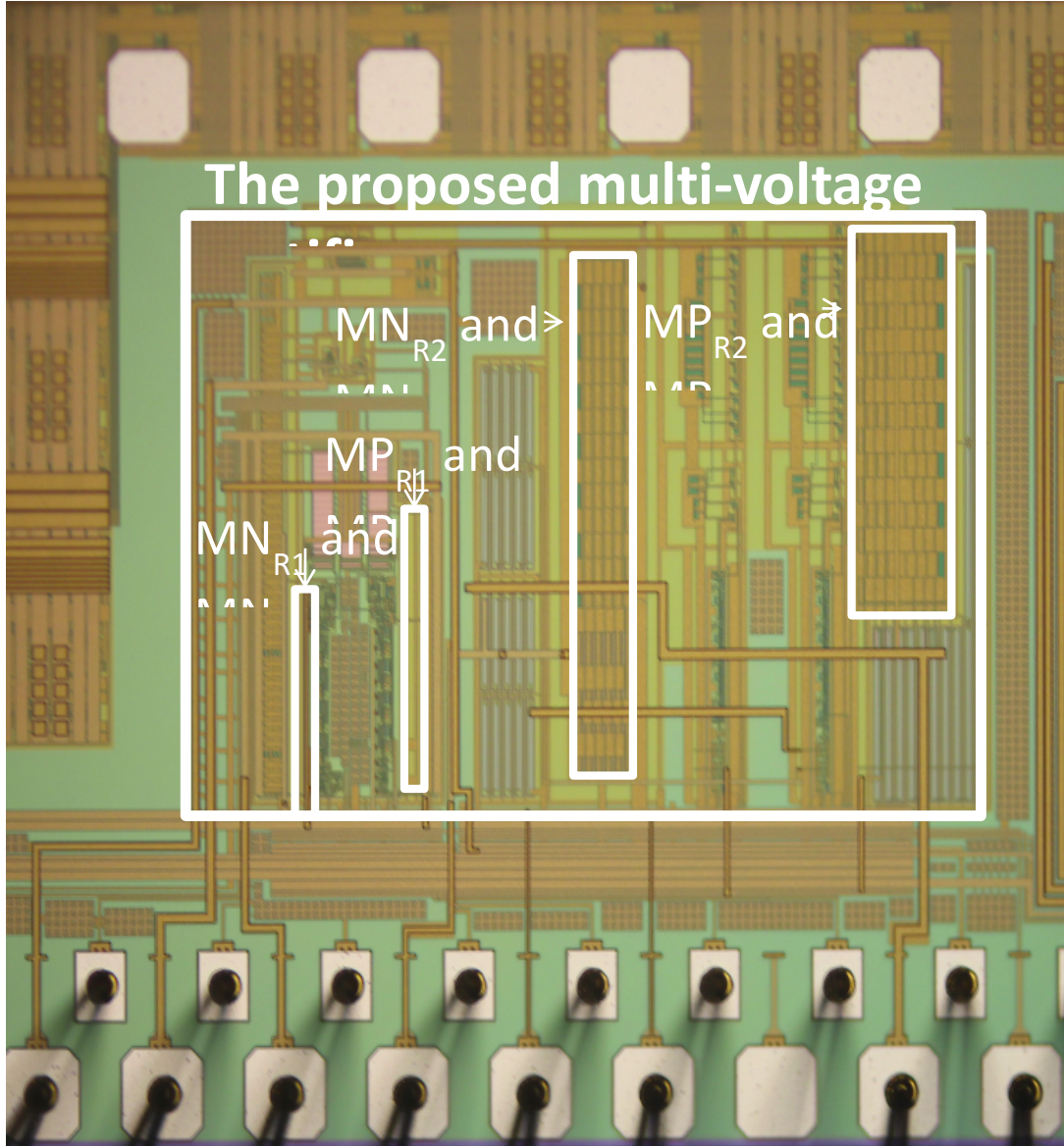


Figure 6. Chip microphotography of a multi-voltage rectifier.

II. Data Link—DPSK telemetry

We designed a DPSK data receiver that can support the data rate of 2Mbps for more than 1000 stimulations channels. Figure 7 is a block diagram of this data receiver circuit. It

comprises of a 1st order HPF with a cutoff frequency at 10MHz, a variable gain buffer, a DC voltage generator, and 8 switched capacitor array cells. It operates at a new 22MHz carrier frequency with 8MHz sampling rate. The data receiver was integrated with other functional blocks such as power telemetry, digital controller, and stimulators in 0.18 μ m High Voltage CMOS process.

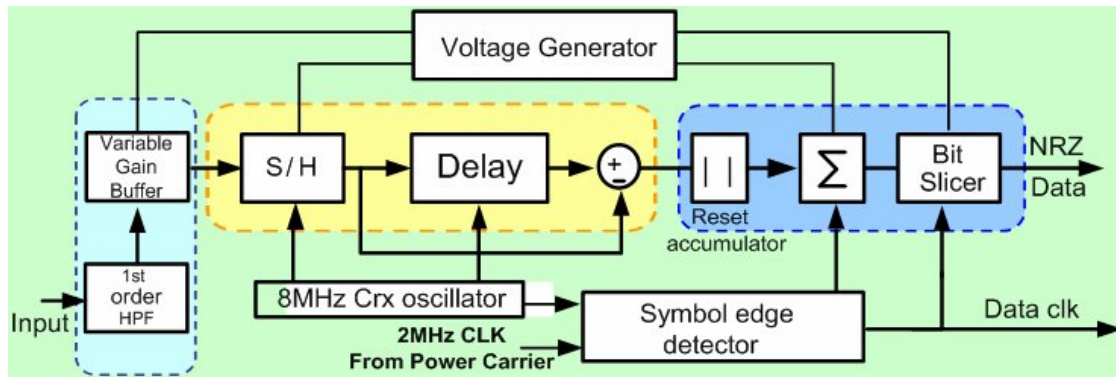


Figure 7. A block diagram of a DPSK data receiver.

Test Setup for a DPSK data receiver chip

Figure 8 shows a photo of the DPSK data receiver system prototype. There are two major parts in the testing apparatus. The first part is the DPSK data receiver prototype PCB, in the lower half of the figure, which is connected to a sliding fixture. In the back there is a sliding fixture that holds two pairs of concentric coils. The separation in axial direction can be adjusted on the sliding fixture. To the right of the metal pedestal of the fixture is an FPGA board whose LED light is lit up. This FPGA takes an input clock of data carrier frequency 22MHz. It then divides it by 11 to obtain a 2MHz clock synchronized by input clock. The data is clocked out of the buffer from FPGA by this divided 2MHz clock and fed to PSK modulator on data transmitter board. Because the input clock drives the data transmitter and the divided clock drives the power transmitter, data signal and power signal are thus synchronized

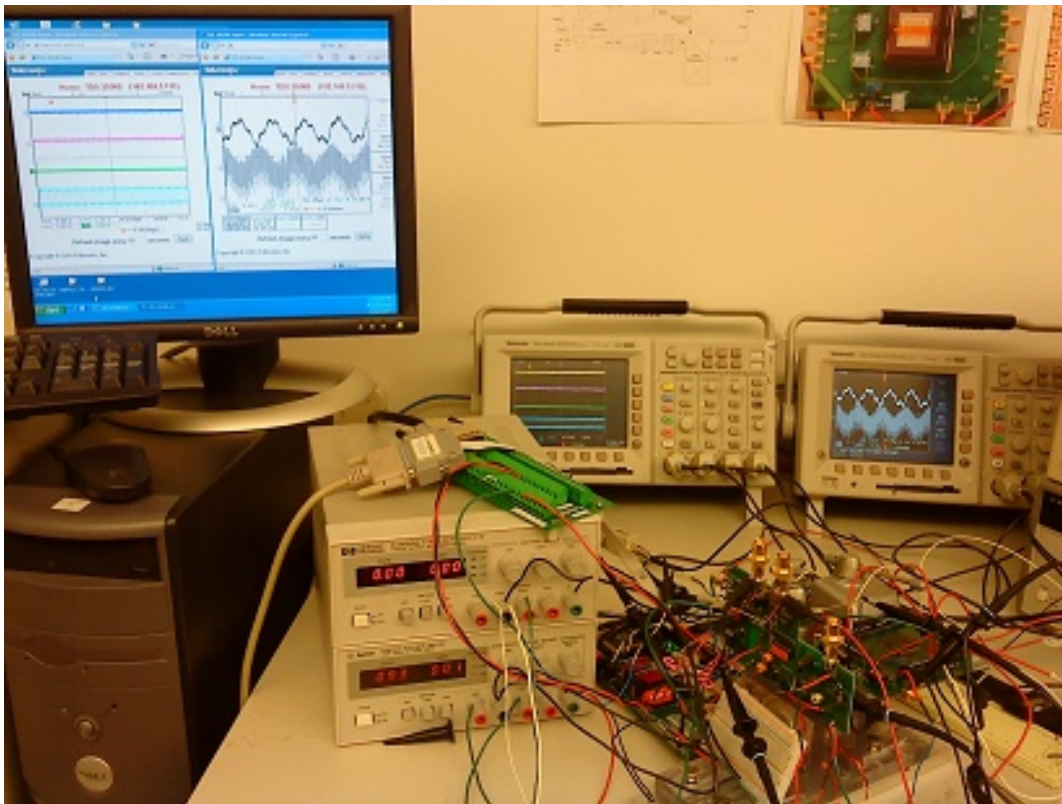


Figure 8. Testing apparatus for data telemetry implementing DPSK.

The measured test results of the new DPSK chip are shown in Figure 9. Trace 1 is a waveform measured at the output of the 1st HPF, which is fed with an incoming 2Mbps data that is modulated with a 22MHz carrier. Trace 2 and 3 show the differential outputs of the integrator circuit. Notice, in Trace 1 when there is no phase shift; the differential outputs of the integration circuit is zero that results a logic '0' as shown in Trace 4. Similarly, a 180-degree phase shift results an accumulated differential outputs that results logic '1'. This experiment shows that 2Mbps baseband data can be faithfully recovered.

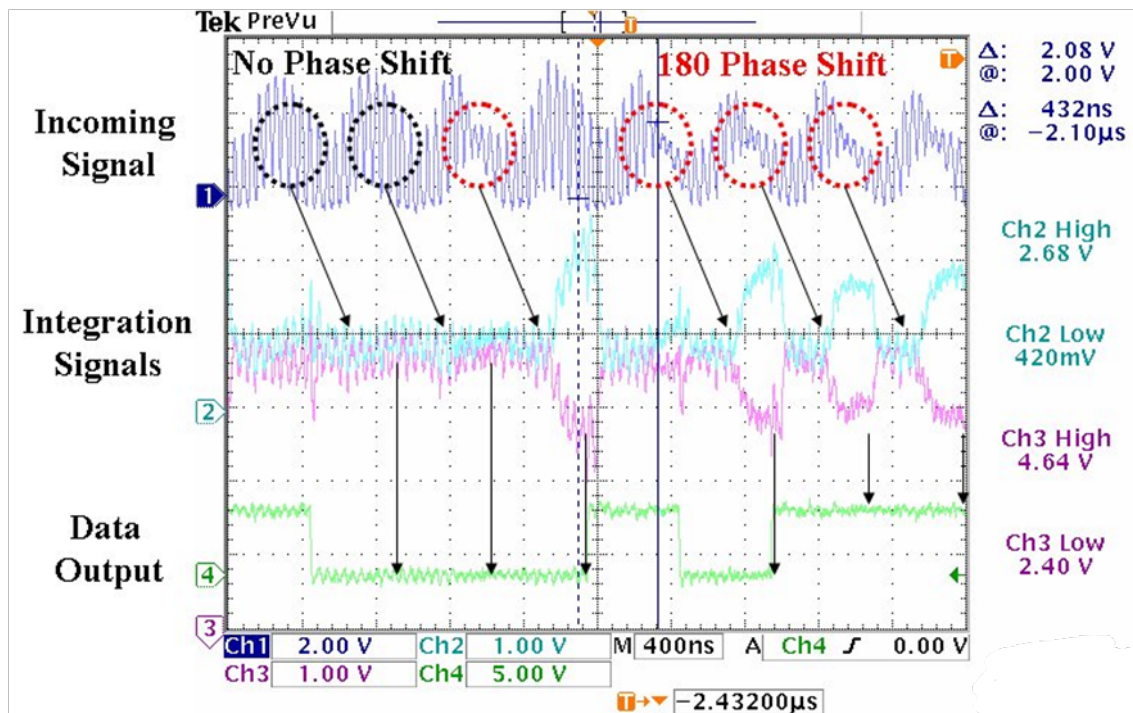


Figure 9. Measured waveforms of a new DPSK chip.

III. Systems Realization—Versatile Stimulation Systems

We completed a new integrated 268-channel retinal IC, which has a new power receiver implemented timing control rectifier (TCR) supporting multi-voltage, a data receiver, analog drivers and digital controllers. The chip size is 5.9mm × 5.8mm. It is interesting to note that this chip occupies *less* area while *quadrupled* the number of channels in comparison to the chip used in current 60-electrode retinal prosthetic device (ARGUS-II, Second Sight) designed in 2000 by Prof. Liu's research group. An individual stimulation pixel occupies 305µm × 310µm that includes an analog driver, a digital controller, a charge cancellation circuitry for tissue safety, biasing capacitors and a surface area pad connected to a stimulus output.

We had built two new versatile stimulation systems using our IC chips and developed software driver and GUI user application for these systems. The first prototype versatile stimulation system I (VSSI) has been shipped to Oak Ridge National Laboratory for Dr. Eli Greenbaum's group in the Fall of 2010. It has 16 channels output and two special channels with capability of generating sinusoid output waveforms. The second prototype versatile stimulation system II (VSSII) has 64 channels output with a form factor box a bit larger than VSSI. Both systems are user-friendly, run in Windows environment, and connect to a workstation or laptop using standard USB 2.0 port. The entire system is enclosed in a plastic box as shown in Figure 10.



Figure 10. A new versatile stimulation system box built using the stimulation IC with full software features support running on Windows workstation.

Versatile stimulation system I (VSSI): 16-Ch. square wave / 2-Ch. sine wave.

Versatile stimulation system I (VSSI) consisting of both hardware and software designs. The major hardware subunits include stimulator, recorder, power telemetry link, and data telemetry link as shown in Figure 11. The software includes system interface and GUI interface.

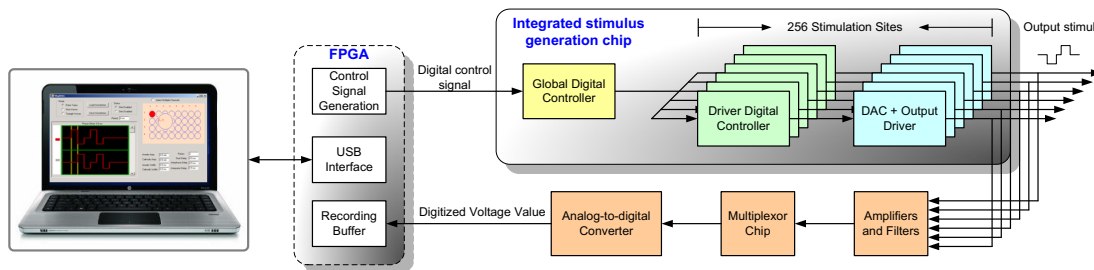


Figure 11. System diagram of the self-contained bioelectronic system.

We have realized a prototype chip which is used to implement a prototype system combining both hardware and software co-design. This prototype system can generate various output waveforms, such as sine wave, square wave, and triangle wave. It is important to point out that each output channel of this device can be independently programmed to achieve a flexible multi-channel outputs with precise temporal offsets among channels. This capability would facilitate biomedical applications, such as brain mapping and dynamics study, which would require detail spatial-temporal information.

In order to take an advantage of the prototype system, a flexible user interface has also been developed. The standardized USB 2.0 interface and the complete C++ application programming interface (API) have been developed and it makes this device easy to link with any graphic user interface (GUI). For example, a user can graphically specify and display the stimulation parameters such as pulse types, pulse amplitude and width, interphasic delay, anodic and cathodic first specification, stimulation frequency and stimulation skew for each frame as shown in the Figure 12. Additional capability such as stimulation and recording waveform display, FFT and spectral density analysis, statistical and analysis tools, could be also added through this versatile interface.

The system has been planned to equip with a recording subunit which supports the read operations. The subunit includes pre-amplifiers, amplifiers, filters, MUXs, ADCs, and FPGA for signal processing.

For self-contained purpose, the system has a power link subunit which consists of resonant circuit, rectifiers, and regulators to provide DC power. Also the system includes a wireless data link subunit which is able to provide bi-directional communication to issue commands, stimulation data and transmit the recording data.

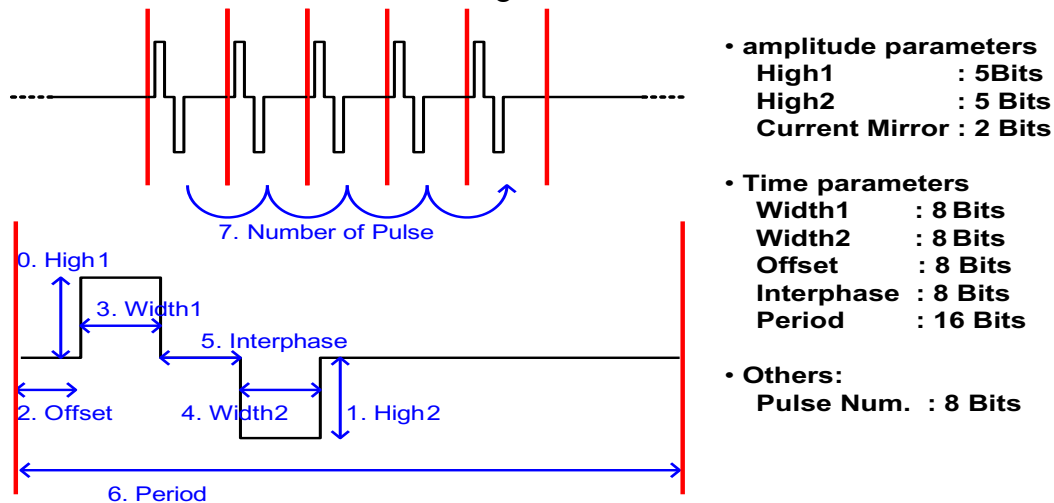


Figure 12: Specification of Stimulation Parameters

Various output waveforms shapes supported by VSSI

This device has 256 independently programmable output channels that can produce square wave. Various output waveforms can be generated using channel grouping (adding the output current of a subset of the channels together) as shown in Figures 13 and 14. By carefully program the timing, width, and amplitude of each square wave, the output waveform of the grouped channels is highly flexible. The generation of sine wave and triangle wave is shown below.

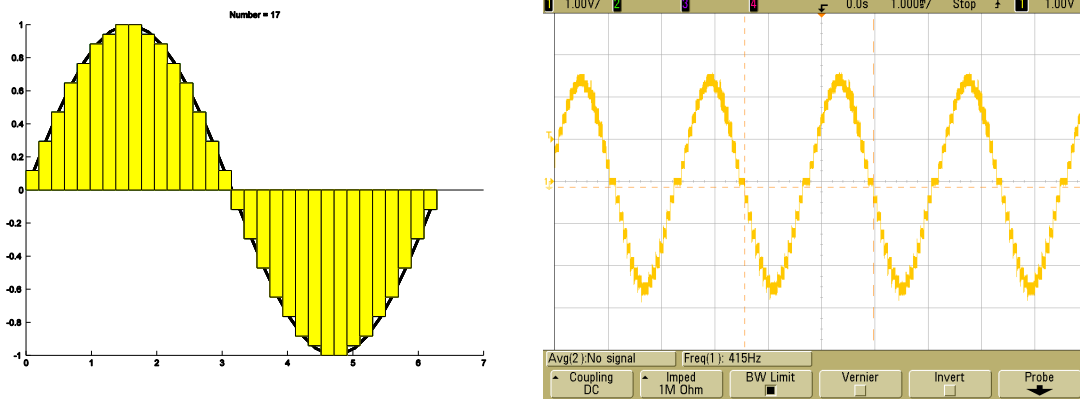


Figure 13. Sine wave generated by grouping 8 square wave channels. Left: simulation result; right; test result recorded from oscilloscope.

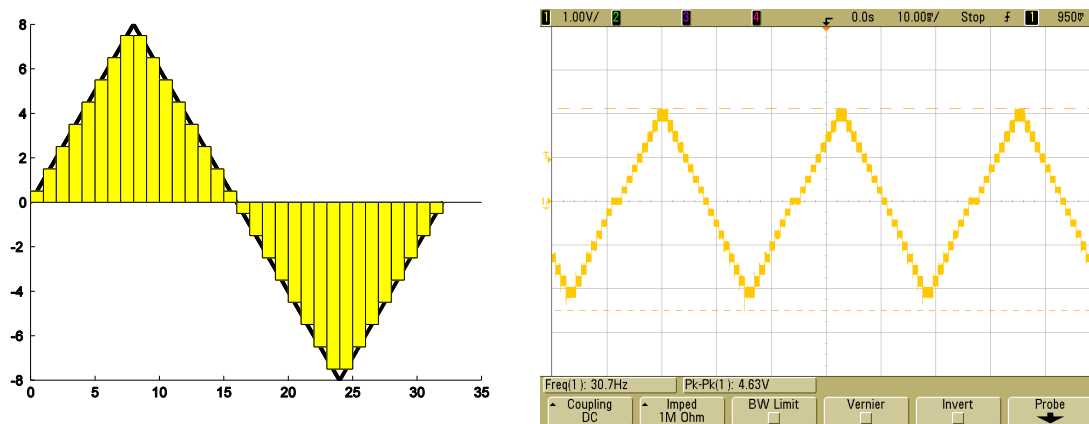


Figure 14. Triangle wave generated by grouping 8 square wave channels. Left: simulation result; right; test result recorded from oscilloscope.

Flexible multi-channel output

Precise and fine temporal *offsets* between any two channels can be programmed and faithfully produced by this device as illustrated in Figure 15. There are two ways to make the offset, through software timing or through hardware timing. In hardware timing mode, the offset value is programmed into the stimulator. Hardware counter is equipped in every output channel and controls the offset timing precisely. Each output channel can also be controlled by the commands sent from the software on-the-fly. This enables software to trigger the output and achieve the desired inter-channel offset. Either the hardware or software timing mode can achieve 20 μ s temporal resolution.

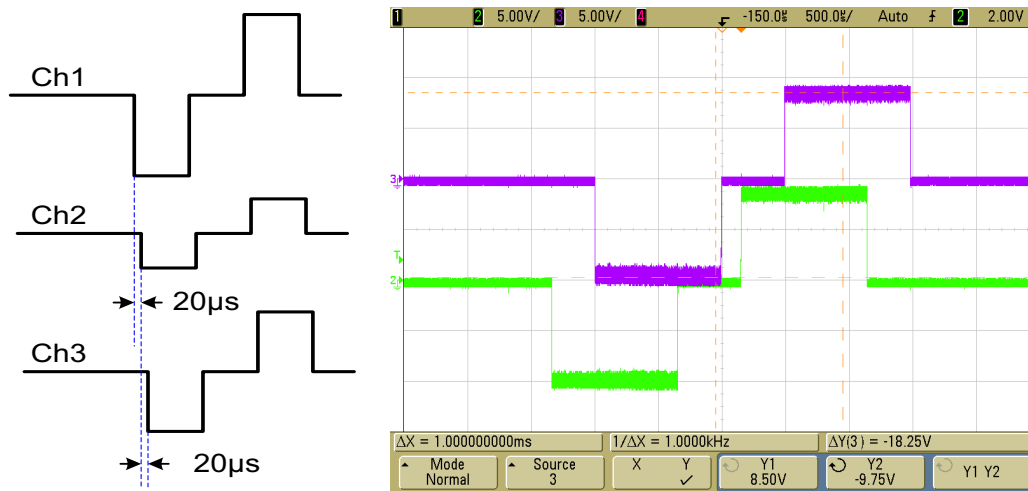


Figure 15. Each output channel is independently programmable, and the temporal offset can be as fine as $20\mu\text{s}$. Left: illustration of temporal offset between the stimuli generated by different output channels; right: test result recorded from oscilloscope.

Standardized interface ready for graphic user interface (GUI)

This device is connected to a computer with USB2.0 interface. With a complete C++ application programming interface (API) library, this stimulator can communicate with software and transfer data easily. These two features make it ready for any graphic user interface (GUI). Users can simply link the API into their existing GUI to configure the stimulation waveform, or build a GUI using popular software development tools such as Microsoft Visual Studio.

The setup of the VSSI prototyping system

This stimulator supports up to 256 output channels. A prototype device with fewer output channels is built for demonstration, as shown in the figures below. This device supports 16 square wave channels and two sine wave channels. Since the circuit is built with high-voltage transistors, the output compliance voltage is $\pm 10\text{V}$. This device is easy to operate, and it can be controlled by any computer with a USB2.0 interface. Figure 16 is a schematic design example of a 16-channel stimulation system. The specifications and features of this system is listed in Figure 17.

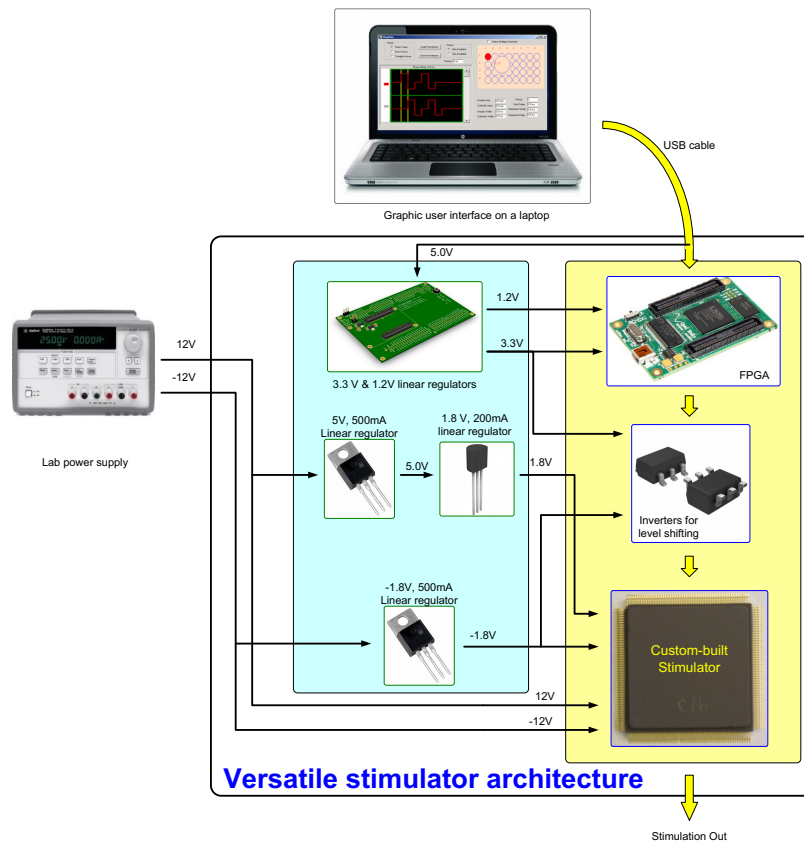
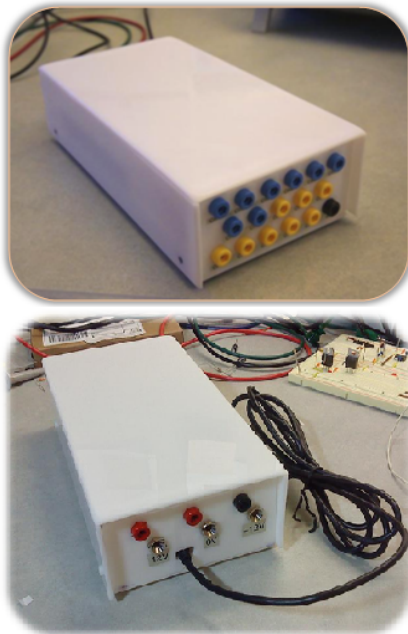


Figure 16. Schematic of the proof-of-concept prototype system. This system is built with a custom-designed stimulator chip and some commercial off-the-shelf components.

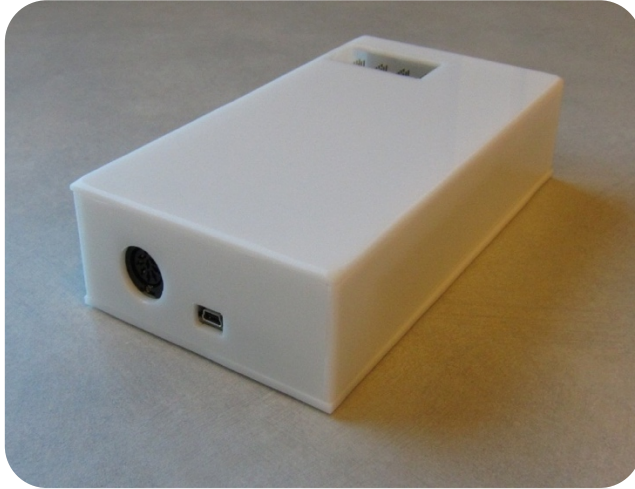


Parameters	Value
Device dimension	7" x 4.5" x 2"
Power source	$\pm 12V$
Power consumption (idle)	3mA (+12V); 17mA (-12V)
Power interface	Standard banana jack
Control interface	USB 2.0
Output channel number	16x square; 2x sine wave
Output connector	2mm banana jack
Square wave amplitude	Up to 500 μA
Sine wave amplitude	Up to 2.5mA

Figure 17. Pictures and the specifications of the prototype system. The system has been used at Dr. Eli Greenbaum's group at Oak Ridge National Lab. It has 16 square wave

output channels and 2 sine wave output channels. Note: The current amplitude for square wave actually could be $nx500\mu A$, where n is the number of electrodes grouped together.

Versatile stimulation system II (VSSII): 64-Channel system



Parameters	Value
Device dimension	7.75" x 4" x 2"
Power source	$\pm 12V, \pm 5V$
Power interface	8-pin DIN
Control interface	USB 2.0
Output channel number	64
Output connector	0.1" header
Square wave amplitude	Up to 500 μA

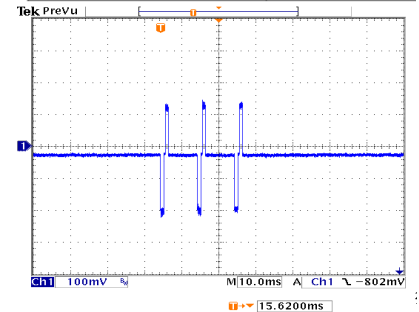


Figure 18. A compact 64-Ch. versatile stimulation system box with a USB 2.0. The system comes with hardware driver and end-user software GUI that allows user to specify stimulation pattern on each of the 64 channels.

Based on the success and usefulness of the previous VSSI, we built a higher number of channel system, versatile stimulation system II (VSSII) as shown in Figure 18, using a new IC to achieve 64 channels. The stimulation box has similar dimension as in VSSI but with a new IC it can provide 64 channels. It can generate monophasic or biphasic stimuli, single-pulse, pulse train or continuous pluses. Like VSSI, it is connected to a Windows workstation using standard USB2.0 cable and any of the 64 channels can be independently programmed. The software API and GUI were written in Visual C# which can be easily modify by the end-user to add certain functionality or feature that we have not included or yet developed.

We developed a user-friendly GUI as shown in Figure 19 that allows a user to specify stimulator parameters for each of the channels as desire. These parameters can be save or load from a file. Detail explanations of each of these buttons from the program panel are explained in Figure 20.

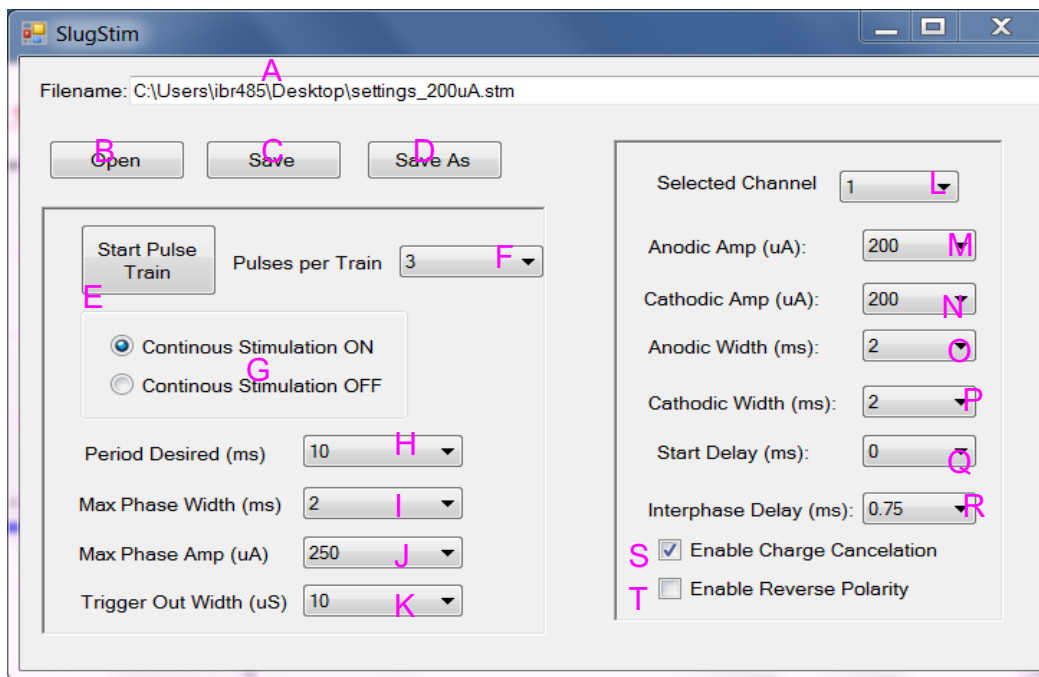


Figure 19. A screenshot of a user application GUI showing controllability of the software and versatile stimulation system hardware.

- A - Read only box displaying name of currently active config file.
- B - Allows user to open previously saved config file.
- C - Saves changes back to file currently open or prompts for new file.
- D - Prompts user to save config to a new file.

Figure 20. Details explanation of the buttons in the GUI program captured in Figure 10.

IV. The active team members in the project

- Prof. Wentai Liu (PI)
- Linh Hoang (Graduate Student)
- Kuanfu Chen (Graduate Student)
- Lao Jian (Graduate Student)
- Yu Han (Graduate Student)
- Yikai Lo (Graduate Student)
- Lewis Zheng (Graduate Student)
- Robby Kelbley (Graduate Student)
- Benz Gong (Undergraduate Student)

V. Deliverables:

Book chapters:

1. M. Chae, Z. Yang, and W. Liu, "Microelectronics for recording, stimulation and wireless telemetry," *Implantable Neural Prostheses: Part II. Techniques and Engineering Approaches*, Springer New York, ISBN: 978-0-387-98119-2, pages 253-330, 2010.
2. Z. Yang, Y. Han, L. Hoang, Y. Lo, K. Chen, J. Lao, and W. Liu, "Wireless Power and Data Telemetry System for Implantable and Wearable Electronics," *Wireless Body Area Networks: Technology, Implementation and Applications*, Pan Stanford Publishing, 2010.
3. E. Basham, Z. Yang, N. Tchomodanov, and W. Liu, "In vitro systems for magnetic stimulation of neural tissue," book chapter in *Implantable Neural Prostheses: Part I. Devices and Applications* (Eds: E.Greenbaum and D. Zhou), Springer New York, ISSN: 1618-7210, pages 293-351, 2009.
4. W. Liu, M. Sivaprakasam, G. Wang, M. Zhou, and M. S. Humayun, "Semiconductor based Implantable Prosthetic Devices," *Wiley Handbook of Biomedical Engineering*, John Wiley and Sons. (Invited chapter), 2008
5. W. Liu, M. Sivaprakasam, G. Wang, M. Zhou, J. D. Weiland, and M. S. Humayun, "Challenges in realizing a Chronic High Resolution Artificial Sight Device," *Artificial Sight*, M. S. Humayun, J. D. Weiland, E. Greenbaum, Eds. *Biological and Medical Physics/Biomedical Engineering Series*, New York: Springer. (Invited), 2008
6. W. Liu, M. Sivaprakasam, G. Wang, M. Zhou, J. D. Weiland, and M. S. Humayun, "Development of an Intraocular Prosthesis to Benefit the Visually Impaired," *Visual Prosthetics and Ophthalmic Devices: New Hope in Sight*, New Jersey: Humana Press, Inc. (Invited), 2007

Journal papers:

1. W. Liu and Z. Yang, "Neural prosthetic devices and nanotechnology," *Nanotechnology II: Global Prospects*, 2011.
2. K. Chen, Z. Yang, L. Hoang, J. Weiland, M. Humayun, and W. Liu, "An Integrated 256-Channel Epiretinal Prosthesis," *Journal of Solid-State Circuits (JSSC)*, Volume:45, pages 1946-1956, Sep. 2010.
3. Z. Yang, Q. Zhao, and W. Liu, "Neural Signal Classification Using a Simplified Feature Set with Energy Based Non-parametric Clustering," *Neurocomputing*, Elsevier, Volume: 73, pages 412-422, Dec. 2009.
4. Z. Yang, Q. Zhao, and W. Liu, "Improving Spike Separation Using Waveform Derivative," *Journal of Neural Engineering (JNE)*, doi: 10.1088/1741-2560/6/4/046006, Aug. 2009.
5. M. Chae, W. Liu, M. Sivaprakasam "Design Optimization for Integrated Neural Recording Systems," *IEEE J. Solid-State Circuits*, vol. 43. no. 9, pp. 1931-1939, Sep. 2008.
6. M. Zhou, M. R. Yuce, W. Liu, "A Non-Coherent DPSK Data Receiver with Interference Cancellation for Dual-Band Transcutaneous Telemetries," *IEEE Journal of Solid-State Circuits*, Volume: 43, No. 9, Sep. 2008.
7. Z. Yang, W. Liu, E. Basham, "Inductor Modeling in Wireless Links for Implantable Electronics", *IEEE transactions on Magnetics*, Volume: 43, No. 10. Oct. 2007
8. W. Liu and M. Sivaprakasam, "Challenges for Integrated Circuits in Implantable Devices," Volume: 20, *Future Fab International*, Jan. 2006.

9. W. Liu, G. Wang, J. D. Weiland, and M. S. Humayun, "Architecture Tradeoffs in High Density Micro-stimulators for Retinal Prosthesis," IEEE Transactions on Circuits and Systems – I (Special Issue on Biomedical Circuits and Systems) Volume: 52, Pages: 2629 – 2641, Dec. 2005.
10. G. Wang, W. Liu, M. Sivaprakasam, and G. A. Kendir, "Design and Analysis of an Adaptive Transcutaneous Power Telemetry for Biomedical Implants," IEEE Transactions on Circuits and Systems – I, Volume: 52, Oct. 2005.
11. W. Liu, M. Sivaprakasam, G. Wang, M. Zhou, J. Granacki, J. LaCoss, and J. Wills, "Microelectronics Design for Implantable Wireless Biomimetic Microelectronic Systems," IEEE Engineering in Medicine and Biology Magazine, Volume: 24, Pages: 66 – 74, Sep. 2005. (Invited)
12. J. D. Weiland, W. Liu and M. Humayun, "Retinal Prosthesis," Annual Review of Biomedical Engineering, Volume: 7, Aug. 2005. (Invited)
13. G. A. Kendir, W. Liu, G. Wang, M. Sivaprakasam, R. Bashirullah, M. S. Humayun, and J. D. Weiland, "An Optimal Design Methodology for Inductive Power Link with Class-E Amplifier," IEEE Transactions on Circuits and Systems – I, Volume: 52, Pages: 857 – 866, May 2005.
14. M. Sivaprakasam, W. Liu, M. S. Humayun, and J. D. Weiland, "A Variable Range Bi-Phasic Current Stimulus Driver Circuitry for an Implantable Retinal Prosthetic Device," IEEE Journal of Solid-State Circuits, Volume: 40, Pages: 763 – 771, Mar. 2005.

Ph.D. Theses:

1. Kuan Fu Chen, An Integrated 256-Channel Epiretinal Prosthesis, 2011
2. Linh Hoang, Digital architecture for high channel count micro-simulator: hardware and software co-design, 2011
3. Eric J. Basham, Platform Development for In Vitro Study of Magnetically Induced Excitation of Neural Tissue, 2010
4. Zhi Yang, Neural spike feature extraction and data classification, 2010
5. Mingcui Zhou, Data telemetry with interference cancellation for retinal prosthesis, 2007
6. Mohanasankar Sivaprakasam, High density micro-stimulators for retinal prosthesis, 2006
7. Guoxing Wang, Wireless power and data telemetry for retinal prosthesis, 2006

MS Theses:

1. Zhi Yang, Inductor modeling for biomedical telemetry, 2007
2. Linh Hoang, Digital architecture for high resolution micro-simulator for retinal prosthesis, 2007

Awards:

1. RD-100 Editor Award, Nov. 2009
2. Popular Mechanics Breakthrough Invention Award, Oct. 2010

Invention disclosures:

1. "Active circuits under pad (CUP) structure to reduce the implatable device size which needs the High Density Electrodes", (with J. Kim, M. S. Chae, W. Liu) UCSC invention disclosure, July 2008

2. "Integrated high voltage stimulus driver with wireless power telemetry for biomedical applications", (with J. Kim, M. S. Chae, W. Liu, M. Sivaprakasam) UCSC invention disclosure, Apr. 2008
3. "System architectures and tradeoffs involved in the design of high density retinal stimulators" (with W. Liu, G. Wang), UCSC invention disclosure, Sep. 2005.
4. "Method and theory of creating virtual electrodes for stimulation in a retinal prosthetic implant" (with W. Liu, Z. Yang), UCSC invention disclosure, July 2005.
5. "Communication protocol for wireless transmission of data to an implantable retinal prosthetic device," (with W. Liu), UCSC invention disclosure, Jan. 2005, UC Case No. 2005-389-1.

News and Interviews:

1. Santa Cruz Good Times ran a cover story about innovative research at UCSC featuring electrical engineer Wentai Liu, Jan. 5 2010
2. Science Today, "An artificial retina recognized for its innovation," Oct. 05, 2009. <http://www.ucop.edu/sciencetoday/article/22039>
3. Science Today, "A microchip that restores eyesight to patients with degenerative diseases," May 11, 2009. <http://www.ucop.edu/sciencetoday/article/21137>
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VI. Major accomplishments at University of California, Santa Cruz

2007:

Design and fabricate the 1Mbps Differential Phase Shift Key (DPSK) data telemetry IC
Develop data telemetry prototype system
Develop the power telemetry prototype system
Setup and test the dual-band power and data telemetry prototypes together

2008:

Design, fabricate, and test the high compliance voltage test chip of stimulator and digital controller with TSMC 0.18um high-voltage CMOS process
Design, fabricate, and test the new 2Mbps DPSK chip (at National Semiconductor 0.35um CMOS process) for data telemetry
Design and layout of the new 2Mbps DPSK chip (at TSMC 0.18um high-voltage CMOS process) for data telemetry

2009:

Design and layout of the integrated 256-channel high compliance voltage stimulator IC (Retina-8.0) using TSMC 0.18um high-voltage CMOS process
Fabricate Retina-8.0 at TSMC
Design the test board for Retina-8.0
Test and characterize Retina-8.0, including DPSK data receiver, digital controller, and stimulator pixel

2010:

Design, analysis, simulation, and layout of the on-chip multiple-voltage Timing-Controlled Rectifier (TCR) and regulator
Characterization and measurement of Argonne National Lab’s capacitors
Assemble and demonstrate a system consisting of camera, power and data transmitters, dual-band coils, Retina-8.0, and LED display board
Develop and assemble a hardware-software co-design of 16-channel high-voltage stimulator with versatile waveforms, delivered to Oakridge National Lab (ORNL)

2011:

Develop both hardware and software and then assemble a prototype system that is capable of support 64 channel stimulator with independent programmable stimulator parameters – amplitude, frequency, width, and off-set.