Efficient Heat Removal from Power Semiconductor Devices Using Carbon Nanotube Arrays and Graphene (165705)
or
Thermal Management Solutions Via Carbon Nanomaterials

SAND2016-1476PE

1100: Mike Siegal (PI), Carlos Gutierrez (PM), Caitlin Rochford, Thomas Beechem, Ryan Shaffer

1700: Graham Yelton, Steven Limmer, Steve Howell, Bob Kaplar, Jack Flicker and Nathan Young

Univ. New Mexico: graduate students

Georgia Tech: Prof. Baratunde Cola

Univ. Illinois (UC): Prof. Nenad Miljkovic

Cambridge University: Profs. Milne and Ferrari

Outstanding Post-Docs and Student Interns

Sandia Post-Docs

Caitlin Rochford
Siegal, 1124
MTS, 5644
Microsystems Assessments

Jack Flicker
Kaplar, 1768
MTS, 1768
Rad Hard CMOS

Steven Limmer
Yelton, 1728
MTS, 1728
Now at Energizer Battery

Sandia Interns UNM M.S. students

Luke Yates
Beechem, 1114
Ph.D. Student
Georgia Tech

Ryan Shaffer
Beechem, 1124
MTS, 1719
MEMS Technologies

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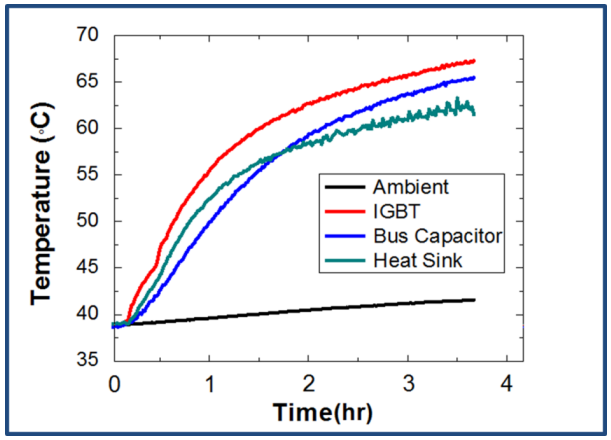
Objectives and Program Relevance

The Problem: Heat Removal from Existing TIMs Is Not Good Enough

Example: Temperature Rise of IGBT in Typical PV Inverter

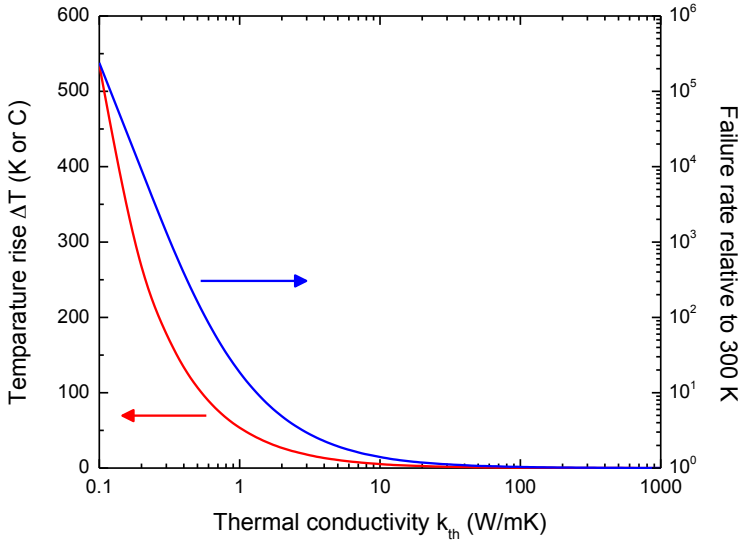


The insulated gate bipolar transistor, IGBT (i.e. power electronics) is a hot element in a typical photovoltaic inverter system.

Most failure mechanisms follow an Arrhenius relationship for the failure rate acceleration factor:

$AF = \exp(-E_A/kT)$

E.g. ~ 2 KW IGBT dissipates 535 W of heat.



- Both temperature rise and device failure rate increase with the use of low thermal conductivity TIM materials.
- Device failure rates are a problem when TIM $\kappa < 20$ W/m•K, and are a serious problem with TIM $\kappa \sim 1$ W/m•K.

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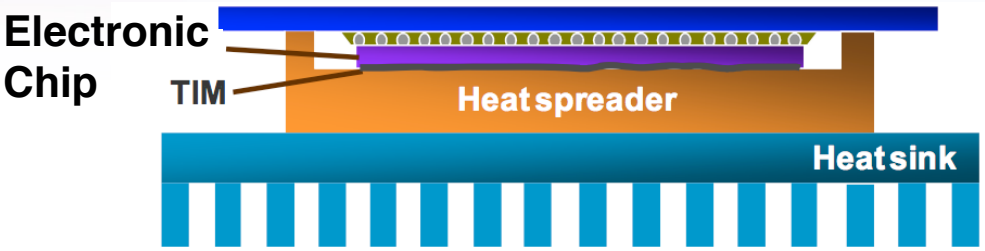
Revolutionary Thermal Interface Materials

Conventional TIM = Thermal Bottleneck!

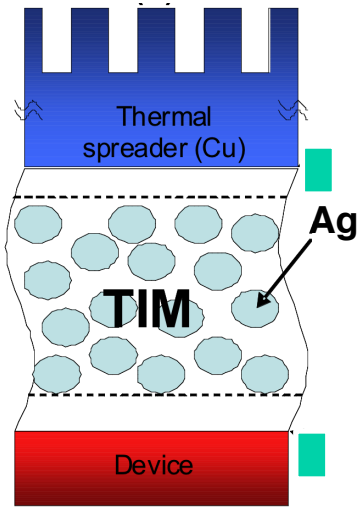


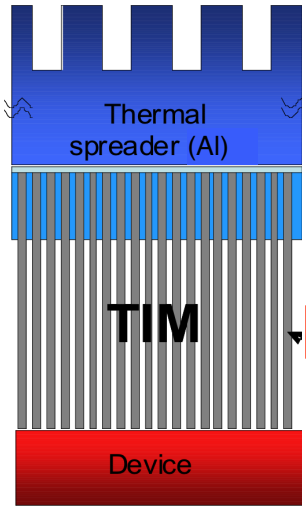
Removing heat generated by high-power electronics devices is often a limiting factor in system performance.

Thermal conductivity

Ag	420 W/m·K
Cu	401 W/m·K
Al	237 W/m·K
Au	317 W/m·K
Si	148 W/m·K
In	82 W/m·K
Epoxy	0.23 W/m·K
Diamond	90 – 2310 W/m·K
Nanotubes	10 – 3000 W/m·K
Graphene	200 – 5000 W/m·K

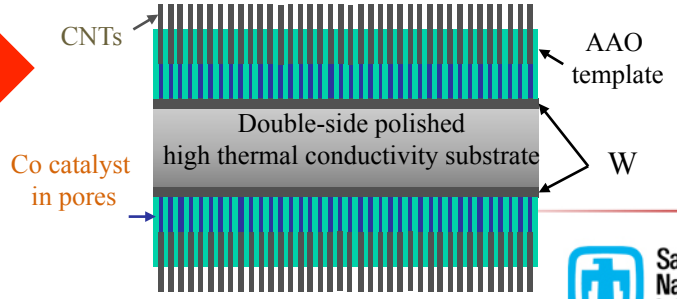
Replacing SOA (Ag Paste) with CNT TIMs





Unfortunately, the thermal conductivity of filled epoxy is dominated by percolation through the epoxy, resulting in values ≤ 1 W/m·K.

Double-Sided CNT TIM



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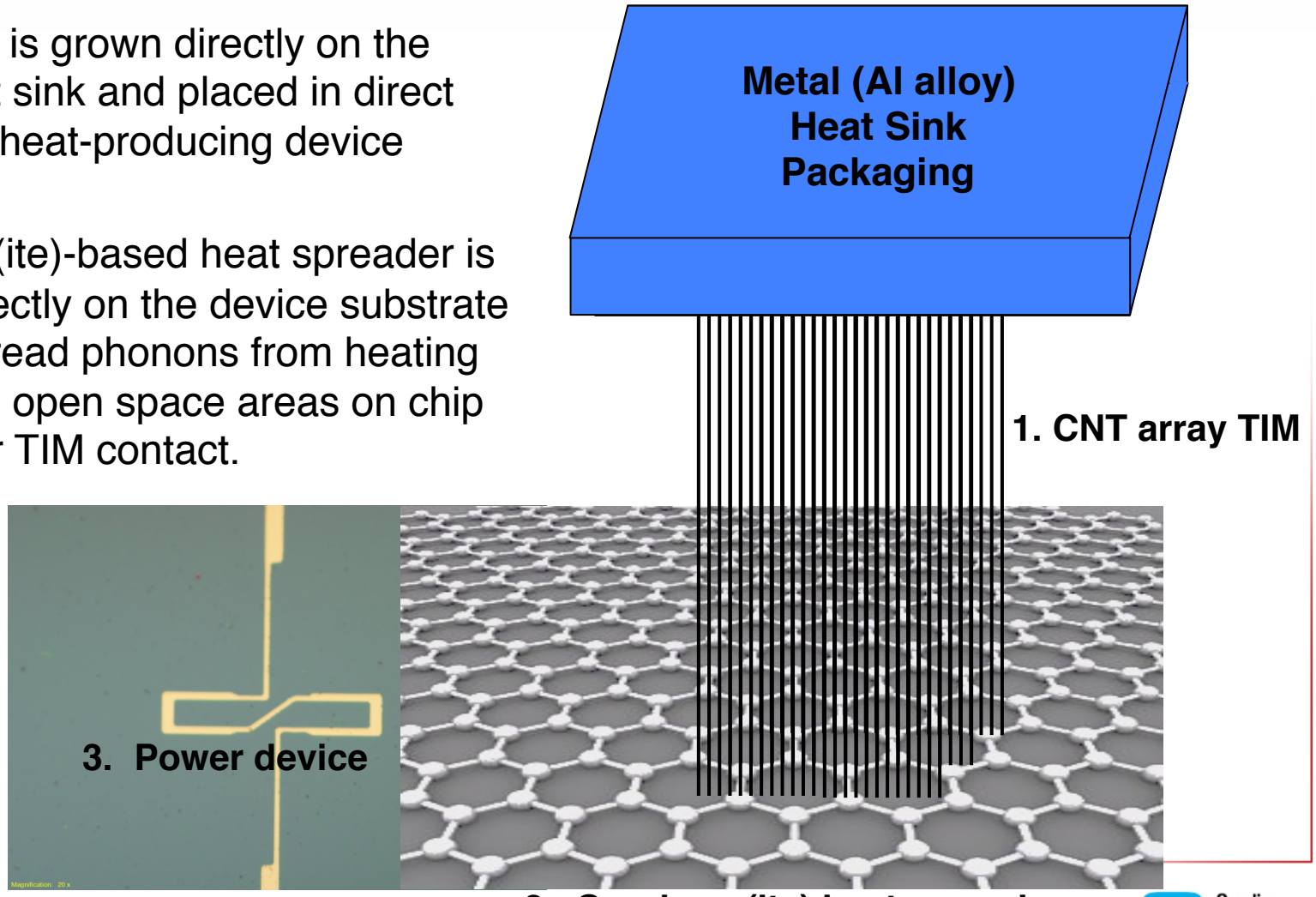
Basic Concept for CNT-Based TIM

(not drawn to scale)

1. CNT array is grown directly on the metal heat sink and placed in direct contact to heat-producing device substrate.
2. Graphene(ite)-based heat spreader is placed directly on the device substrate to help spread phonons from heating element to open space areas on chip surface for TIM contact.



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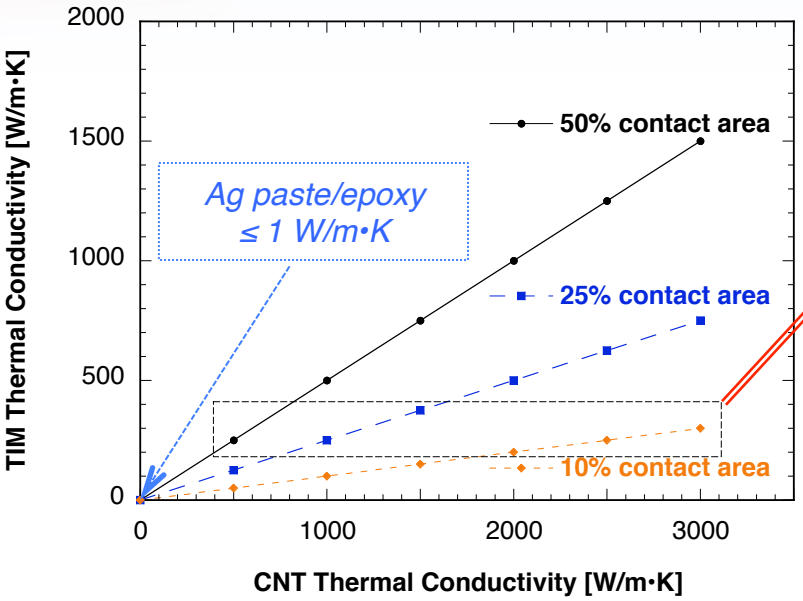
Required Properties for CNT TIMs

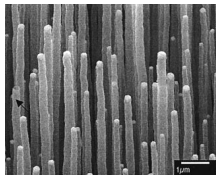


Goal: **eliminate TIM thermal bottleneck and improve performance *by factors of 10 – 500x without even full optimization!***

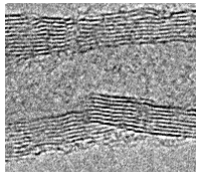
For optimal CNT-TIM performance:

1. No adhesives in thermal path.
2. High-crystalline quality CNTs to minimize phonon scattering for high thermal conductivity.
3. High CNT density to increase number of thermal pathways – NO ENTANGLEMENT!
4. Planarized array tips to maximize thermal contacts to hot device surfaces.

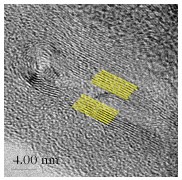
~ CNT Quality →



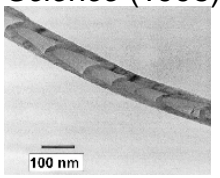
Siegal et al. *Science* (1998)



Siegal, Huang (unpublished)



Siegal et al. *J. Phys. Chem.* (2010)

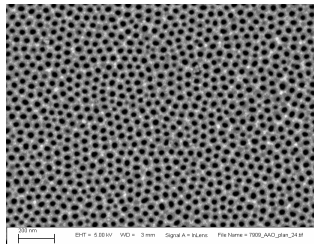


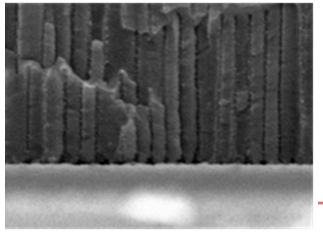
Lee et al, *Chem Phys Lett* (2000)

Higher growth rate *plasma-enhanced* CVD

Slower growth rate *thermal* CVD

Sandia Approach Uses Nanopore Templates on Substrate-of-Choice





5 – 300 nm diameter control

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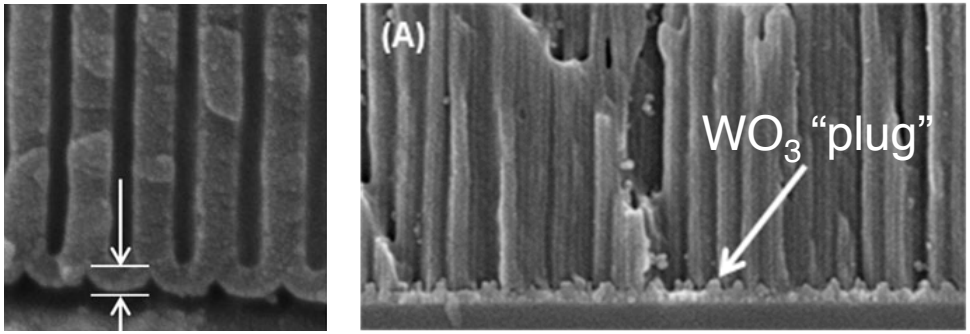
Vertical Orientation of CNT Arrays via Nanopore Templates and Thermal CVD Growth

Anodized Aluminum Oxide (AAO) Nanopore Templates on Substrates

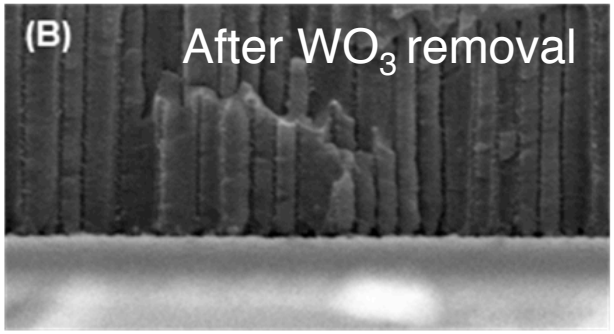
Sputter low-stress, mirror-smooth Nd-doped Al films onto thermal sink substrate.

1 to 10's *μ*m Nd-doped Al	**forms nanopore template following anodization**
100 nm W	**sacrificial W layer that prevents Al-oxide 'crud' at pore bottoms**
High Thermal Conductivity Substrate	**Al, Al-alloy, Si, sapphire (depends on application)**

no W layer **with W layer**



Chemically-selective etching (pH 7 phosphate buffer solution) of sacrificial W-oxide "valve" layer leaves a conductive W layer at pore bottoms, *critical for electro-chemical deposition of Co-metal catalysts for CNT growth.*



Limmer et al, *JES*, **159**, D235 (2012)
Rochford et al, *JMR*, **30**, 316 (2015)

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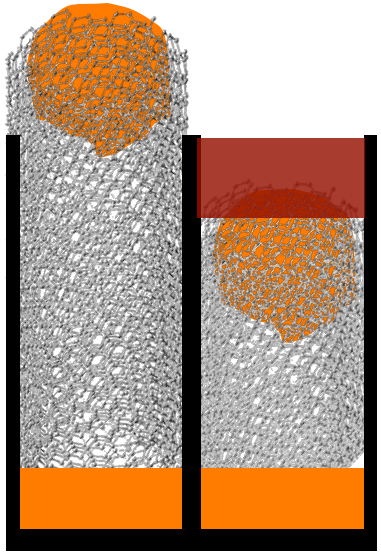
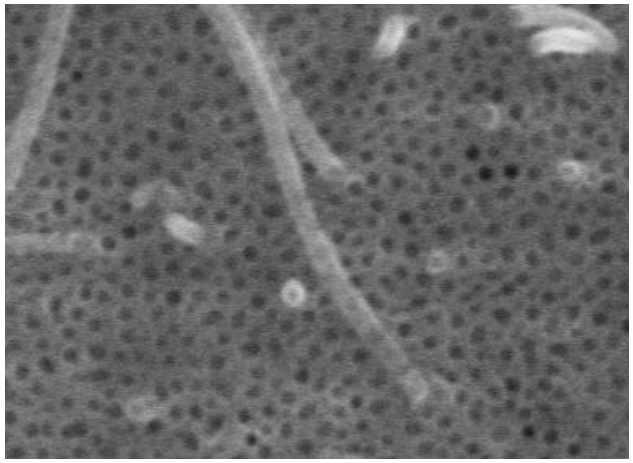
Optimizing CNT Site Density in Nanopores

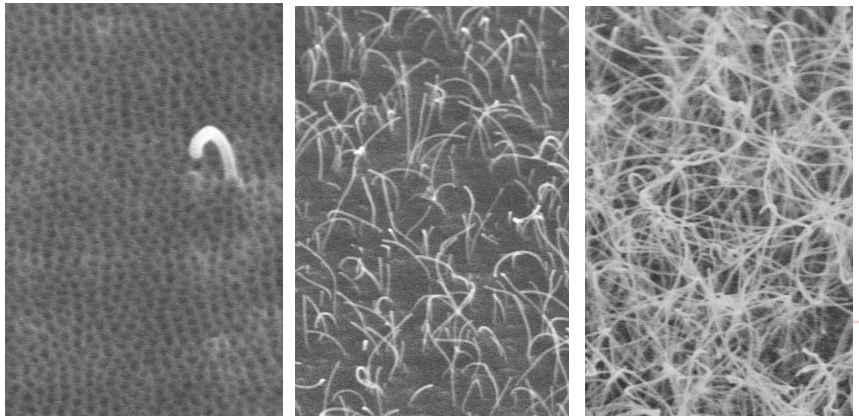
AAO catalyzes C_2H_2 decomposition and can plug the pore openings with amorphous-carbon, preventing the emergence of CNTs.





Most nanopores are dull gray, **while a few appear much darker.** The gray pores are filled with a-C that preventing CNTs from growing 'up and out'.

Competition exists between CNT and a-C growth. Need short distance between top of catalyst and template surface, *i.e. small aspect ratios.*



Rochford et al, *JMR*, **30**, 316 (2015)

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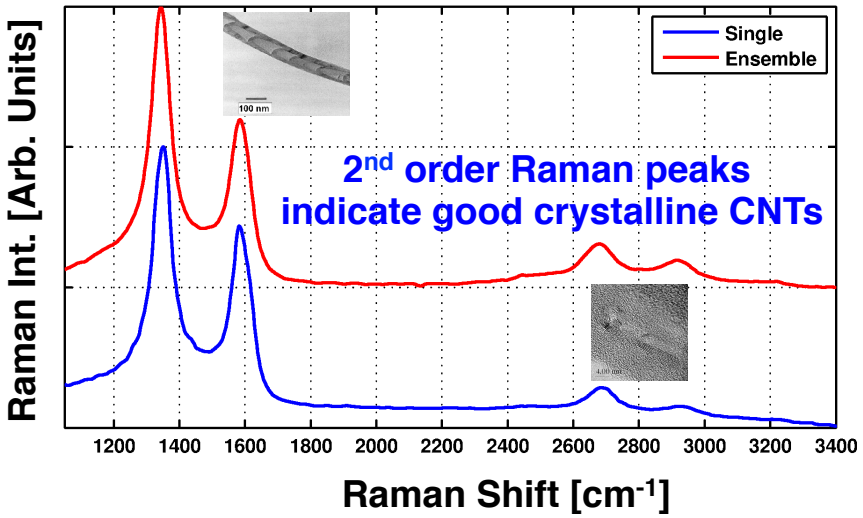
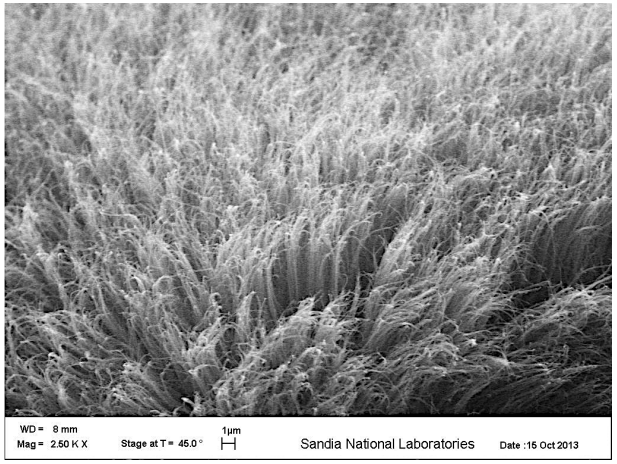
Achieving Required Properties for CNT TIMs

High Crystalline CNTs = High Thermal Conductivity CNTs



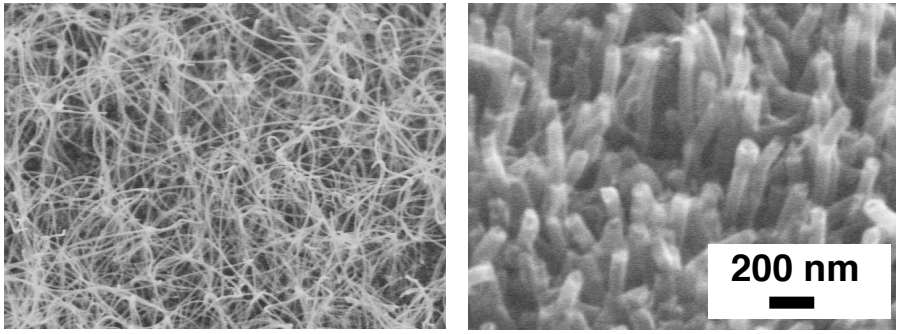
High CNT Areal Density = Large # of Thermal Pathways



- Literature SOA ≤ 5% areal coverage (due to entanglement, poor nucleation)
- **Sandia SOA ~ 40% area coverage 10^{10} CNTs/cm^2 w/ 75 nm diameters.** ***(due to use of nanopore templates)***

Thermal properties of CNT-TIM arrays still need to be confirmed,
in collaboration with Prof. Cola – Georgia Tech

Planarization = Higher Contact Area



Sandia SOA: from many µm's to tens of nm's

Rochford et al, *J. Mater. Res.* (2015)

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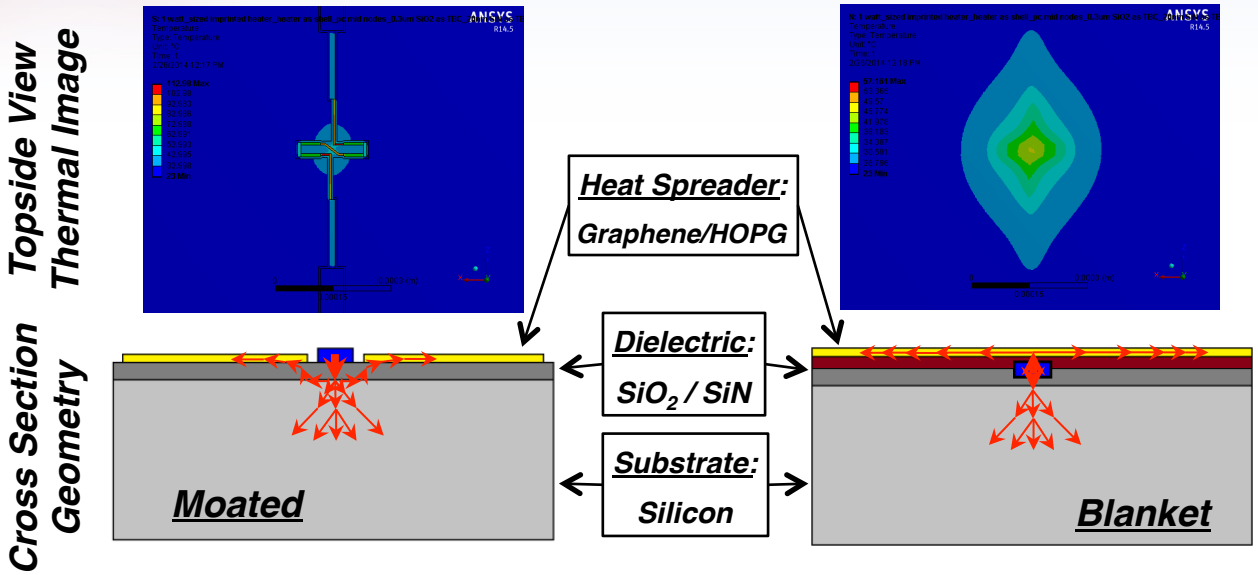
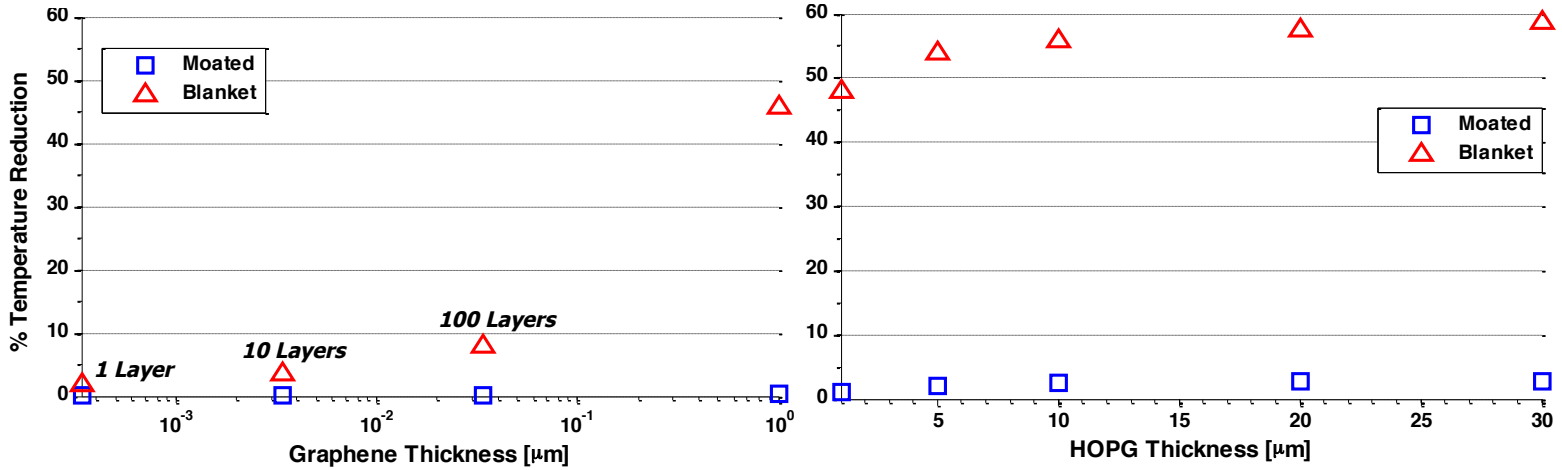
Graphene(ite) Heat Spreader



Takeaways:

- Single to few layer graphene insufficient heat spreader.
- Direct path from heat generation to spreader necessary for significant reduction of junction temperature.
- Placing a thick HOPG layer over the thermally-active region models to be a very effective thermal solution.



- Cooling increases with heat spreader thickness.
- *Using a HOPG heat spreader can greatly improve the cooling capability of a TIM by itself.*

Beechem, Shaffer (UNM MS Thesis)

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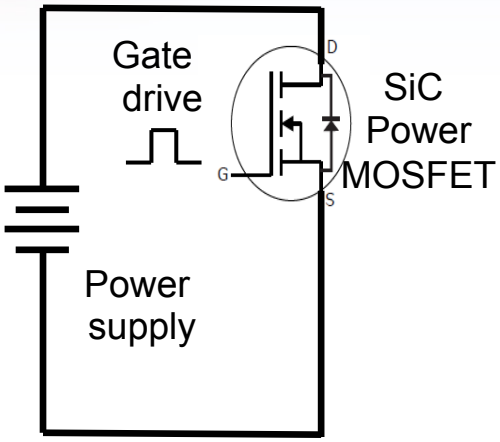
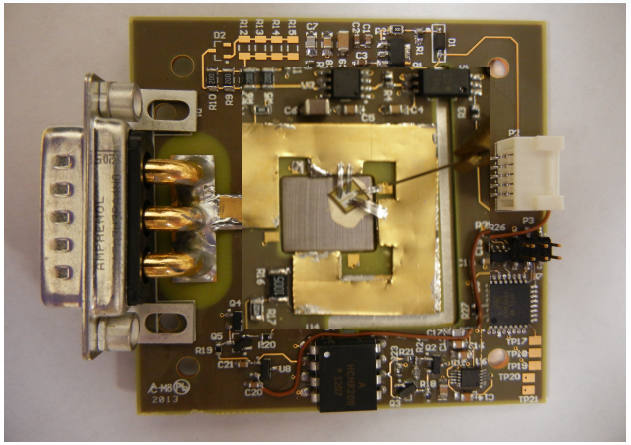
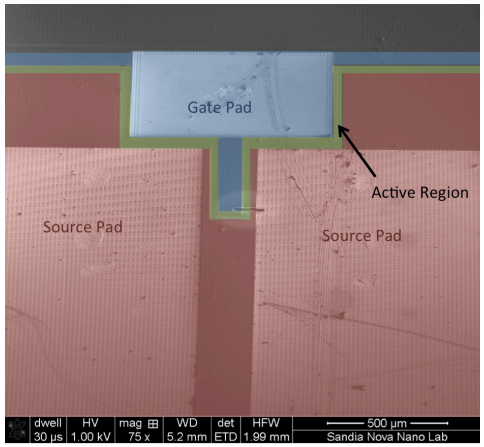
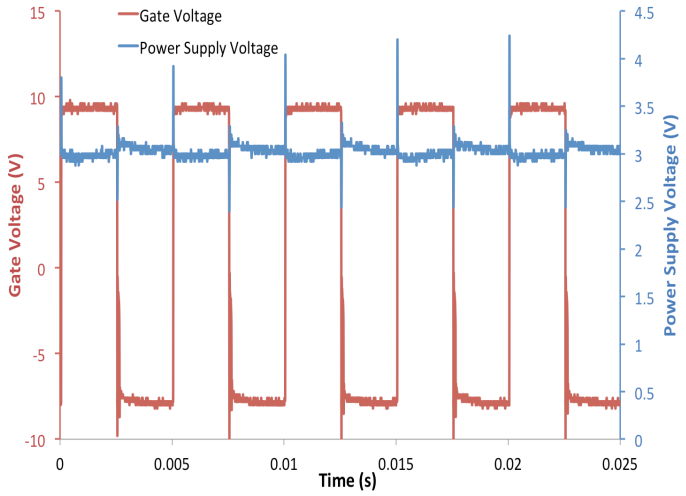
Using Test Platform to Measure TIM Efficiency









- Quantifying effective of Ag-paste TIM using test structure with commercial SiC power device.
- Conduction losses lead to heating (minimal switching loss here, since no high-voltage blocking state).
- Drive current through MOSFET via power supply (blue trace) and gate drive (red trace).
- Measure temperature increase of real device (commercially available SiC MOSFET) via IR-thermography.

Young, Flicker, Kaplar

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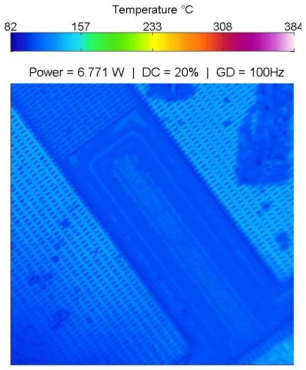
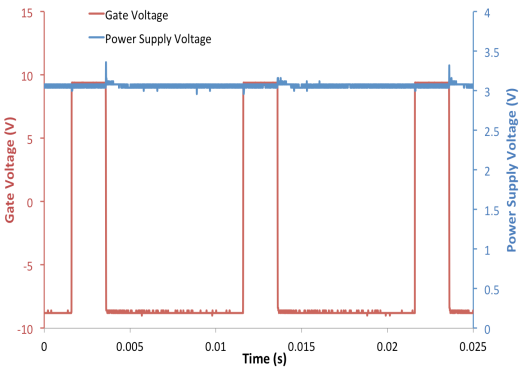
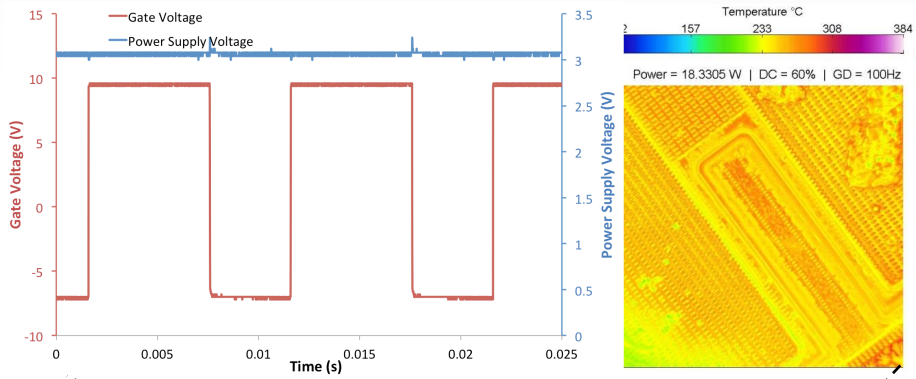
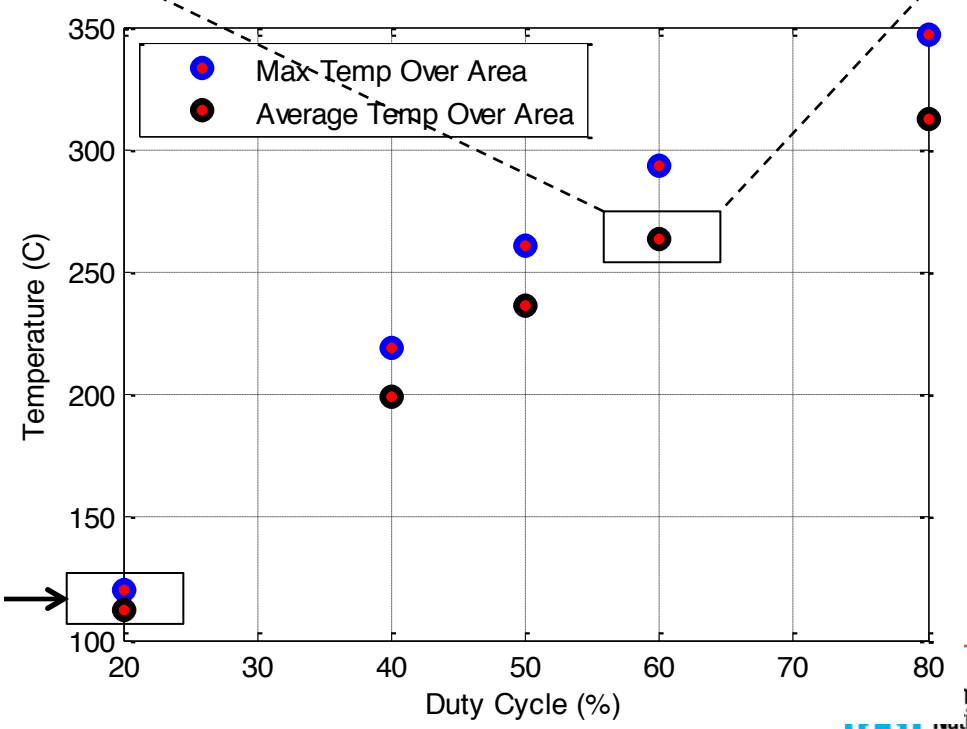
Measuring Ag-Paste Efficiency vs. Duty Cycle

- Surface temperature of device monitored as a function of duty cycle (% of time in on-state).
- Conduction losses (and heating) expected to vary linearly with duty cycle.
- Real temperature increase measured is approximately linear, as expected.









Beechem, Shaffer, Young, Flicker, Kaplar

Laboratories

Facilities and Capabilities Used

IMRL, 897

- Chemical vapor deposition lab for carbon nanotubes
- Low-stress thin film metal deposition lab
- Electrochemical anodization and deposition lab
- Thermal and optical measurement lab
- Scanning electron microscopy

MESA, 858

- Device packaging/testing facility

PETL, 701

- Graphene lab
- Conductive atomic force microscopy
- Scanning thermal microscopy
- Field-emission scanning electron microscopy

unique to Sandia:
having these facilities in a single Division, run by recognized experts.

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Publications, Presentations, Proposals, Metrics

Publications:

1. Rochford, Limmer, Howell, Beechem, and Siegal, "Planarized arrays of aligned, untangled, multiwall carbon nanotubes with Ohmic back contacts," *J. Mater. Res.* **30**, 315 (2015).
2. R. Shaffer, "Evaluation of Top-Side Thermal Solutions for Hot Spot Management of Microelectronics," M.S. Thesis (w/Distinction), Univ. of New Mexico, Fall 2015.
3. Choi, Peake, Keeler, Geib, Briggs, Clevenger, Patrizi, Klem, Tauke-Pedretti, Shaffer, Beecham and Nordquist, "Thermal design and characterization of hetergeneously integrated InGaP/GaAs HBTs," Components, Packaging and Manufacturing Technol. (submitted).
4. Shaffer, Howell, Moorman and Beechem, "Volumetric averaging of infrared thermography," Rev. of Sci. Instr. (in progress).
5. Siegal, Rochford and Yelton, "Aligned CNT arrays for thermal interfaces," (in progress).
6. Siegal, Yelton, and Cola, "Thermal conductivity of carbon nanotube arrays," (in progress).
7. Howell, Siegal, Rochford and Yelton, "Scanning thermal microscopy of vertically-aligned carbon nanotubes,"(in progress).
8. Shaffer, Howell, Moorman, McDonald and Beechem, "Thickness dependence of carbon-based top-side thermal solutions," (in progress).

Presentations:

1. Invited: M. P. Siegal, "Nanomaterial strategies for thermal cooling", Colloquium at Cambridge University, Aug. 7, 2015.
2. Siegal, Rochford, Yelton, Beechem and Howell, "Toward carbon nanotube based thermal interface materials," 227th Electrochemical Soc. Meeting, Chicago, IL, May 2015.
3. Rochford, Siegal, Beechem, Howell and Yelton, "Improving structure and performance of CNT thermal interface materials," 2015 Spring MRS Meeting, San Francisco, CA, April 2015.
4. Rochford, Limmer, Howell, Beechem and Siegal, "Toward CNT-based TIMs," 2014 Fall MRS Meeting, Boston, MA, Nov. 2014.
5. Young, Shaffer, Flicker, and Kaplar, "Reworkable power module for low thermal resistance," 2014 IMAPS Advanced Technology Workshop on Thermal Management, Los Gatos, CA, Oct. 2014.
6. Rochford, Siegal, Limmer and Beechem, "Planarized untangled CNT arrays," 2014 Spring MRS Meeting, San Francisco, CA, April 2014.
7. Beechem, Howell, Moorman, Yates and McDonald, "Graphene based heat spreaders: comparing layer number with thermal performance, ASME 2013 Summer Heat Transfer Conference, July 2013.
8. Yates, Beechem, Howell, Hamilton, Moorman and McDonald, "Graphene-based heat spreaders," NM-AVS Spring Symposium, May 1013.
9. Rochford, Siegal, Beechem and Provencio, "CNT growth and structure at low growth temperatures," 2013 Spring MRS, San Francisco, CA, April 2013.

External Collaborations:

- Prof. Baratunde Cola, *Georgia Tech University*
- Prof. Nenad Miljkovic, *University of Illinois – UC*
- Profs. William Milne and Andrea Ferrari, *University of Cambridge*

Intellectual Property:

- SD-12323, Siegal, Beechem and Howell, "Carbon nanomaterials for thermal management," 2012.
- SD-12805, Siegal, Yelton, Limmer and Rochford, "Carbon nanotube based thermal interface materials," 2013.
- SD-13593, Beechem and Shaffer, "Simulating IR thermography physics to approximate measurement errors," 2015.
- SD-13659, Beechem, Forest and Shaffer, "Infrared contrast imaging device for containment detection," 2015.

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Accomplishments and Significance/Impact

- **TIM:** Progress toward high density, planarized arrays of high-quality CNTs.
  - 1st demonstration of high-density, untangled CNT arrays with ~ 40% surface coverage.
  - 1st demonstration of planarized CNT arrays, critical to achieving high contact area.
  - Potential remains to improve TIM SOA by 1 – 2 orders of magnitude.
  - Success will impact power electronics (GC, RC, NW, WFO-OGA, WFO-Industry, etc.)
- **Heat Spreader:** Modeling/experiments show that HOPG can greatly improve TIM performance.
  - Spreading layer must be sufficiently thick to carry high phonon density.
  - Cooling can be greatly improved whenever "blanket" coverage over a heat-producing element is allowable.
- **Power device:** TIM test platform completed.
  - *demonstrated utility by testing SiC MOSFET power device using SOA Ag-paste TIM.*
- **Collaborations:** CNT-TIM work will continue via collaborations with
  - *Georgia Tech (Prof. Cola) to measure full array thermal properties*
  - *UIUC (Prof. Miklovic) to study TIM effectiveness at system level w/WBG power devices.*
  - *Cambridge University (Profs. Milne and Ferrari) to study high-power graphene device performance with CNT-TIMs for improved cooling.*

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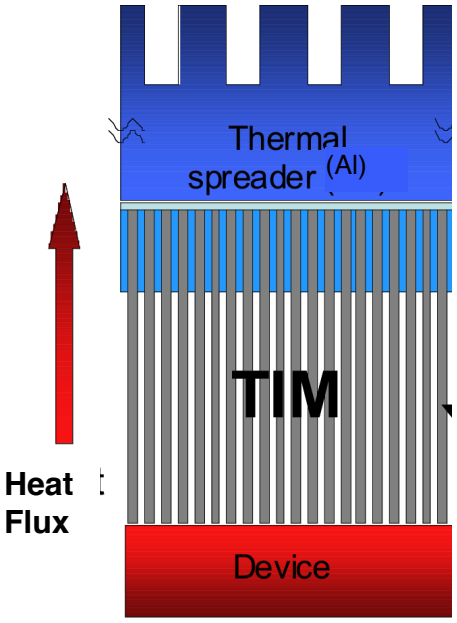
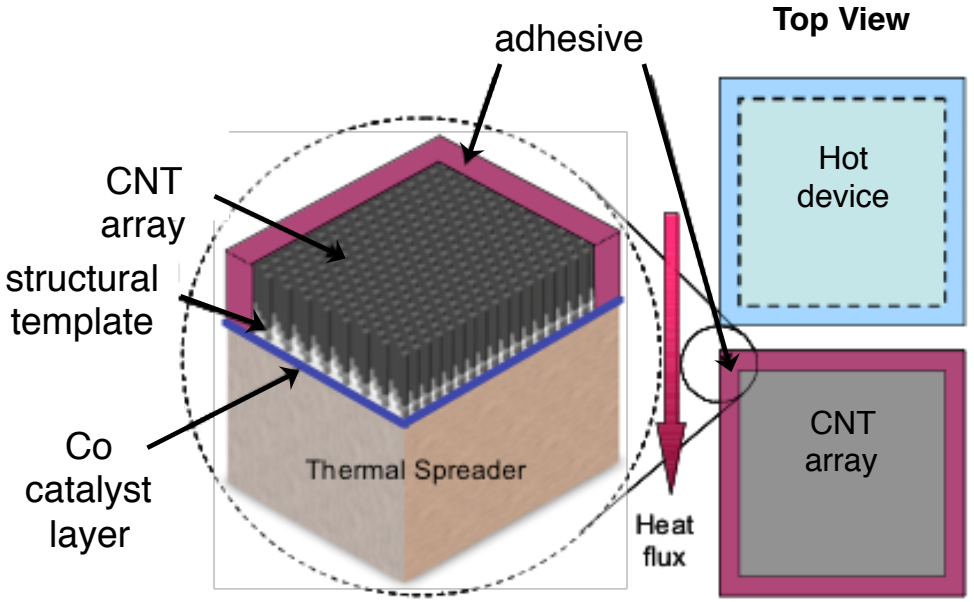
Additional Slides

Basic Design for CNT TIMs





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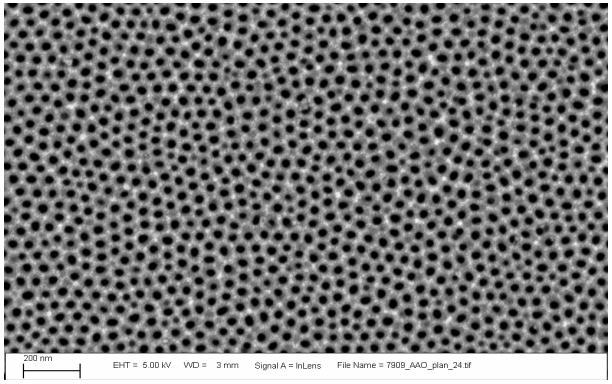
Vertical Orientation of CNT Arrays via Nanopore Templates and Thermal CVD Growth

Anodized Aluminum Oxide (AAO) Nanopore Templates on Substrates

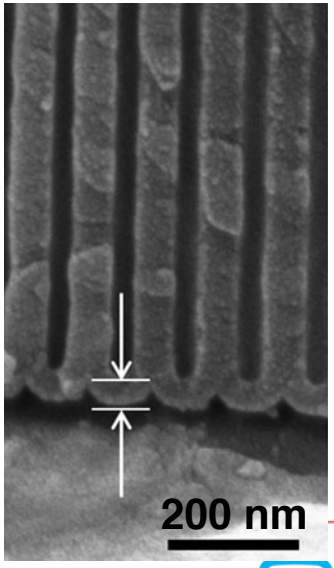
Sputter low-stress, mirror-smooth Nd-doped Al films onto thermal sink substrate.



1 to 10's *μ*m Nd-doped Al

forms nanopore template following anodization

oxide barrier at well bottoms prevents the ECD of metal catalysts for CNT growth



High Thermal Conductivity Substrate

Al, Al-alloy, Si, sapphire (depends on application)

Limmer et al, *JES*, **159**, D235 (2012)

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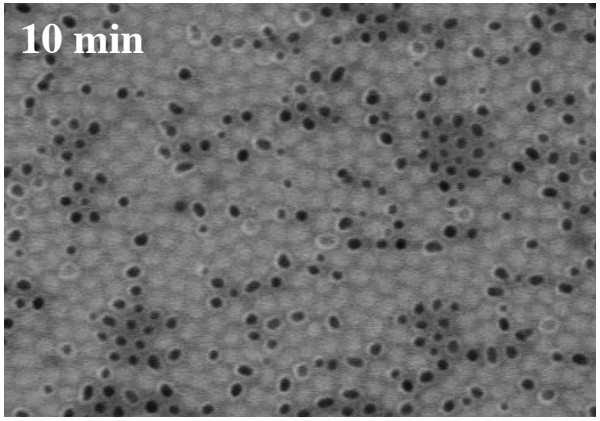
Optimizing CNT Site Density

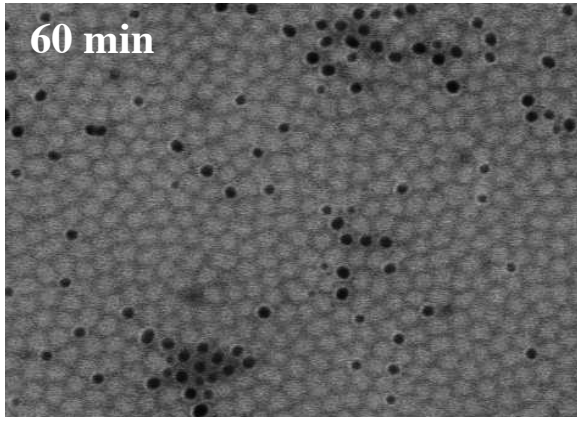
Electrochemical deposition of Co nanowires inside AAO pores

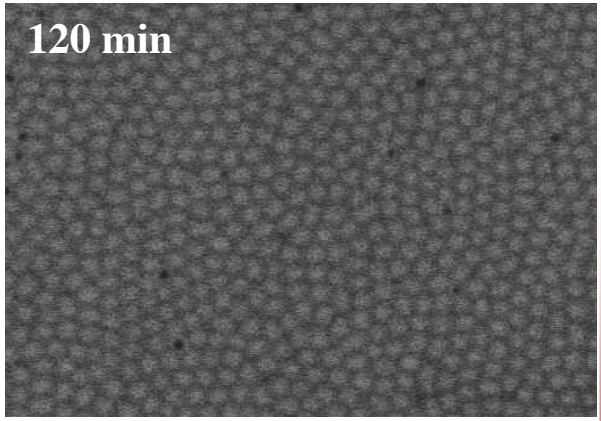
(Nanotubes will only grow from catalyst-filled pores)

Controlling the duration of the WO_3 etch step controls the catalyst site density!

(0.2 M, pH 7 phosphate buffer solution)

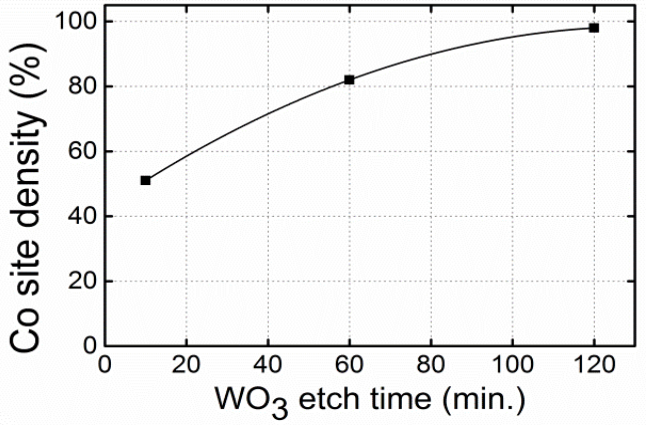






To study catalyst site density, samples are ion-milled to expose catalyst wires inside pores. Dark pores are empty, light-colored pores are full of Co.

10^{10} nanopores/cm^2 and 75 nm diameters yields > 44% surface coverage!



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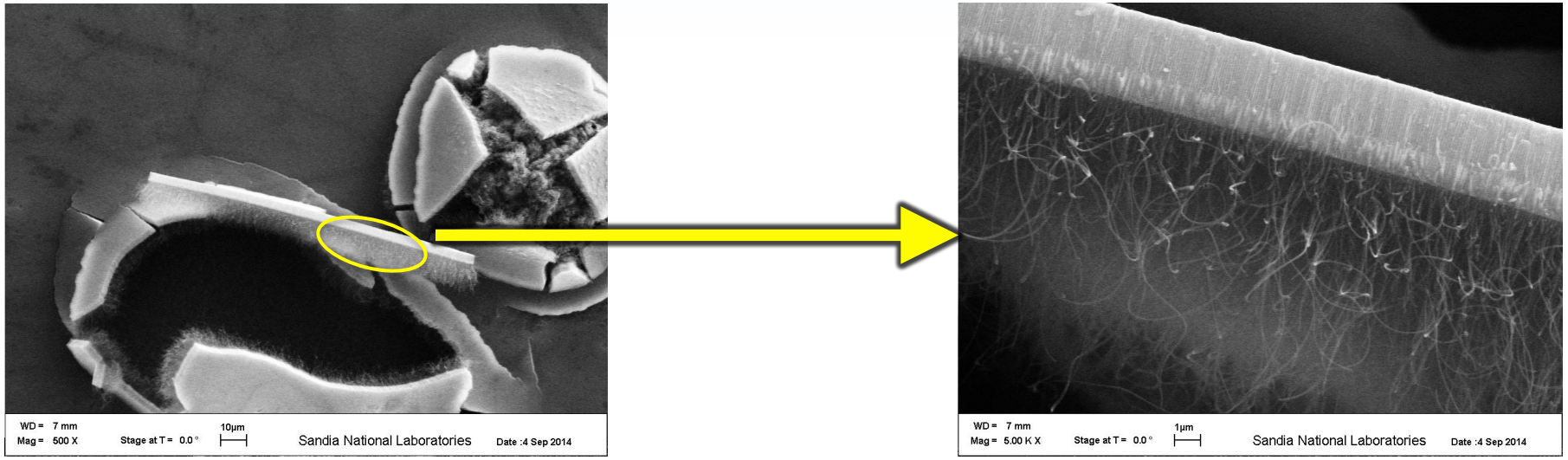
Rochford et al, *JMR*, **30**, 316 (2015)

Optimizing CNT Site Density in Nanopores
(Controlling the Co Catalyst Position)



- *Near the end of project,* we experienced a film stress situation where the AAO template cracked and partly lifted from the substrate, exposing the underside.
- Note that Co filled ~ 30% of the AAO pore depth. No CNTs grew from the AAO surface, however…
- **Note the very high CNT density from the underside of the template where the Co-catalyst is flush with the template, *perhaps 1 CNT per nanopore…***
- ***Can we control this catalyst geometry on the top surface?***

Siegal et al, (in progress)

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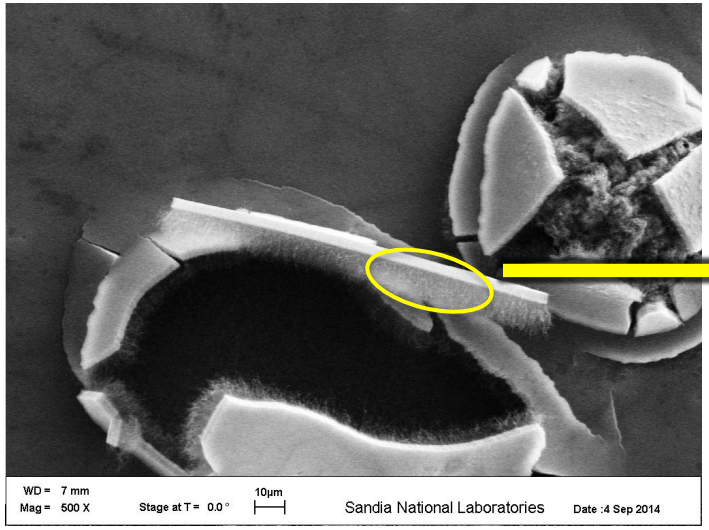
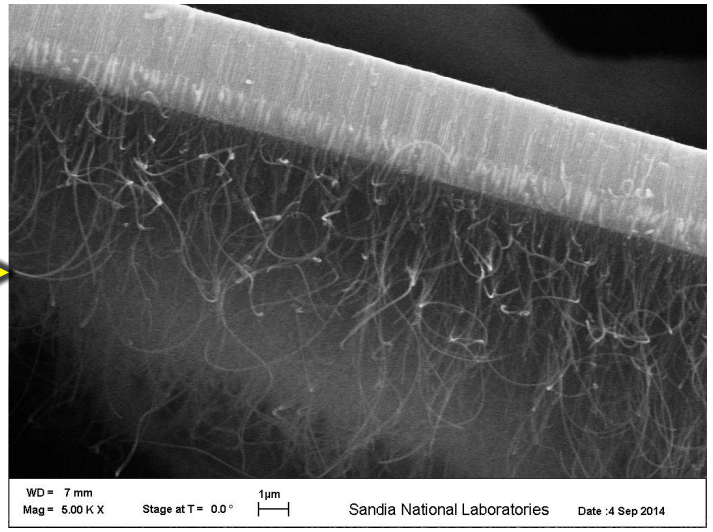
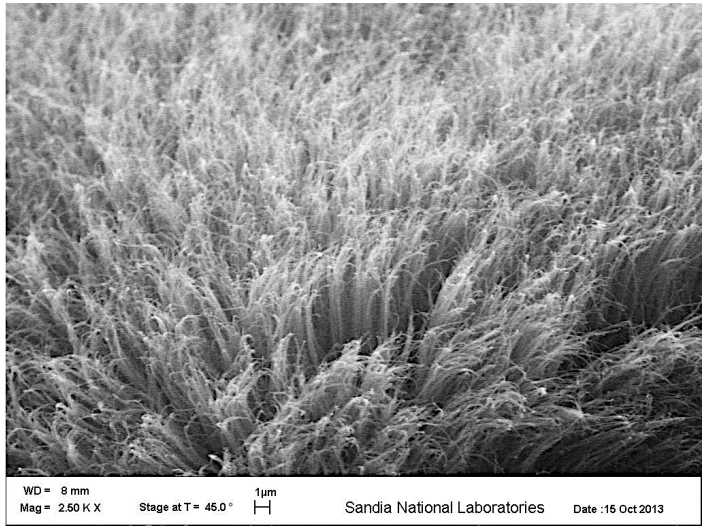
Optimizing CNT Site Density in Nanopores
(Controlling the Co Catalyst Position)







- Now we embrace the inability to precisely control ECD height of catalyst, and allow it to slightly over-coat the template surface.
- Use ion beam milling to polish the surface so that the catalyst is flush with the AAO surface.
- CNTs may be growing from every pore! *44%?*
- *This needs further study. E.g. how far can we etch the Co back into the pores?*

Siegal et al, (in progress)

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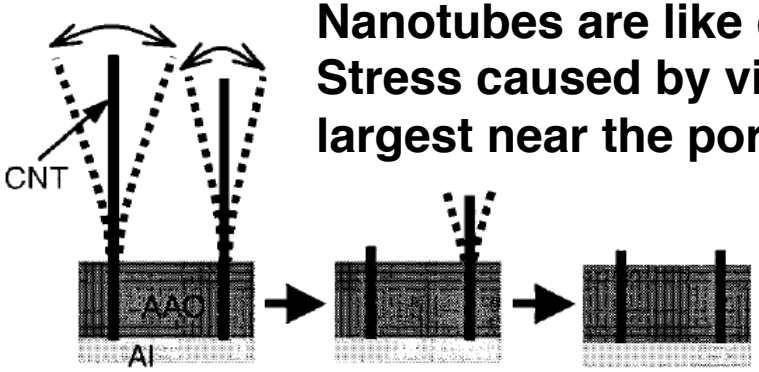
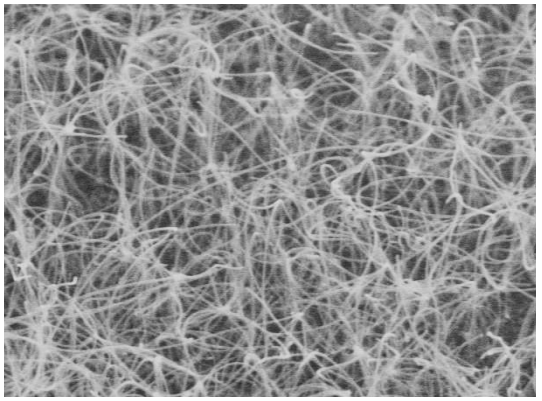
Planarization of CNT Arrays

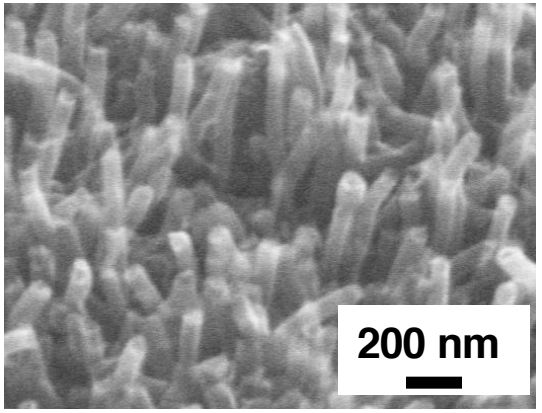
40 kHz ultrasonication for 1 minute in acetone bath



Nanotubes are like cantilevers. Stress caused by vibration is largest near the pore mouth.

Jeong et al. *Chem. Mater.* (2002)





- CNTs uniformly cut to ~ few tenths of a *μ*m above the AAO.
- CNT site density remains high after cutting, suggests that the CNTs are not being pulled out of pores or cut below the AAO surface.
- *Will need to etch catalyst somewhat below the template surface to prevent CNTs from detaching.*

Rochford et al, *JMR*, **30**, 316 (2015)

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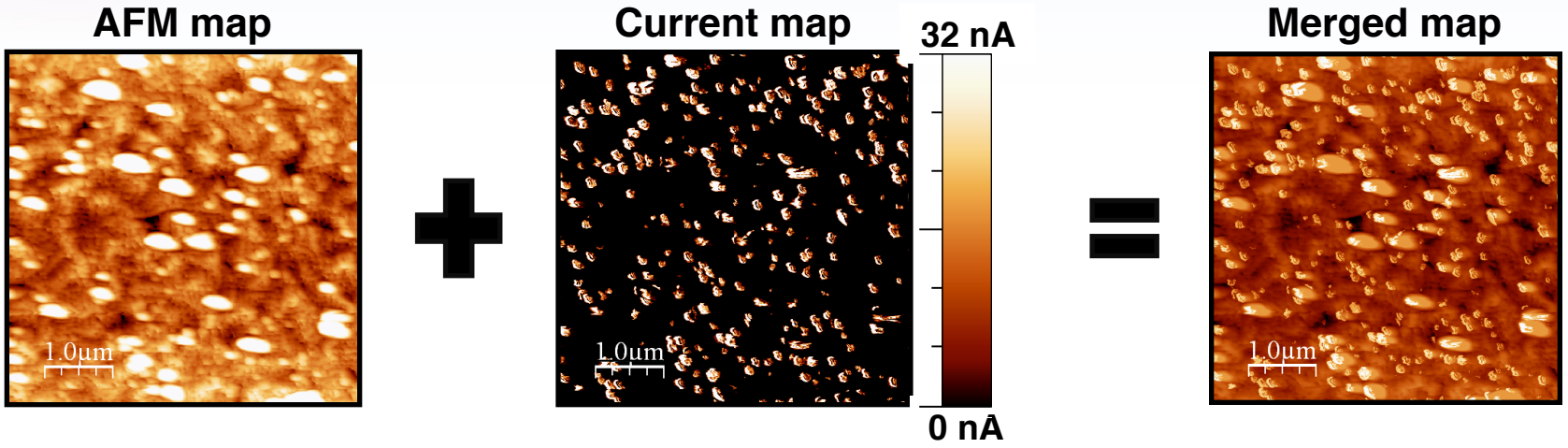
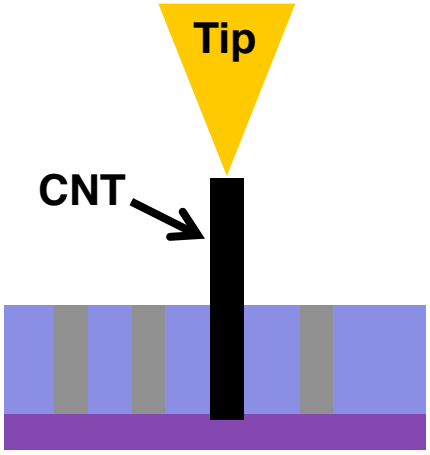
CNT-Substrate Ohmic Contacts

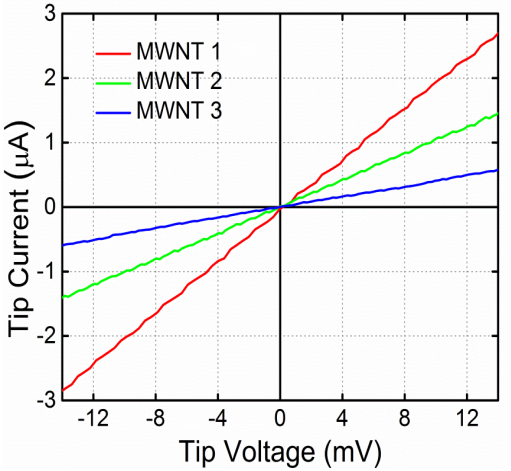


AFM provided evidence that cleaved CNTs remain highly conductive



Loading Force ~ 1.6 μN

Conductive AFM IV



Conductive AFM confirms that electrical continuity to the substrate *is preserved after ultrasonic cutting!*

Rochford et al, *JMR*, **30**, 316 (2015)

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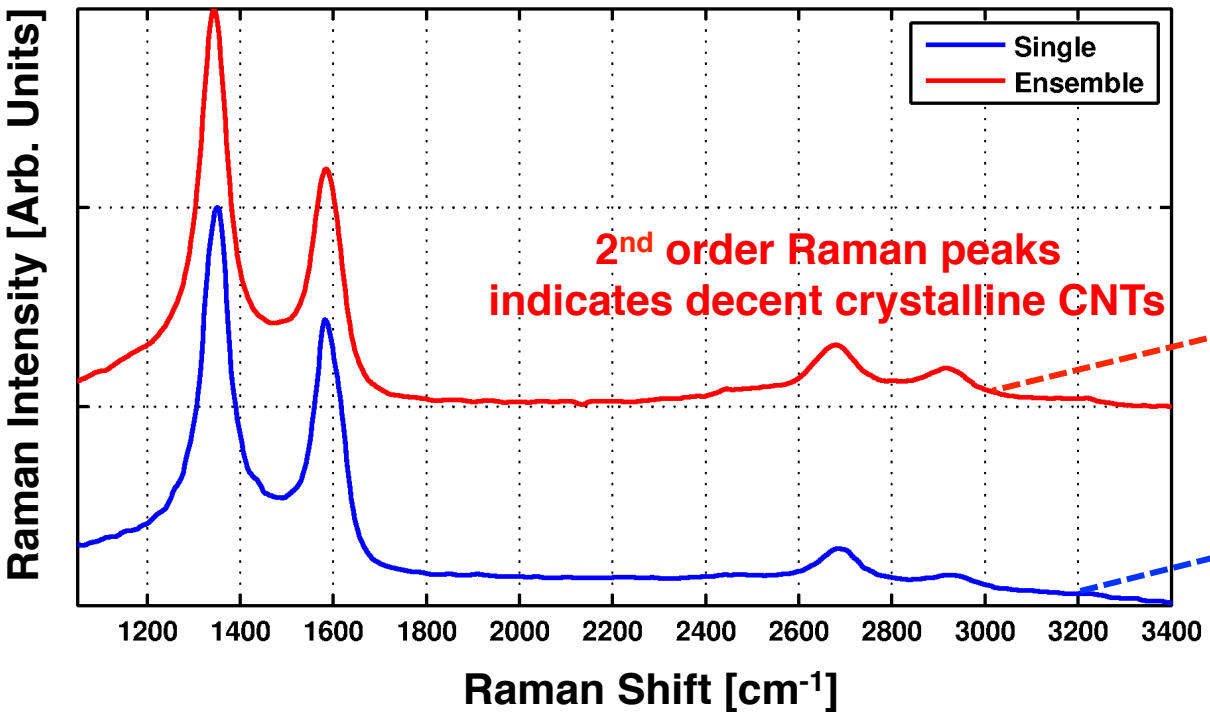
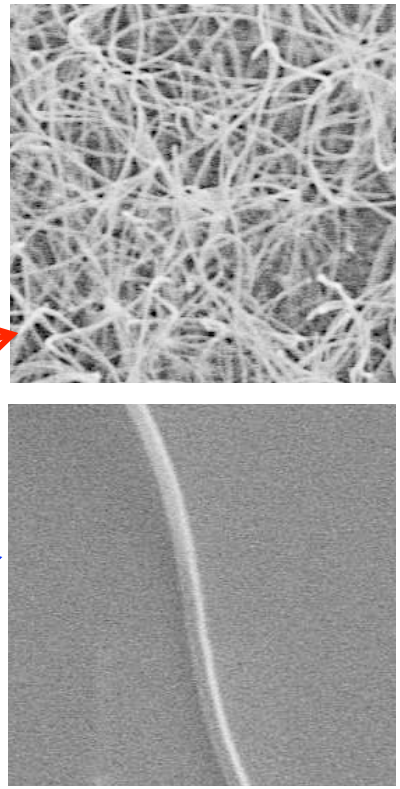
Assessing CNT Microstructural Quality
(individual CNTs vs. full arrays)

Raman spectroscopy confirms growth of uniform MWNTs

Individual spectrum is the same as the array!





- Little variation between MWNTs
- I(D)/I(G) of 1.9 implies moderate disorder
- Consistent with non-graphitized CVD-grown MWNTs

Rochford et al, *JMR*, **30**, 316 (2015)

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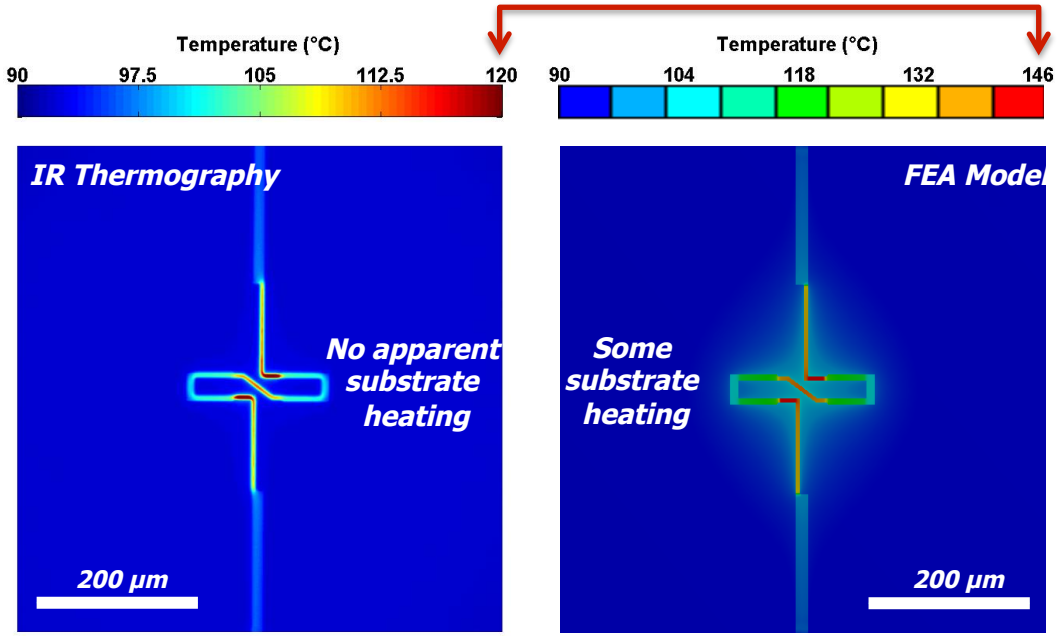
IR Thermography Volumetric Averaging

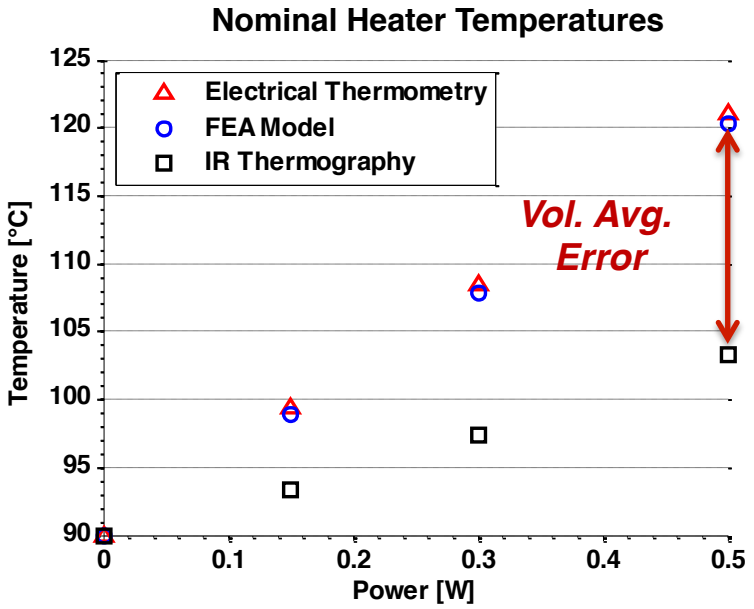
Why IR Thermography?

1. Passive technique, utilizing natural emission
2. Quick high resolution images over “large” areas
3. Versatile qualitative and quantitative analysis

Why NOT IR Thermography?

1. Long wavelength of averaged IR light means semi-transparency through many materials
2. Microscope diffraction limitations
3. **RESULT: Volumetric Temperature Average**





Providing a method to model volumetric averaging in IR thermography greatly increases the utility of this widely used temperature mapping technique.

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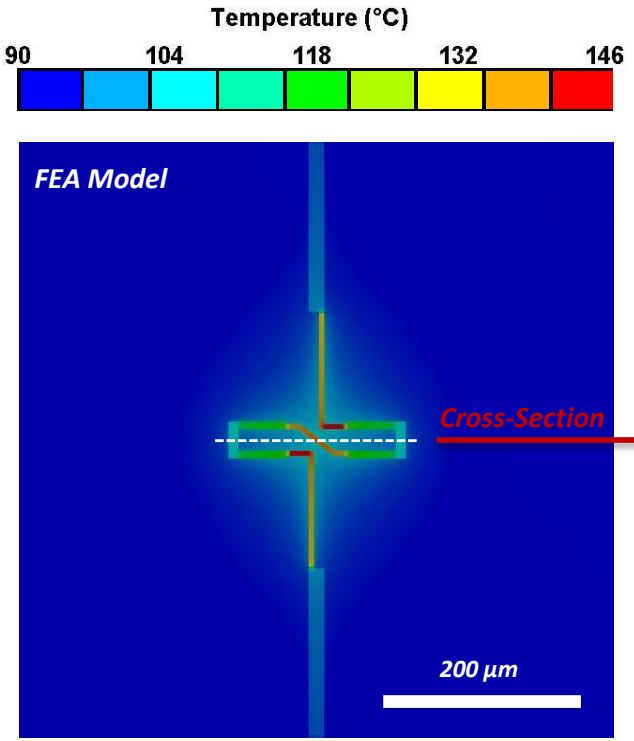
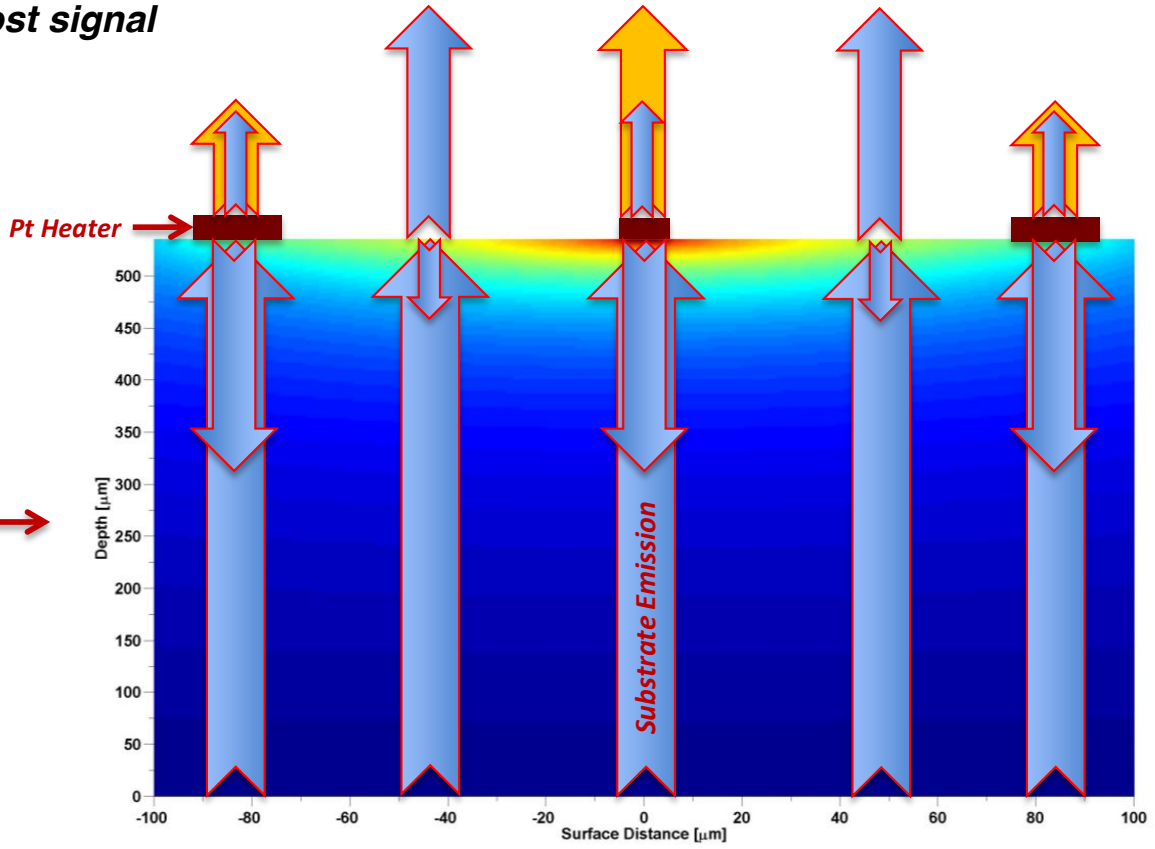
IR Thermography Depth Averaging

Premise:

1. All points throughout device emit IR at a rate $\propto (\varepsilon missivity * Temperature^4)$
2. Some percentage of that emission will transmit to the IR camera
3. The percentage will depend on the optical properties of the materials around it
4. Rule of Thumb: The measurement will be weighted toward the temperature of the region *that contributes the most signal*

IR Camera

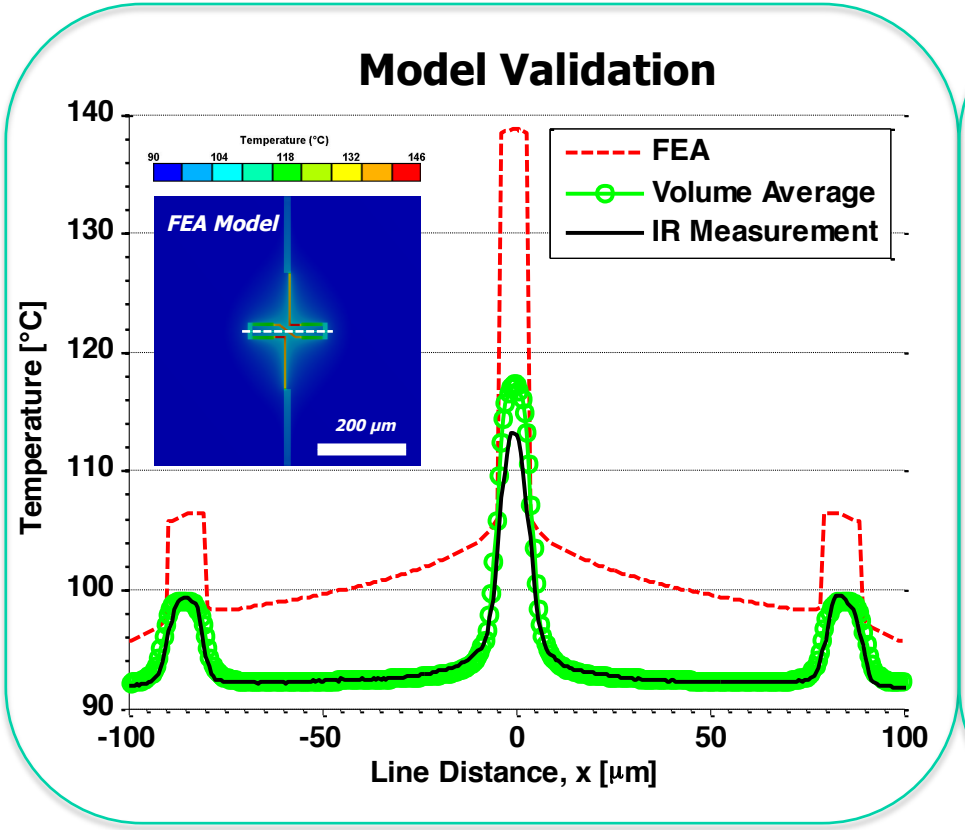


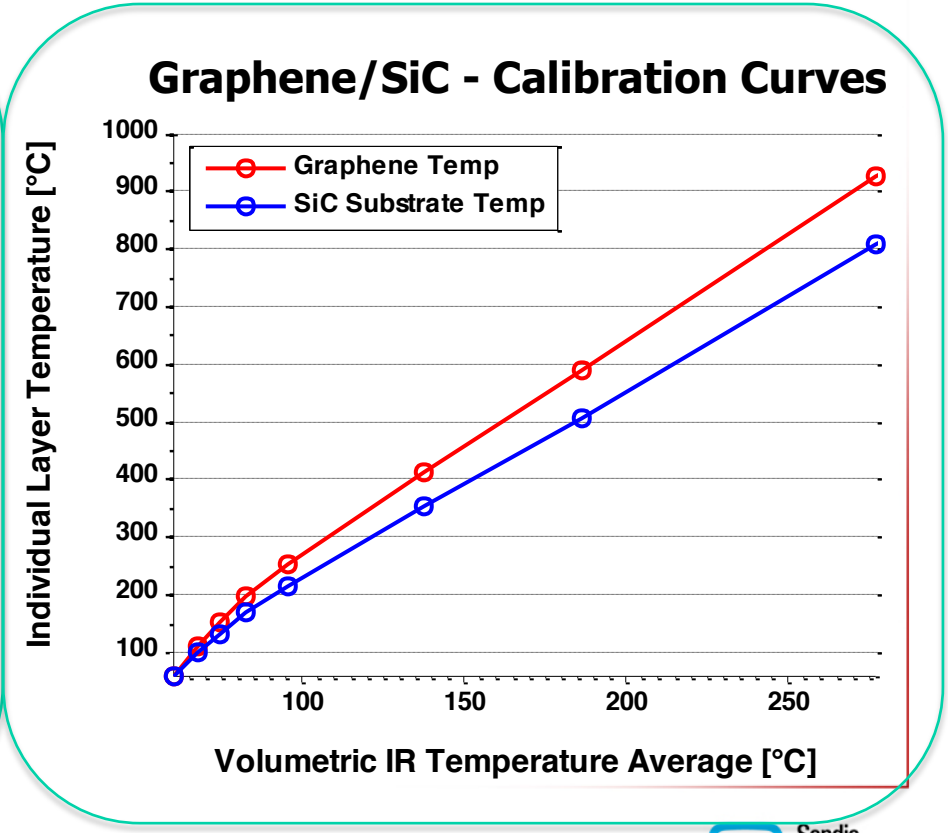


IR Thermography Volumetric Averaging

Volumetric Averaging Program:

1. **Total IR Emission =** Planck's Distribution + Transfer Matrix + Numerical Integration + Temperature Profile
2. Perform a series of calibrations to convert calculated emissions to an effective **depth averaged temperature**.
3. Apply diffraction induced lateral averaging to depth averaged temps to complete the **volumetric average**.





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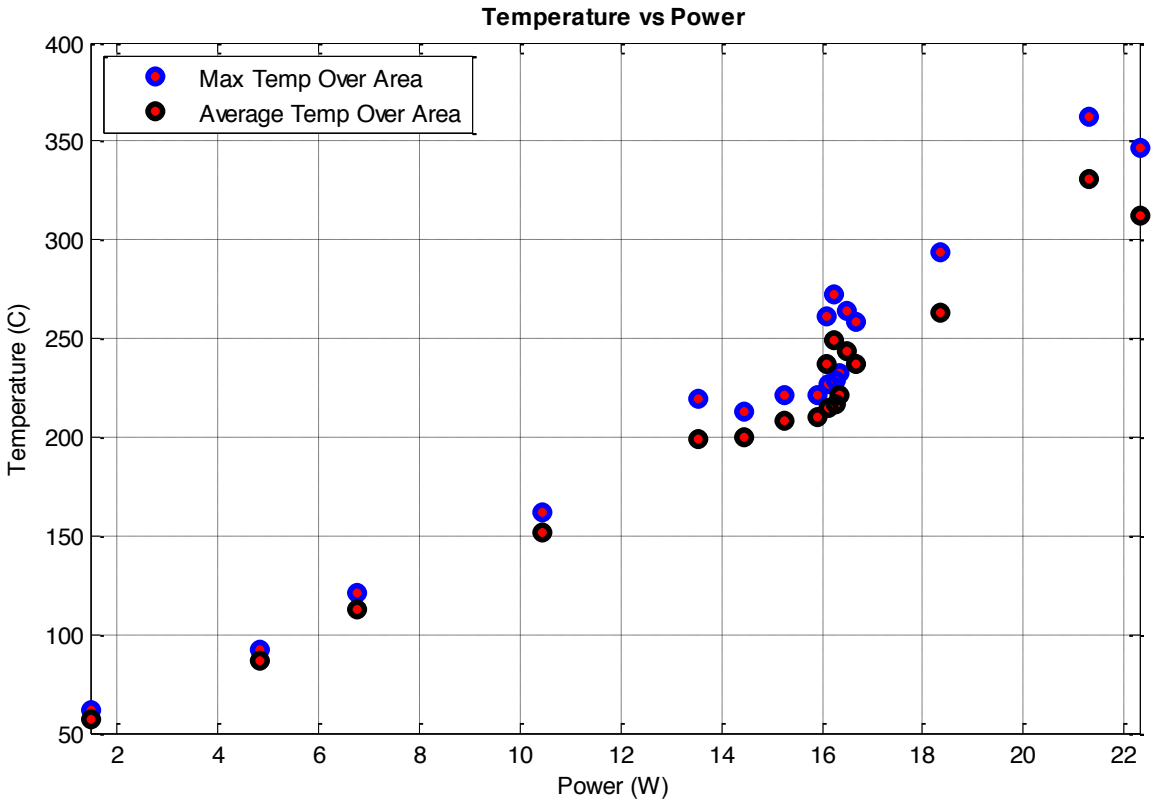
Measuring Ag-Paste Efficiency vs. Device Power

Experiments completed for temperature rise due to changes in (a) duty cycle, (b) frequency, and (c) input voltage



- Currently looking at variation in thermography results due to device-to-device and TIM deposition variability
- Will then analyze efficiency of different TIM materials
- **Demonstrates ability to measure temperature variation as a function of electrical stress**

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