

# Microsystem Enabled Photovoltaics

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# MEPV Program Overview

- Initial ideas in 2005
- First funds in (EERE Solar Program) in 2007
- Total program funds to date: ~\$20M
  - Sandia LDRD, EERE Solar Program, Army, ONR, NASA
- ~30 member diversified team at Sandia
- Many industry, university, and national laboratory partners
- ~45 patent applications filed
- ~60 technical publications
- Complete system-level R&D program
  - Cells: c-Si, GaAs, InGaP, InGaAs, InGaAsP, InGaN, CdTe
  - Optics: AR coatings, concentration, light trapping, etc.
  - Module design and manufacturing
  - Power electronics
  - Tracking
  - Cost modeling
  - Accelerated lifetime testing and failure analysis

# Scaling Benefits of Micro-Scale PV

1. Enhanced Carrier Collection due to short diffusion lengths <sup>2</sup>
2. Statistical minimization of semiconductor defects per cell <sup>2</sup>
3. Reduced semiconductor material usage <sup>1</sup>
4. Fabrication possible with arbitrarily large wafers <sup>1</sup>
5. Reduced edge exclusion area for CPV cells <sup>1\*†</sup>
6. Back Contacts/no metal shading lines for c-Si *and* III-V <sup>1,2</sup>
7. Multi-junction cell architectures are possible that eliminate the need for lattice matched semiconductors or metamorphic epitaxial layers <sup>1,2,3</sup>
8. Multi-junction cell architectures are possible that eliminate the need for current matching between individual junctions <sup>1,2,3</sup>
9. Cells/modules utilize existing manufacturing facilities and supply chains in the Integrated Circuit, MEMS, LED, and Electronics Assembly industries <sup>1</sup>
10. Extremely flexible PV modules (1 mm bend radius) with high efficiency, single crystal semiconductor solar cells <sup>2,3\*†‡</sup>
11. 3D molding of the PV arrays is possible due to small, discrete cells making possible PV integration into products/systems in a way not possible with traditional PV <sup>3\*†‡</sup>
12. High optical concentration (up to 600X or more) within a thin (~1cm) module <sup>1,3\*†</sup>
13. High optically efficient optics (refractive optics instead of Fresnel optics) for concentrated systems <sup>2\*†</sup>
14. More sophisticated optical systems are possible which allow a larger acceptance angle than traditional CPV (reduces tracking portion of BOS costs) <sup>1,2\*</sup>
15. Heat rejection capacity significantly enhanced reducing or eliminating thermal management structures in CPV <sup>1,3\*†</sup>
16. Many small cells allows new interconnect networks (instead of simple series connections) between cells that provide optimal partial shade tolerance and robustness to damage, opens, shorts, failed cells, or variations in cell performance. <sup>2,3</sup>
17. Manipulation of optical coatings to create sophisticated images is possible due to the combination of manufacturing techniques, cell size, and interconnects <sup>3\*†</sup>
18. Interconnect designs are possible that allow elimination or significant reduction of bypass protection diodes. <sup>1,3</sup>
19. Interconnect designs for electrically independent cells allows for simple, passive voltage matching between different junctions within a module of different junction types <sup>1,2,3</sup>
20. Direct high voltage output (up to 1000V or higher) from a module is possible which reduces internal resistive losses and system wiring costs <sup>1,3</sup>
21. Active semiconductor devices can be placed within the module to allow “on-the-fly” switching of output voltages with high efficiency and low cost <sup>1,3</sup>
22. New, module-integrated inverter architectures are possible that eliminate or reduce large discrete components (inductors and capacitors) that current inverters require <sup>1,2,3\*†</sup>
23. Improvements in cell, optics, and inverter efficiencies reduces BOS cost components dependent on system efficiency (e.g., land and land prep, installation labor, racking/trackers, wiring, O&M, shipping, etc.) <sup>1,2\*</sup>

## Category(s) of scaling benefits:

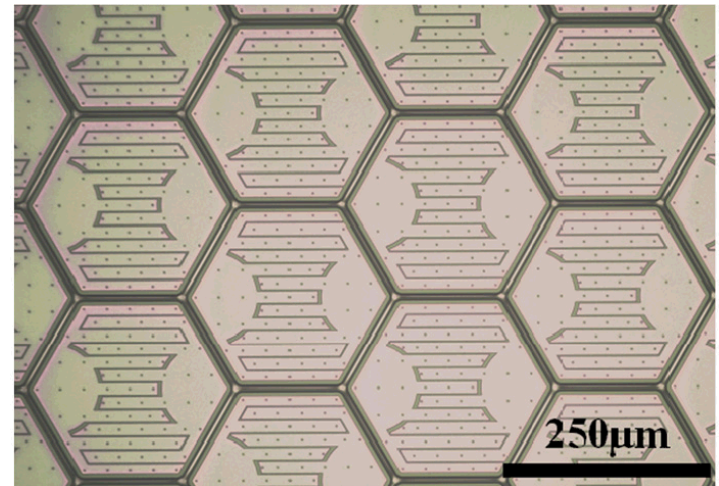
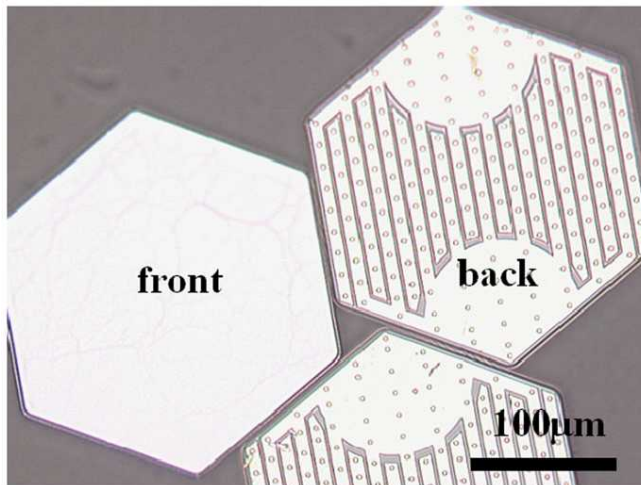
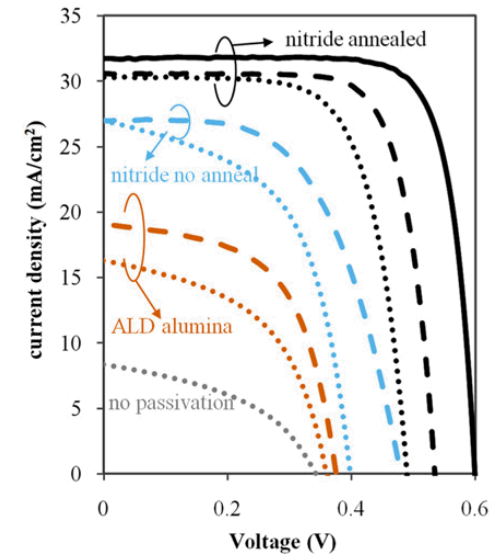
- 1 Cost reduction
- 2 Improved Performance
- 3 New Functionality

## Application space benefiting from scaling effect (if all applications benefit no application is indicated):

- \* Grid-tied PV (Utility/Commercial)
- † Grid-tied PV (BIPV)
- ‡ Flexible/Conformal PV (mobile)
- ◆ Flexible/Conformal (Space)

# C-Si Cell Results

- C-Si interdigitated back contact (IBC) cells 14-20  $\mu\text{m}$  thick, 200-700 mm across.
- Cell efficiencies up to 14.9%.
- Prototype modules created with up to approximately 500 interconnected cells.
- Module efficiencies up to 13.75%.
- Manufactured with methods allowing wafer reuse and/or conservation of c-Si material.



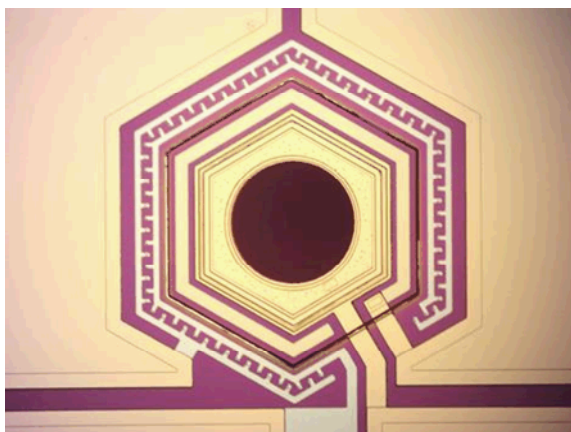
J. L. Cruz-Campa, et al., "Microsystems enabled photovoltaics: 14.9% efficient 14  $\mu\text{m}$  thick crystalline silicon solar cell," Solar Energy Materials & Solar Cells, **95**, pp. 551-558, 2011.

J. L. Cruz-Campa, et al., "Ultrathin flexible crystalline silicon: microsystems enabled photovoltaics," IEEE Journal of Photovoltaics, **1**, pp. 3-8, 2011.

# Cell Results

## InGaP/GaAs:Si

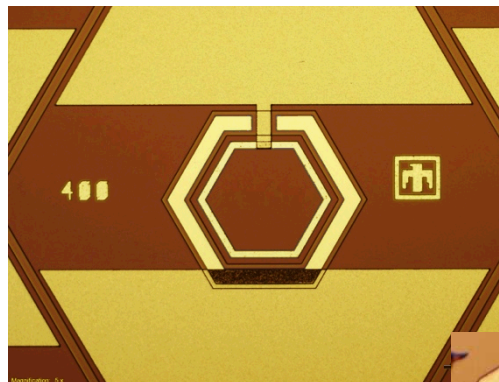
- Developed GaAs and InGaP/GaAs single-side contacted cells
- Bonded GaAs and InGaP/GaAs cells to silicon and fully processed
- Demonstrated active (i.e., power producing) Si cell as part of InGaP/GaAs:Si cell stack
- Achieved a 29.5% InGaP/GaAs cell efficiency bonded to an active silicon cell (not included in efficiency).



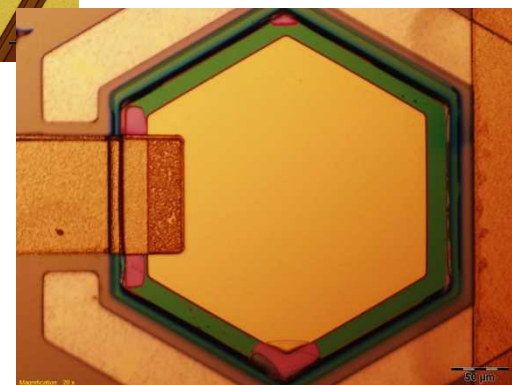
InGaP/GaAs cell on Si

## Si:InGaAsP/InGaAs

- Developed both InGaAs and InGaAsP/InGaAs cells
- Bonded InGaAs and InGaAsP/InGaAs cells to silicon and fully processed
- InGaAs cell behind silicon achieved 3% conversion efficiency at one-sun



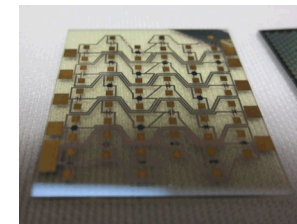
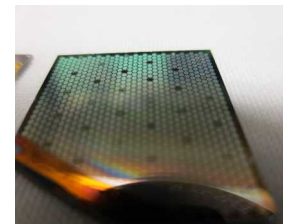
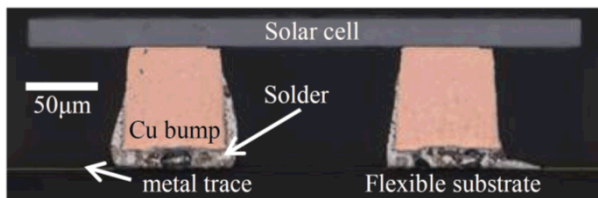
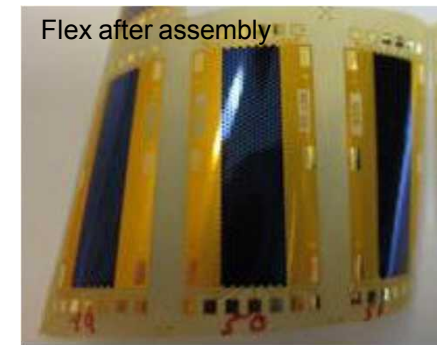
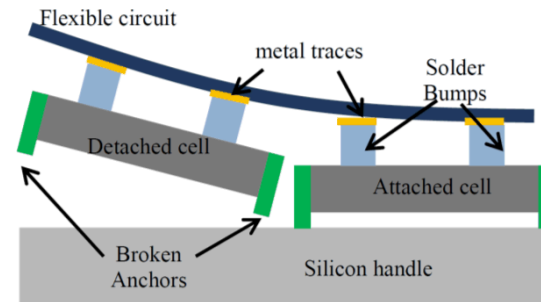
InGaAs solar cell  
on InP substrate



InGaAsP/InGaAs cell  
bonded to Si

# Cell Assembly

- **Pick-and-Place**
  - Industry standard
  - Serial assembly
  - Not compatible with thin III-V cells
- **Bump-Bond and Peel**
  - Parallel assembly
  - Limited to wafer size
  - Sparse and dense cell arrays
- **Activated Bond/ELO release**
  - Parallel assembly
  - Limited to wafer size
- **Self-Assembly**
  - Unlimited assembly area
  - Allows dissimilar wafer sizes
  - Challenging technical issues



G. N. Nielson, et al., "216 cell microconcentrator module with moderate concentration, +/- 4° acceptance angle, and 13.3 mm focal length," IEEE PVSC, pp. 465-469, 2013.

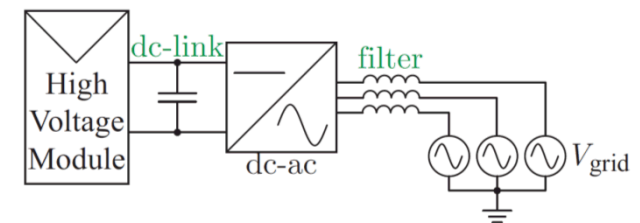
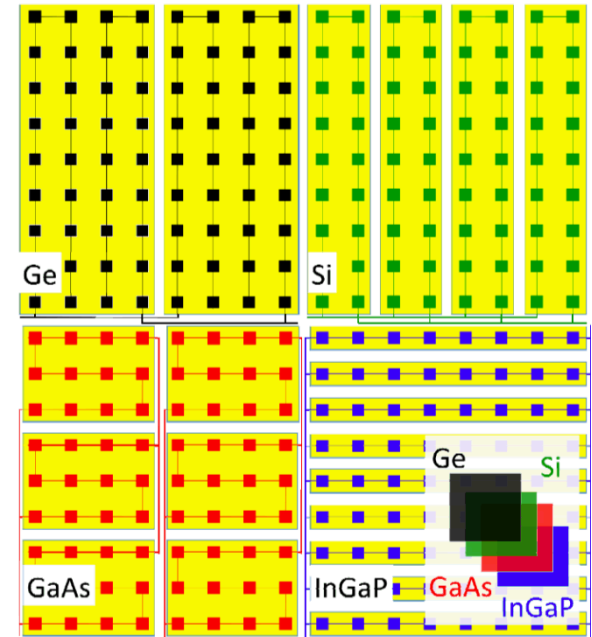
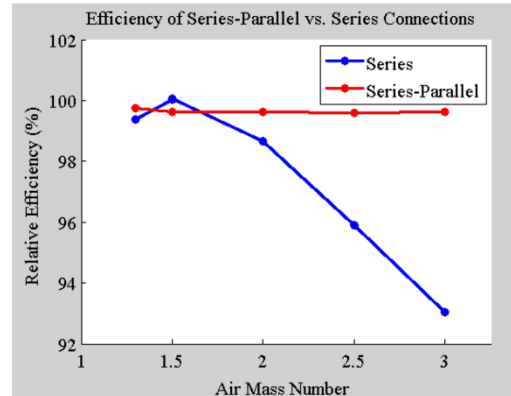
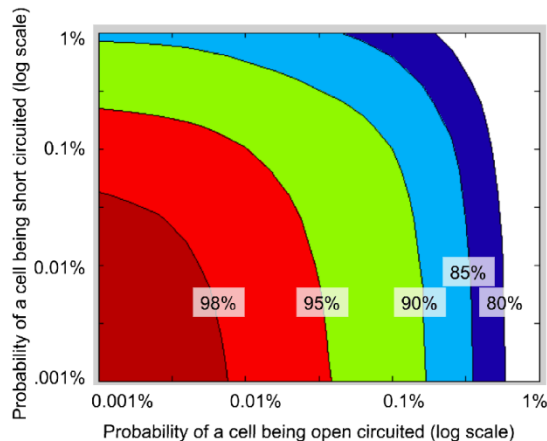
J. L. Cruz-Campa, et al., "Ultra-thin single crystal silicon modules capable of 450 W/kg and bending radii < 1 mm: fabrication and characterization," 39<sup>th</sup> IEEE PVSC, pp. 1218-1223, 2013.

N. B. Crane, et al., "Self-assembly in additive manufacturing: opportunities and obstacles," Rapid Prototyping Journal, pp. 211-217, 2011.

J. L. Cruz-Campa, et al., "Self Assembly of Micro Photovoltaic Devices for Inexpensive Solar Energy," Self-Assembly of Materials Workshop, 2011.

# Cell Interconnects

- **Series/Parallel Connections**
  - Improves damage tolerance
  - Improves performance in partial shade
- **Independently connected multi-junction cells**
  - Improves performance under spectral variations
  - Allows greater flexibility in PV cell bandgaps
- **Parallel, Interleaved 3-phase Inverter**
  - Simplified AC module architecture with improve efficiency and reliability at lower cost



A. L. Lentine, et al., "Optimal cell connections for improved shading, reliability, and spectral performance of microsystem enabled photovoltaic (MEPV) modules," 35<sup>th</sup> IEEE PVSC, pp. 3048-3054, 2010.

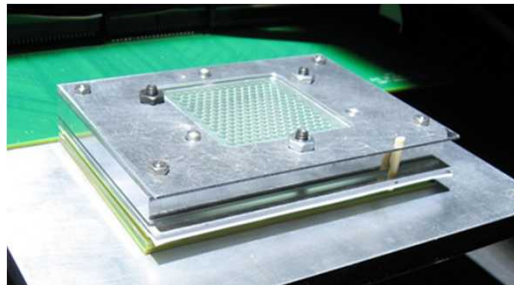
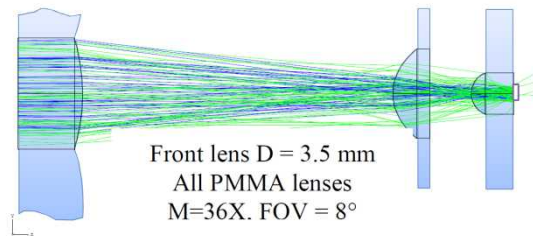
B. Johnson, et al., "A single-stage three-phase AC module for high-voltage photovoltaics," 27<sup>th</sup> IEEE APEC, pp. 885-891, 2012.

A. L. Lentine, et al., "Enhanced efficiency for voltage matched stacked multi-junction cells: Optimization with yearly temperature and spectra variations," 39<sup>th</sup> IEEE PVSC, pp. 788-791, 2013.



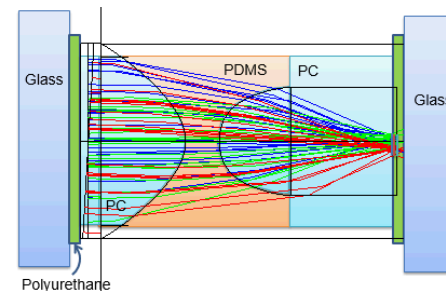
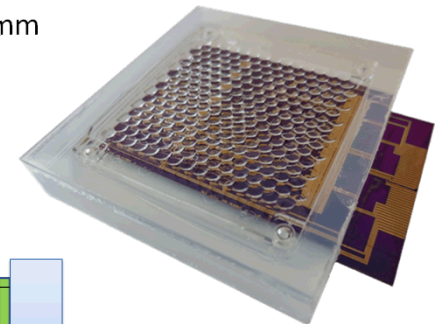
## ■ Prototype I

- 50X concentration
- $8^\circ$  acceptance angle
- 60% optical transmission
- 3 lens optical system
- 13 mm focal length
- Module thickness  $\sim 20$  mm
- Module efficiency: 6%



## ■ Prototype II

- 100X concentration
- 4.5 degree acceptance angle
- 90% optical transmission
- Immersion lens system (no air gap)
- Short focal length ( $\sim 5$  mm)
- Demonstrated parallel manufacturing of cells in sparse array
- Hybrid architecture (diffuse and direct collection)
- Module efficiency: 20%
- Module thickness of  $\sim 10$  mm



B. H. Jared, et al., "Micro-concentrators for a microsystems-enabled photovoltaic system," *Optics Express*, **22**, pp. A521-A527, 2014.

G. N. Nielson, et al., "216 cell microconcentrator module with moderate condensation,  $\pm 4^\circ$  acceptance angle, and 13.3 mm focal length," *IEEE PVSC*, pp. 465-469, 2013.

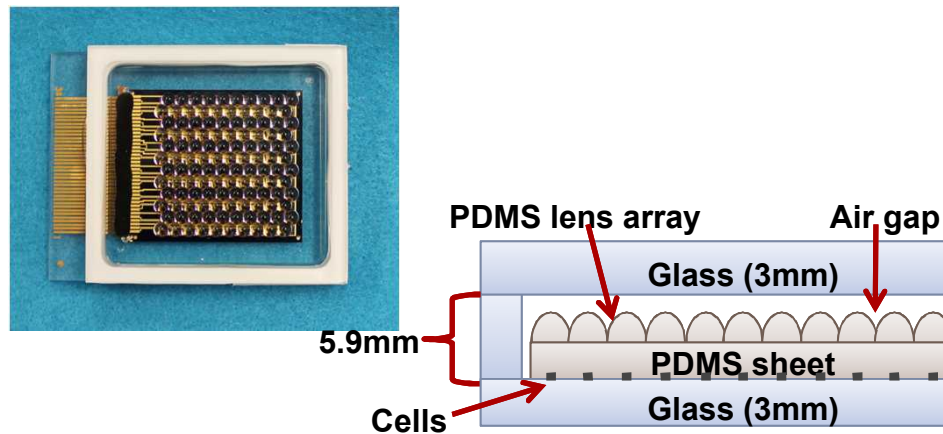
W. C. Sweatt, "Micro-optics for high-efficiency optical performance and simplified tracking for concentrated photovoltaics (CPV)," *International Optical Design Conference*, pp. ITuC4, 2010.

W. C. Sweatt, et al., "Photo-voltaic system using micro-optics," *Optics for Solar energy*, pp. SM2A, 2012.



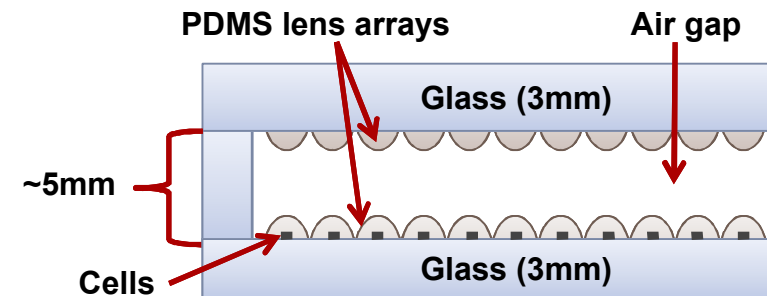
## Prototype III

- 200X concentration
- 3 degree acceptance angle
- Simple single lens element
- Short focal length (~5 mm)
- 90% optical efficiency (not demonstrated)
- Hybrid architecture (direct/diffuse collection)
- Potential module efficiency of up to 30% with project cells (up to 40% with optimized cells)
- Module thickness of ~12 mm



## Prototype IV (not built)

- 200X Concentration
- > 3° acceptance angle
- 2 lens element
- 5 mm focal length
- 90% optical efficiency
- Hybrid architecture possible
- Potential module efficiency up to 40%
- Module thickness ~12 mm
- Reduced optics materials costs
- Reduced module complexity
- Reduced cell manufacturing complexity



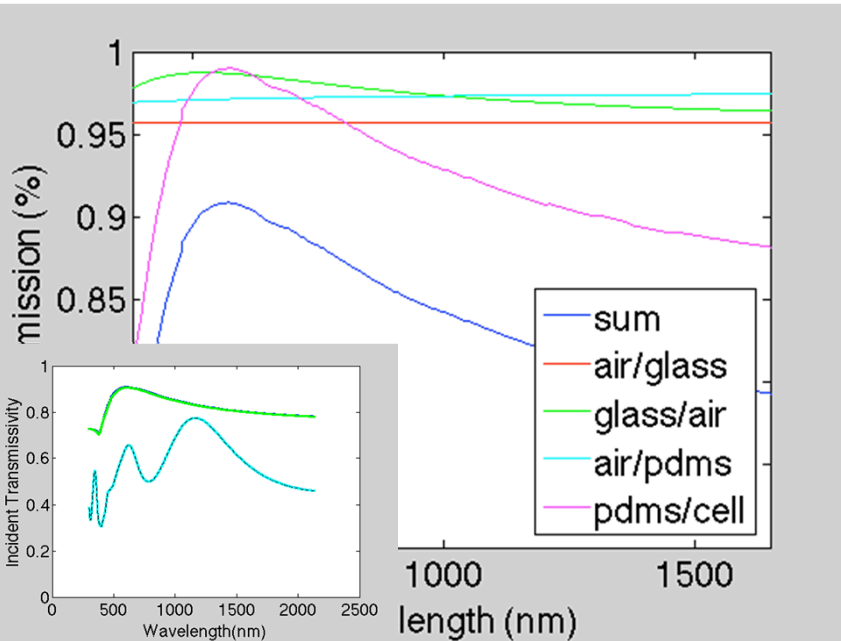
B. H. Jared, et al., "Micro-concentrators for a microsystems-enabled photovoltaic system," Optics Express, **22**, pp. A521-A527, 2014.

G. N. Nielson, et al., "216 cell microconcentrator module with moderate condensation, +/- 4° acceptance angle, and 13.3 mm focal length," IEEE PVSC, pp. 465-469, 2013.

W. C. Sweatt, "Micro-optics for high-efficiency optical performance and simplified tracking for concentrated photovoltaics (CPV)," International Optical Design Conference, pp. ITuC4, 2010.

W. C. Sweatt, et al., "Photo-voltaic system using micro-optics," Optics for Solar energy, pp. SM2A, 2012.

# Expected Module Efficiency: Prototype 3

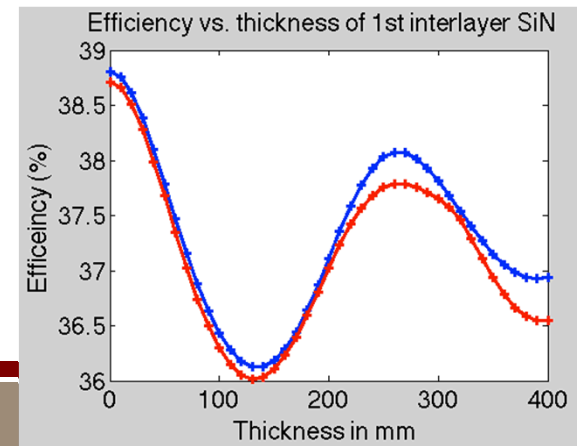
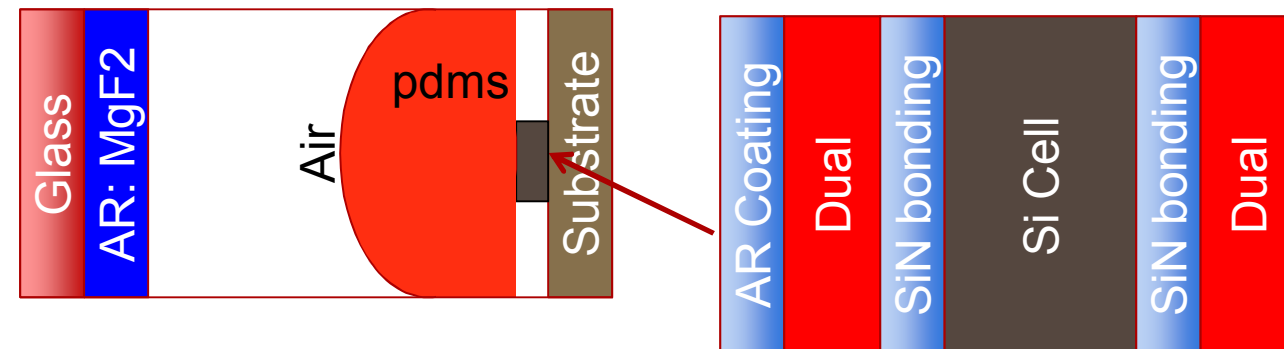


- One sun efficiency fit estimates:
  - Measured InGaP/GaAs > 29% at 100X
  - Good Si ~ 20%, C=1
  - Measured InGaAs ~ 2.9% after Si
- Optical Loss = 13.8% (380-1127 nm, incl. AR)
  - Improved 2% excess loss!
  - 380nm wavelength cutoff
- P3 (100X) expected efficiency: 37.8% (AM1.5D, 200X/100X cell)

■ Top Dual Contribution:	27.7%
■ Si Contribution:	4.6%
■ InGaAs Contribution:	3.5%
■ Diffuse Light	~2.0%



Glass/AR/Air

GOAL: 40%



# Cost Rationale for MEPV R&D

$$\text{LCOE} = \frac{\text{NPV} \left[ \begin{array}{c} \text{Module Cost} \\ + \text{BOS Cost} \\ + \text{Tracker Cost} \\ + \text{Installation Cost} \\ + \text{O\&M Cost} \end{array} \right]}{\text{NPV} \left[ \begin{array}{c} \text{Energy generation} \end{array} \right]}$$

 Lower costs  
 Increase energy generation

LCOE Component	PV	CPV	MEPV
Module Cost	Low	High	TBD
Tracker Cost	Low	High	Low
Installation Cost	Low	High	Low
O&M Cost	Low	High	Low
BOS Cost	High	High	TBD
Energy Generation	Low	High	High

# Cost Modeling Effort

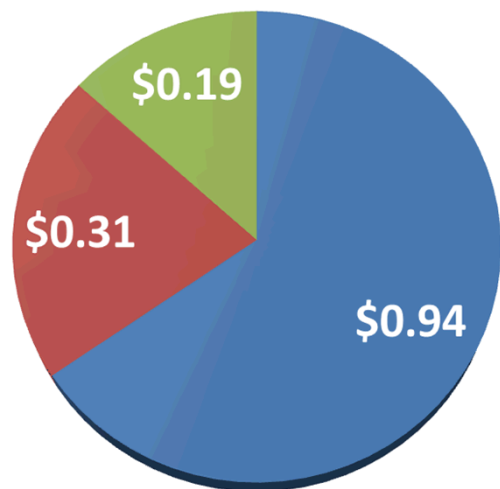
- Completed multi-junction cell cost model
- Employed cost model in cost-benefit analysis of additional junctions
- Investigated cost implications of alternative module architectures
- Leveraged previous modeling efforts to arrive at a “final” MEPV cost
- Identified potential pathways for future MEPV cost reductions

EPITAXY			Total Cost of All Epitaxy Steps:				
			Step 20				
			Layer 1	Layer 2	Layer 3	Layer 4	Layer 5
Category	Item	Units	Value	Value	Value	Value	Value
Process Definition			Total Cost of All Litho				
Substrate Type			LITHOGRAPHY				
Layer Description			Includes Coat, Expose, Develop, and Strip operations				
Substrate Diam			Step 3 Step 4 Step 10 Step 11				
Equipment			Category	Item	Units	Value	Value
Process Definition			THERMAL OXIDE DEPOSITION				
Substrate Type			Step 3 Step 9 Step 10				
Substrate Dia			Category				
Wafer Track			Item				
Model			Units				
Stepper or			Value				
Stepper/Co			Value				
Vendor & M			Value				
Asher Vend			Value				
Input Performance Parameters			Value				
Heat-up and			Value				
Wafer load/un			Value				
Thickness			Value				
Average Gro			Value				
NH3 flow rate			Value				
Substrates/r			Value				
Intermediate Technical Calculations			Value				
Total Substrate			Value				
Growth time			Value				
Total Cycle Time			Value				
TM/G Total			Value				
TM/n Flow			Value				
TM/n Total			Value				
TM/A Flow			Value				
TM/A Total			Value				
ASH3 Flow			Value				
ASH3 Total			Value				
FH3 Flow			Value				
FH3 Total			Value				
NH3 Total			Value				
H2 Total			Value				
N2 Total			Value				
W/H ratio			Value				
Cost Inputs and Calculations			Value				
Labor			Value				
Equipment			Value				
Installed Equipm			Value				
Maintenance Co			Value				
Equipment Life			Value				
Equipment Over			Value				
Equipment Foot			Value				
Utilization			Value				
Average Power			Value				
Raw Materials Costs			Value				
GaAs Substrate			Value				
TM/G			Value				
TM/n			Value				
TM/A			Value				
ASH3			Value				
FH3			Value				
NH3 HP			Value				
H2			Value				
N2 HP			Value				
Epitaxy Consum			Value				
Process Step			Value				
			3 4 10 11				

# Overview of MEPV module costs

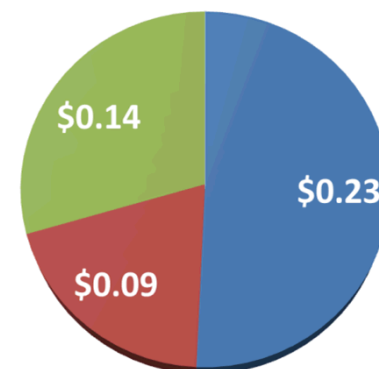
## *Prototype 3*

Current estimate: **\$1.44/W<sub>p</sub>**



## *Prototype 4*

2020 estimate: **\$0.46/W<sub>p</sub>**



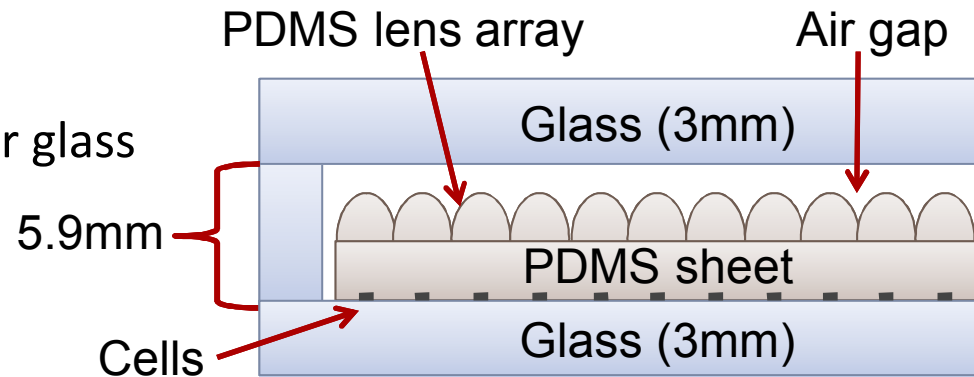
■ Cells  
■ Optics system  
■ Module production

- Fabrication of cells represents largest cost  
→ Also the largest potential near-term cost reductions

# Prototype 3 optics cost

## ■ Prototype 3 architecture

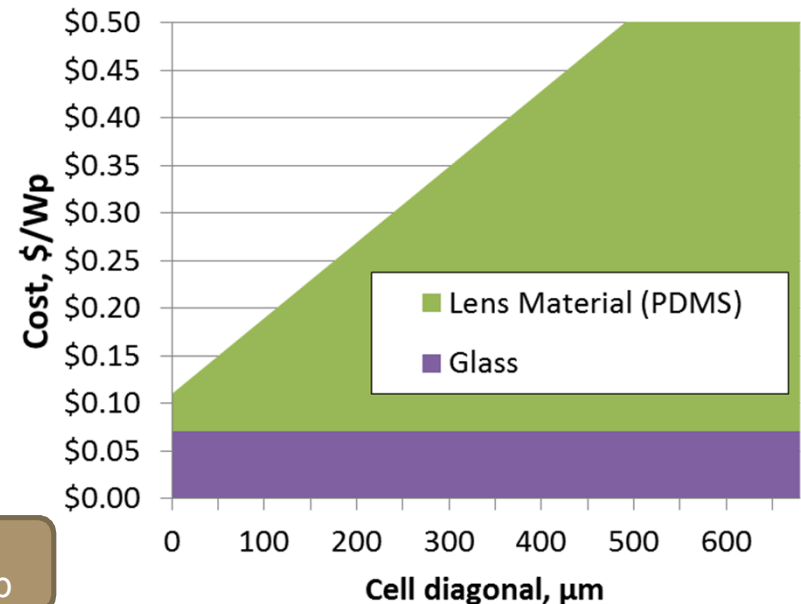
- PDMS sheet & lens array on rear glass
- Front glass protects lenses
- Concentration ratio (CR) = 200X



## ■ Prototype 3 advantages

- Lower materials costs
  - Air gap → Eliminate fill material
  - 250 $\mu$ m cell size → Thinner lenses
- Simple design: PDMS cast on glass

## ■ Key trade-off: Optics vs cell costs



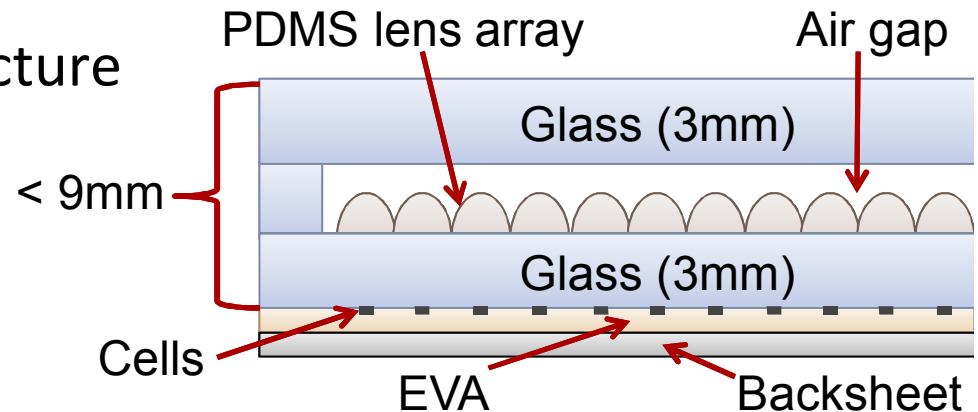
Estimate of current optics costs: \$0.31/W<sub>p</sub>



# “Modified Prototype 3” optics cost

## ■ Modified Prototype 3 architecture

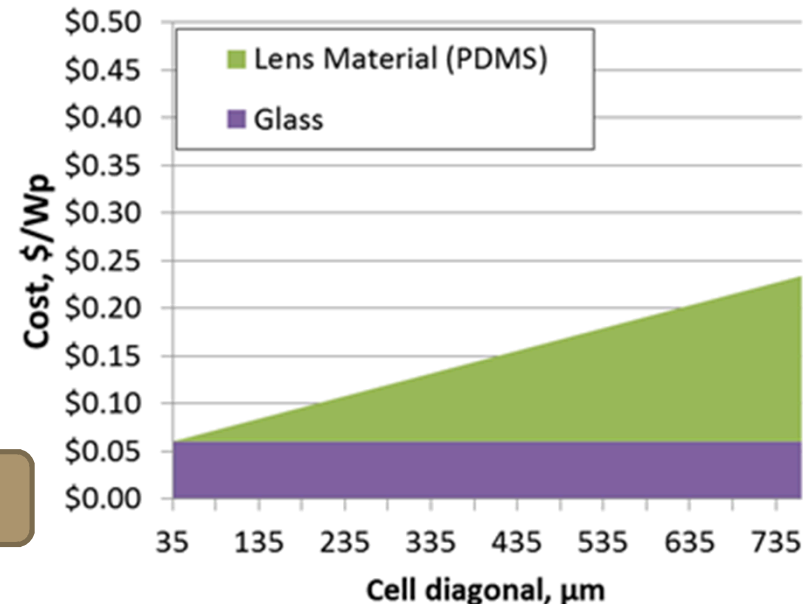
- PDMS sheet replaced by glass
- Front glass protects lenses
- Concentration ratio = 200X
- EVA encapsulant and Tedlar backsheet



## ■ Modified Prototype 3 advantages

- Lower materials costs
  - Replace PDMS sheet with glass
- Thinner PDMS reduces casting time

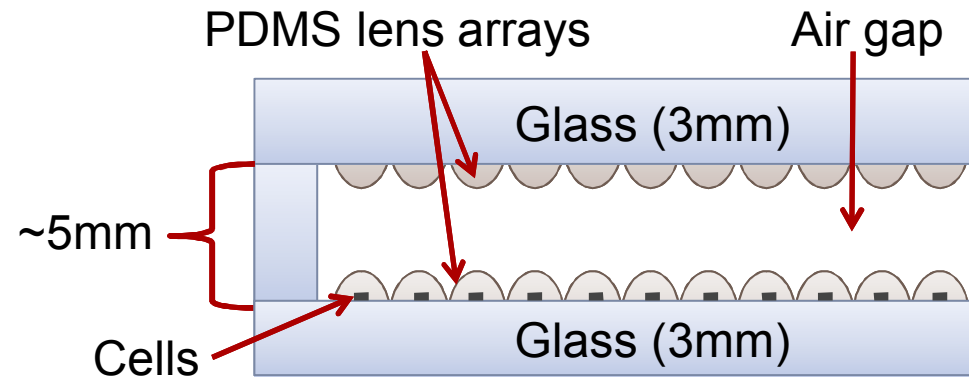
Estimate of 2020 optics costs:  $\$0.11/W_p$



# “Prototype 4” optics cost

## ■ Prototype 4 architecture

- PDMS lens arrays on front and rear glass
- Cells on top of rear glass  
→ no EVA, Tedlar, or frame
- Concentration ratio = 200X



## ■ Prototype 4 advantages

- Lower materials costs
  - Reduced PDMS usage →  $\$0.04/W_p$
  - No EVA or Tedlar
- Potential for higher concentration ratio

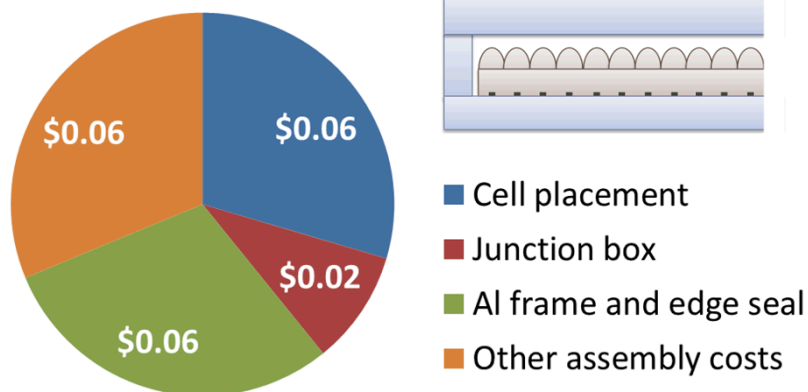
Prototype 4 architecture  
assumed for 2020  
module cost estimates

Estimate of 2020 Prototype 4 optics costs:  $\$0.09/W_p$

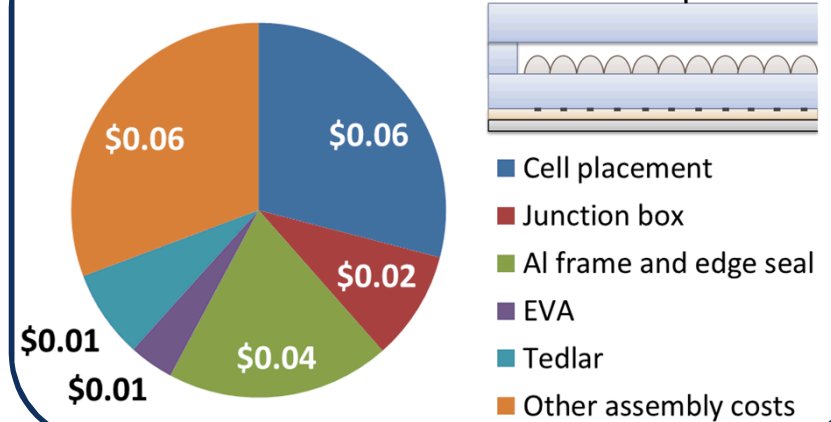
# MEPV module assembly leverages Si PV materials and processes

- Main module assembly steps
  - Screen print interconnects on glass
  - Transfer cells to glass in sparse array
  - Cast PDMS lens array (optics cost)
  - Align and assemble glass sheets
  - Laminate EVA & Tedlar (Modified P3)
  - Install frame (P3) & junction box

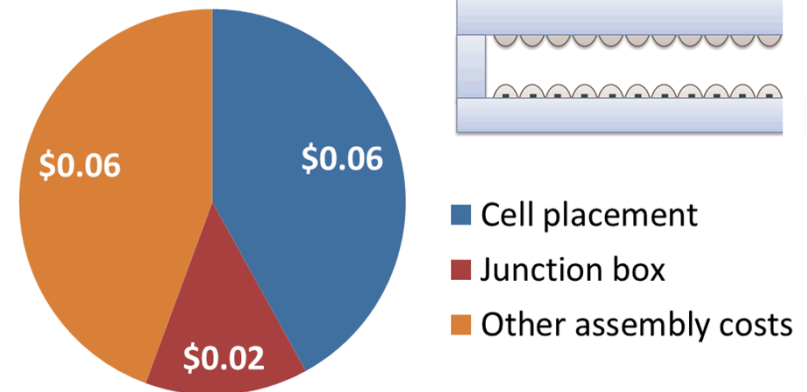
Prototype 3:  $\$0.19/W_p$



Modified P3:  $\$0.20/W_p$

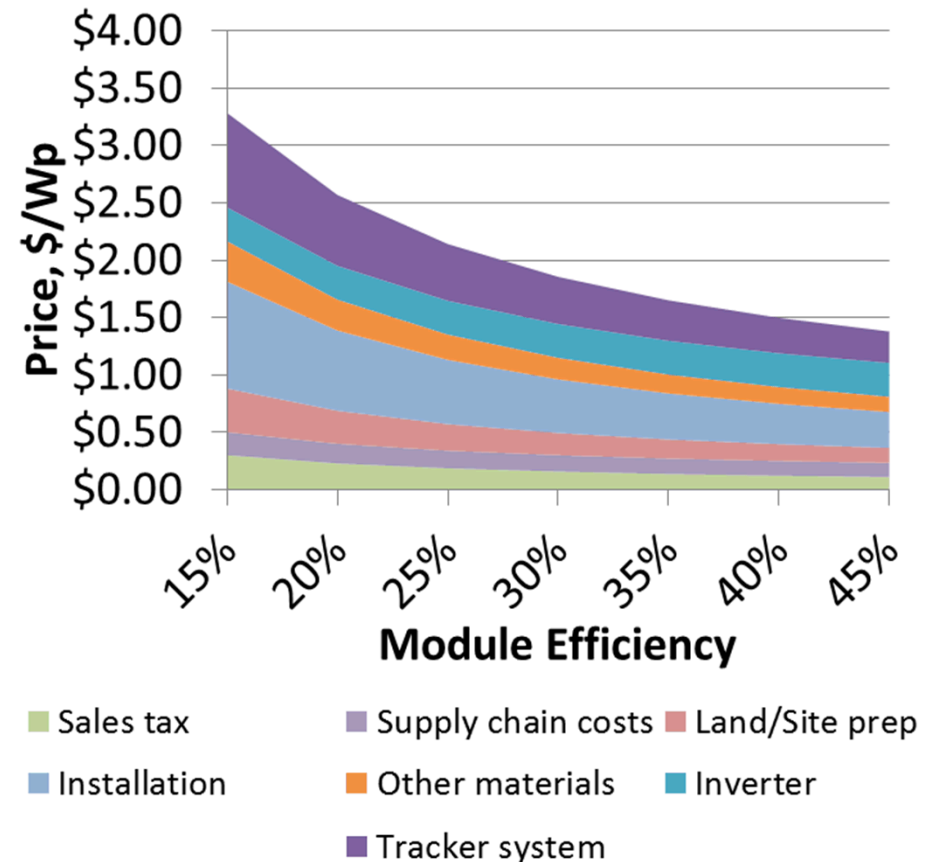


Prototype 4:  $\$0.14/W_p$

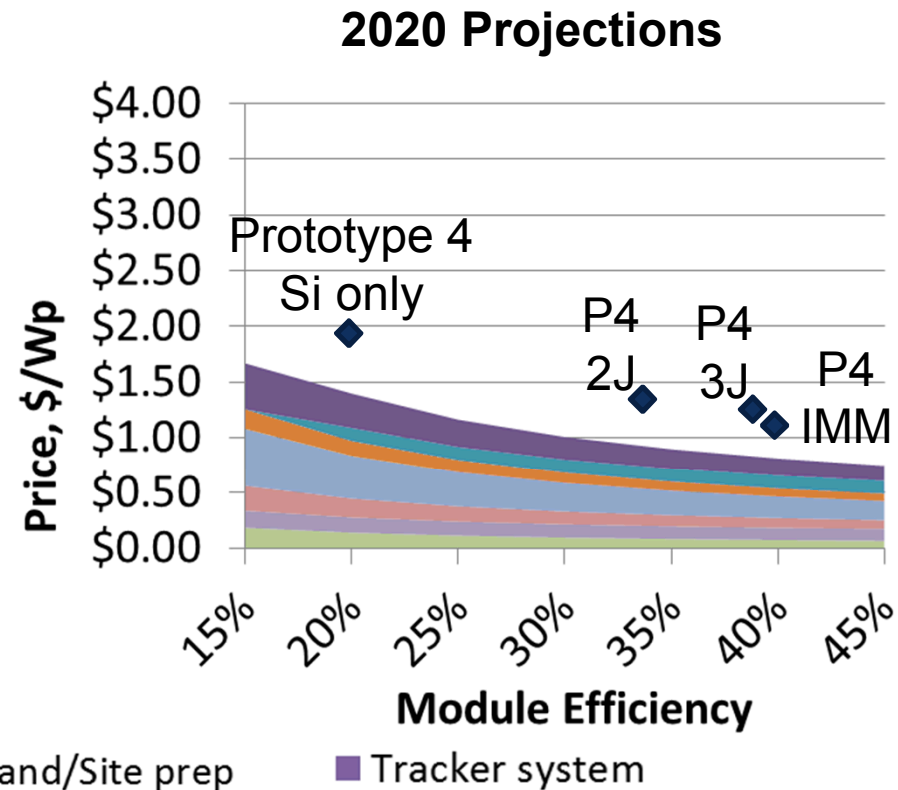
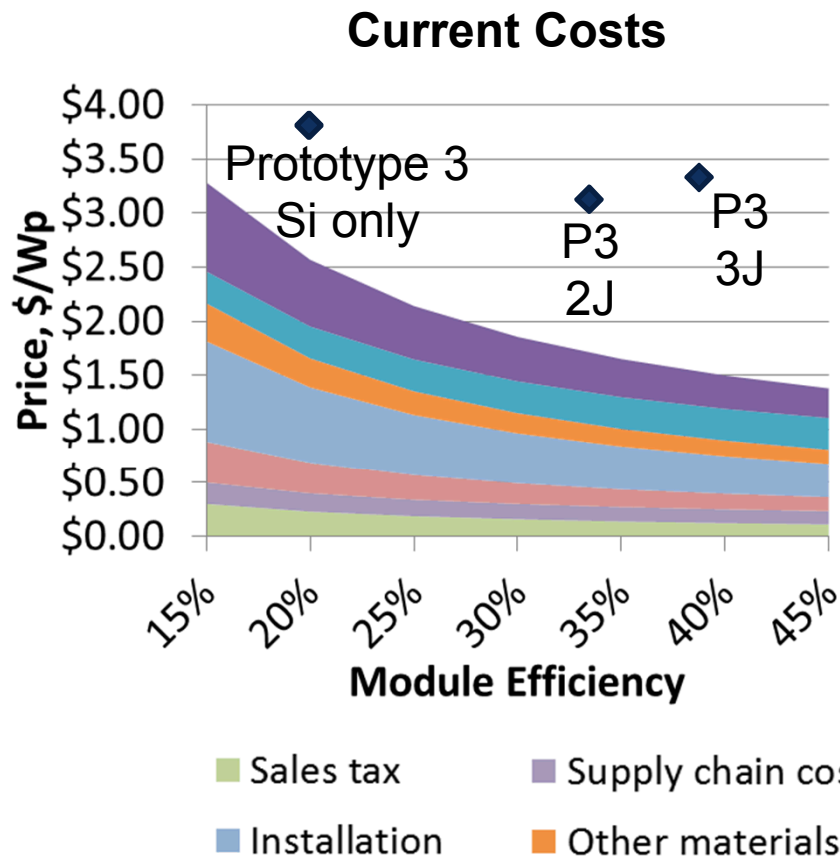


# MEPV BOS, installation, and O&M costs will not exceed one-sun Si PV costs

- MEPV form factor and weight is similar to conventional PV
  - No unique installation or O&M requirements
- Higher MEPV module efficiency effectively reduces system costs
- MEPV may reduce BOS costs by
  - Connecting cells in parallel to produce high voltage output, eliminating DC-to-DC converters and thicker, more expensive wiring
  - Enabling module-integrated inverters



# The optimal number of junctions depends on assumptions about BOS costs & efficiency



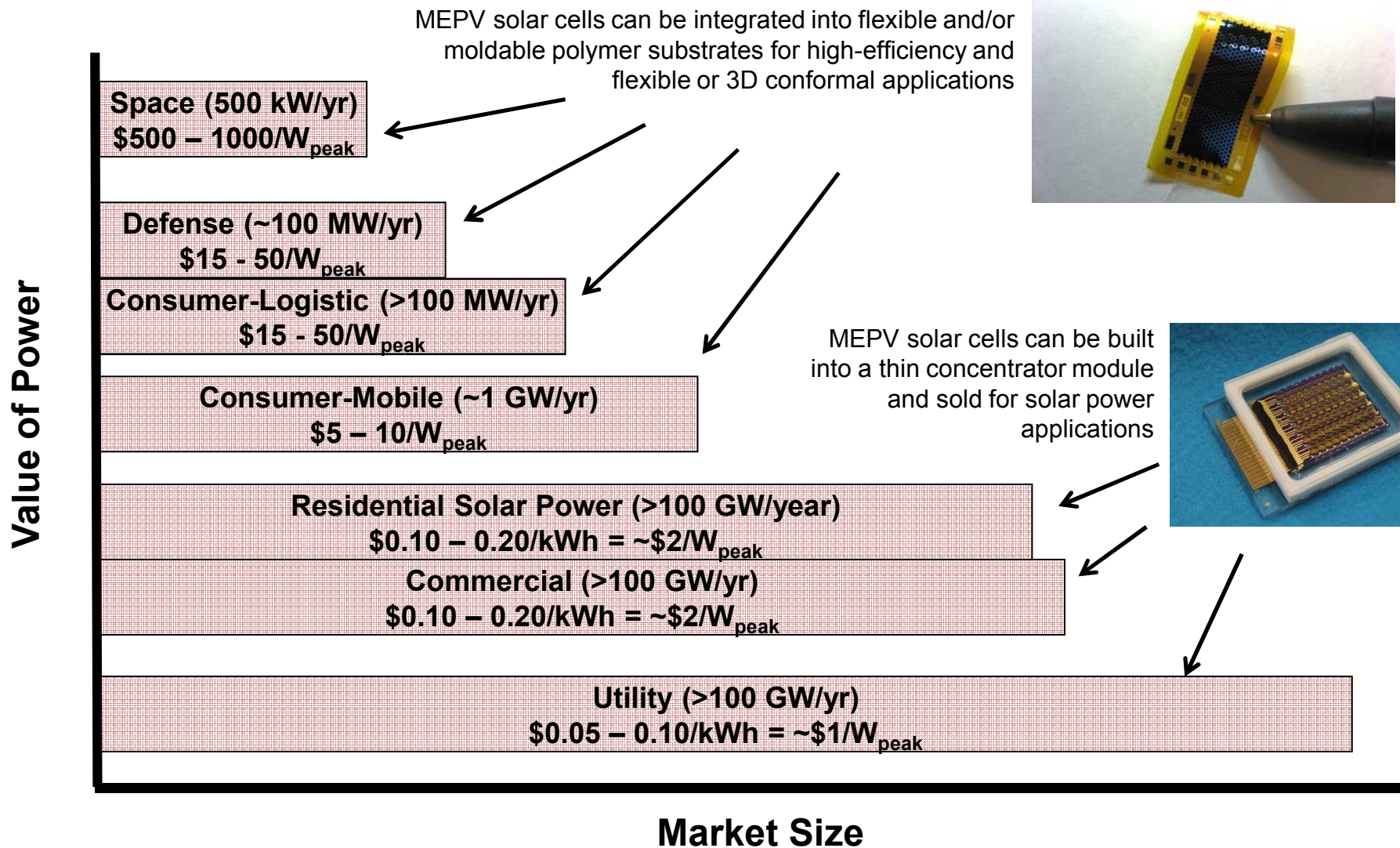
Modules with 3 junctions have the lowest 2020 system cost

# Commercialization

- Target cost and performance at product launch date
- Efficiency impact on system cost
  - System cost breakdown
- What is price/performance limit of c-Si?
- Rapid cost reductions create opportunities for module start-ups
- Usage/space constrained rooftops
  - Community Solar (Yeloha)
- Rooftop (distributed) vs. utility solar
- Policy driven industry
- Product test and code requirements
  - UL, IEC, NFPA, etc.



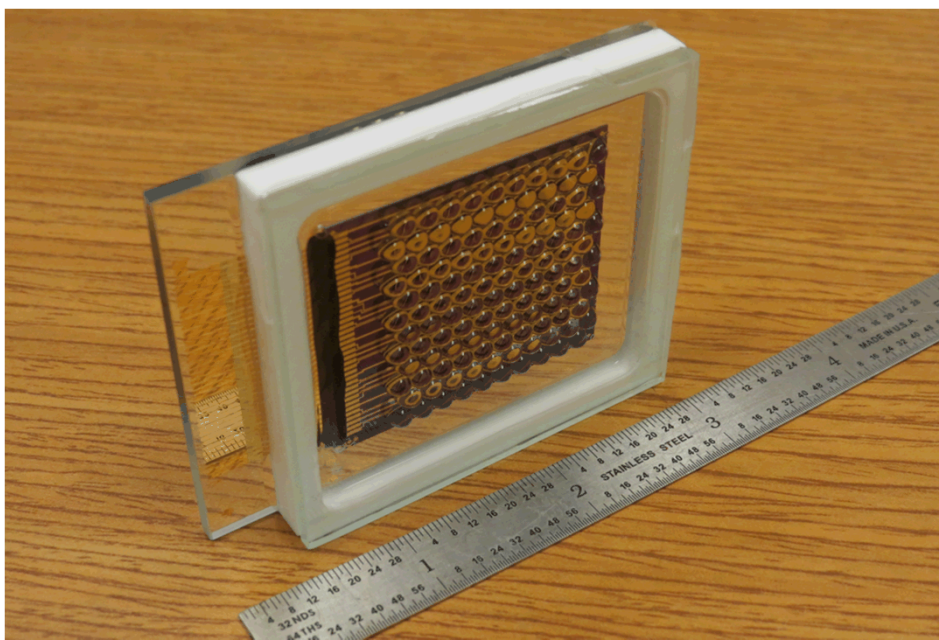
# Multiple Power Markets: PV to fit the system



# Conclusion

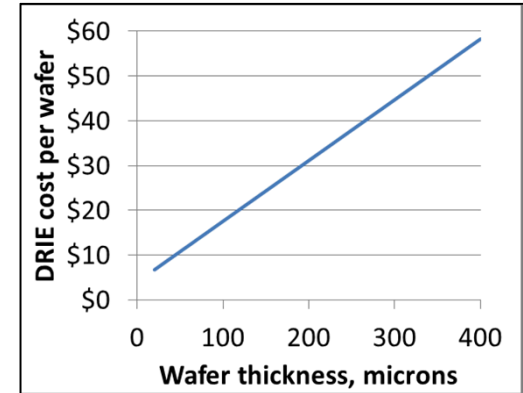
# Cost Model

- Costs as low as ~\$0.50/Wp are possible with module efficiencies of up to 35-40%
- Further cost reductions are potentially possible with further refinements of overall process flows, process steps, and module designs
- Cell processing, module components, and BOS are based on wafer Si PV where possible so cost reductions achieved by wafer Si PV may also benefit MEPV

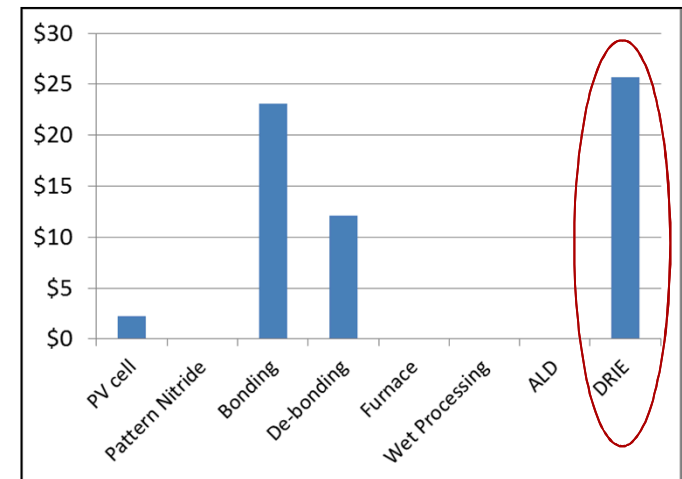
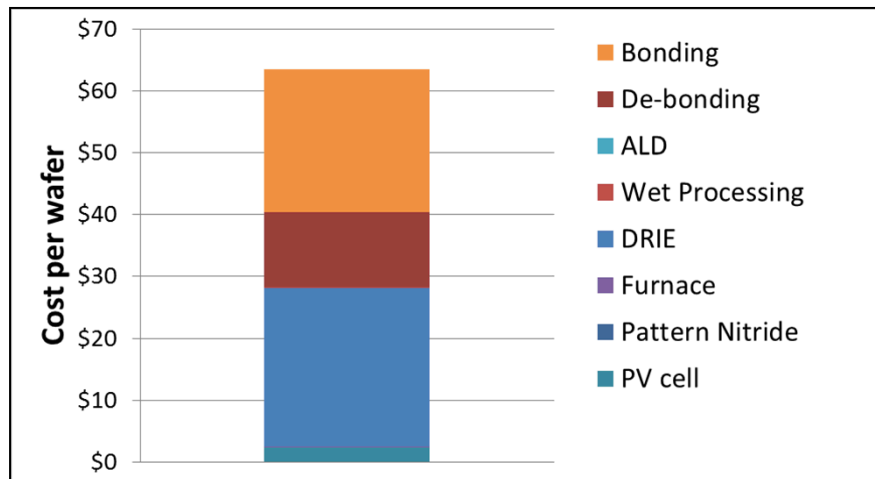


# Costs of III-V cell transfer and Si singulation

- Primary costs are temporary bonding/de-bonding and deep etch to define cells
- Etch (DRIE) cost increases with thickness  
→ Explore options to thin wafer before etch

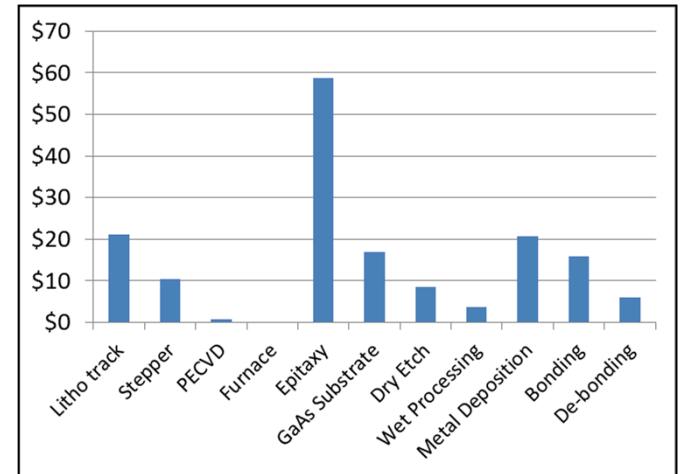
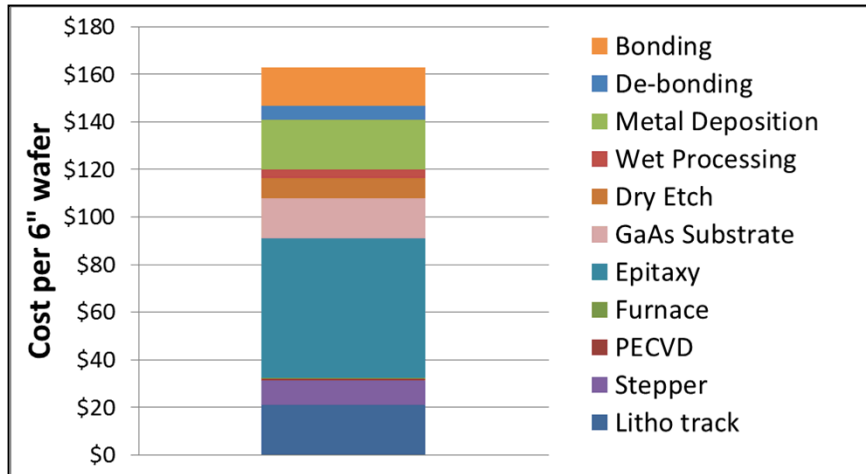


**Total cost: \$64/wafer**



# Current III-V processing costs

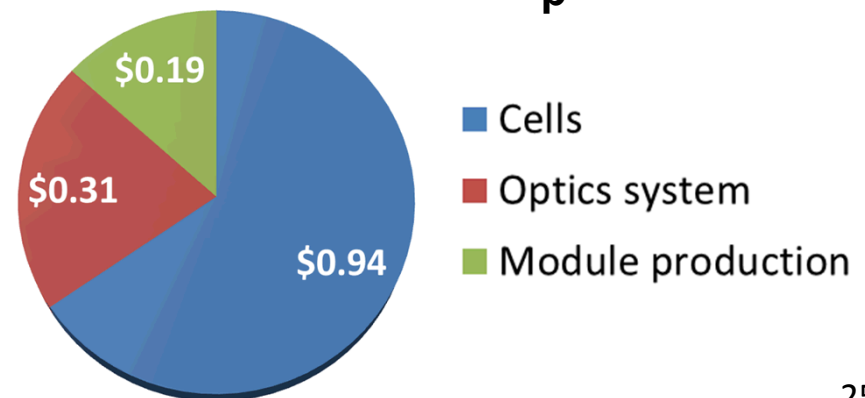
**Total cost: \$163/wafer**



## Prototype 3

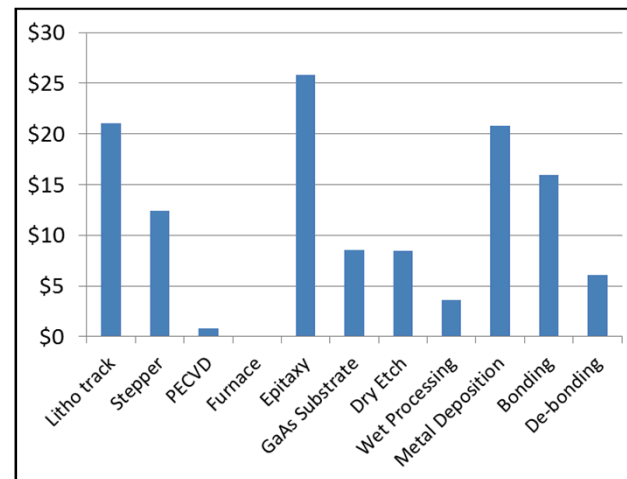
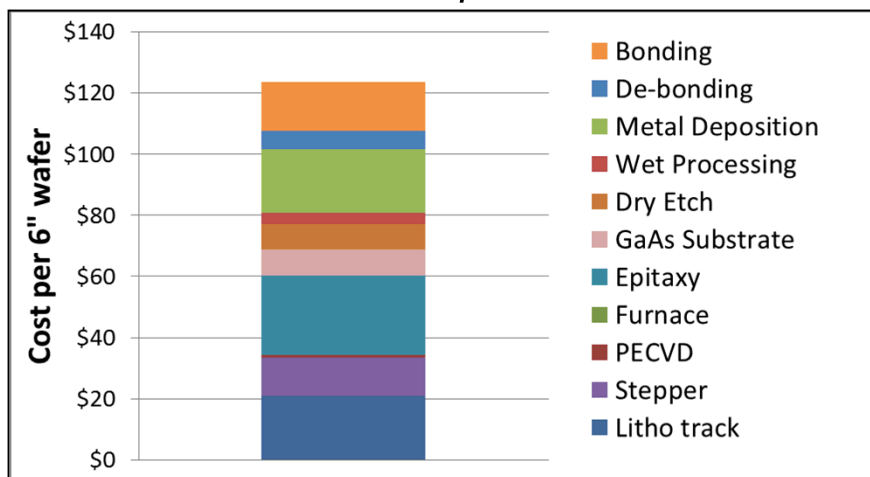
Current estimate: **\$1.44/W<sub>p</sub>**

- Epitaxy and GaAs substrates are the largest costs
- Other major costs:
  - Lithography
  - Metal deposition
  - Bonding/de-bonding



# Projected 2020 III-V processing costs

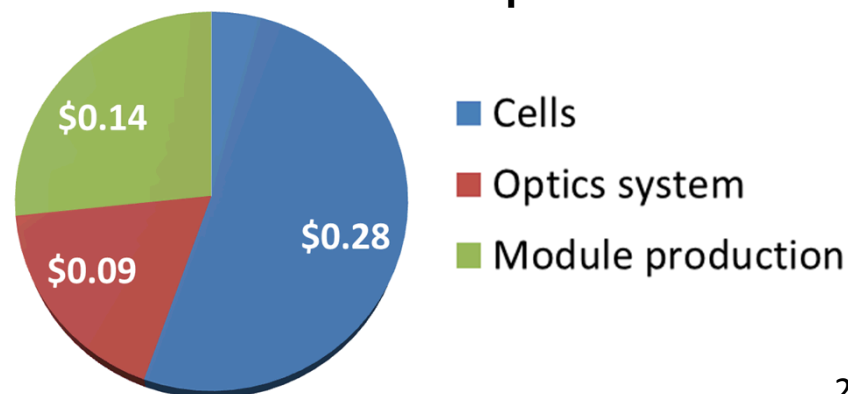
**Total cost: \$124/wafer**



## Prototype 4

2020 estimate: **\$0.51/W<sub>p</sub>**

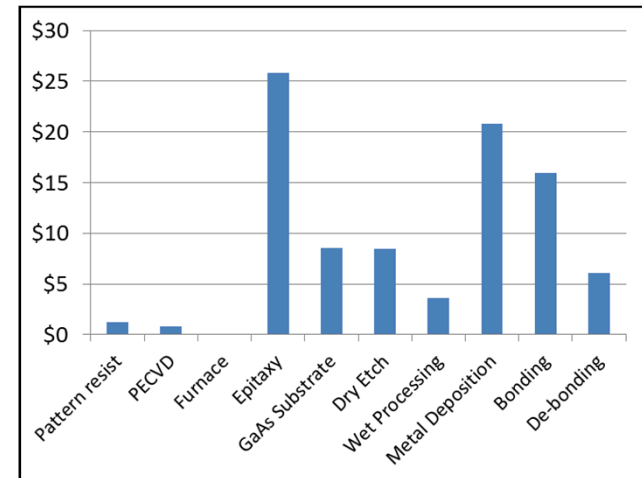
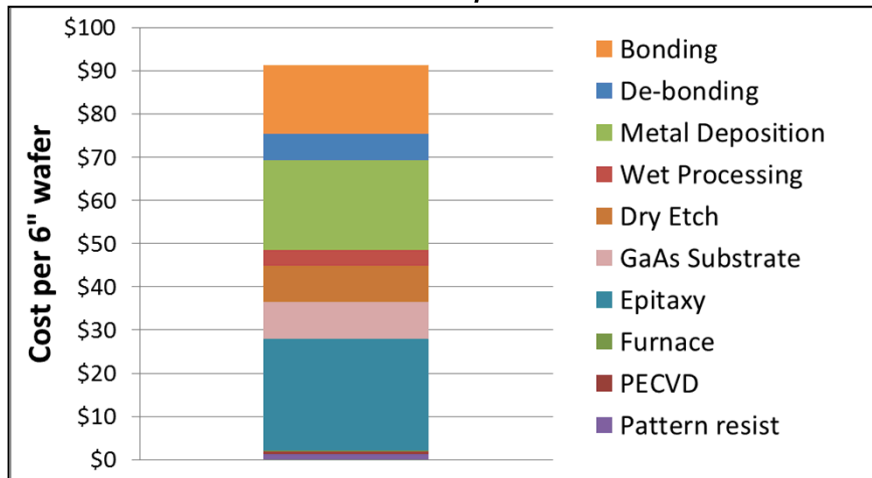
- Epitaxy process improvements specified by tool vendor
- Assume optimization of GaAs substrate re-use
- Also assume a thinner non-illuminated cell border





# Lithography-free III-V processing costs

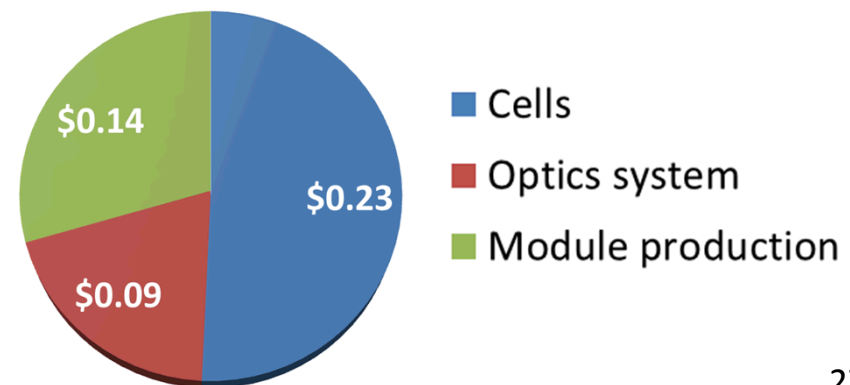
**Total cost: \$91/wafer**



## Prototype 4

2020 estimate: **\$0.46/W<sub>p</sub>**

- Alternatives to lithography :
  - Ink-jet printed resists
  - Aerosol printing
  - Laser ablation of nitride
- Each technology is significantly cheaper than lithography  
→ lower resolution is acceptable



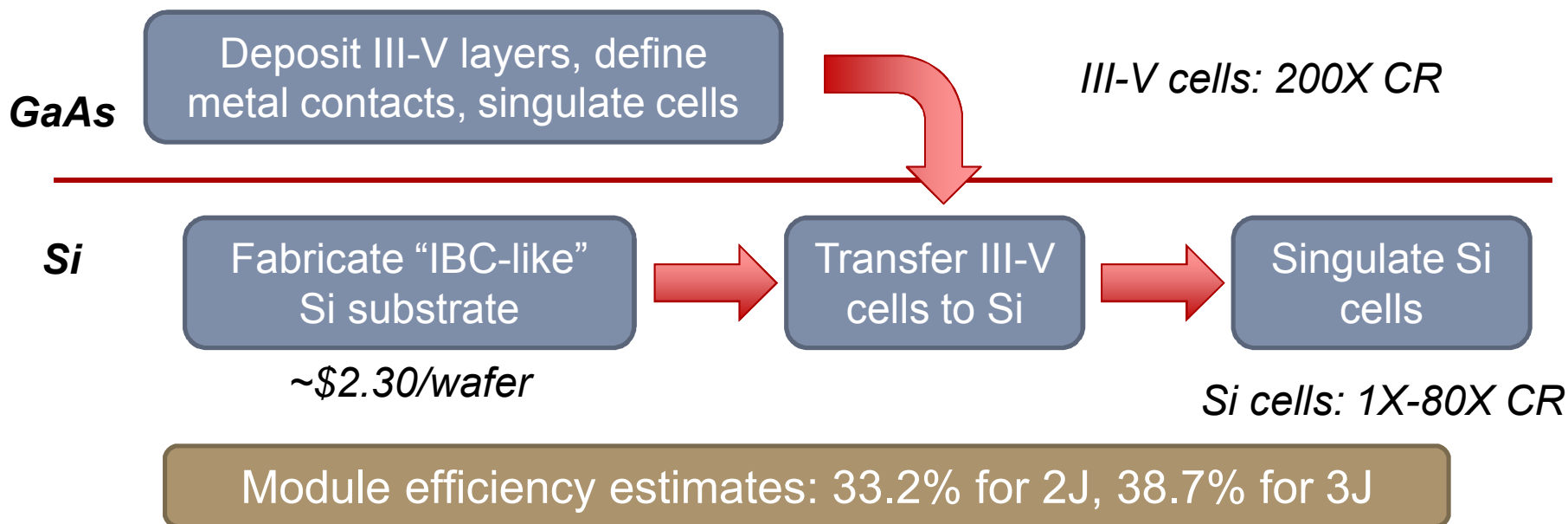
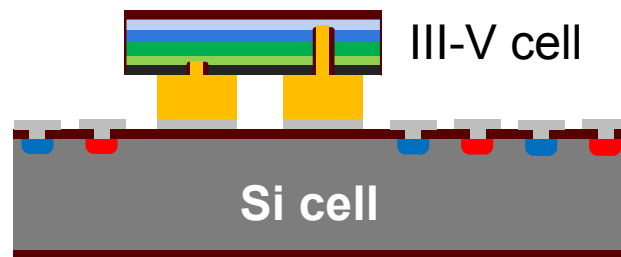
# MEPV cell production cost model

- Cell production cost is estimated on a per-wafer basis
  - Assume 6" GaAs substrates for III-V semiconductor processing
    - Final cell size: 250  $\mu\text{m}$  (200X concentration)
  - 8" silicon substrates
- Cost for each major process step is calculated based on estimates of equipment, materials, labor, and overhead costs
  - 200+ individual process steps
  - Each step corresponds with a single operation carried out by one piece of equipment
  - Equipment performance parameters obtained directly from vendors when possible

LITHOGRAPHY			Total Cost of All Litho			
Includes Coat, Expose, Develop, and Strip operations			Step 3	Step 4	Step 10	Step 11
Category	Item	Units	Value	Value	Value	Value
Process Definition			THERMAL OXIDE DEPOSITION			
Substrate Type	Substrate Dia		Step 3	Step 9	Step 10	Step 11
Wafer Track Model	Category	Item	Units	Value	Value	Value
Stepper or Coater	Process Definition		ETCH			
Vendor & Model	Substrate Type	Substrate Dia	Category	Item	Units	
Asher Vendor	Equipment		DRY ETCH			
	Thickness	Growth rate	Process Definition			
	Substrate Dia	Substrate Dia	Substrate Type	Substrate Dia	mm	
	Throughput	Throughput	Equipment	Equipment		
Input Performance Parameters			Input Performance Parameters			
Throughput	Throughput	Throughput	Etch Depth	Substrates/run	um	
Batch size	Batch size	Batch size	Etch rate	um/hr		
Cycle time	Cycle time	Cycle time	Etchant			
Resist usage	Resist usage	Resist usage	Etchant Flow	scm		
Developer usage	Developer usage	Developer usage	Intermediate Technical Calculations			
Throughput	Throughput	Throughput	Total Substrate Area	cm <sup>2</sup>		
			Cycle Time	hr		
			Etch time	hr		
			Etchant Total	liters		
Intermediate Technical Calculations			Cost Inputs and Calculations			
Litho time/hr	Litho time/hr	Litho time/hr	Labor	Man		
Wafer yield	Wafer yield	Wafer yield	Equipment			
Resist Usage	Resist Usage	Resist Usage	Installed Equipment Cost	\$		
Developer Usage	Developer Usage	Developer Usage	Maintenance Cost	\$/yr		
Number of wafers	Number of wafers	Number of wafers	Equipment Lifetime	yr		
			Equipment Overhead	\$/hr		
			Equipment Footprint	m <sup>2</sup>		
			Utilization	%		
			Average Power	kW		
			Raw Materials Costs			
			Etchant	\$/L		
			Output			
			Materials Costs			
			Labor Costs			
			Overhead Costs			
			Total Cost (no yield)			
			Cost/wafer			
Raw Materials Costs			Mask/Feticle	\$/yr	\$10,000	\$10,000
			Photoresist	\$/mL	\$0.158	\$0.158
			Developer	\$/mL	\$0.011	\$0.011
			Hg arc lamp	\$/yr	\$20,000	\$20,000
			None	-	\$0.000	\$0.000
Output			Process Step	3	4	10
						11

# MEPV cell fabrication

- Cell architecture: III-V cell bonded to a silicon cell
- III-V processing on 6" GaAs substrates
- Si processing on PV wafers → Assume a structure similar to interdigitated back contact cells (IBC)

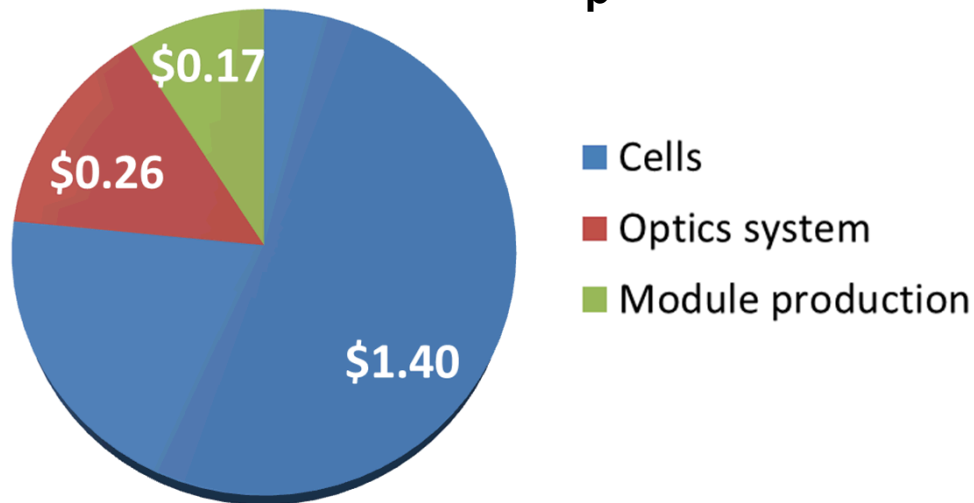


# Additional III-V junctions



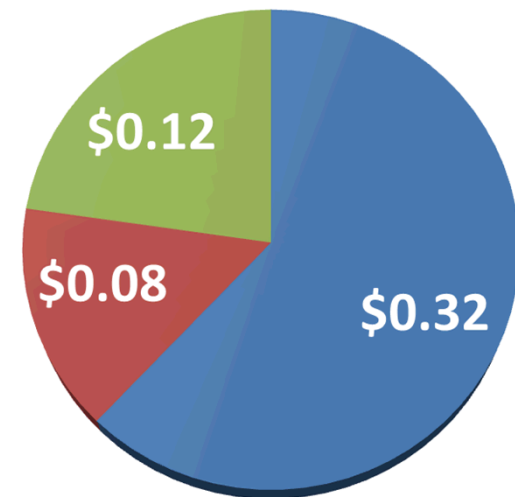
## Prototype 3

Current estimate: **\$1.83/W<sub>p</sub>**



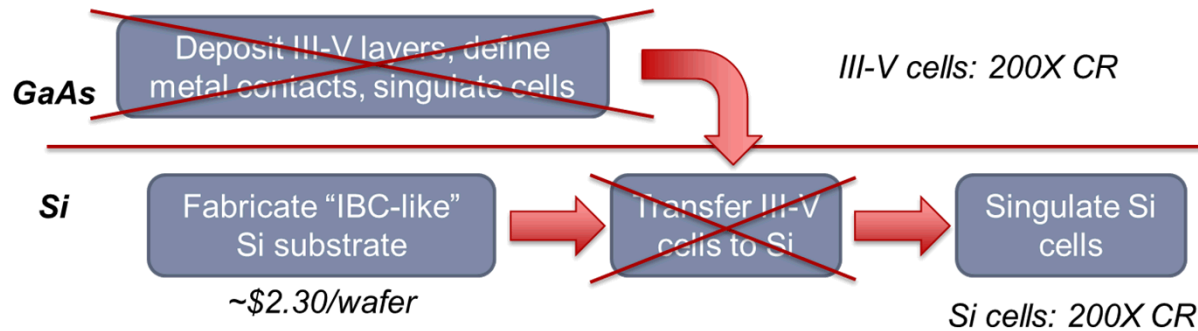
## Prototype 4

2020 estimate: **\$0.51/W<sub>p</sub>**



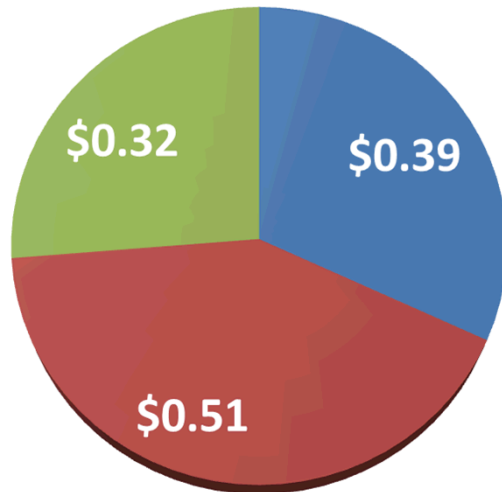
Addition of III-V junctions: Cell costs ↑ but efficiency ↑

# Single junction Si cells for MEPV



## Prototype 3

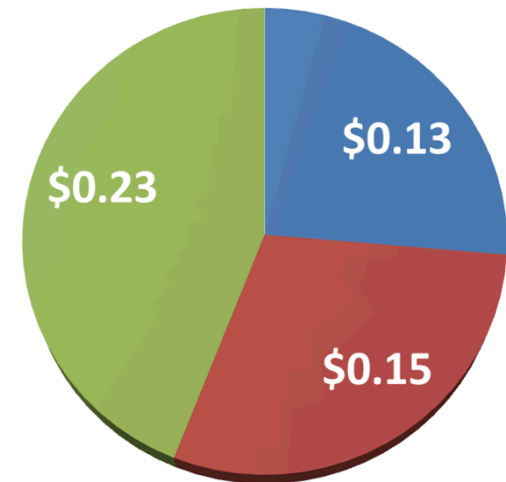
Current estimate: **\$1.22/W<sub>p</sub>**



- Cells
- Optics system
- Module production

## Prototype 4

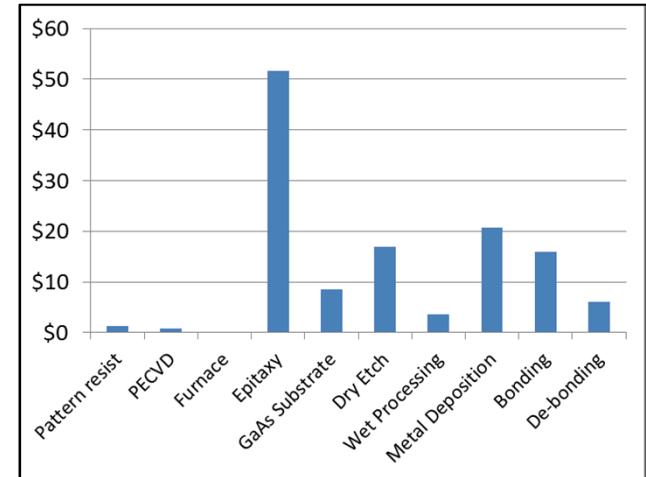
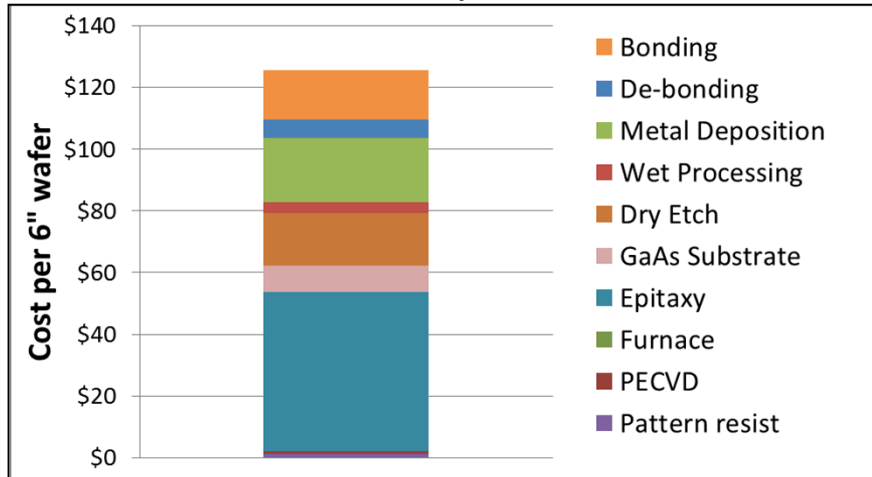
2020 estimate: **\$0.51/W<sub>p</sub>**



Elimination of III-V cells: Cell costs ↓ but efficiency ↓

# Inverted Metamorphic Multi-junction (IMM) cells

**Total cost: \$126/wafer**



## Prototype 4

2020 estimate: **\$0.36/W<sub>p</sub>**

- Grow 3-junction cells on one GaAs substrate
  - No silicon cells → Transfer directly to modules
- III-V processing costs ↑ slightly, but Si costs are eliminated
  - Estimated module efficiency: 40%

