SAND2016-1348PE

Sandia National Laboratories

SECANT QKD Grand Challenge LDRD

Sandia Enabled Communications and Authentication Network using Quantum Key Distribution

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LDRD

Chip-scale Quantum Photonics

Paul Davids and Team

U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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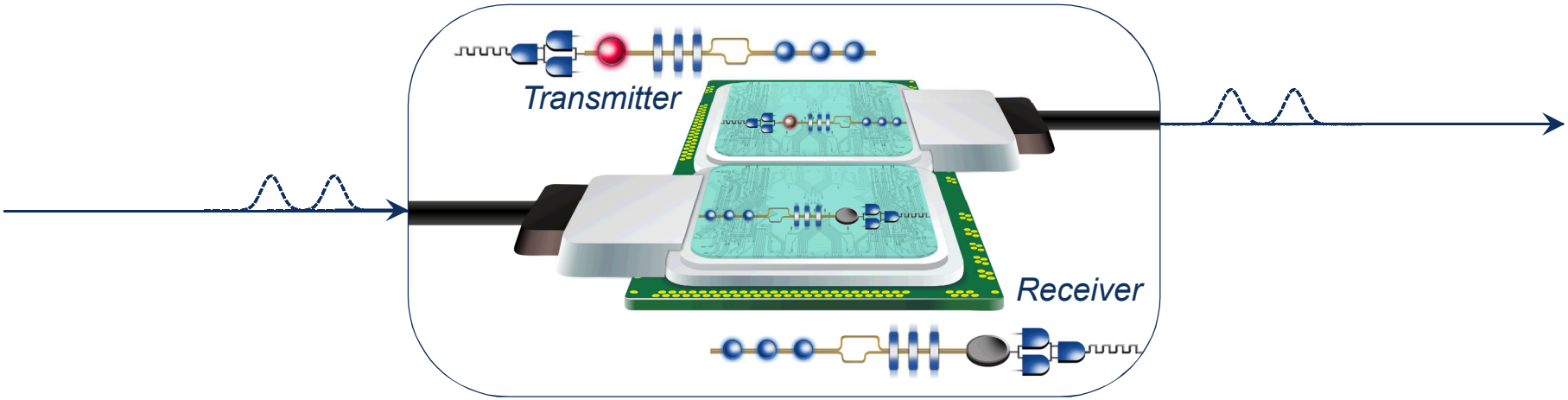
Team

- *SPD Development:* Chris DeRose, Nick Martinez, Andrew Starbuck, Andy Pomerene, Reinhard Brock, Doug Trotter.
- *CV-QKD & QCFC:* Chris DeRose, Daniel Soh, Mohan Sarovar, Andrew Hollowell, Mark Ballance, Chris Nordquist.
- *Heterogeneous Integration:* Bruce Burckel, Andy Pomerene, Chris DeRose, Erik Skogen, Jeff Cederberg, Anna Pedretti-Tauke.
- PI- Ryan Camacho/ PM – Dan Barton.

Chip-scale Quantum Photonics



- Develop a chip-scale quantum photonics platform.
- Leverage Si Photonics development for large scale integration.
- Why?
  - Multi-node complex quantum circuits for quantum networks.
- 1st Application: Quantum Key Distribution

State of the Art

- Many groups pursuing chip-scale quantum photonics
  - Bristol, NIST, UCSD, MIT, Oxford, ORNL, LANL, Duke, Toshiba, CUDOS ….. and many more.
- Sandia is uniquely positioned
  - Co-located CMOS fabrication facility with III-V fabrication facility.
  - CMOS compatible Si photonics platform.
  - III-V Photonics platform and high performance electronics.

Core Silicon Photonics

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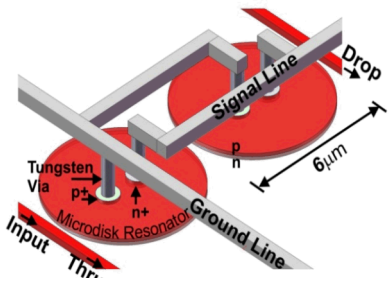
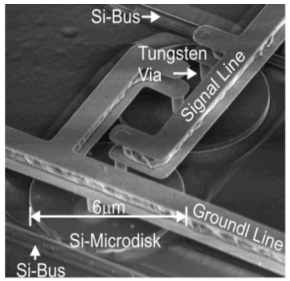
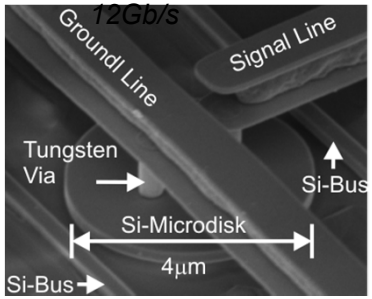
Free-carrier Effect (high-speed)

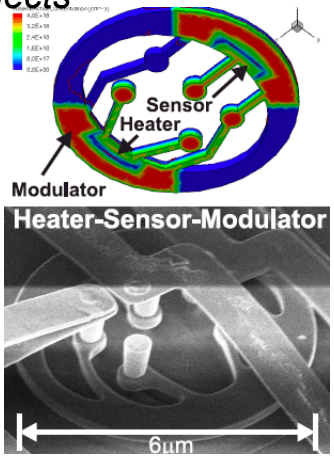




Fast Reconfigurable Interconnects

3.2fJ/bit at 12Gb/s



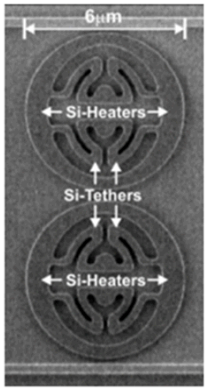


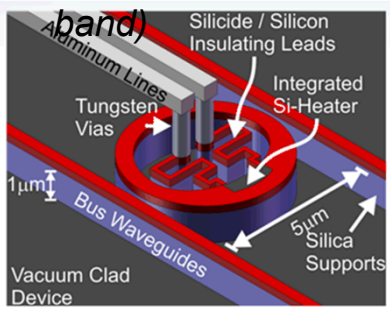
Resonant Optical Modulator/Filter

Thermally stabilized modulator

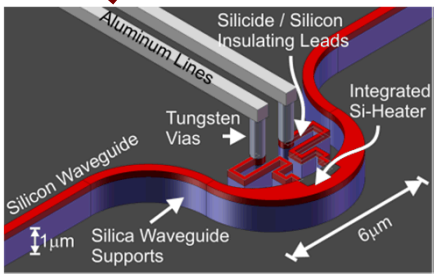
Broadband Mach-Zehnder Filter/Switch < 1V-cm at 10 Gb/s

Thermal Optic Effect (wide-band)

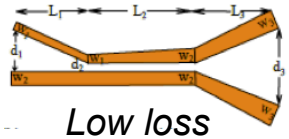




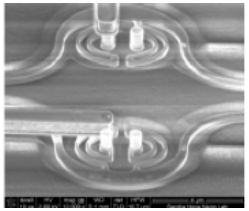
Tunable Resonant Filt



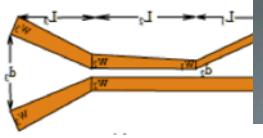
Thermo-optic Phase Shifter

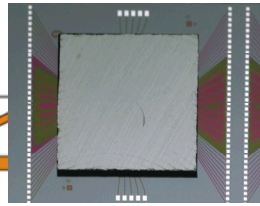


Low loss optical coupler

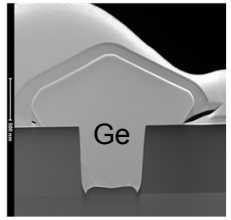


Switch Arrays

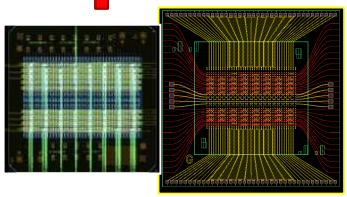




High-speed Ge Detector in



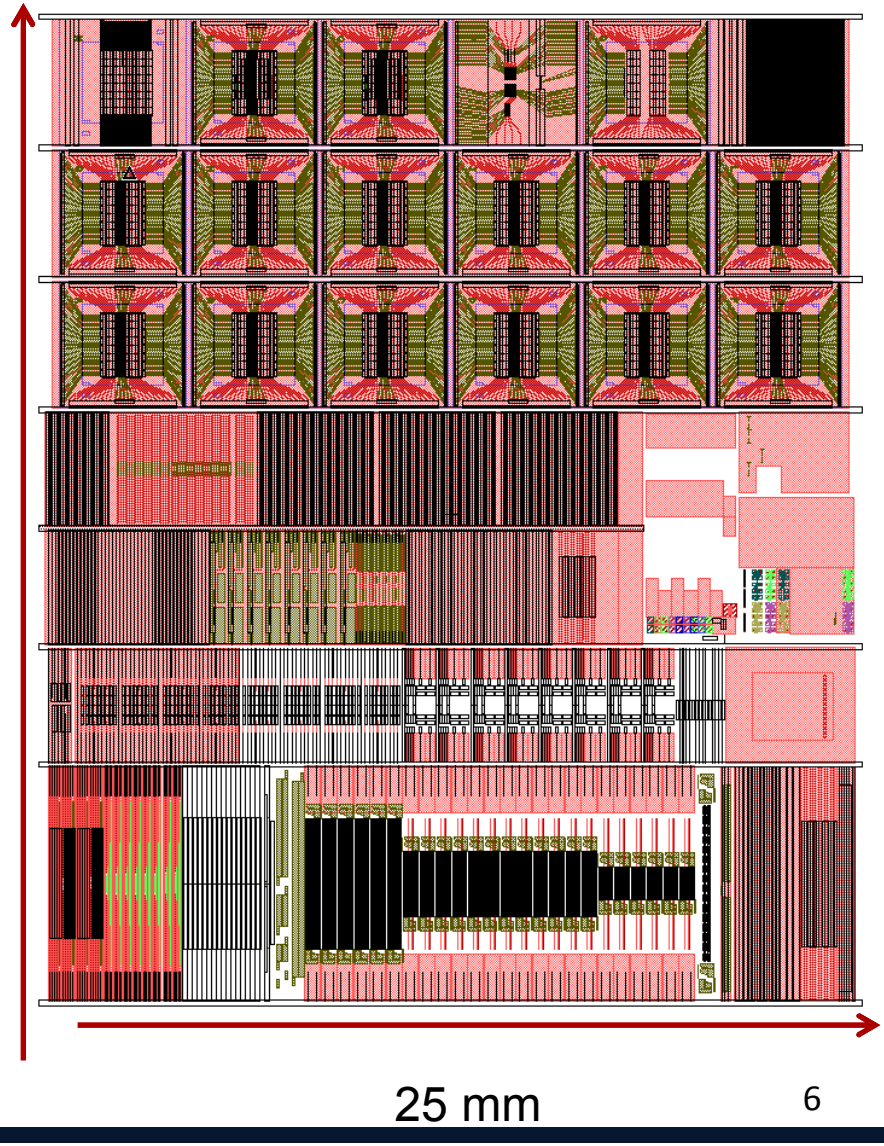
Si Photonics-CMOS Integration



Integration Advantages

- High data rate – multiple wavelengths per channel
  - Requires dense integration.
  - High index contrast system – compact devices
- CMOS compatible photonics
  - Leverage existing infrastructure
  - Large number of active devices (SPAD's)
  - Low cost
- High efficiency
  - Compact devices – give lower dark current
  - Ge on Si offers best chance for integrated compact devices.

Optical Transceiver for Exascale



Chip-scale Quantum Photonics Platform

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- Key Platform Components
  - Single Photon Detection (SPD) Capability
  - Single Photon Source (SPS)
- Heterogeneous integration methods
  - Enable integration of SPS
  - Non-linear media and incompatible new devices
- Differences between bench-top and chip-scale quantum optics.
  - Loss, polarization, dispersion and mode conversion.
  - Waveguide non-linearities

Outline

- Highlight early progress in 3 areas:
  - Integrated Single Photon Avalanche Detector (SPAD)
  - Integrated quantum optoelectronic circuits
  - Heterogeneous integration of III-V laser source on Si Photonics substrate.

Ge in Modern CMOS

Germanium old semiconductor technology.

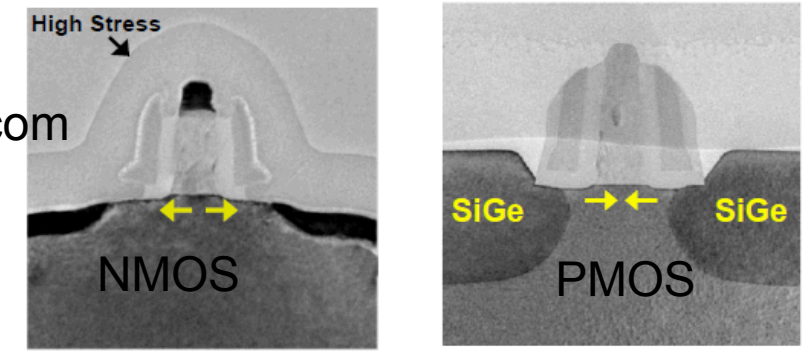
- Indirect Bandgap at 0.66 eV.
- Direct Bandgap at 0.8 eV (1550 nm) in telecom band.
- Not efficient optical emitter.

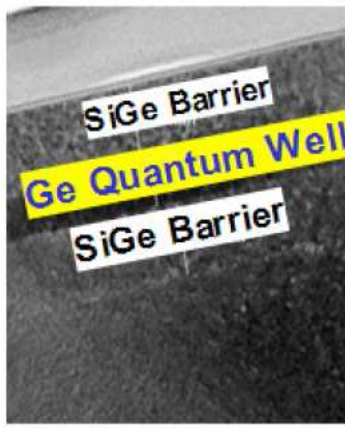
Selective epitaxial growth of Ge on Si has enabled advanced strain engineering in modern CMOS.
Fully CMOS Compatible.
High electron and hole mobilities.

Ge optoelectronics: direct bandgap at 1550nm implies good absorption.

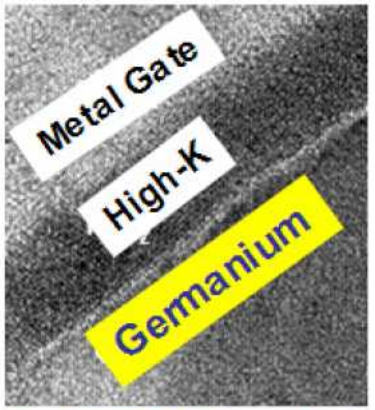
Strain engineering in CMOS

Intel 45nm





Ge Quantum-well



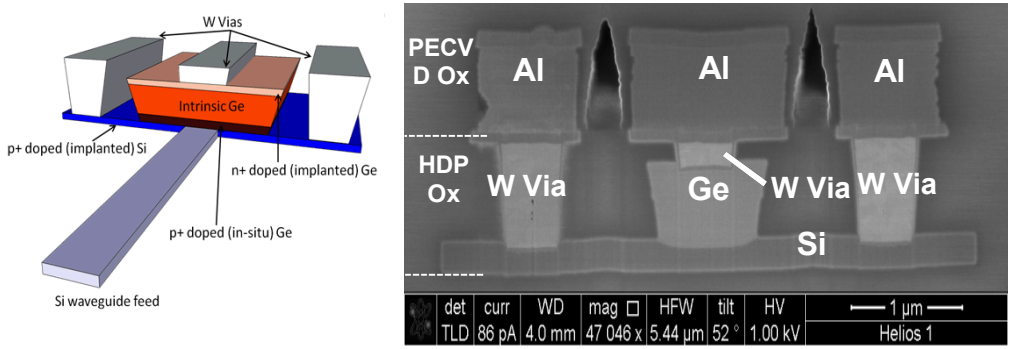
Ge MISFET Transistor

Sources: (1) ESSDERC 2008, (2) www.intel.com/silicon research/R&D pipeline

Ge on Si Detector Development

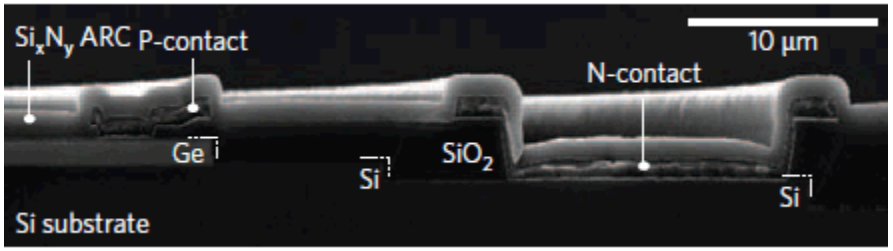
Compact high speed photodiode

Sandia



Ge on Si Avalanche Photodiode

Intel, UCSB, UVa



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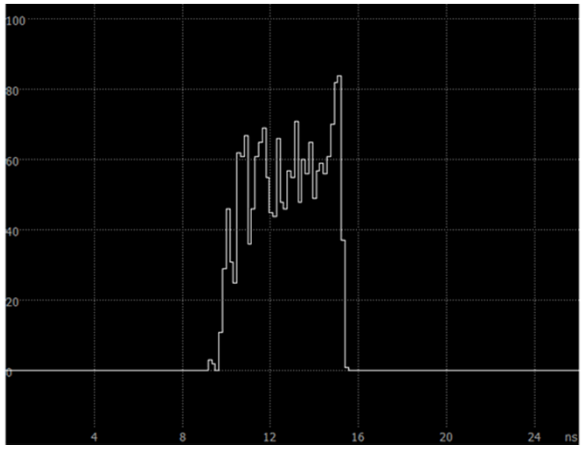
5 December 2011 / Vol. 19, No. 25 / OPTICS EXPRESS 24897

- Integrated waveguide Ge on Si photodetector demonstrated best in class performance.
- Ge on Si linear mode separate absorption multiplication avalanche photodiode demonstrated 340 GHz gain bandwidth product.
- **Combining new device concepts would enable integrated single photon detection and launch Quantum Si Photonics.**

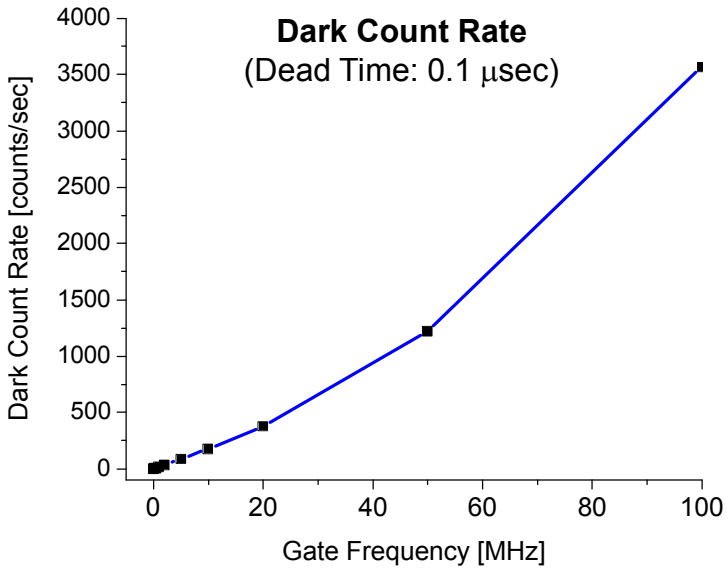
Target integrated SPAD performance

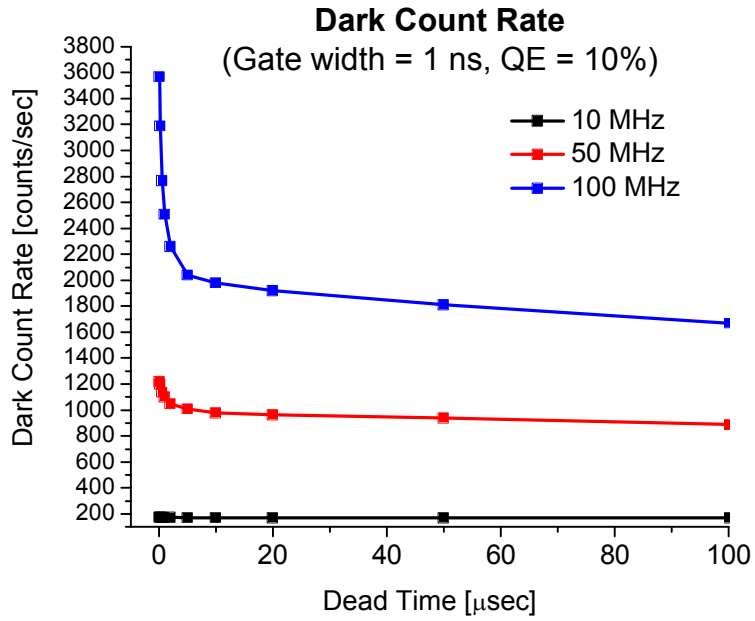
IDQ InGaAs APD



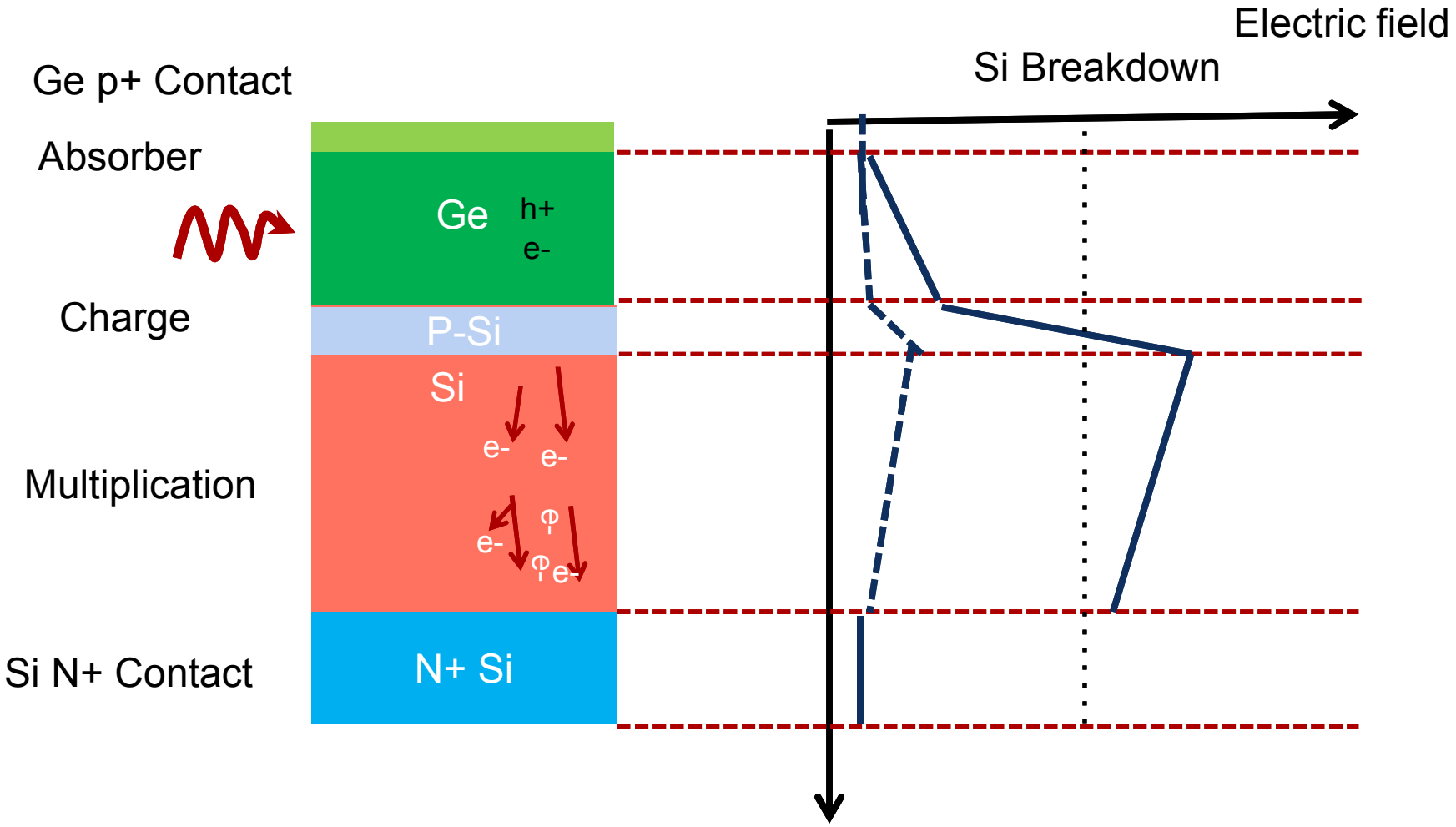
TDC Gate Width Histogram

Product	InGaAs SPAD
QE at 1550nm	10-25%
Spectral range	950-1600
Dark count rate	<10kct/s
Timing resolution	<300 ps
Afterpulsing	1%
Detection rate	100MHz (trigger)
Gate width	0.1 - 100 ns
Hold-off time	1 - 3000us
Price	$25k



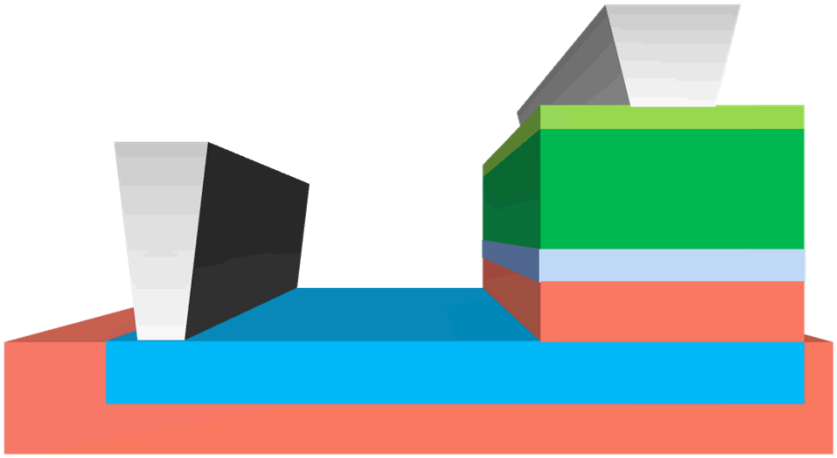


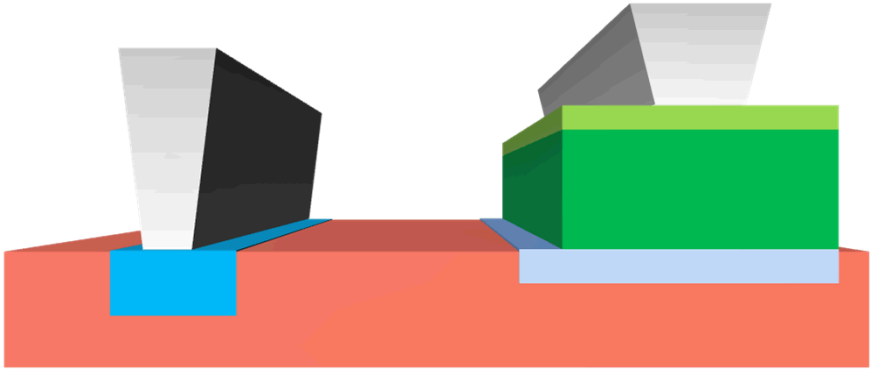
Separate absorption and charge multiplication APD.



Separate absorption and charge multiplication APD.

Two types of Ge on Si SACM





- Selective Si & Ge epi growth.
- In-situ doped charge layer.
- Vertical multiplication.

- Selective Ge epi growth.
- Implanted charge layer
- Lateral multiplication.

Integrated Waveguide Coupled SPD

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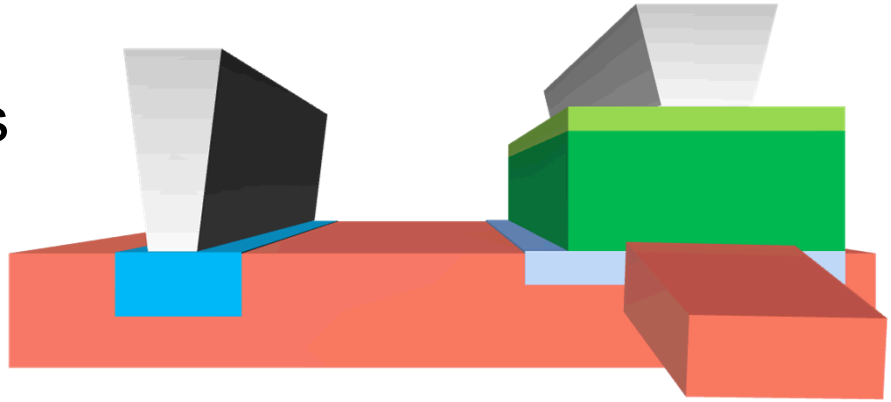
Two coupling types

Si end-fired



P+ Ge

Ge

Si

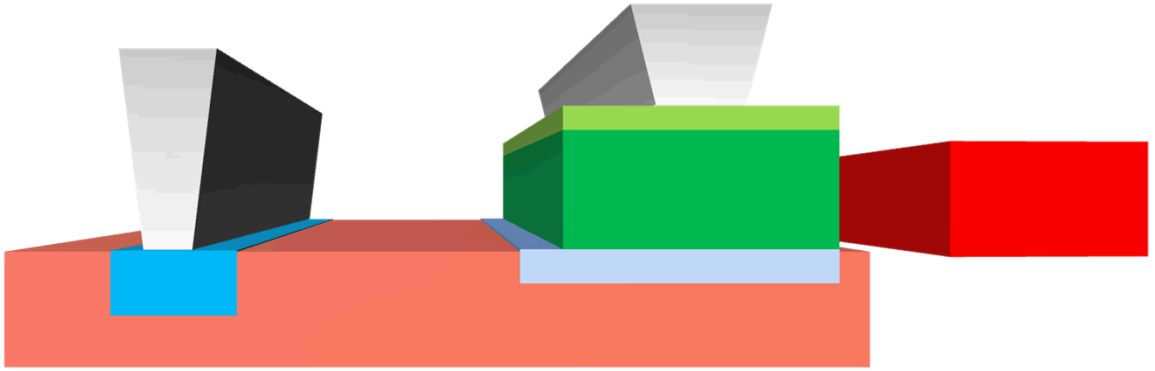
P-Si

N+ Si

Nitride

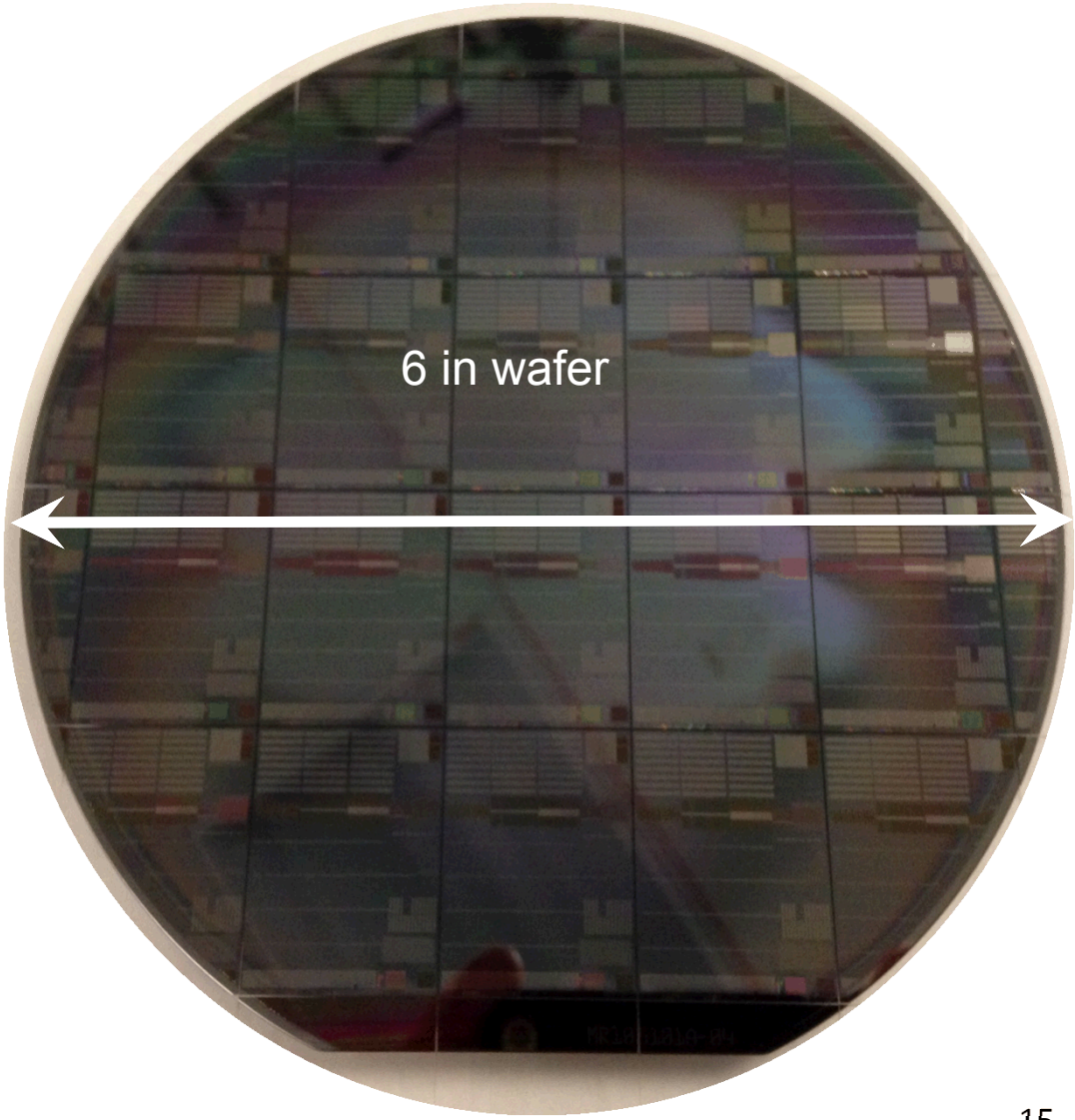
For vertical and lateral APD

Evanescent coupled

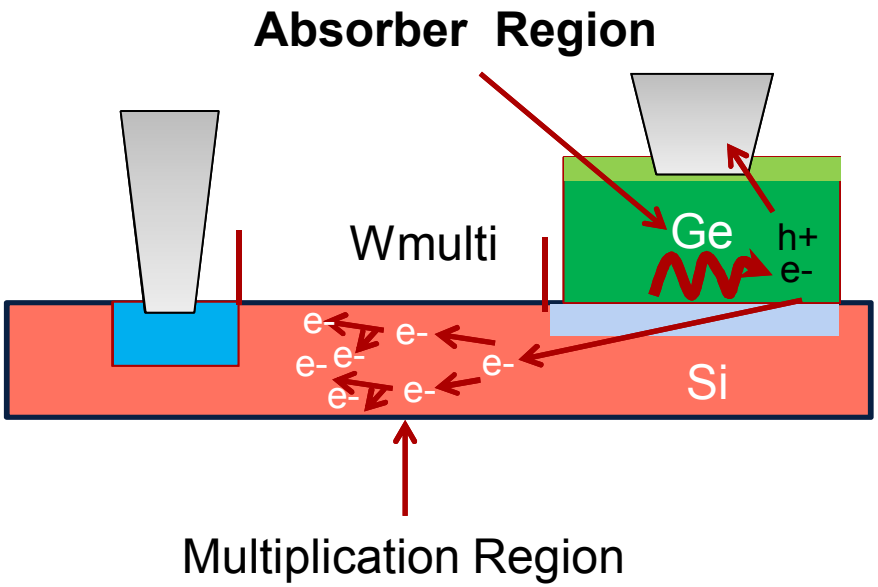


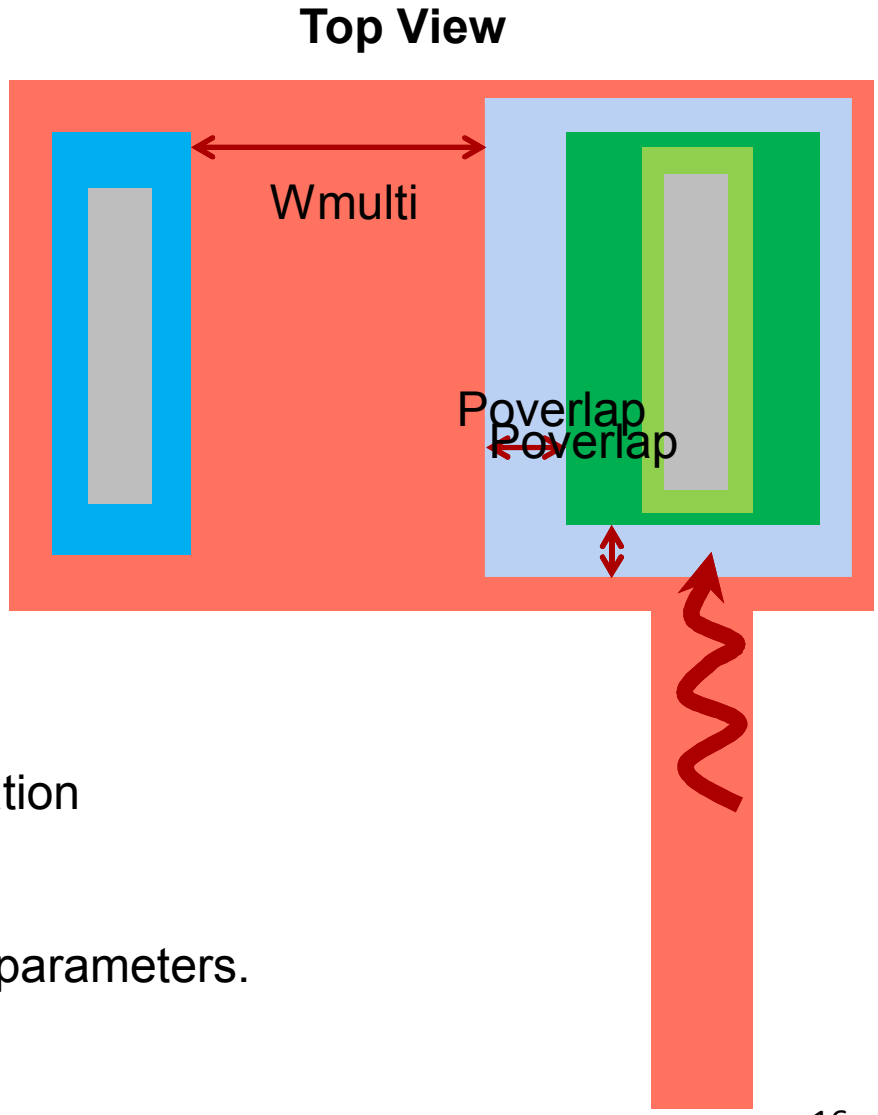
SPAD Test-Chip

- SPD test –chip
- 24 wafers
- Lateral and vertical designs
- Si and nitride waveguide coupled
- Optimized Device and Process Splits.
- Automated testing required



Integrated lateral APD results



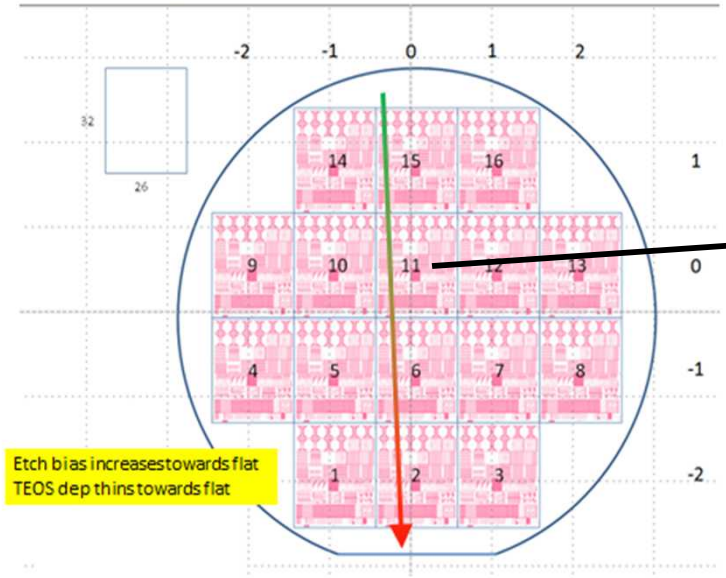


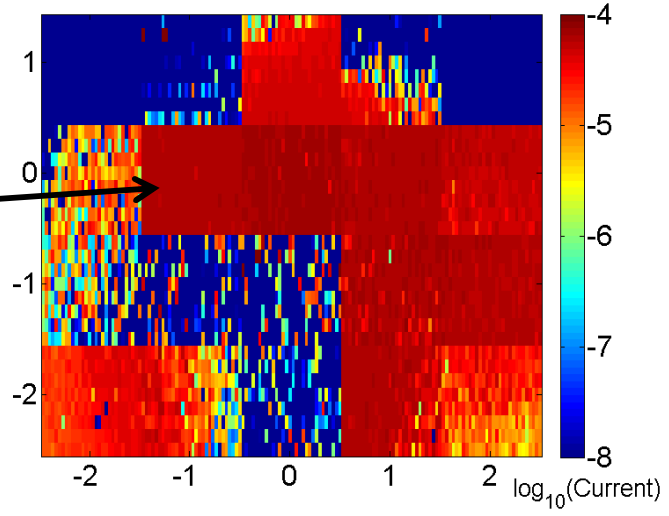
Lateral APD in X-section

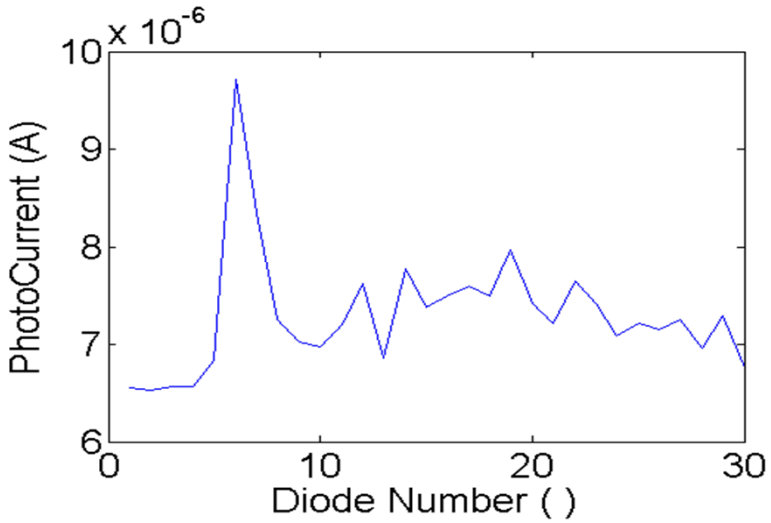
Top down view shows variation of multiplication Width and p-Charge layer overlap.

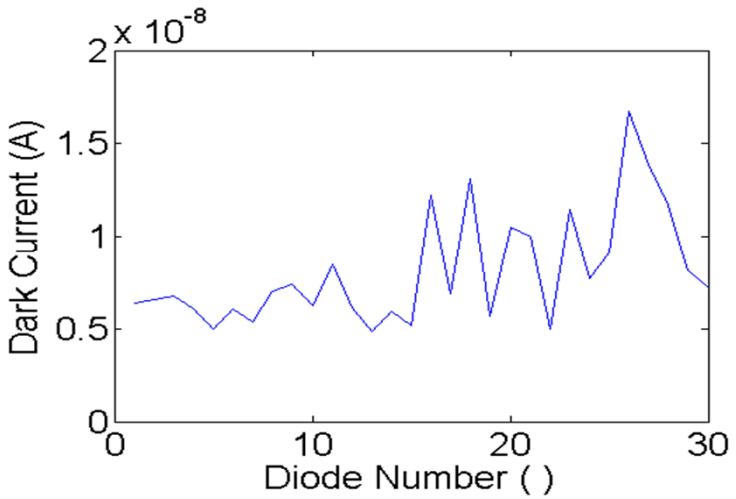
Together with implant doses we vary these parameters.

Die Map: Yield & Calibration







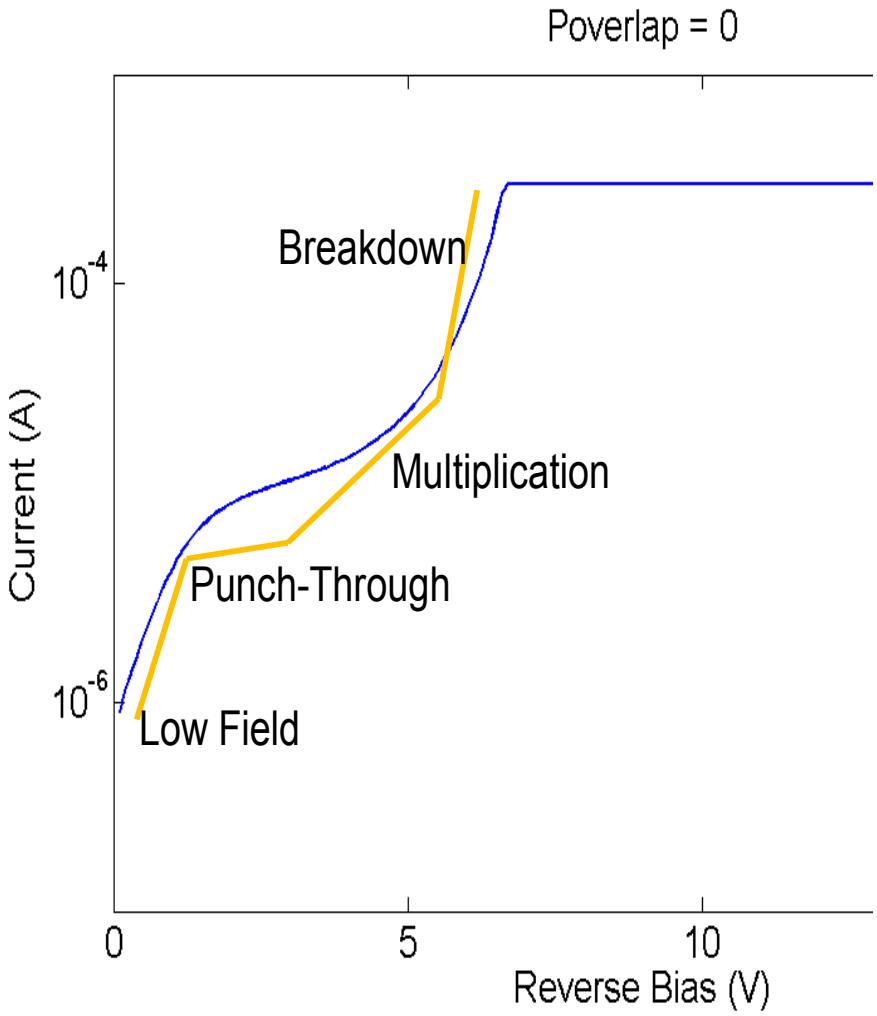


Experimental illumination condition

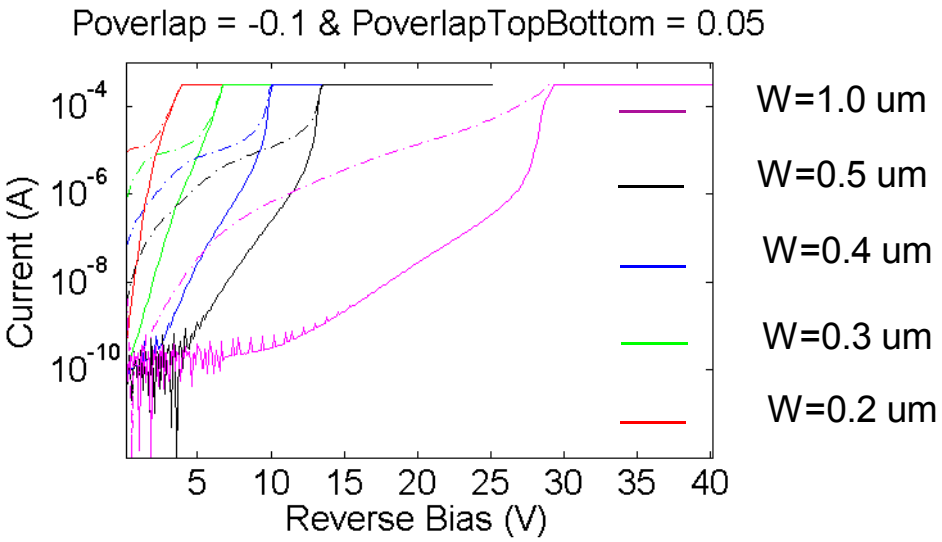
- Done with 100 uW incident on grating coupler
- Wavelength set to 1540 nm.
- Estimate ~ 8 uA photocurrent in equivalent PIN structure.
- Fiber array position optimized fo each measurement.

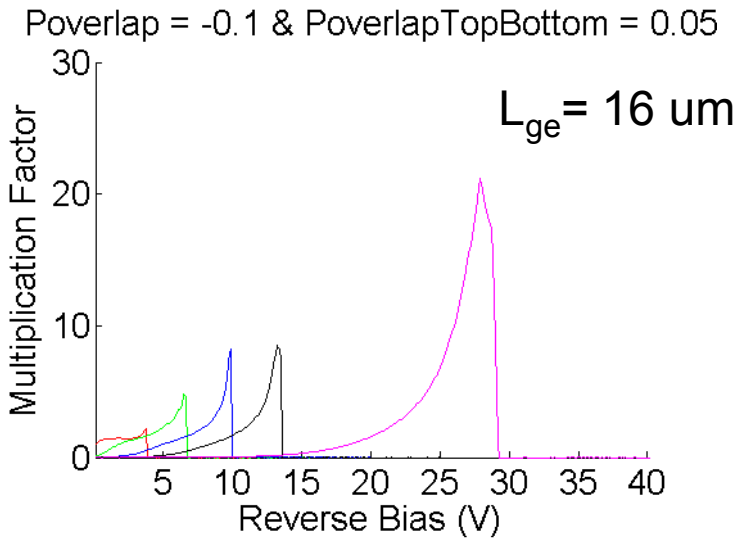
- Automated APD measurements
- APD Gain approximated by

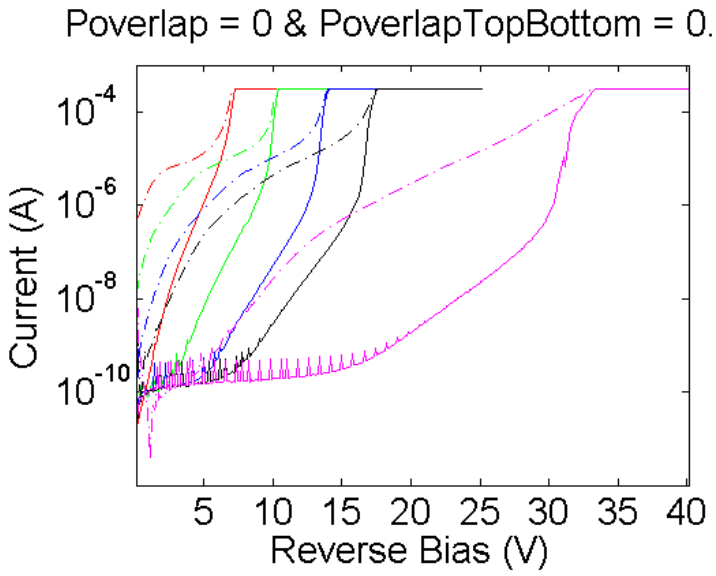
$$M = (i_{light} - i_{dark})/8uA$$

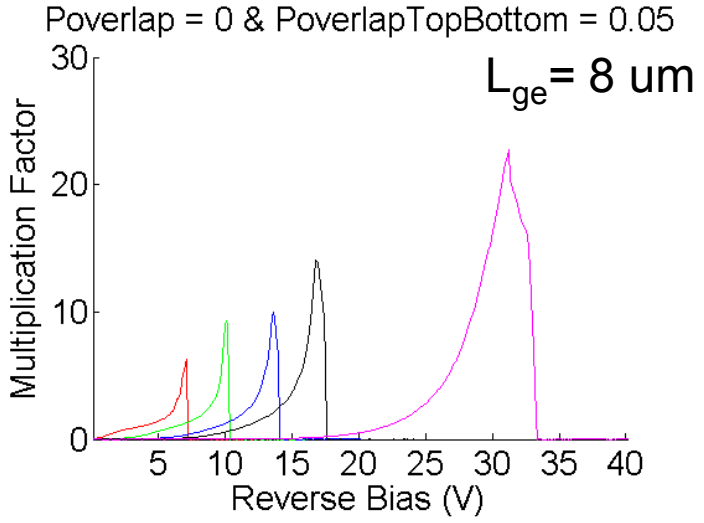


Linear mode APD measurements







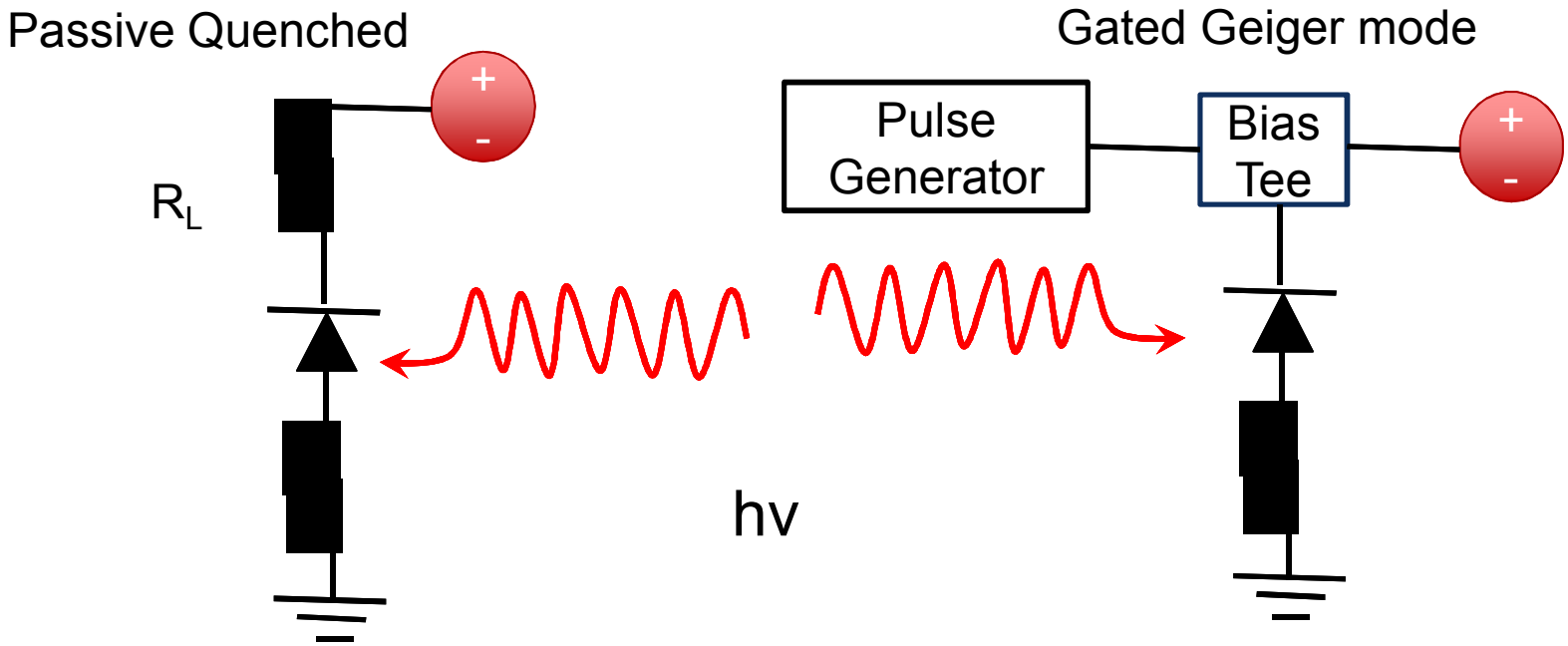


Summary of Linear mode APD's

- Waveguide coupled linear mode APD's show multiplication gain exceeding M> 20.
- Compact nature of device ~16 μm^2 gives
  - Higher strain and responsivity for wavelengths > 1550 nm.
  - Low dark current.
  - Low capacitance.
- High speed testing underway for determination of gain-bandwidth product.
- Useful in low noise receiver application.

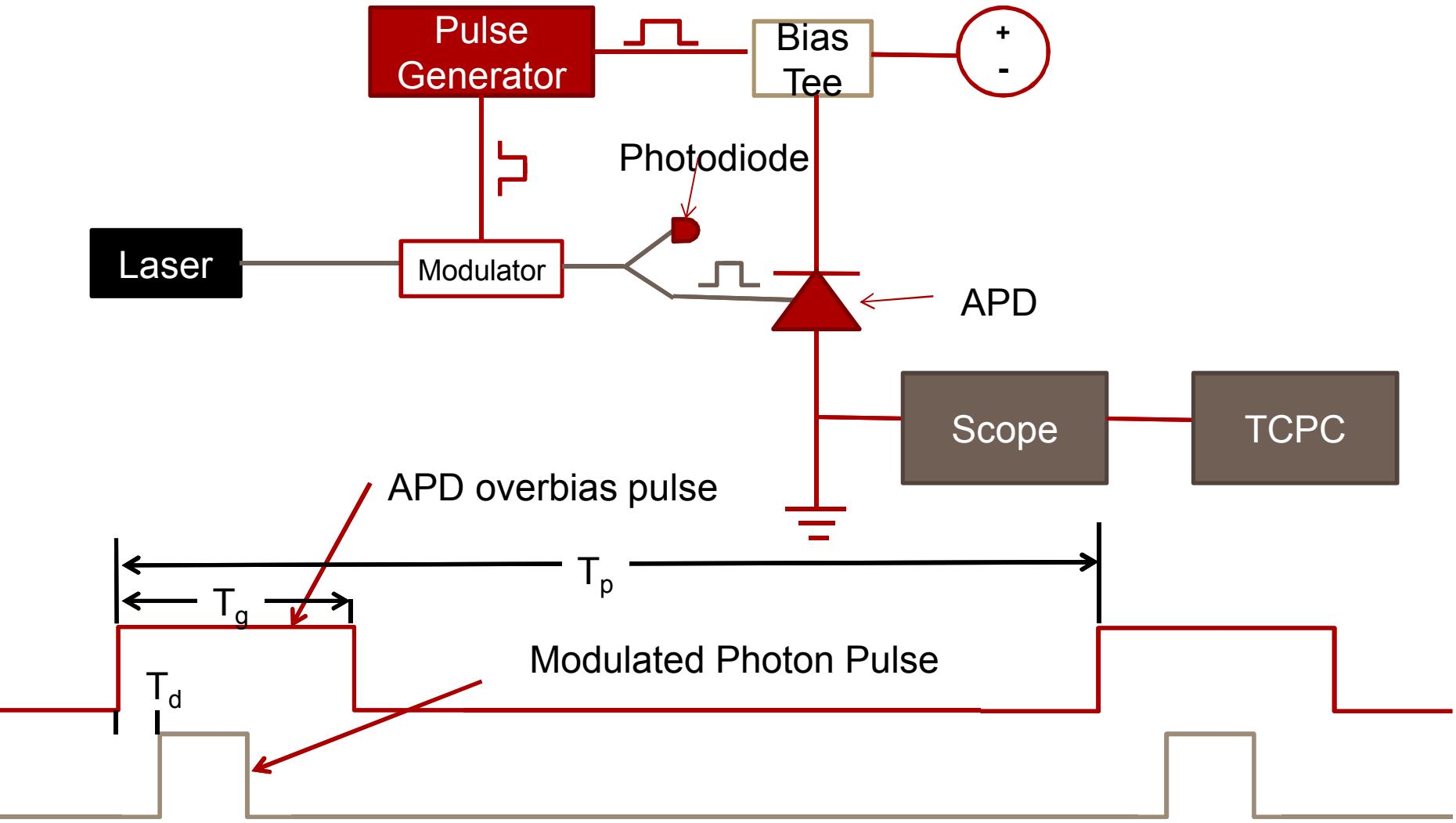
Geiger mode operation enables single photon detection.

Geiger mode APD (SPD)

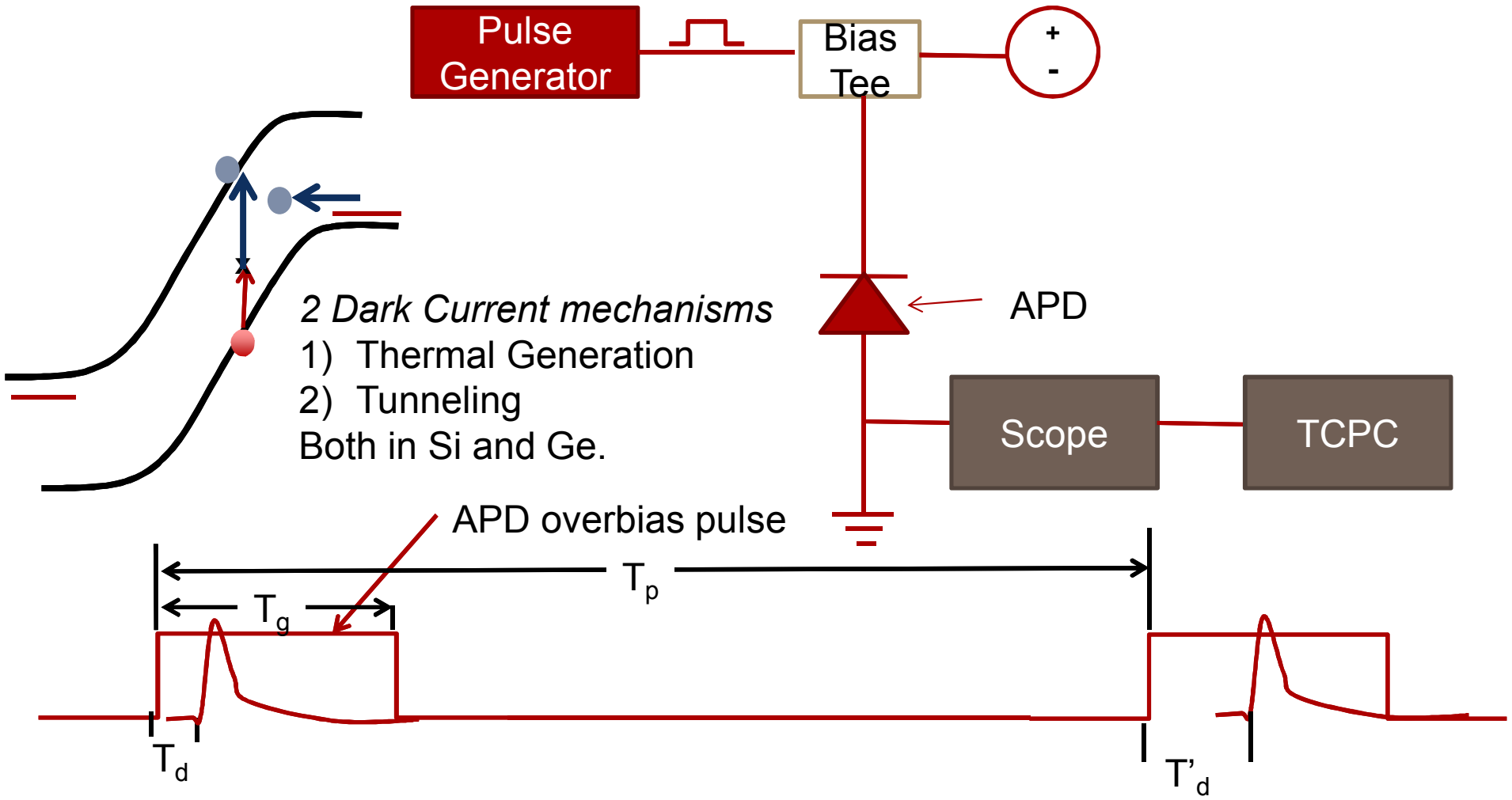


- Two types of Geiger mode operation
  - Passively quenched
    - External quench resistor R_l
  - Gated Geiger mode
    - Electronic gate and photon pulse are timed with variable delay.

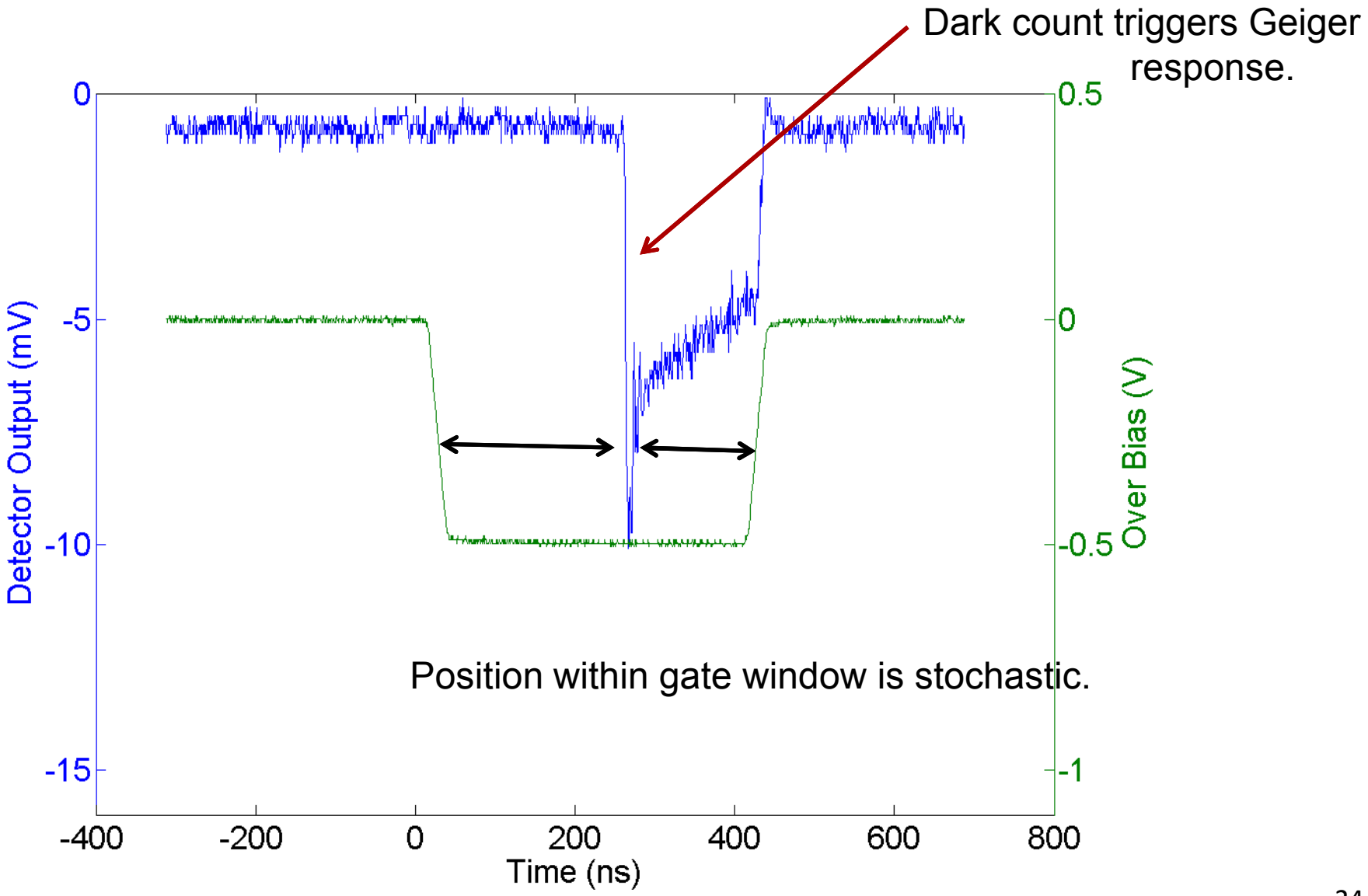
Gated Geiger Mode Setup



Dark Count Measurement



Measured Dark Counts



Dark Count Rate

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Dark count probability: p_d
Dark count rate: ρ

$$p_d = 1 - \exp(-\rho T_g)$$

$$p(n) = \frac{\mu^n}{n!}\exp(-\mu)$$ ← Poisson distribution

$$p(n \geq 1) = \exp(-\mu)\sum_{n=1}^{\infty}\frac{\mu^n}{n!} = \exp(-\mu)\left(\exp(\mu) - 1\right) = (1 - \exp(-\mu))$$

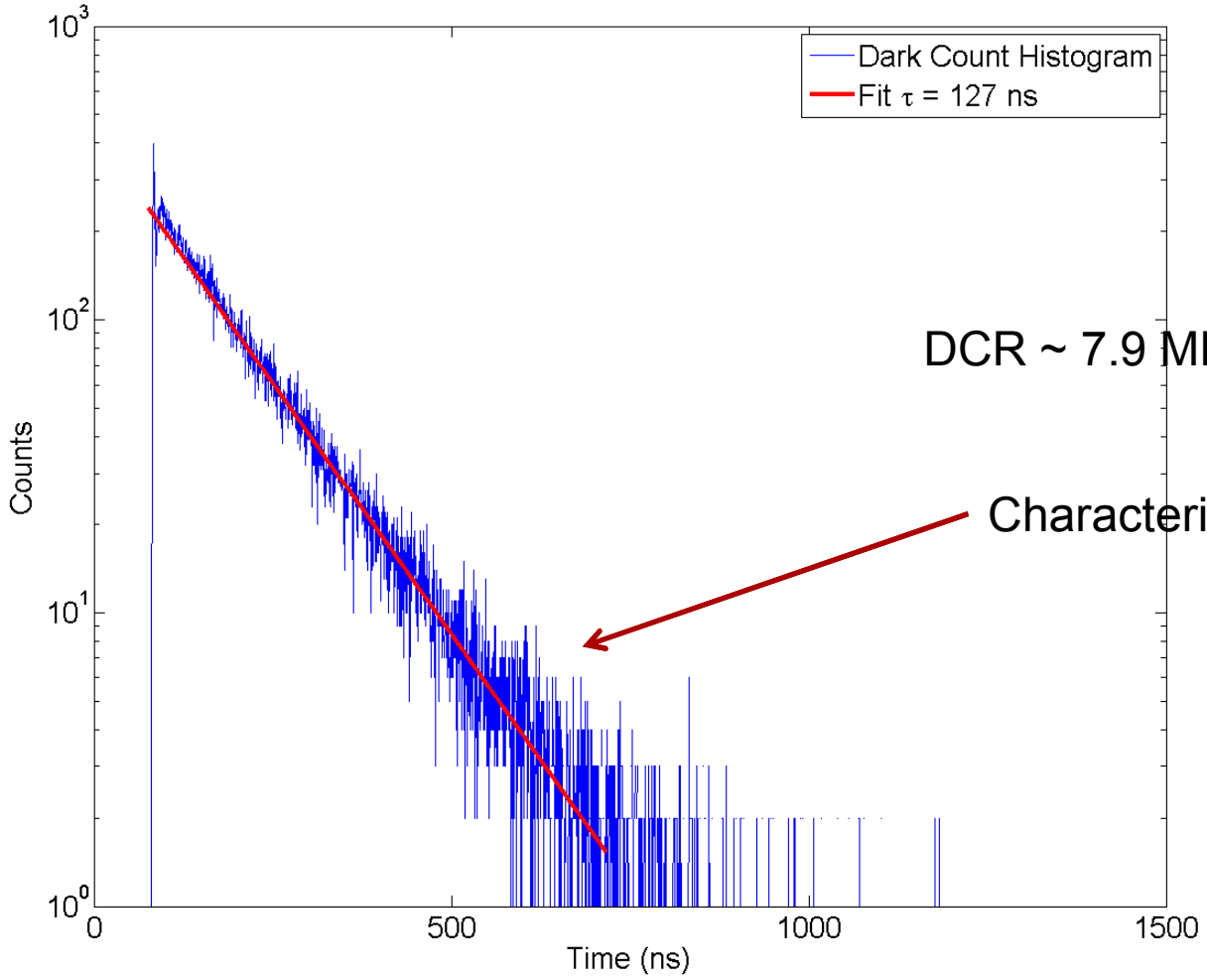
$$p_d = p(n \geq 1) = (1 - \exp(-\mu))$$

$$\mu \equiv \rho\tau$$

Note: The dark count probability can be determined by counting avalanche events in the gated mode unilluminated diode and divided by total number of gates.

$\rho = -\ln(1-p_d)/ T_g$ where p_d = # of dark counts /total # of gates

Dark Count Histogram



Room Temperature DC data for 1 micron wide multiplication.

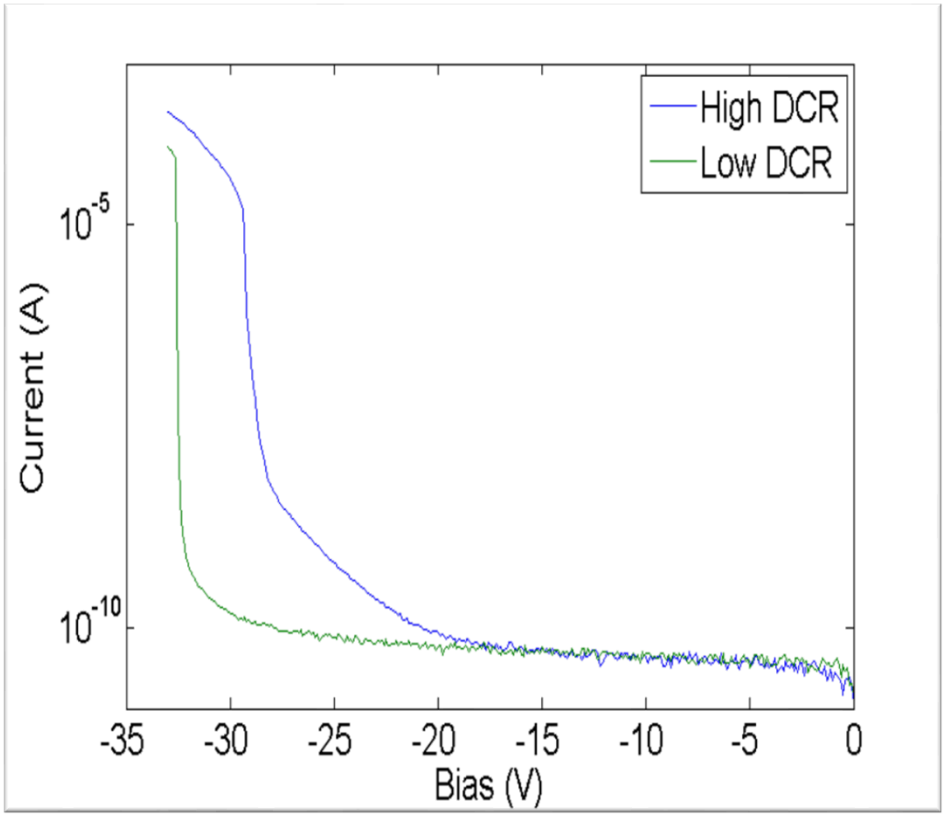
DCR ~ 7.9 MHz

Characteristic exponential decay

Gated Geiger mode operation

- Blue curve has high dark counts but shows better photon collection
- Green Curve shows low dark counts but inefficient photon collection.
- May need to cool device to have efficient collection and low DCR

I-V characteristics



1 um Multiplication Region Dark Counts

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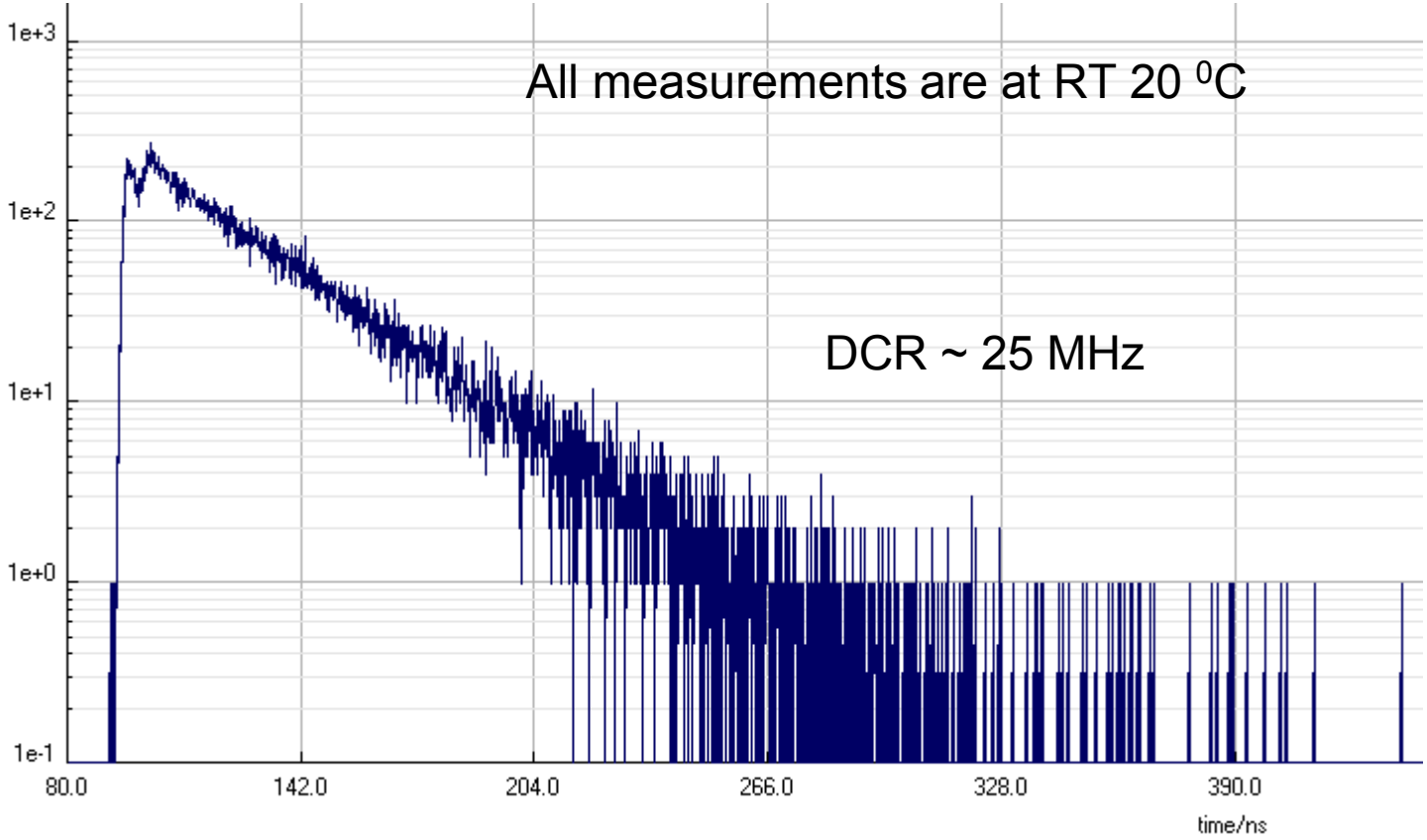
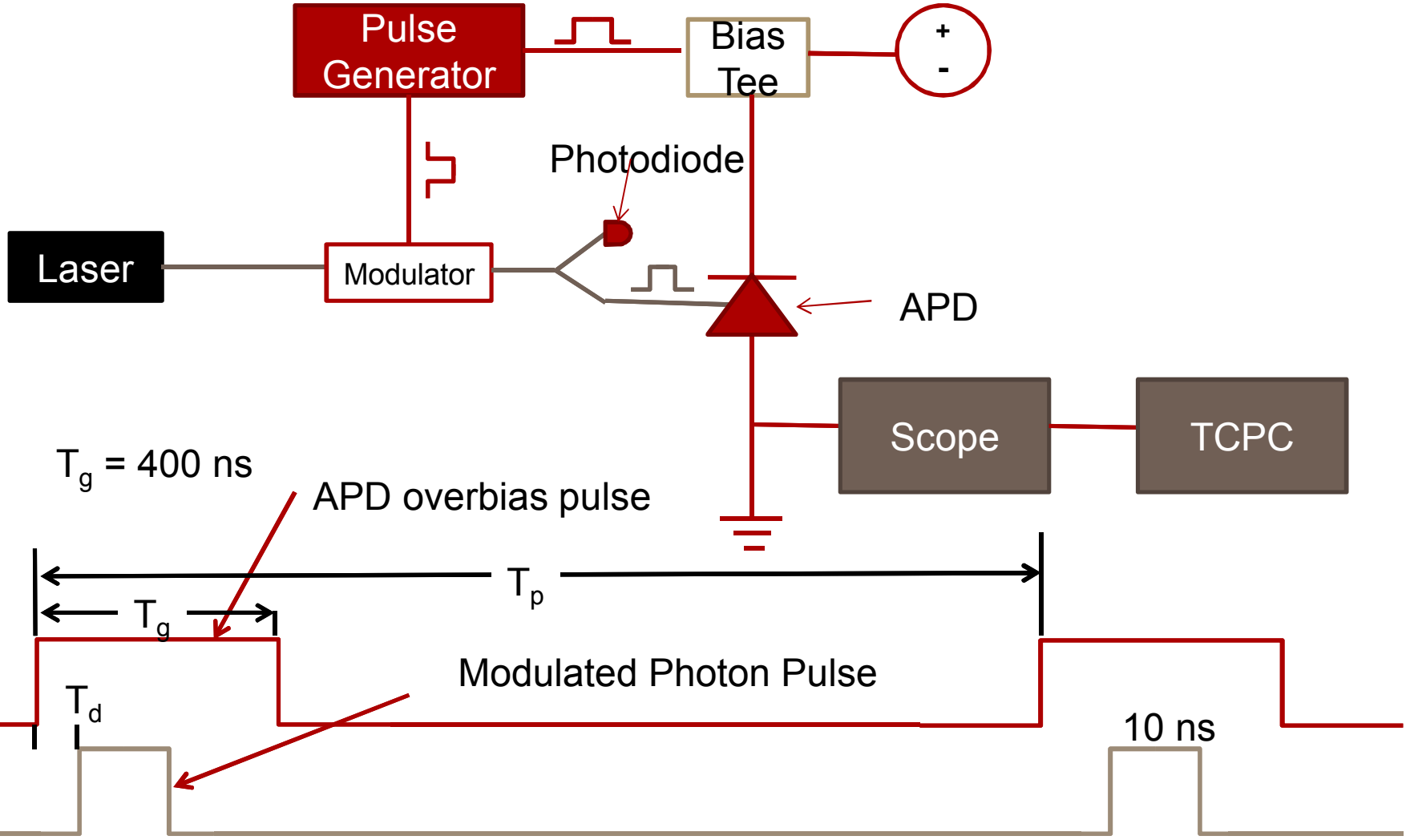
Noise in background detector.

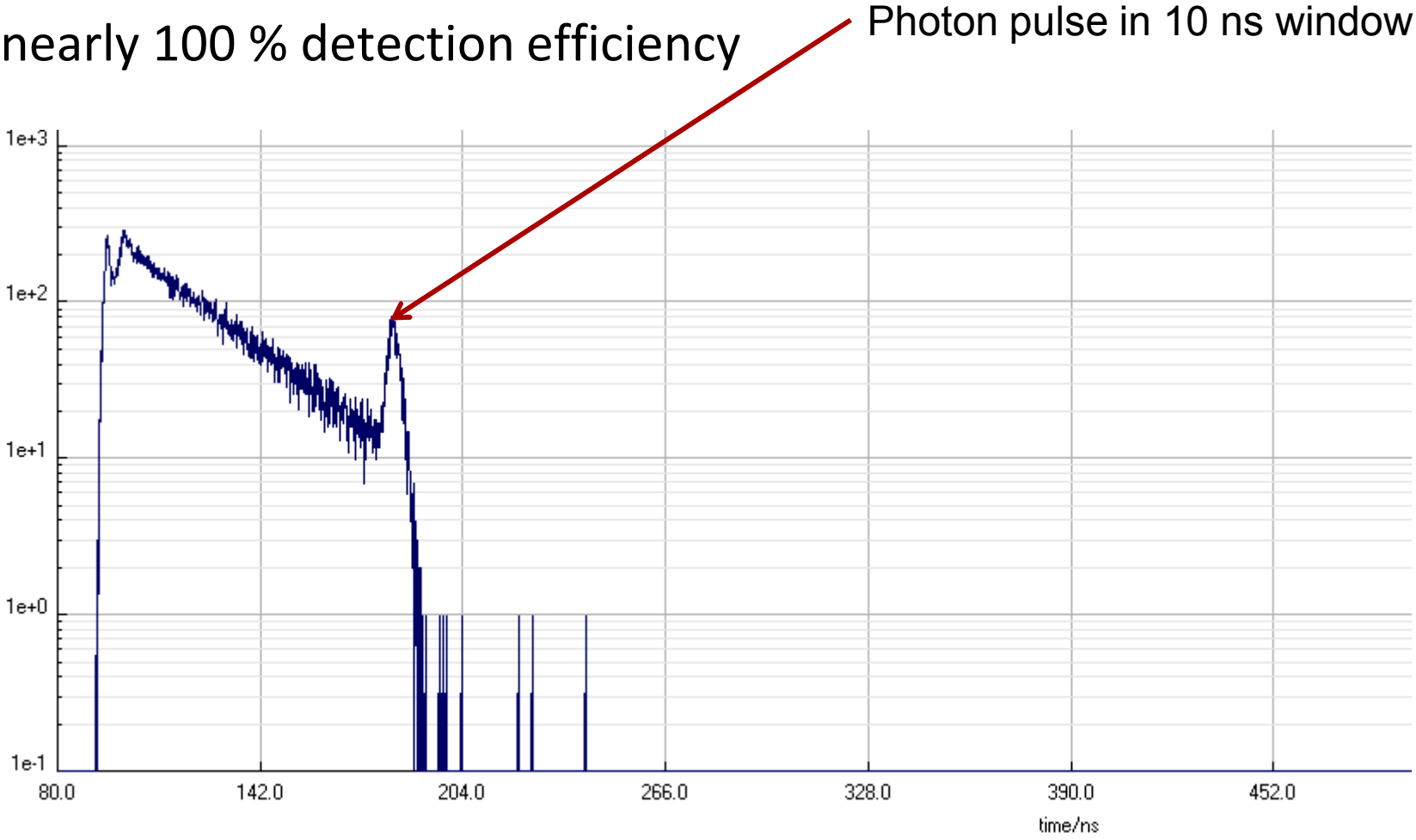


Gated Geiger Mode Experiment



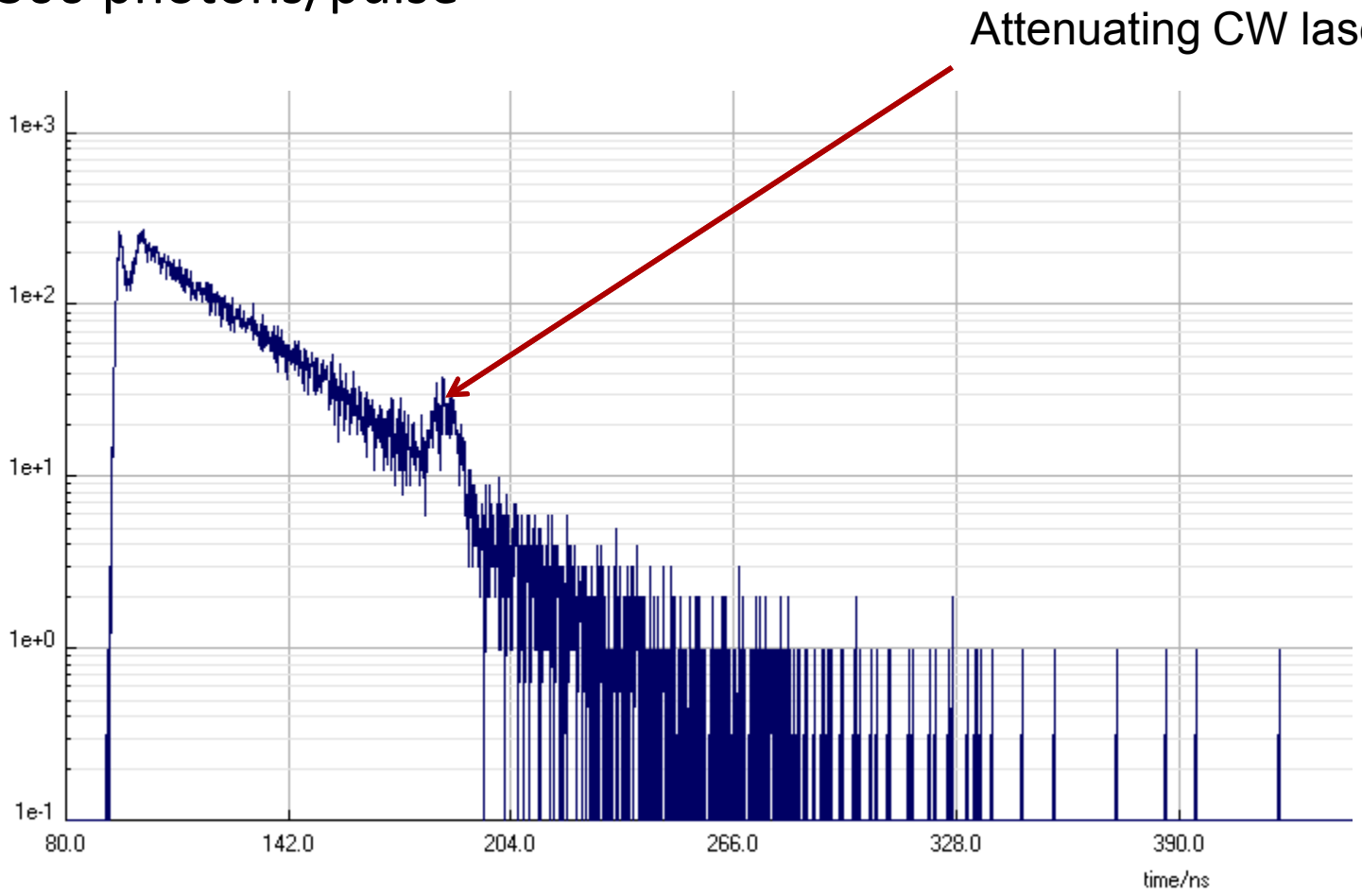
1 um Multiplication Region

- 3000 photons/pulse
- nearly 100 % detection efficiency



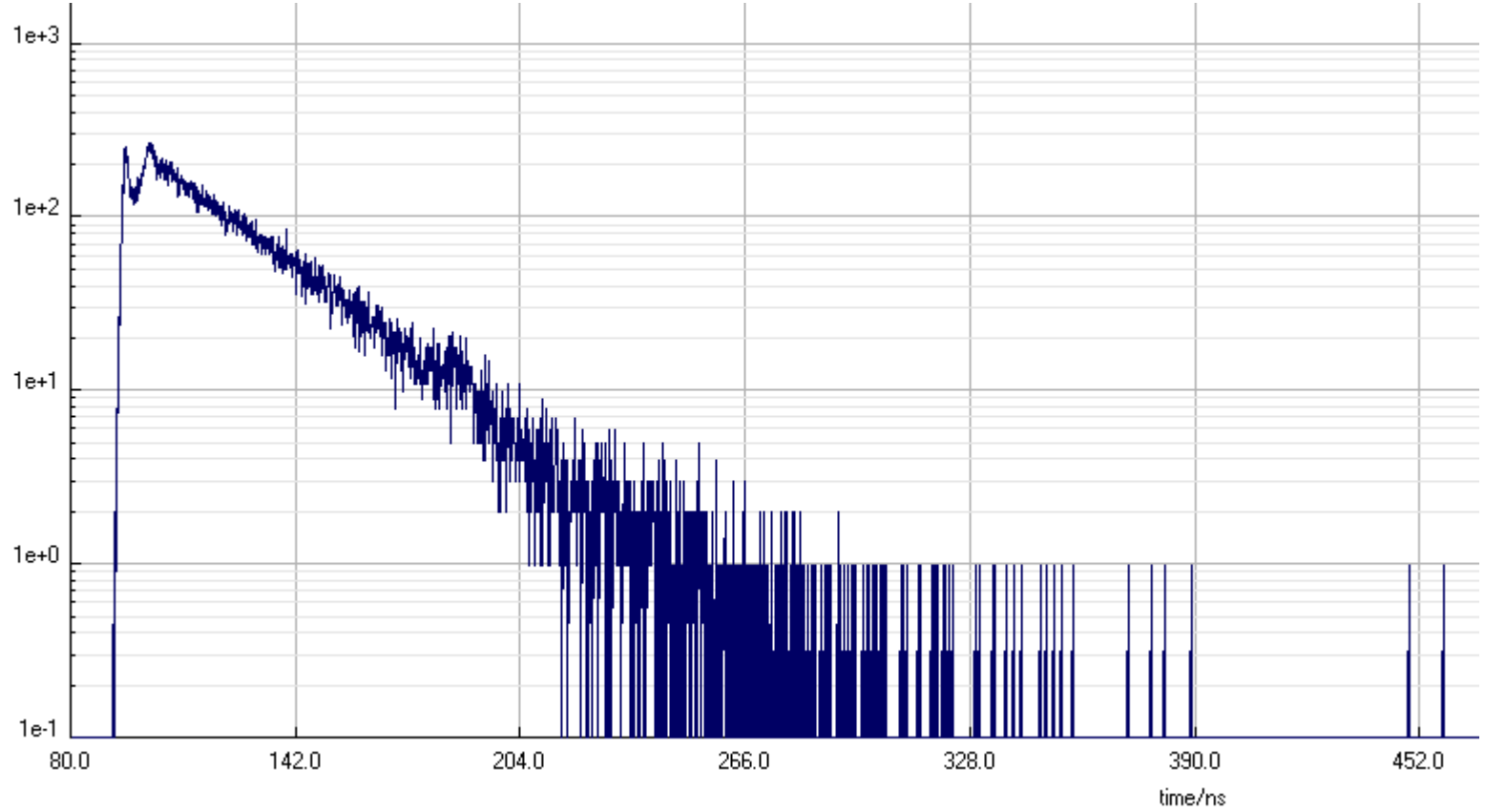
1 um Multiplication Region

- 300 photons/pulse



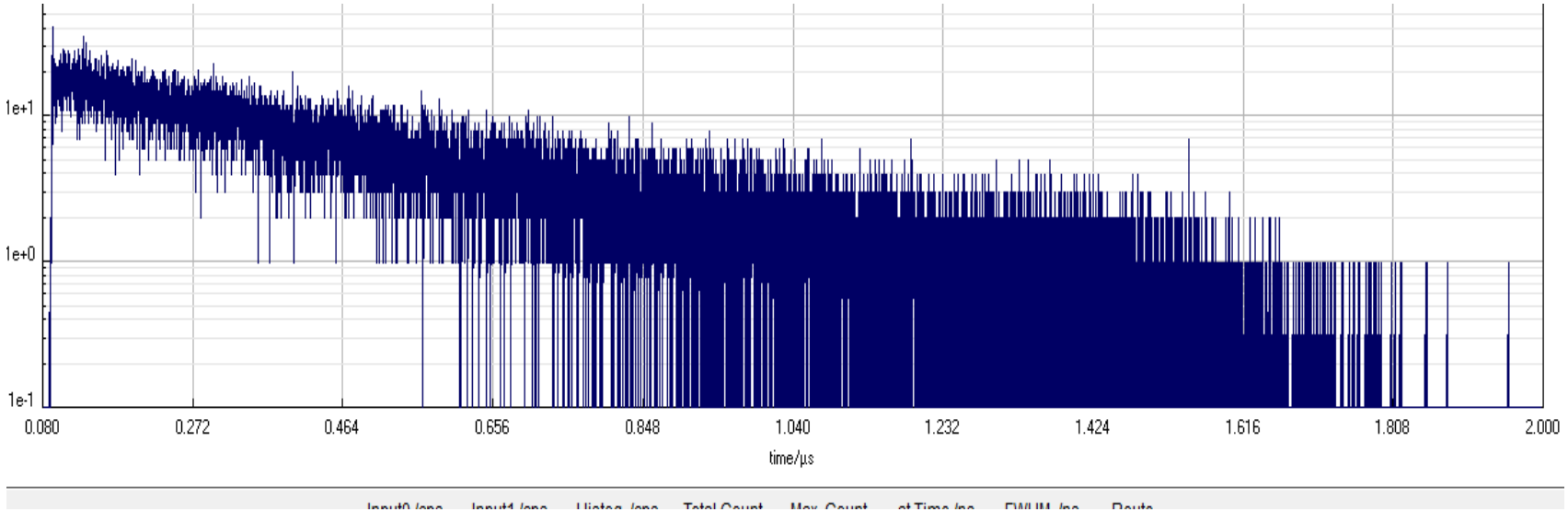
1 um Multiplication Region

- 100 photons/pulse



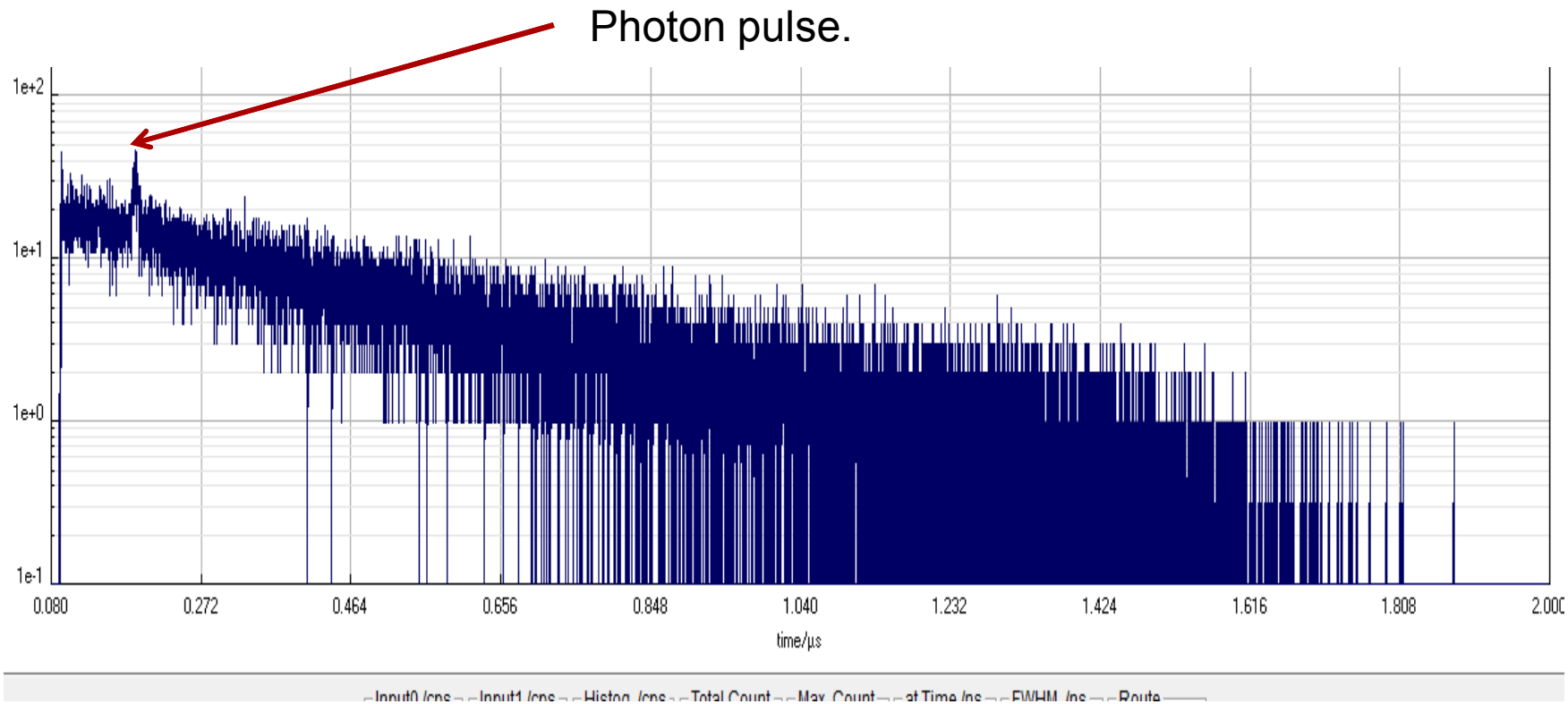
1 um Multiplication Region

- Dark Counts different doping low dark counts



1 um Multiplication Region

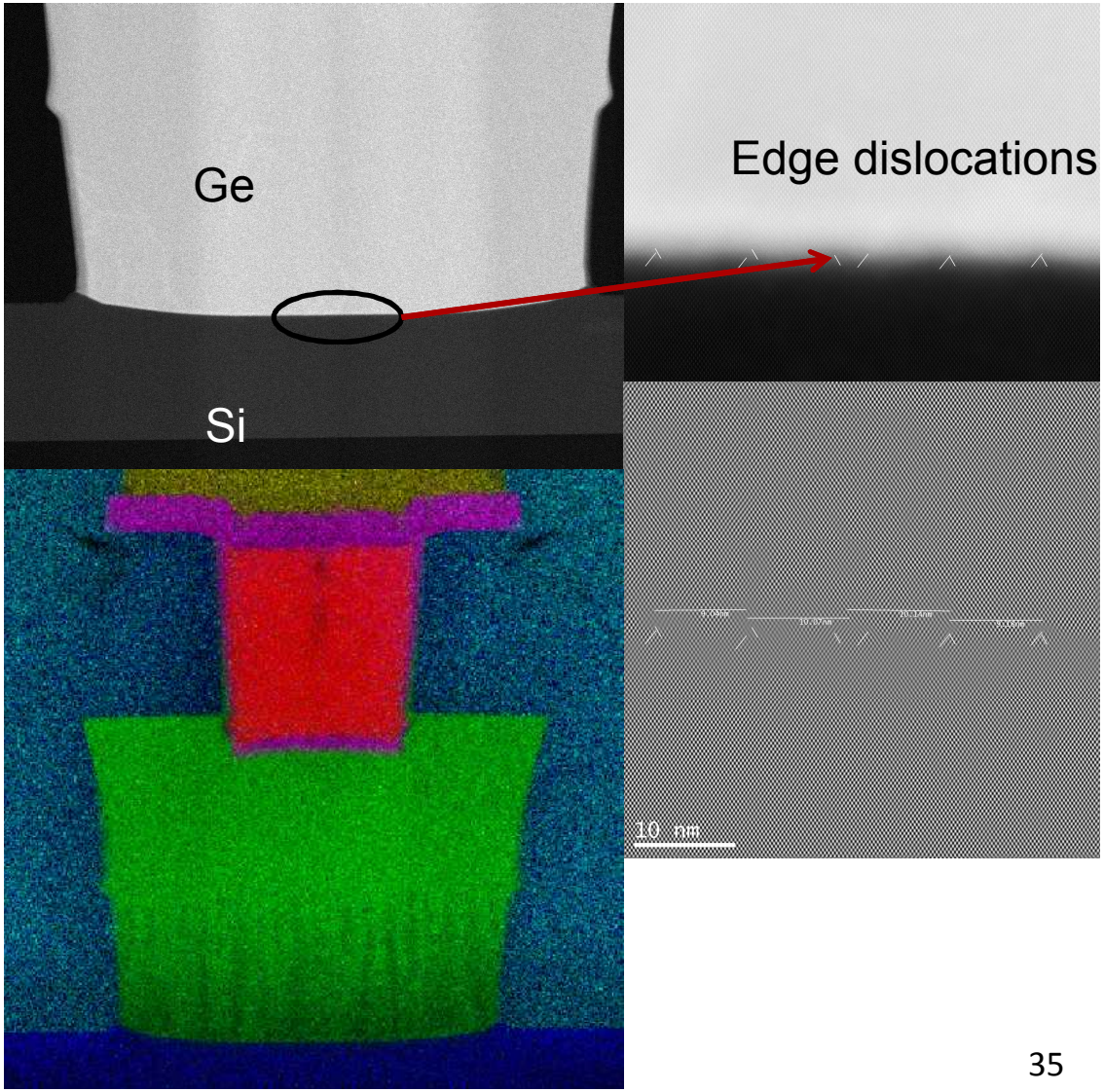
- 30000 photons/pulse different doping low dark counts poor photon counting



Low Dark Count Detection

- Our Selective Ge on Si gives low defect count at Si/Ge interface.
- We need to reduce dark current.
- Apply analytic tools to reduce defects at interface.
  - Very low defect density.
- Field engineering, cooling, and vertical designs must reduce dark current levels.

Our Ge device



Outline

- Highlight early progress in 3 areas:
  - Integrated Single Photon Avalanche Detector (SPAD)
  - Integrated quantum optoelectronic circuits
  - Heterogeneous integration of III-V laser source on Si Photonics substrate.

Quantum Photonics

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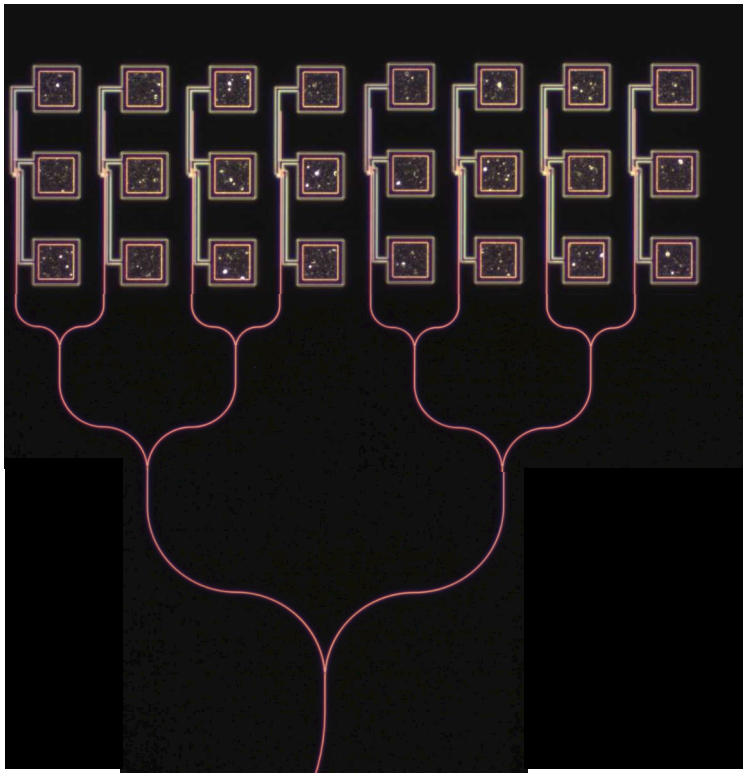
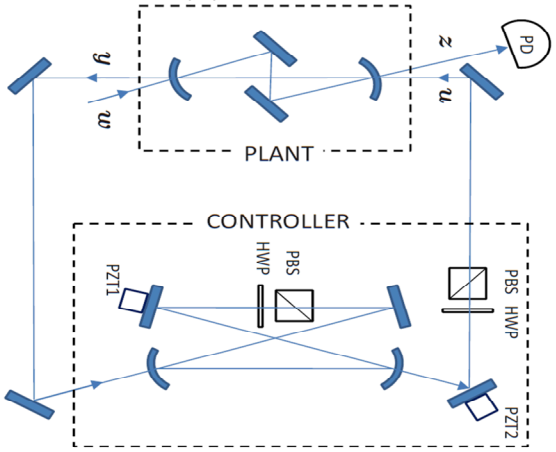
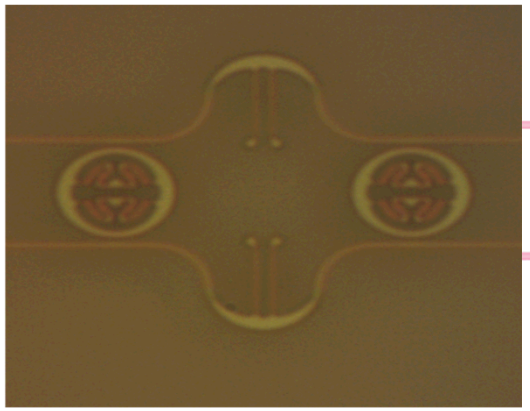
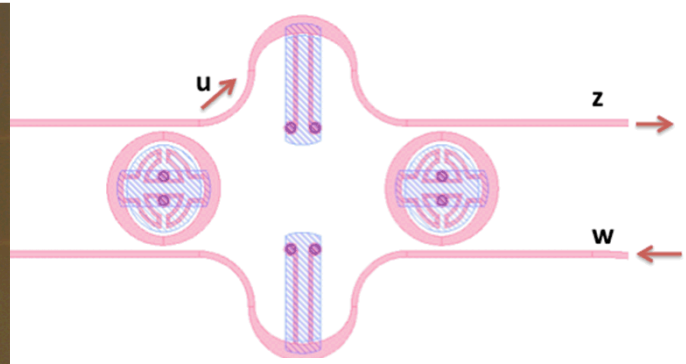
- Putting building blocks together.
  - Create large scale spatially and temporally multiplexed SPD's.
  - PNR detection.
- Explore simple quantum coherent feedback and control circuit.
  - H. Mabuchi. Coherent-feedback quantum control with a dynamic compensator. Physical Review A, 78(3):032323, 2008.

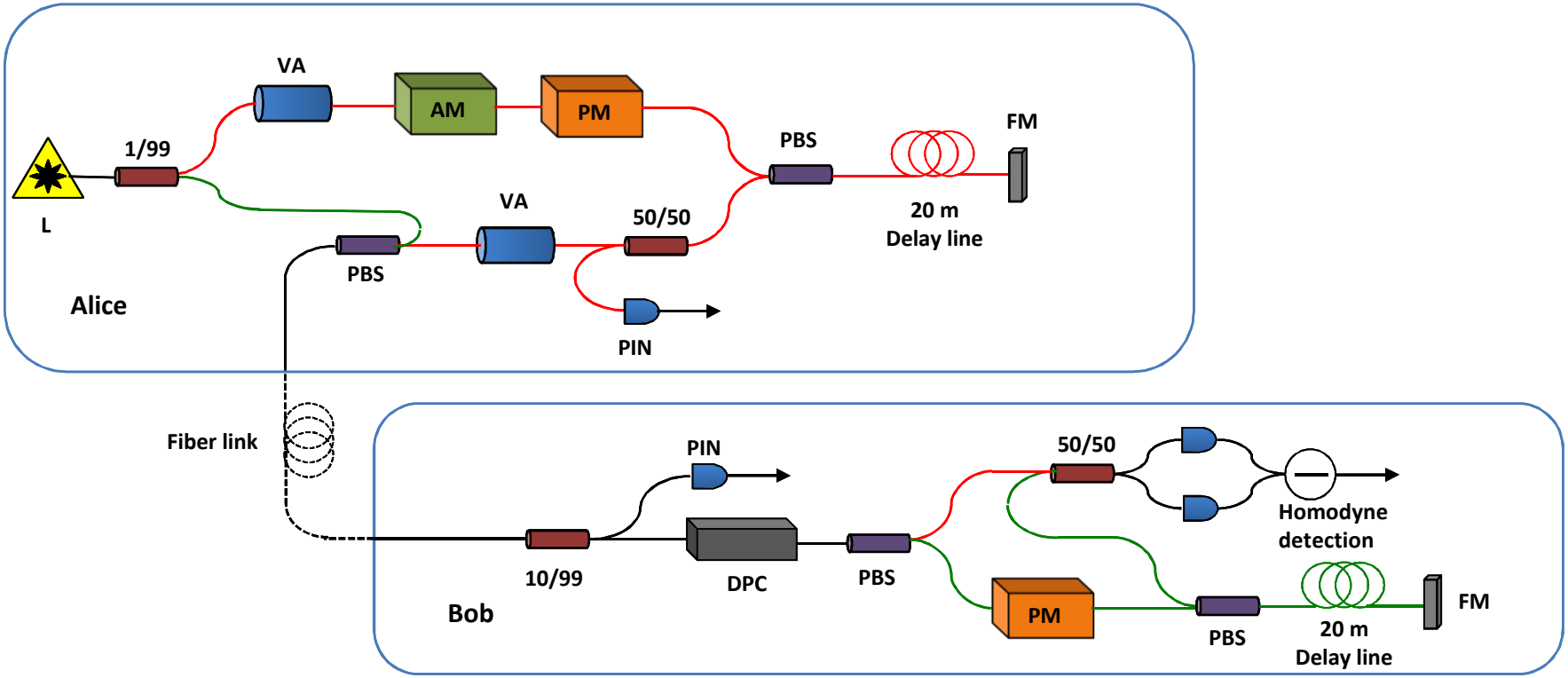








Bench-top CVQKD link



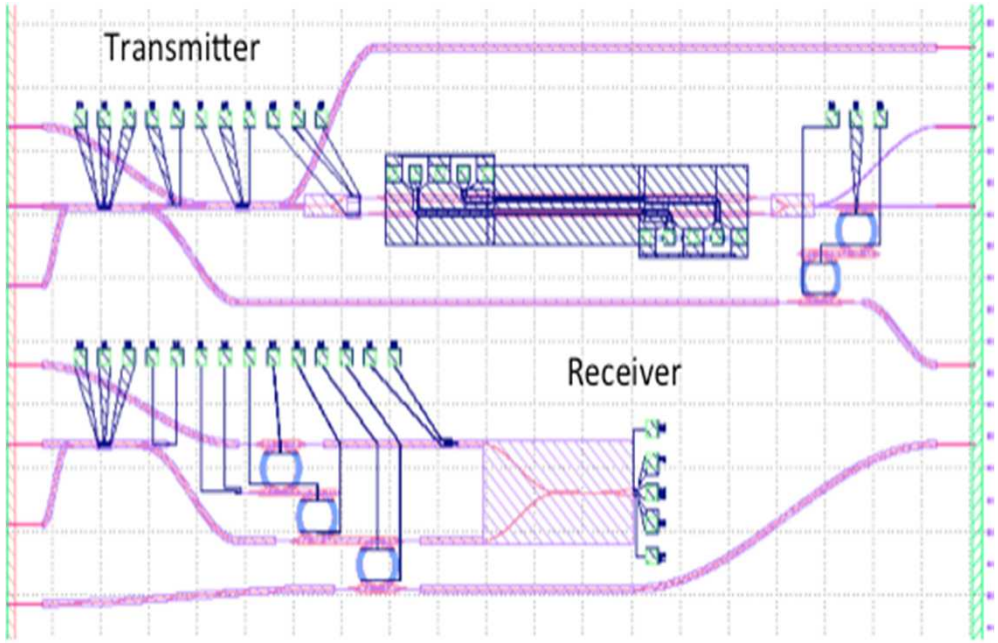
Current State of the Art CVQKD link using coherent state source

P. Jouguet, S. Kunz-Jacques, A. Leverrier, P. Grangier, and E. Diamanti. Experimental demonstration of long-distance continuous-variable quantum key distribution. Nature Photonics, 7(5):378–381, 2013.

Quantum Photonics: CVQKD Tx/Rx

- Implement a CV-QKD transceiver on-chip.
- Chip-scale version of bench top design.
- Long delay is difficult on chip.
- Quantum system (CVQKD Tx/Rx) works with existing photonic building blocks.

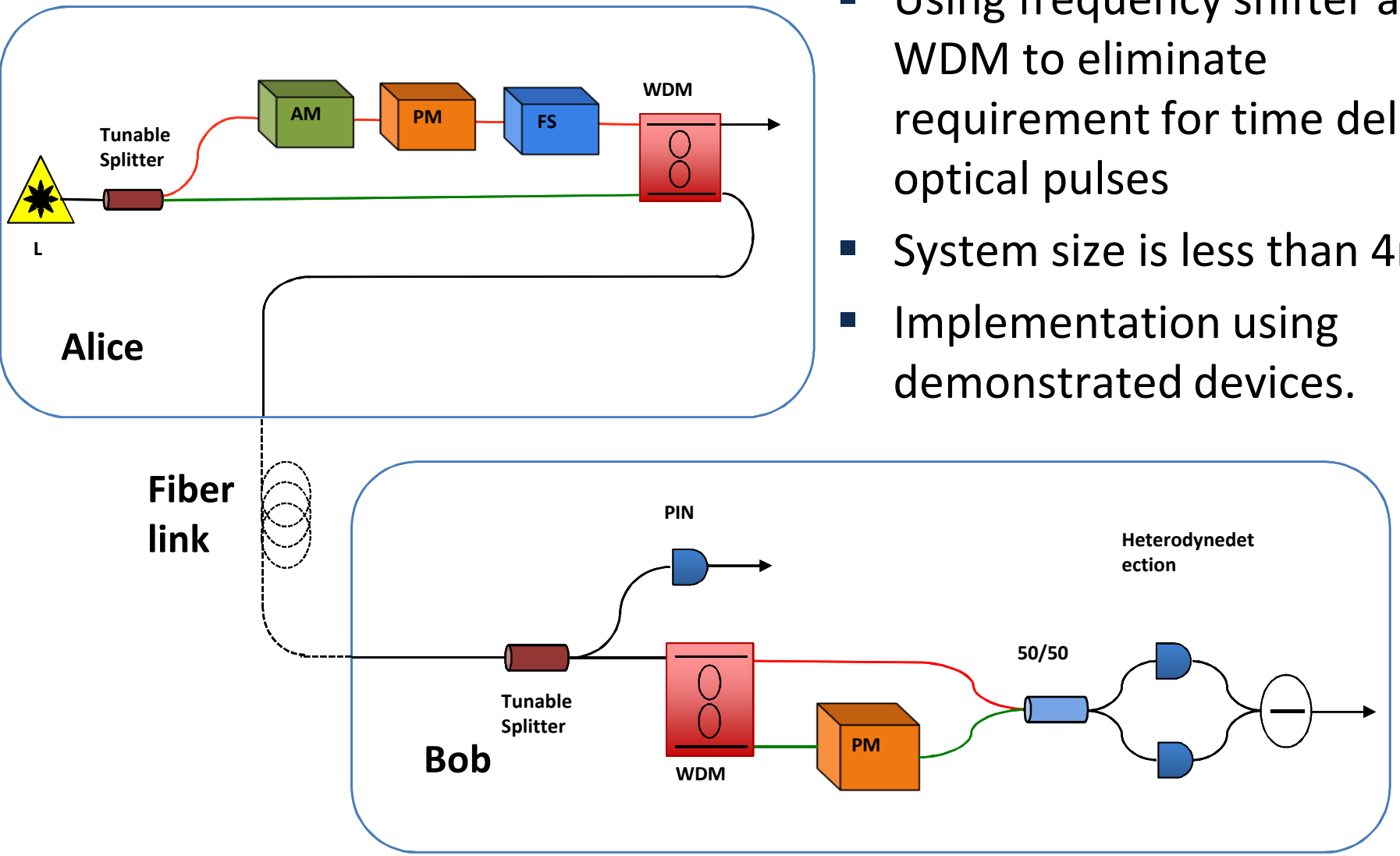
CV-QKD Tx/Rx



Chip-scale design by C. DeRose, D. Soh.

P. Jouguet, S. Kunz-Jacques, A. Leverrier, P. Grangier, and E. Diamanti. Experimental demonstration of long-distance continuous-variable quantum key distribution. Nature Photonics, 7(5):378–381, 2013.

On-Chip CVQKD System



- Using frequency shifter and WDM to eliminate requirement for time delayed optical pulses
- System size is less than 4mm^2
- Implementation using demonstrated devices.

On-Chip CV-QKD Transmitter (Alice)

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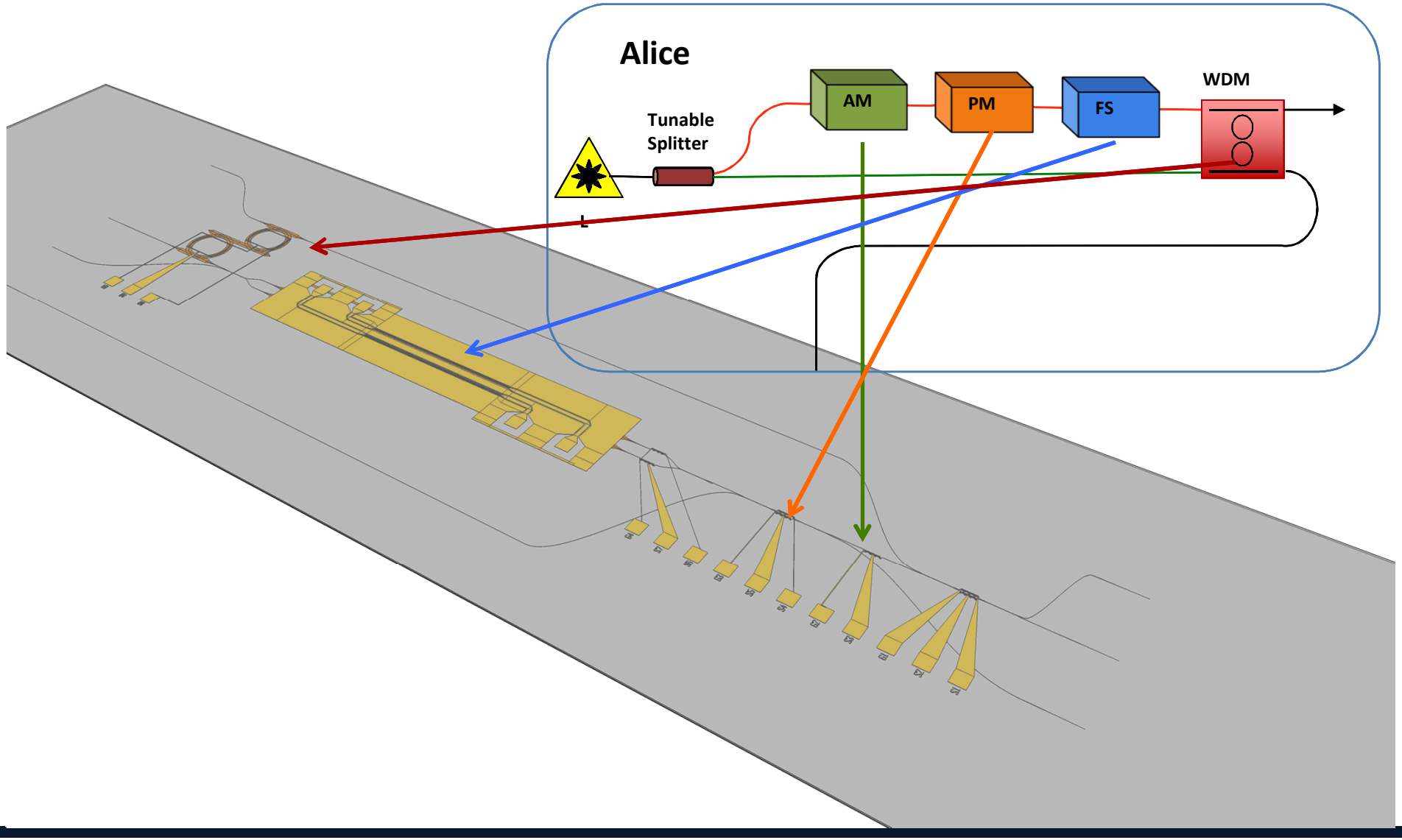

On-Chip CV-QKD Receiver (Bob)

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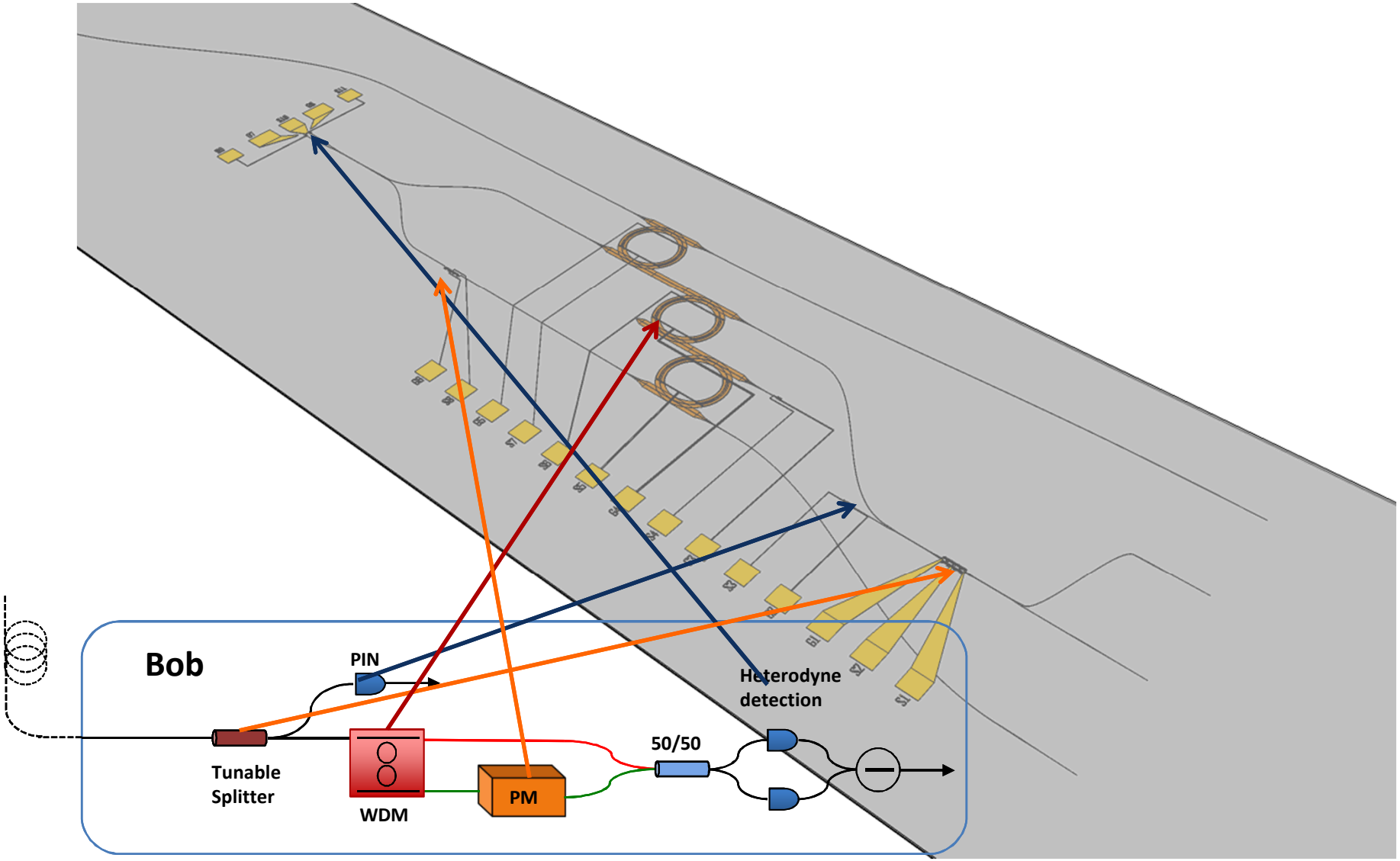
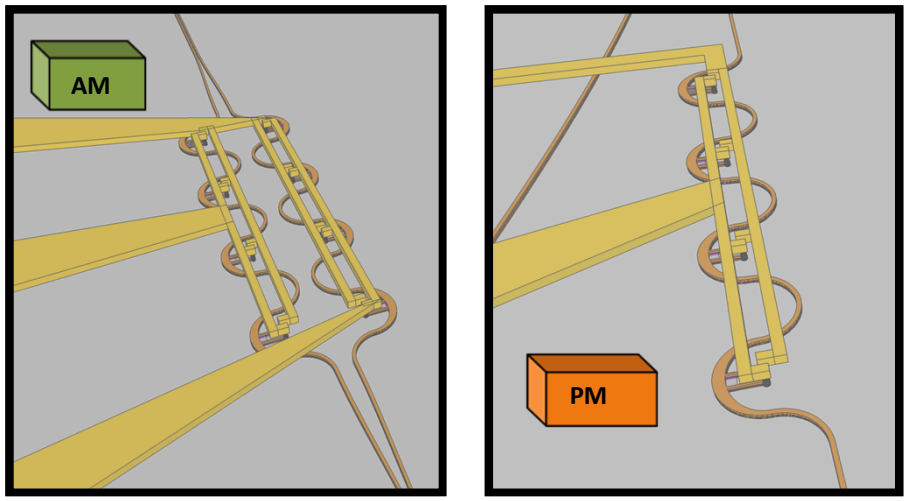
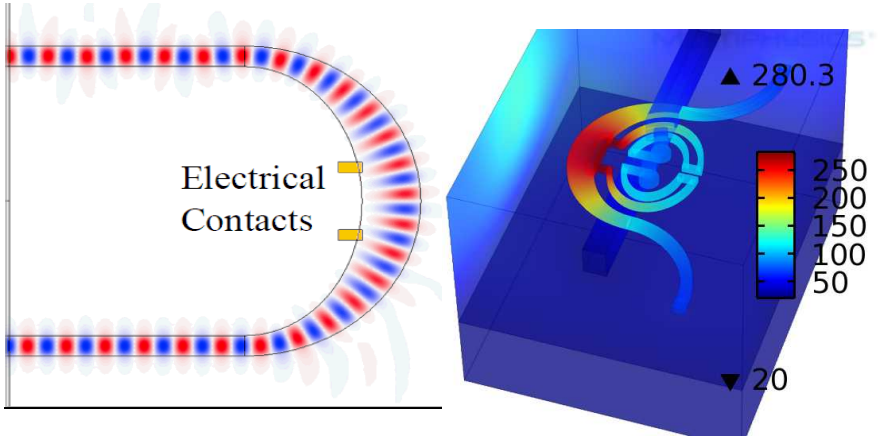
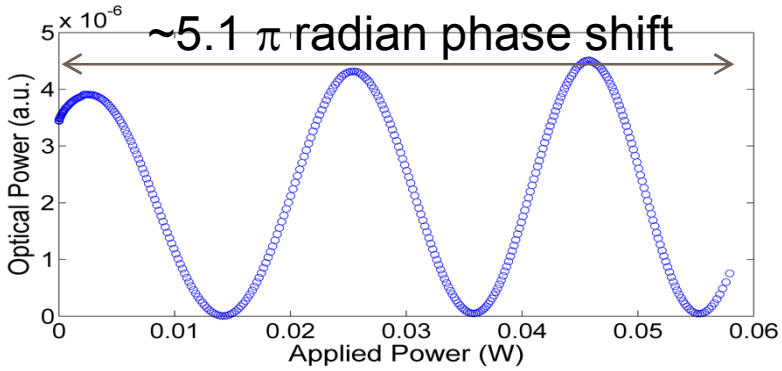


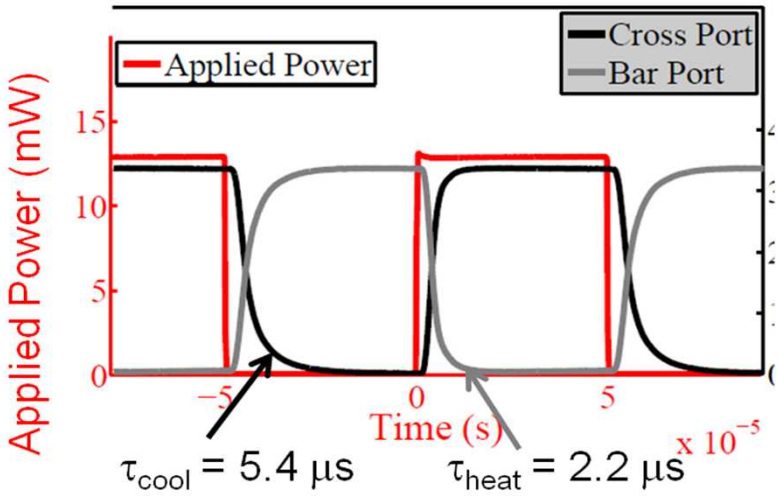
On Chip CV QKD Components

- Thermo-optic effect
- Adiabatic bends for low loss
- Directly heated silicon for low power



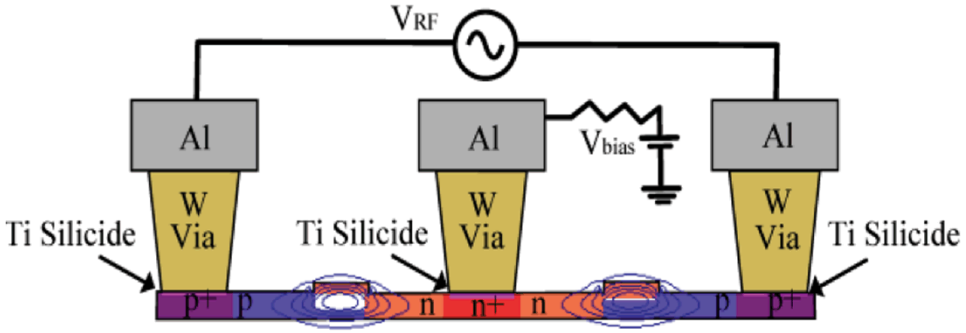


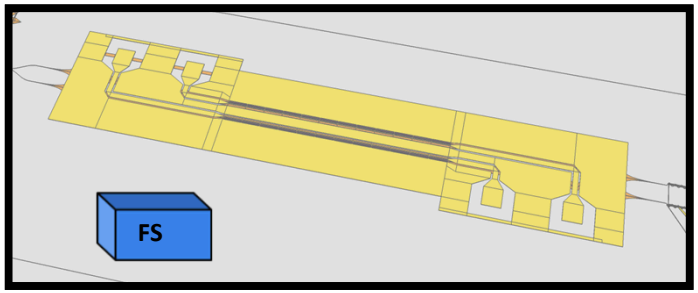


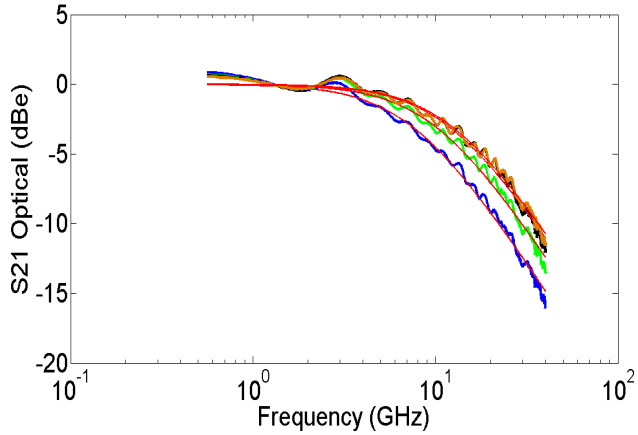


On Chip CV QKD Components

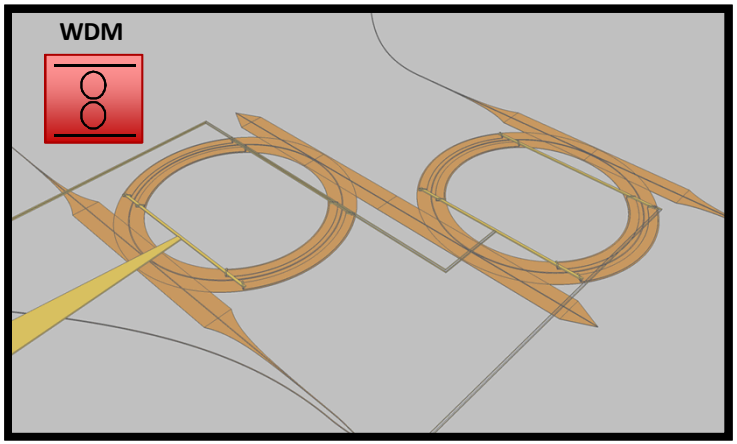
- Carrier depletion silicon MZM
- Capacitively loaded design
- High Bandwidth > 23GHz

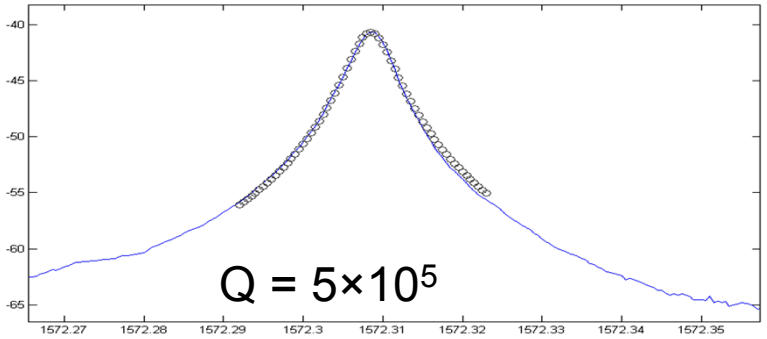




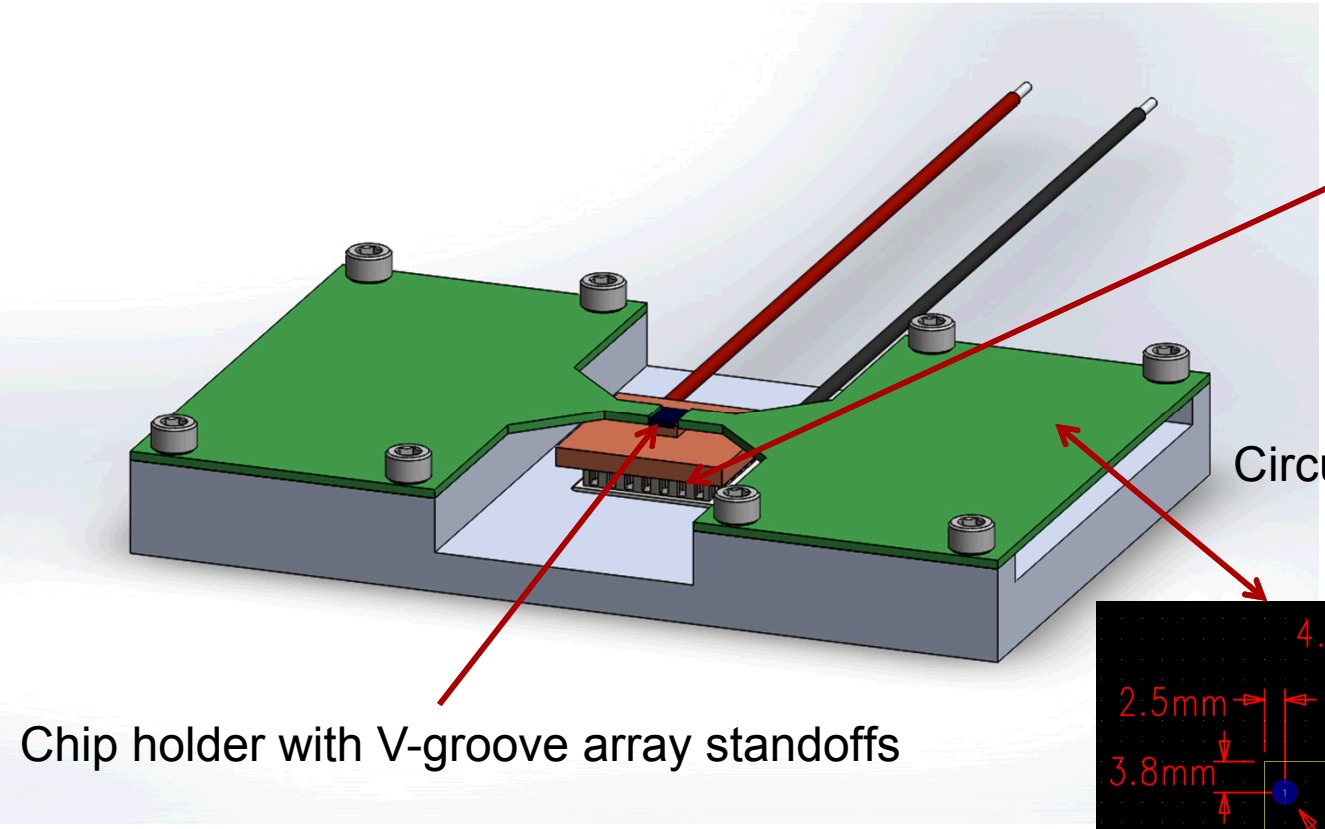


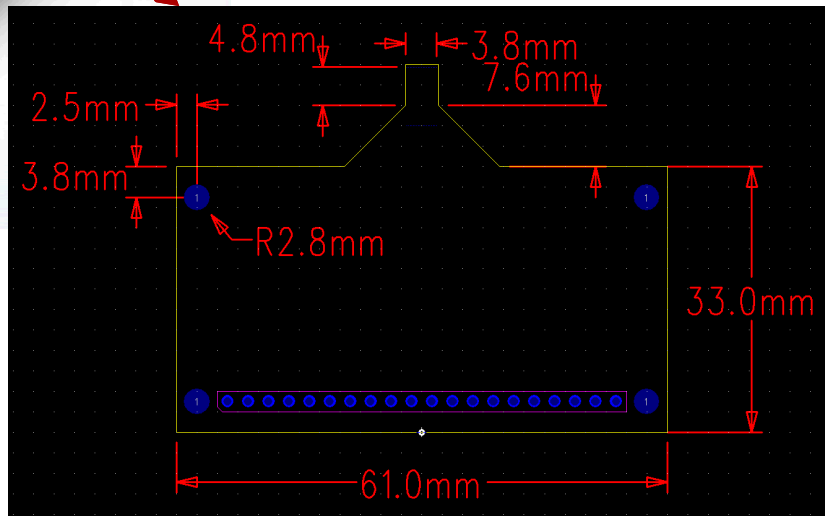
- High-Q filter, thermally tunable
- 2nd order design for > 60 dB suppression





Packaged CV-QKD Tx/Rx





Outline

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InP Lasers & PIC Platform

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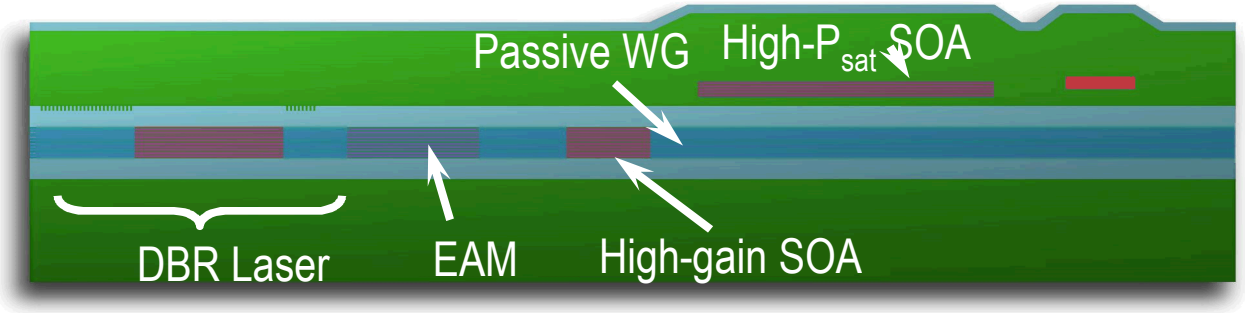
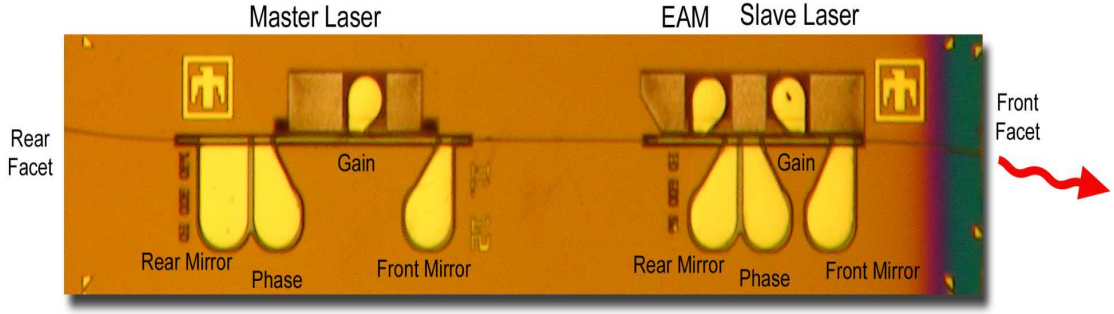
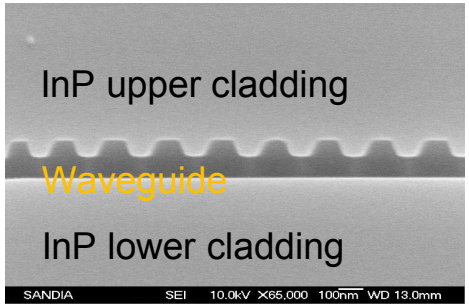
1550 nm wavelength

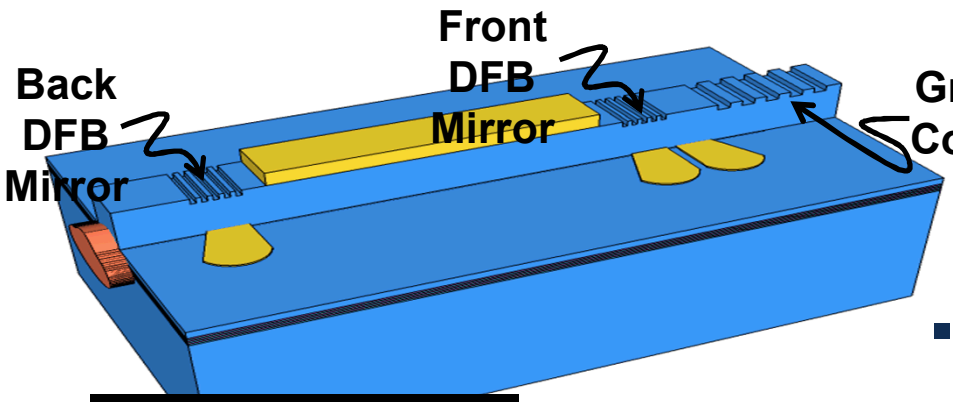
- State-of-the-art discrete photonic component performance from a single chip.
- E-Beam patterned grating couplers.
- DBR lasers, EAMs, WGs, High-gain SOAs, High-Psat SOAs, Evanescent PD.

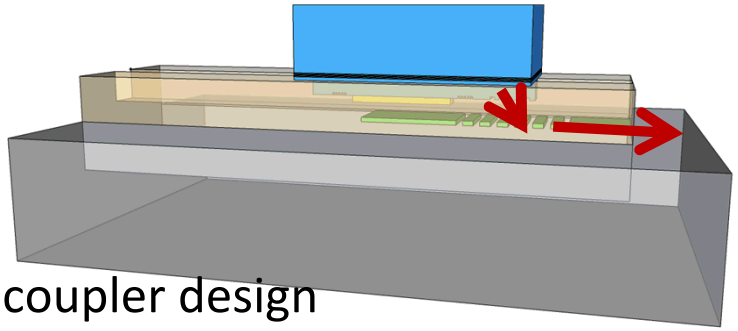


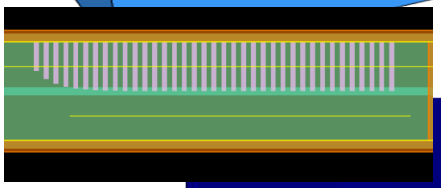




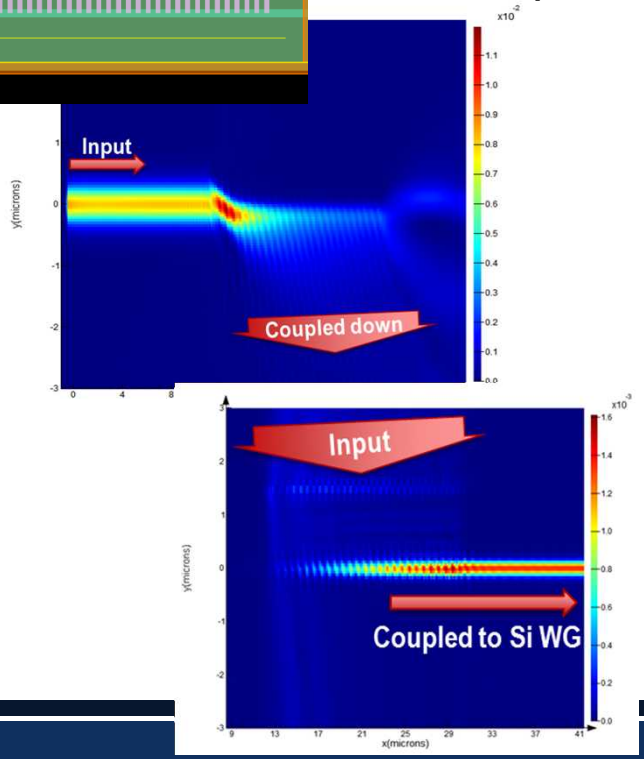
InP to Si Waveguide Grating Coupling







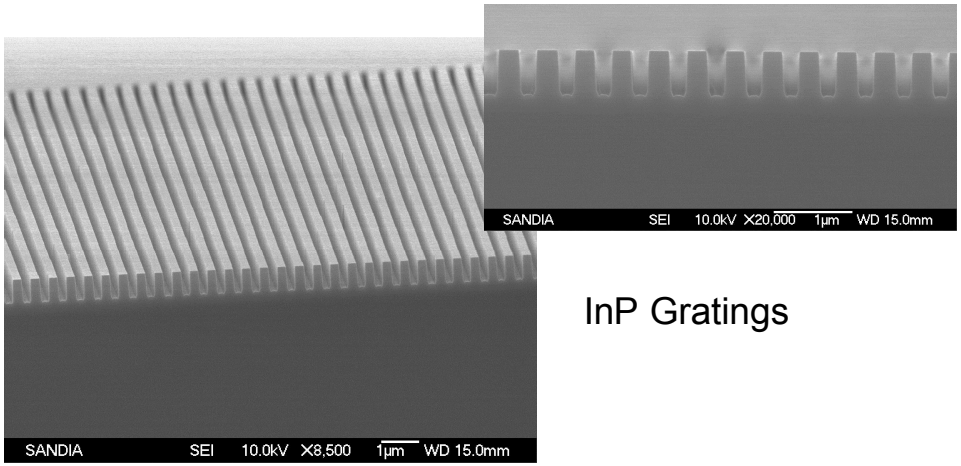
InP coupler



- InP coupler design
  - > 52% power coupled down
  - < 5° farfield angle
- Si coupler design
  - Input the InP coupler mode field
  - ~30% is coupled into the Si WG
- Next step
  - Combine InP and Si simulations
    - Will allow more design optimization

Grating Couplers

- InP-to-Si grating couplers
  - 2nd order grated designed to have light exit chip vertically
  - Allows for optimized mode shape for larger alignment tolerances
    - > 1 µm
  - Avoids flip chip integration
    - Light exits InP chip through the substrate
    - Couples into the top of the Si chip
    - Top contacts on both chips

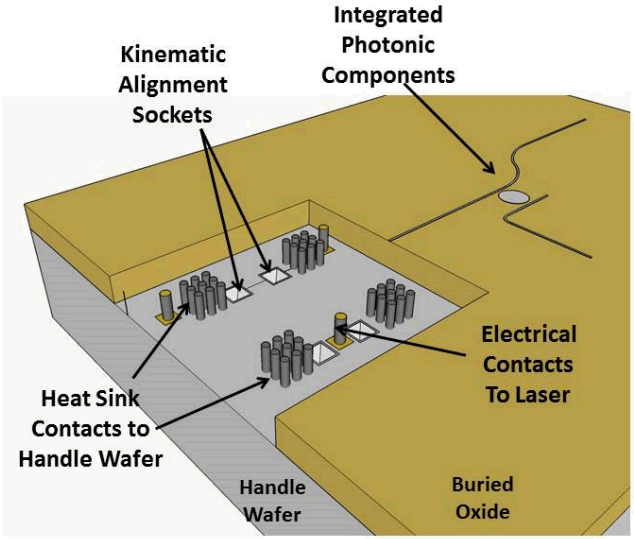


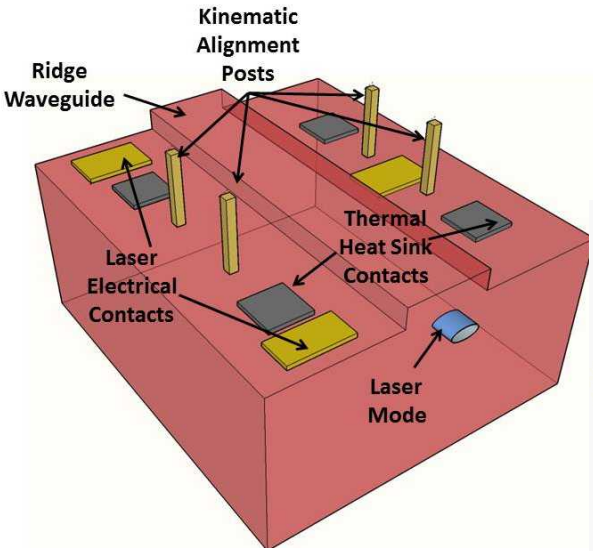
InP Gratings

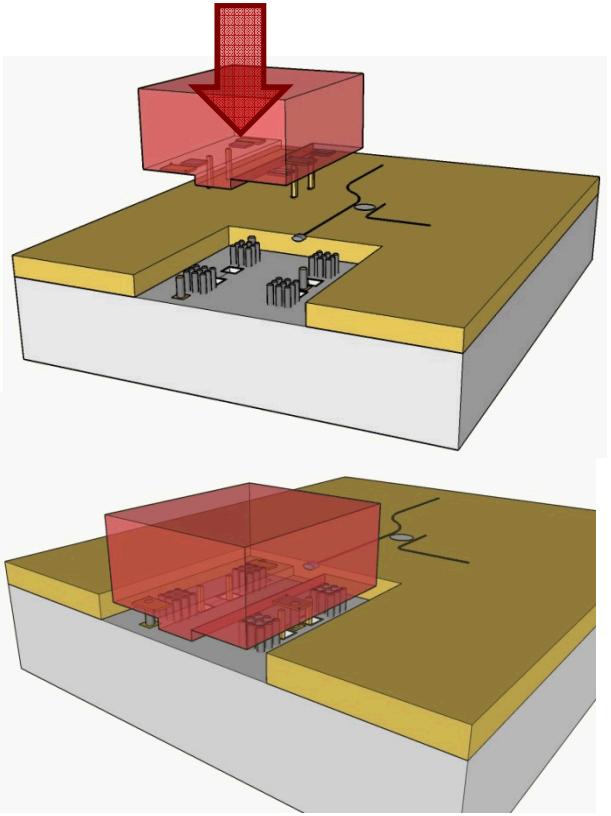
- Process development
  - Developing InP ICP etch process for high aspect ratio gratings
    - ~500 nm pitch
    - Targeting 1 µm depth
  - InP gratings defined by ebeam lithography
    - Allows for many different designs on a single wafer
  - Complementary Si and InP masks are currently being laid out
    - Access alignment tolerances
    - Demonstrate laser to Si waveguide coupling
  - Si gratings will leverage previous work for fiber coupler

Heterogeneous Kinematic Mounting

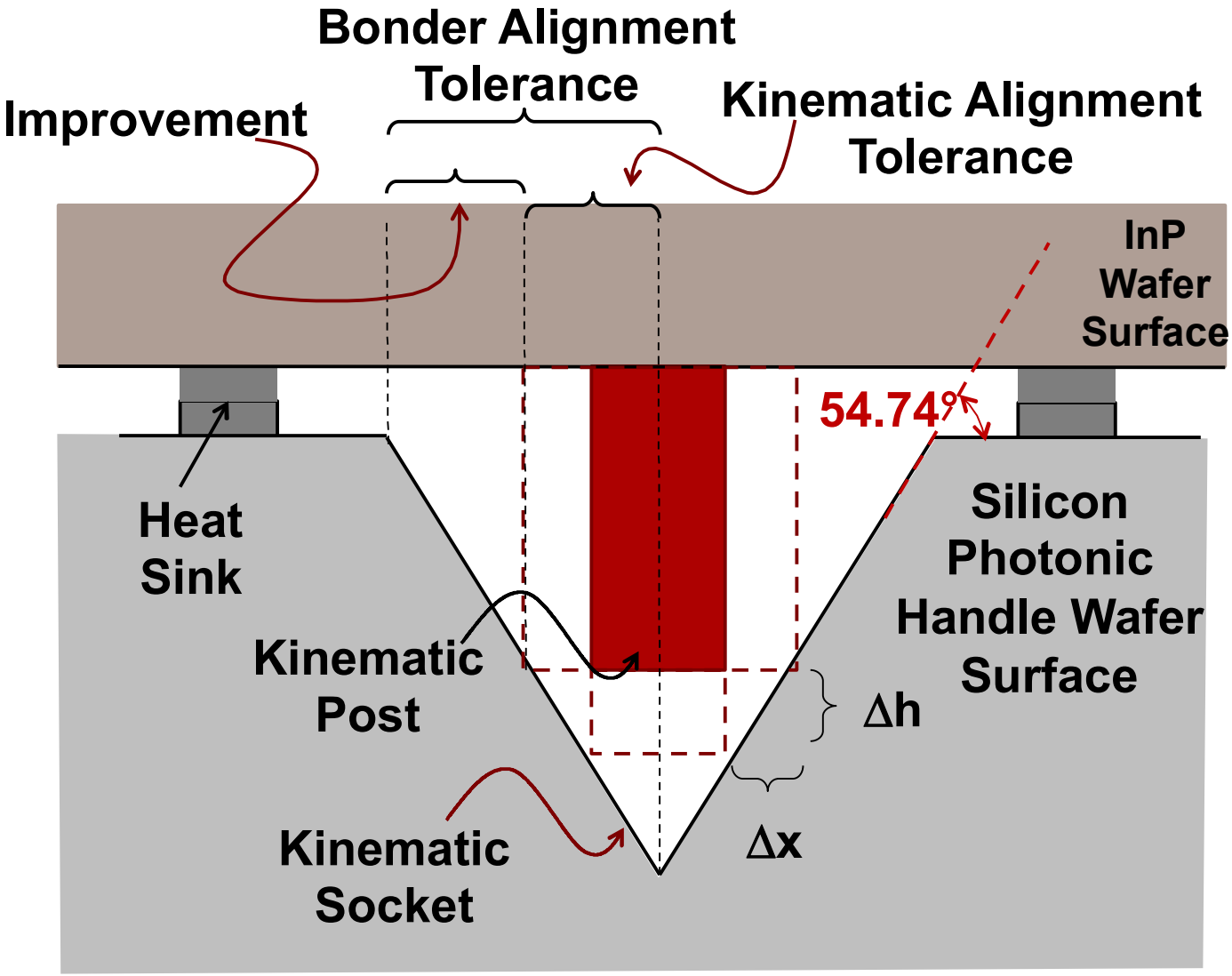
- Precision kinematic mounting for general integration of devices with Si Photonics substrate.
- Nitride posts mate with Si pyramids
- FC 150 bonder used to mate parts







Precision alignment



Socket & Post Process flow

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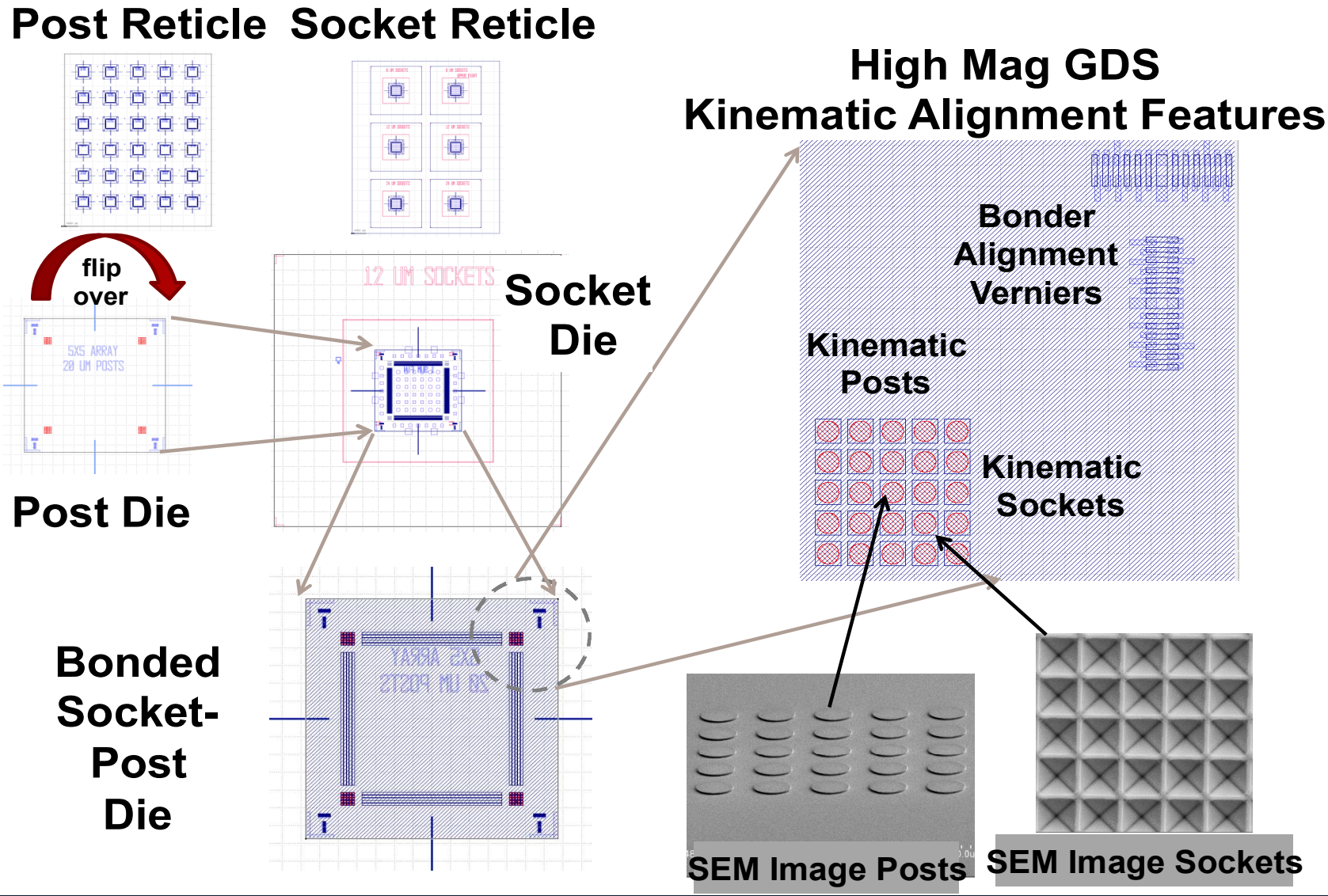

Heterogeneous Integration

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- InP chip with grating coupling to Si Photonics carrier designed and currently in process.
- Developed general sub-micron alignment and bonding of full processed devices onto Si substrate.
- Socket and post test chip fabricated and currently under test.
- Use cases:
  - III-V actives with Si
  - Fiber alignment.
  - Non-linear crystals not compatible with CMOS processing.
  - Etc….

Summary

- We are at the early stages of development of a chip-scale quantum photonics platform.
- We are developing
  - Single Photon Detectors based on Ge on Si Gm-APD's.
  - Complex quantum photonic circuits for exploration of new ideas.
  - An electronic and optical packaging scheme (not discussed).
  - An integrated InP laser source onto Si Photonics substrate.
  - A heterogeneous integration approach that will enable general integration of complex devices and new materials onto active Si substrate.
- We are leveraging multiple efforts
  - III-V optoelectronics development
  - Si Photonics development
  - RF/optoelectronics/CMOS/pakaging

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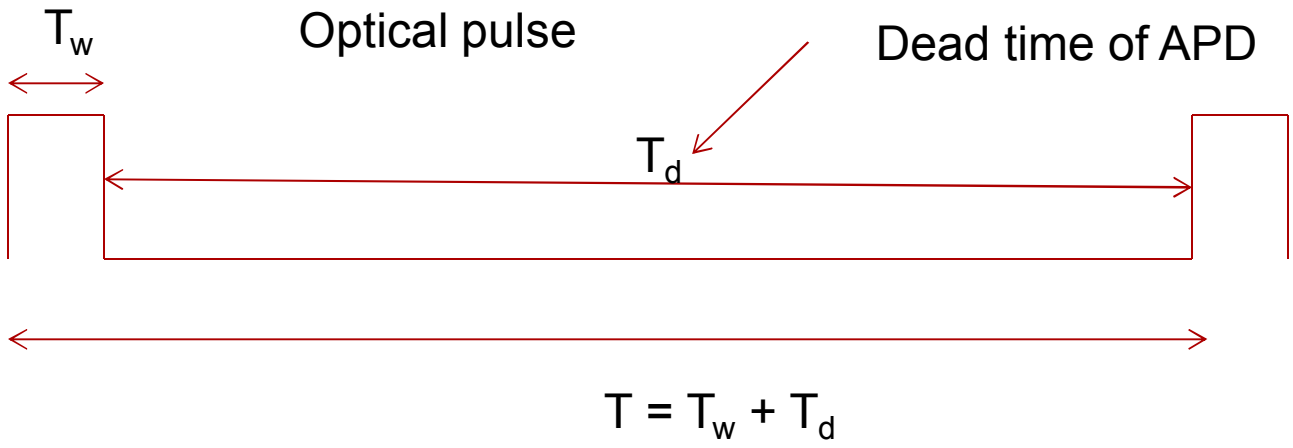
Thank You !

Gated APD Characterization



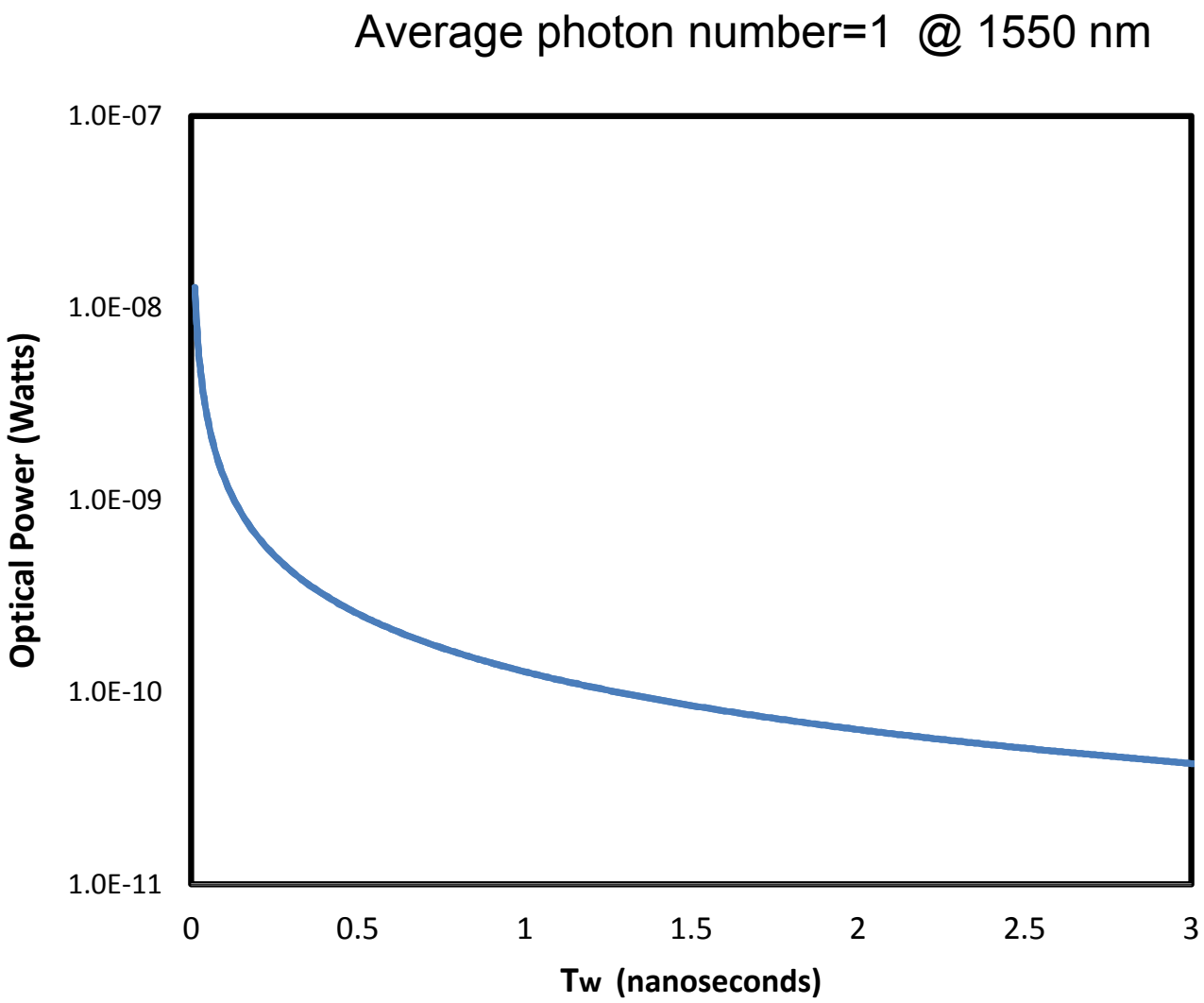
Average number of photons in pulse

$\mu = P_{opt}\, T_w\, \lambda/hc$ $\qquad$ $hc = 1.98649 \times 10^{-25}$ J m

$P_{opt} = 1.98649 \times 10^{-25}/(T_w\ 1.55 \times 10^{-6})$

T_w =0.3 ns $P_{opt} = 4.27 \times 10^{-10}$ W
T_w= 0.5 ns $P_{opt} = 7.12 \times 10^{-10}$ W
T_w= 1.0 ns $P_{opt} = 1.42 \times 10^{-9}$ W

Power vs pulse width



Dark Counts

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Dark count probability: p_d
Dark count rate: ρ

$$p_d = 1 - \exp(-\rho T_w)$$

$$p(n) = \frac{\mu^n}{n!}\exp(-\mu)$$ ← Poisson distribution

$$p(n \geq 1) = \exp(-\mu)\sum_{n=1}^{\infty}\frac{\mu^n}{n!} = \exp(-\mu)\left(\exp(\mu) - 1\right) = (1 - \exp(-\mu))$$

$$p_d = p(n \geq 1) = (1 - \exp(-\mu))$$

$$\mu \equiv \rho\tau$$

Note: The dark count probability can be determined by counting avalanche events in the gated mode unilluminated diode and divided by total number of gates.

$\rho = -\ln(1-p_d)/ T_w$ where p_d = # of dark counts /total # of gates

Dark Counts

Sandia National Laboratories

Dark count probability: p_d
Dark count rate: ρ

$$p_d = 1 - \exp(-\rho T_w)$$

$$p(n) = \frac{\mu^n}{n!}\exp(-\mu)$$

Poisson distribution

Overbiased dark current

Net Dark current during gate is

$\Delta I_d = e\, n/T_w - I_{0d}$

$\Delta I_d = e\rho - I_{0d}$ $\quad \rho = (\Delta I_d + I_{0d})/e$

Reverse bias dark current
Below breakdown

Note: The dark count probability can be determined by counting avalanche event
the gated mode unilluminated diode and divided by total number of gates.

$\rho = -\ln(1-p_d)/T_w$ where p_d = # of dark counts /total # of gates

Estimate of Dark Counts

$I_{0d} = 1x10^{-12}$ A ≈
$n = (1x10^{-12} A \times 0.5x10^{-9}) / 1.602x10^{-19} = 0.00312$ per gate

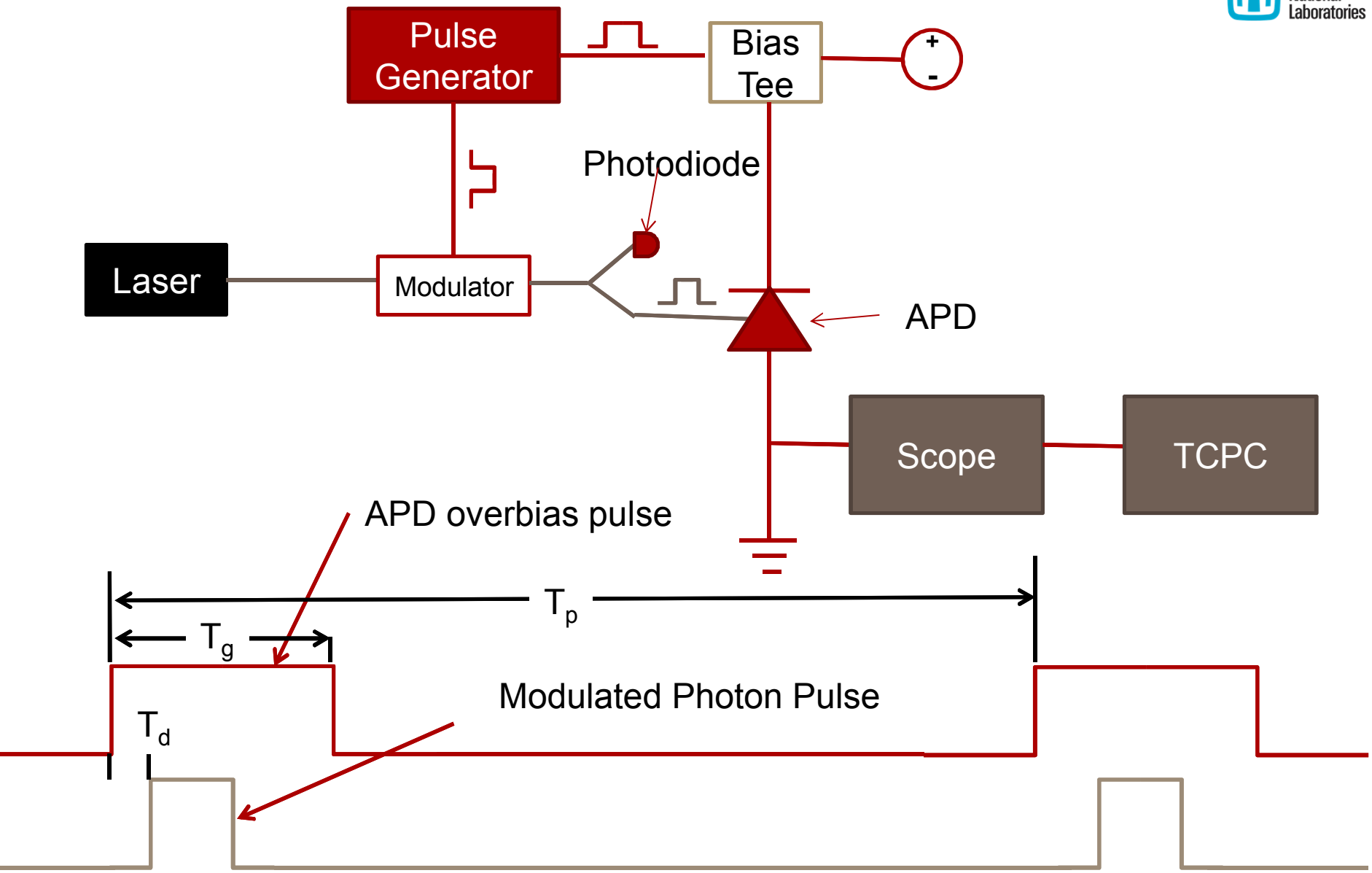
If we assume $p_d \approx 0.003$, $\rho \approx 6x10^6$ Dark Counts per second

Note, $\rho \approx n/T_w$
For KHz dark count rates, we need dark current of 1 fAmp.
This is readily doable with TE cooler.

Detection Efficiency

$$\eta = \frac{1}{\mu} \ln\left(\frac{1-p_d}{1-p_t}\right)$$

p_t = # of avalanche counts (light on)/ total # of gates
μ = average photon number


Pulse Generator
Bias Tee
+
-
Photodiode
Laser
Modulator
APD
Scope
TCPC
APD overbias pulse
T_p
T_g
Modulated Photon Pulse
T_d

Exceptional service in the national interest

Sandia National Laboratories

Photos placed in horizontal position with even amount of white space between photos and header

QKD Delay

U.S. DEPARTMENT OF ENERGY

National Nuclear Security Administration

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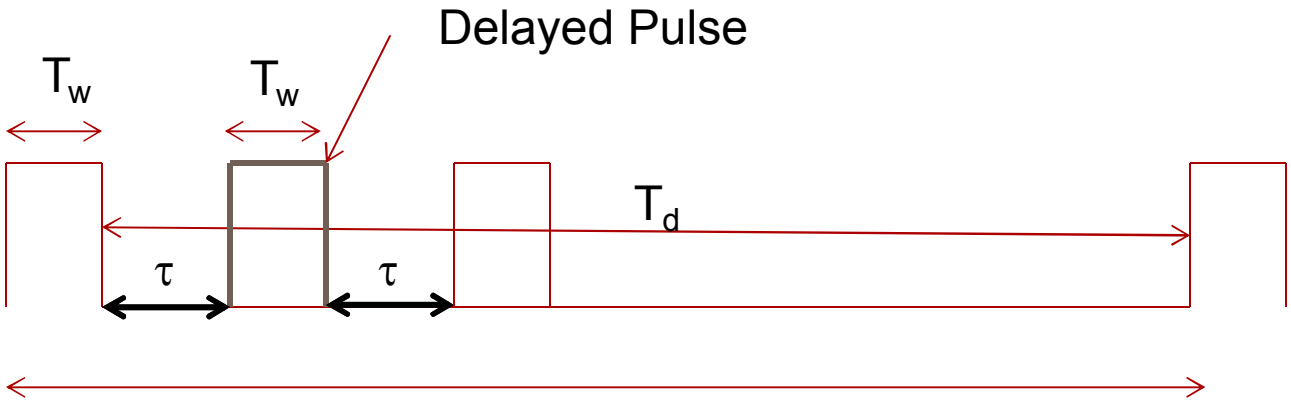


$T = T_w + T_d$

$T_w \sim 300$ ps

$\tau \sim 500$ ps

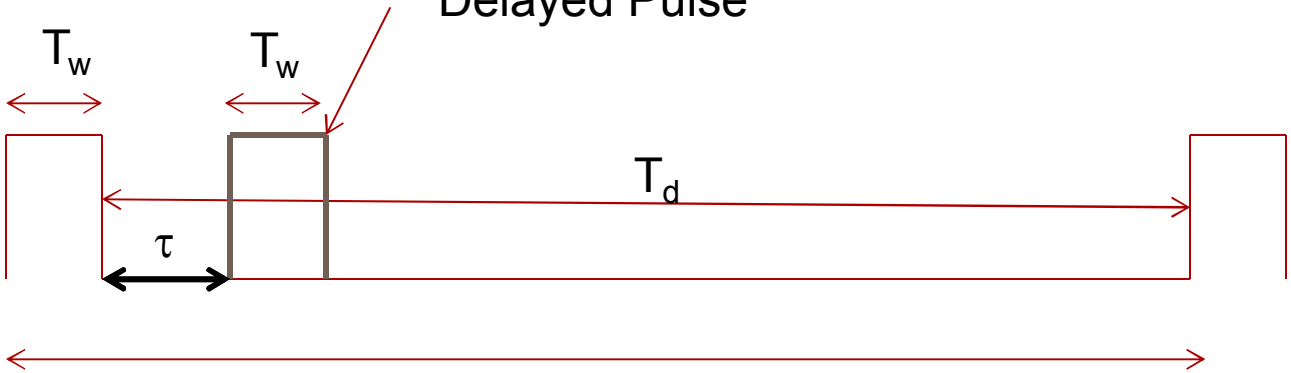
Total delay = $T_w + \tau =$ 500 ps +300 ps = Δt

$$\Delta l = \frac{c}{n_g}\Delta t$$

$\Delta l = 3.0 \times 10^{14}\ 0.8 \times 10^{-9} / 3.0 = 0.8 \times 10^{5}$ micron

$\Delta l = 8$ cm

Minimum Period of modulation= $T_{dmin} = 2T_w + 2\tau = 1.6$ ns –> 625 MHz



$T = T_w + T_d$

T_d= 50 ns

T_w ~ 300 ps

τ ~ 500 ps

Total delay = $T_w + \tau =$ 500 ps +300 ps = Δt

$$\Delta l = \frac{c}{n_g}\Delta t$$

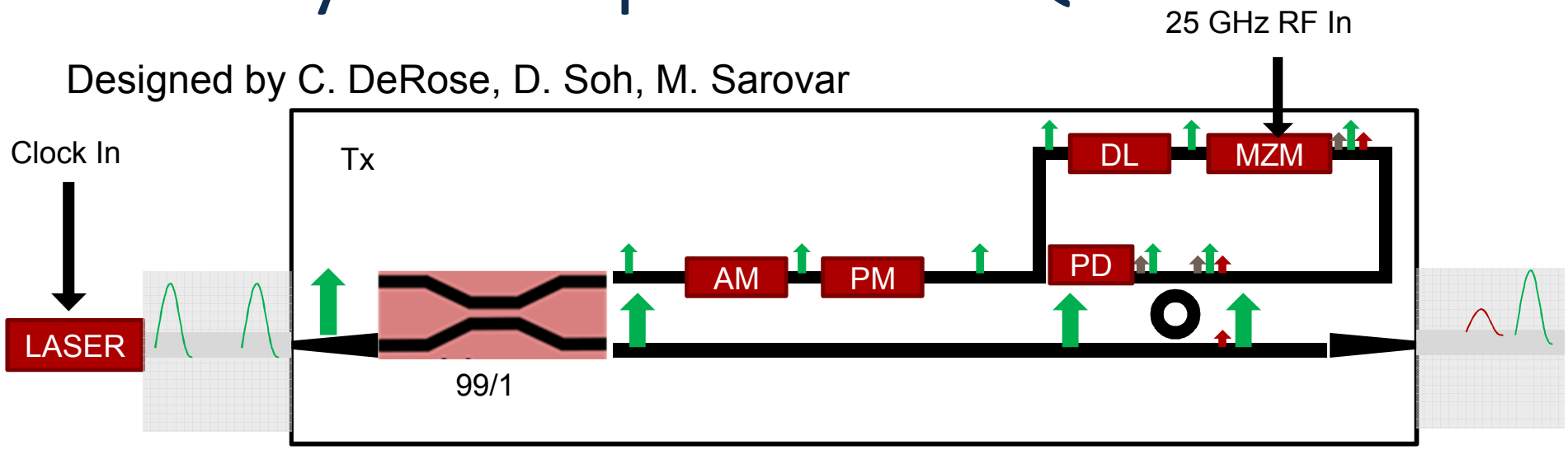
Δl= 3.0×10^{14} 0.8×10^{-9} /3.0 = 0.8×10^{5} micron

Δl= 8 cm

Minimum Period of modulation= $T_{dmin} = T_w + T_d$ =50.3ns –> 19.8 MHz

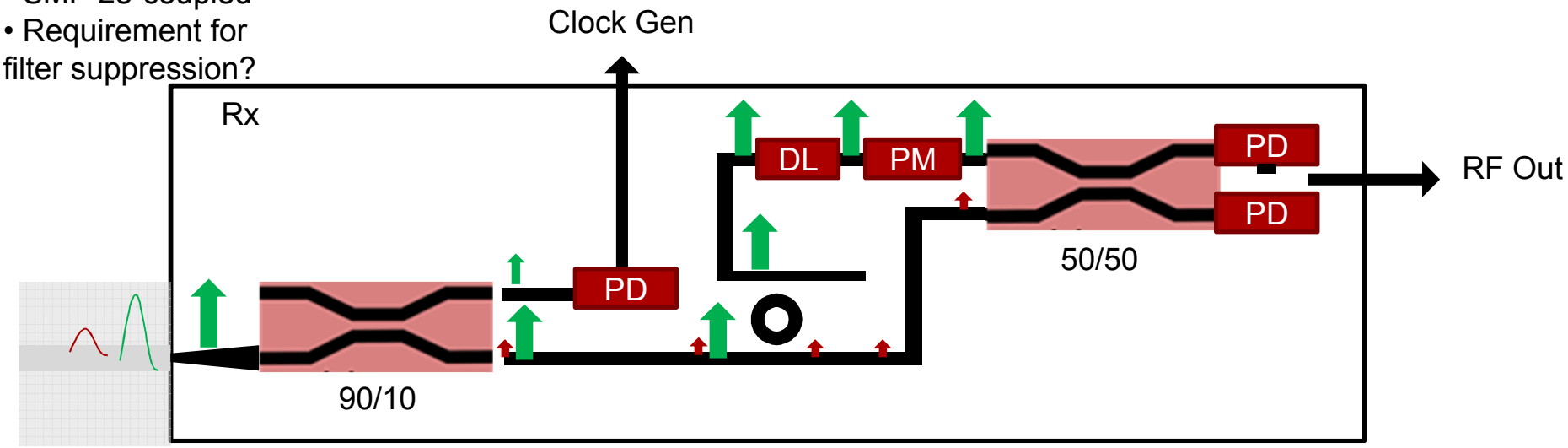
Heterodyned Chip-scale CV-QKD

Designed by C. DeRose, D. Soh, M. Sarovar



- 1 ns pulse
- 1 MHz rate
- SMF-28 coupled
- Requirement for filter suppression?

AM – amplitude modulator, PM – phase modulator, DL – 2 ns delay line, MZM – Mach-Zehnder modulator, PD - photodiode



BACK

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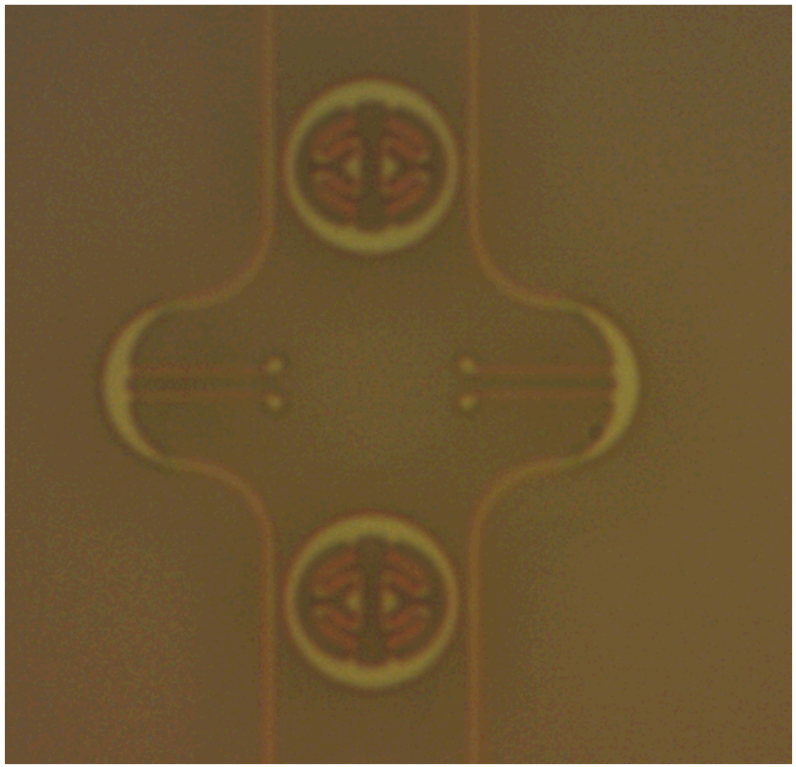
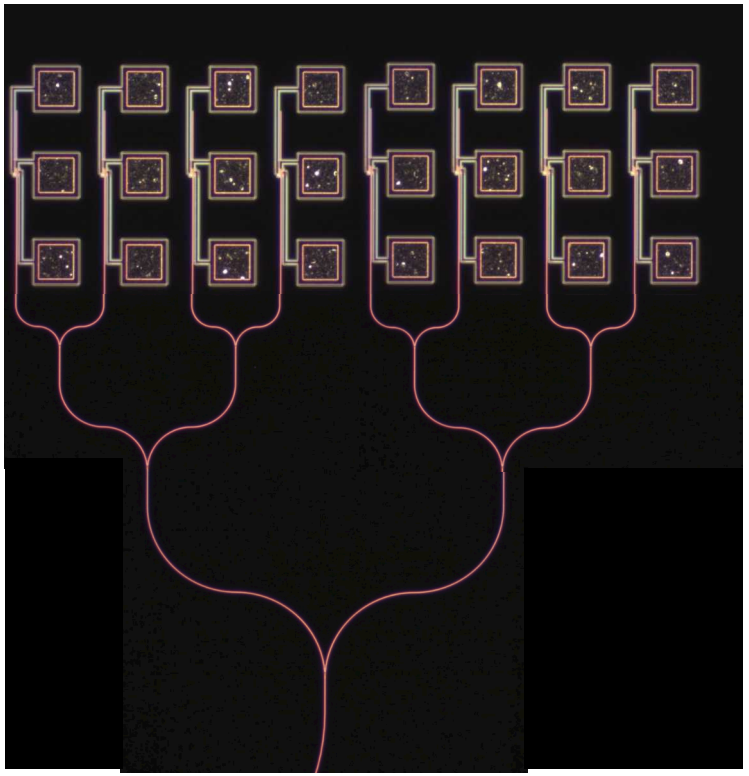
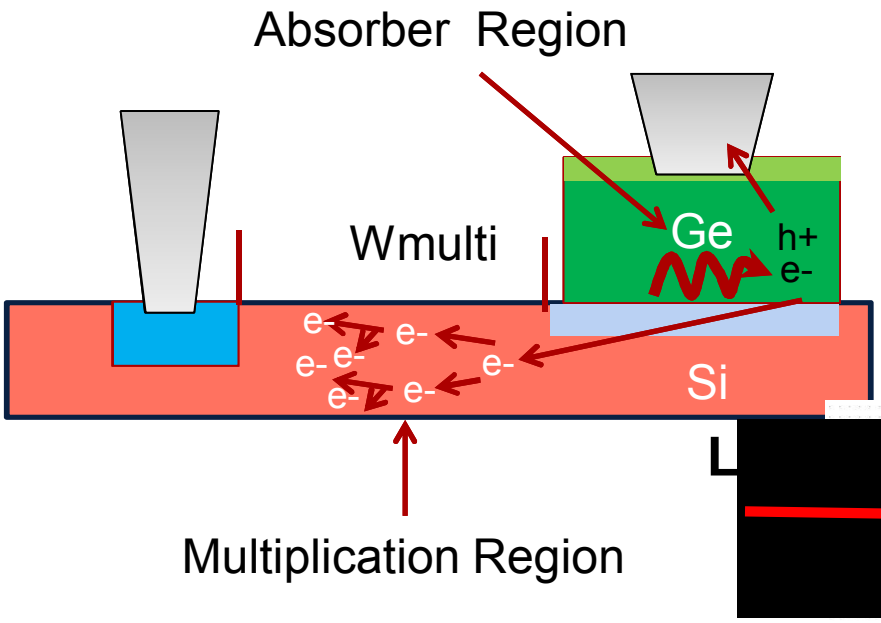
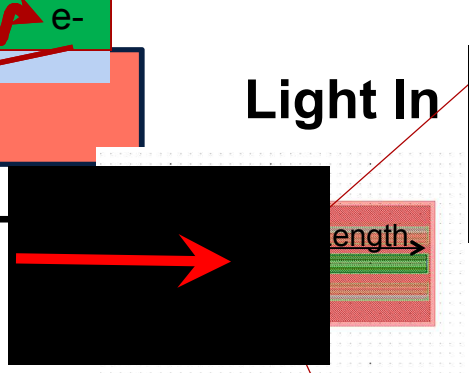




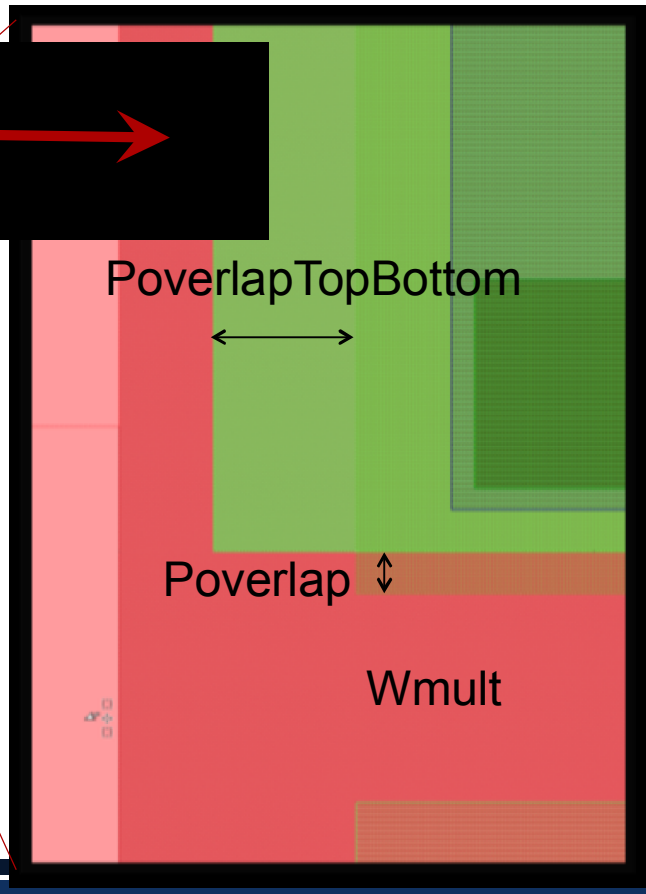
Integrated lateral APD results



Lateral APD in X-section

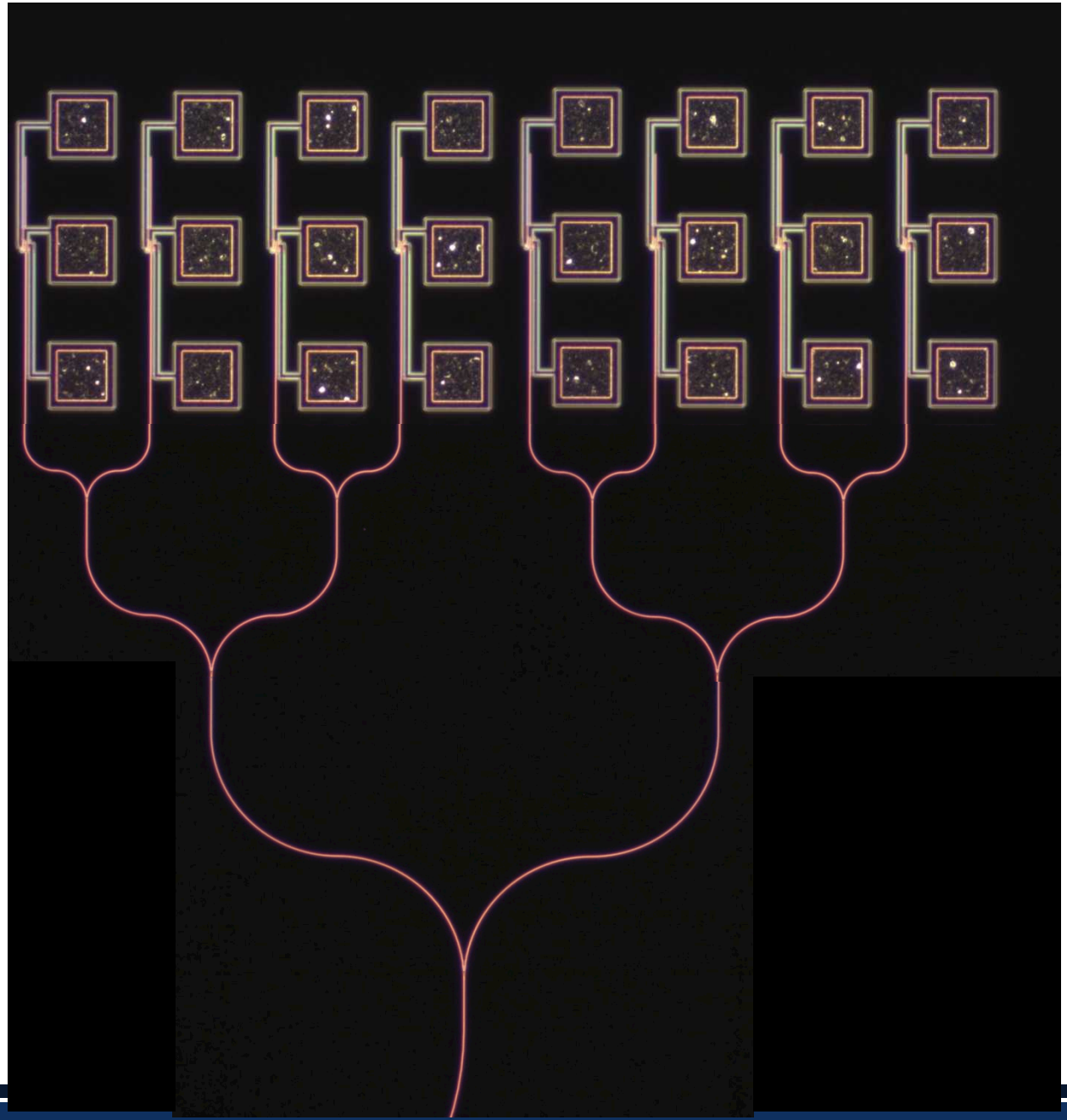


Top down view



Top down view shows variation of multiplication Width and p-Charge layer overlap.

Together with implant doses we vary these parameters.



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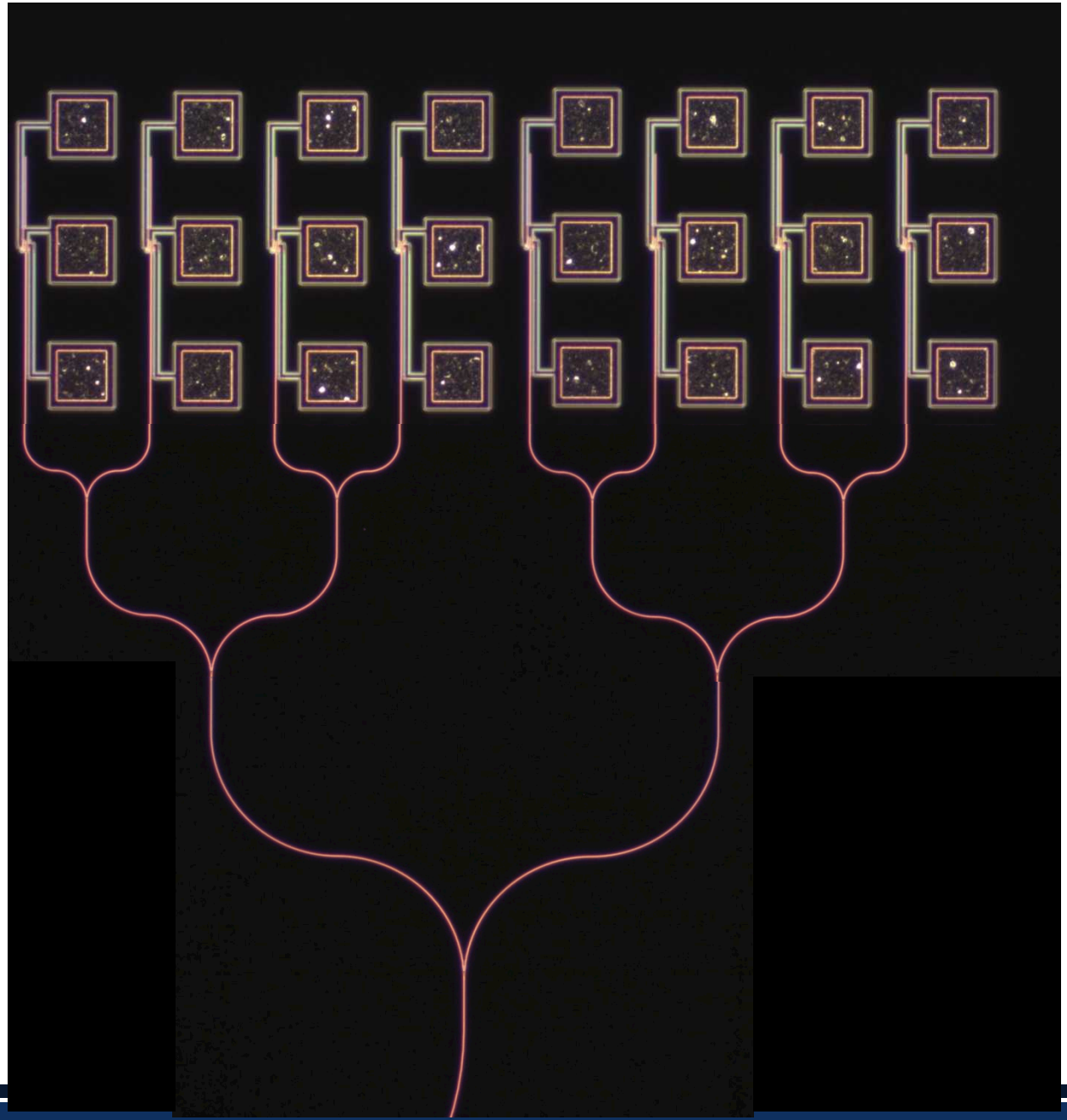

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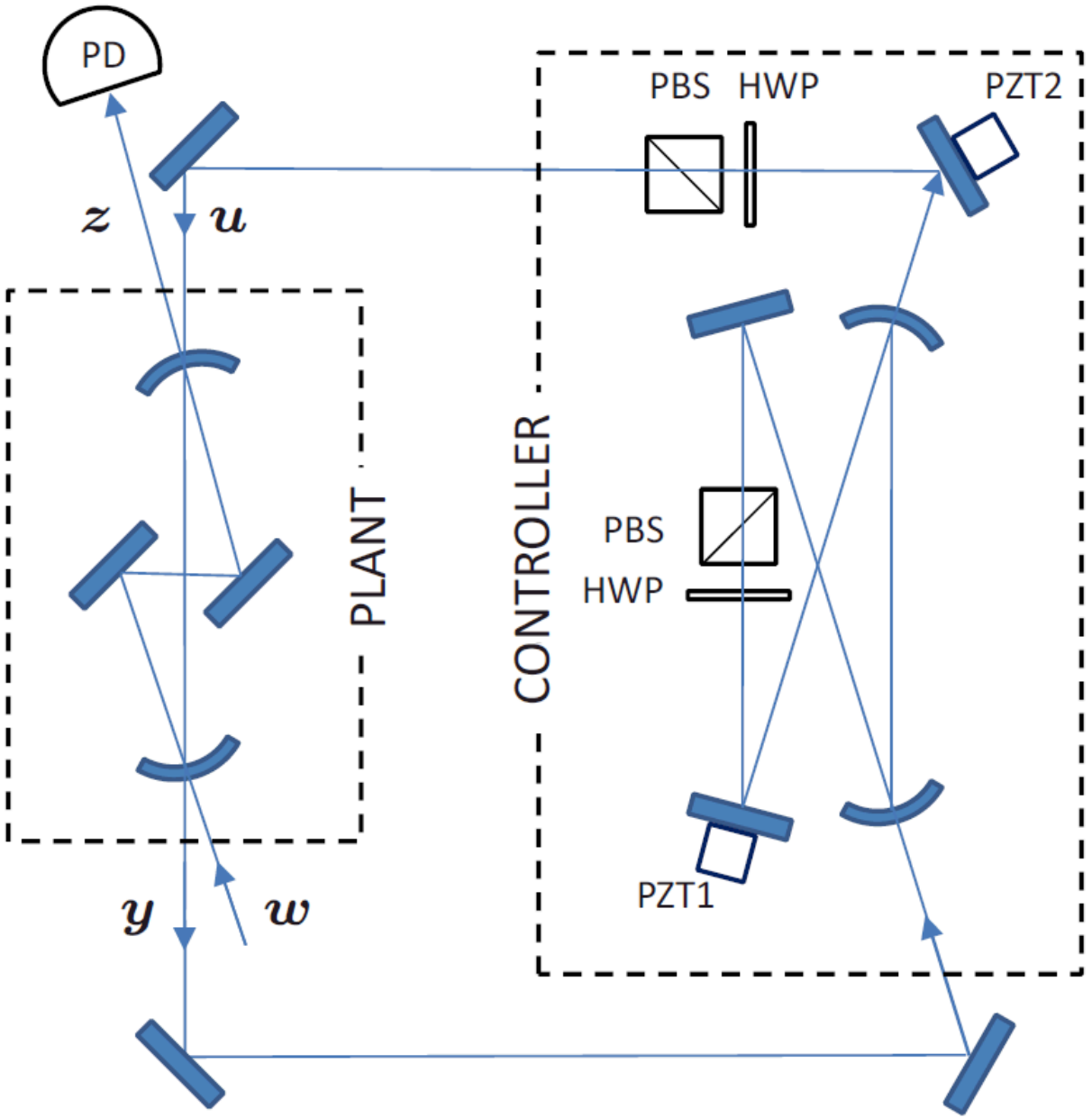
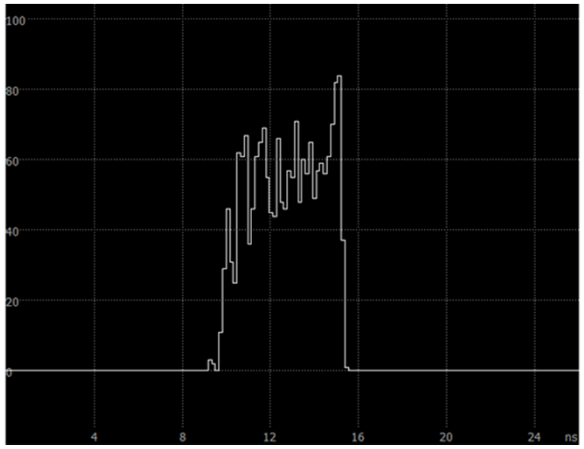

PD
z
u
PLANT
y
w
CONTROLLER
PBS
HWP
PZT2
PBS
HWP
PZT1

Product	InGaAs SPAD
QE at 1550nm	10-25%
Spectral range	950-1600
Dark count rate	<10kct/s
Timing resolution	<300 ps
Afterpulsing	1%
Detection rate	100MHz (trigger)
Gate width	0.1 - 100 ns
Hold-off time	1 - 3000us
Price	$25k

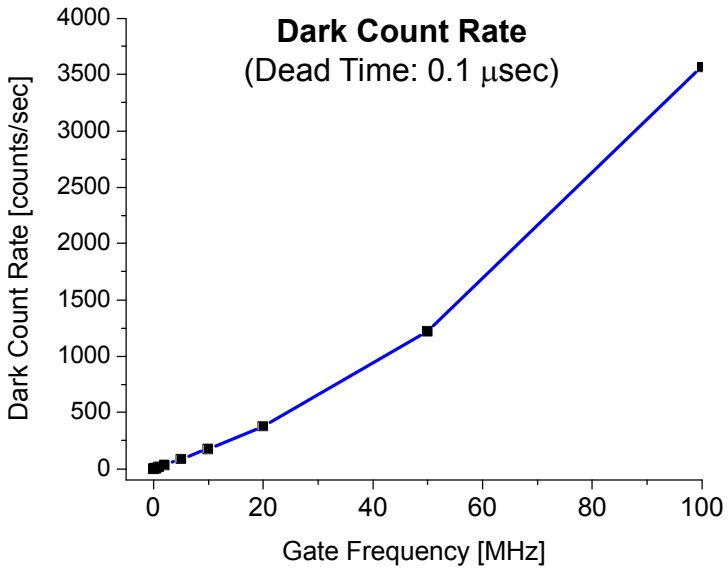
Target integrated SPAD performance

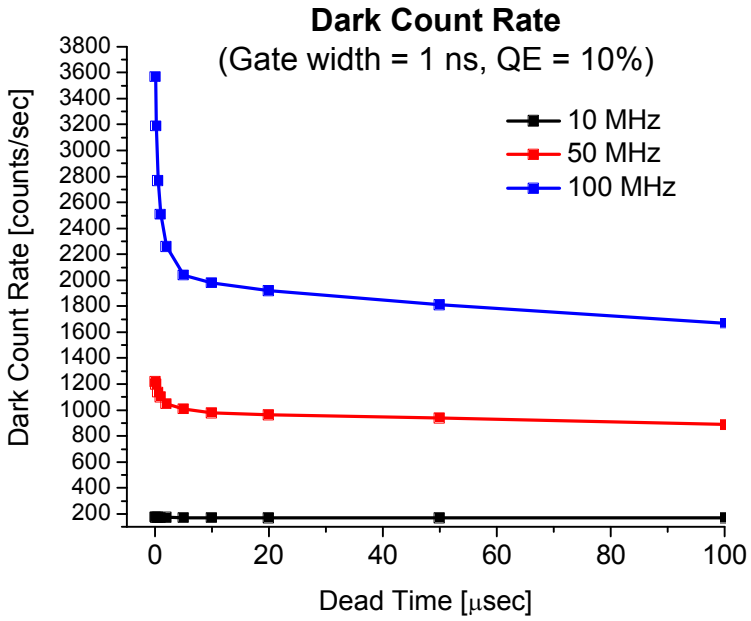
IDQ InGaAs APD



TDC Gate Width Histogram

Product	InGaAs SPAD
QE at 1550nm	10-25%
Spectral range	950-1600
Dark count rate	<10kct/s
Timing resolution	<300 ps
Afterpulsing	1%
Detection rate	100MHz (trigger)
Gate width	0.1 - 100 ns
Hold-off time	1 - 3000us
Price	$25k





Component Characterization: COTS APDs

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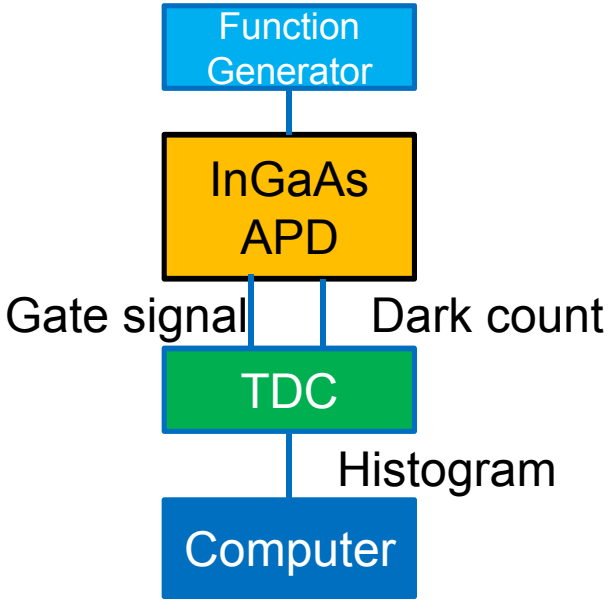
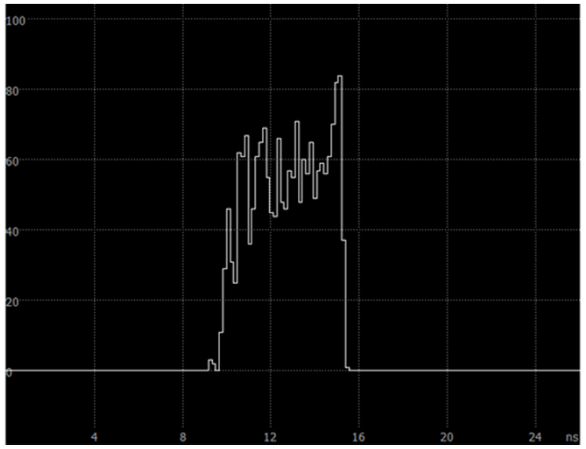
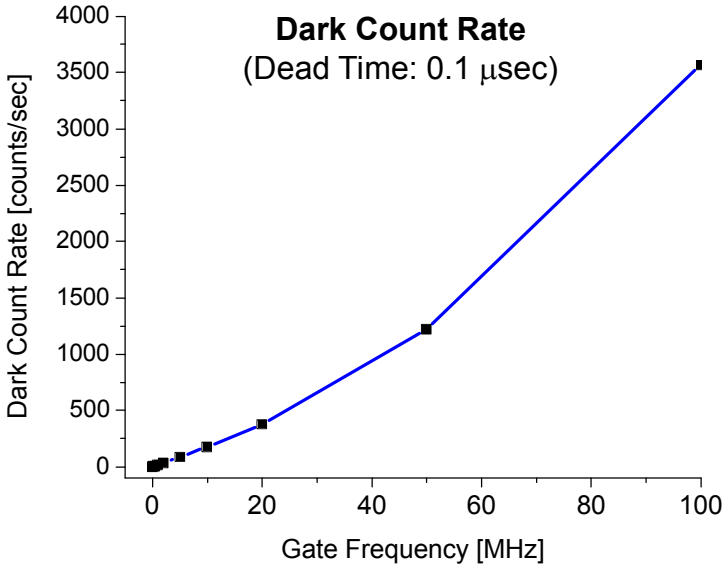
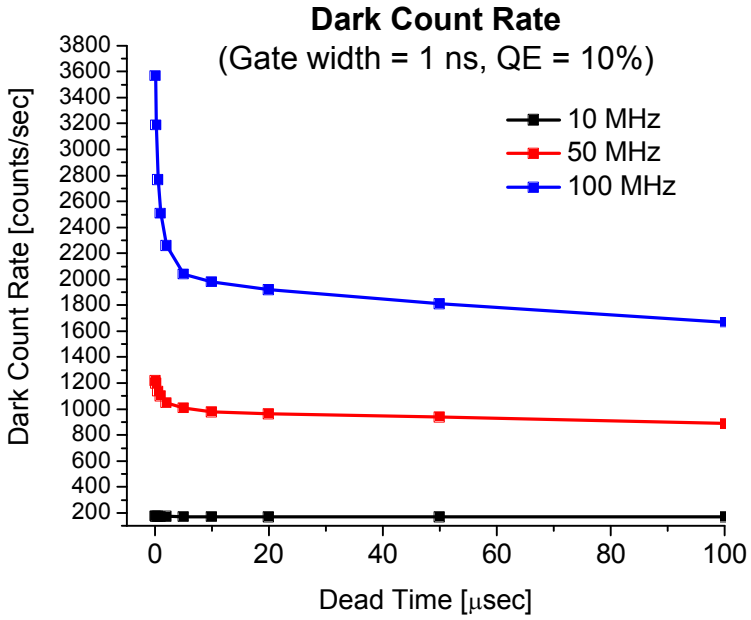


IDQ InGaAs APD



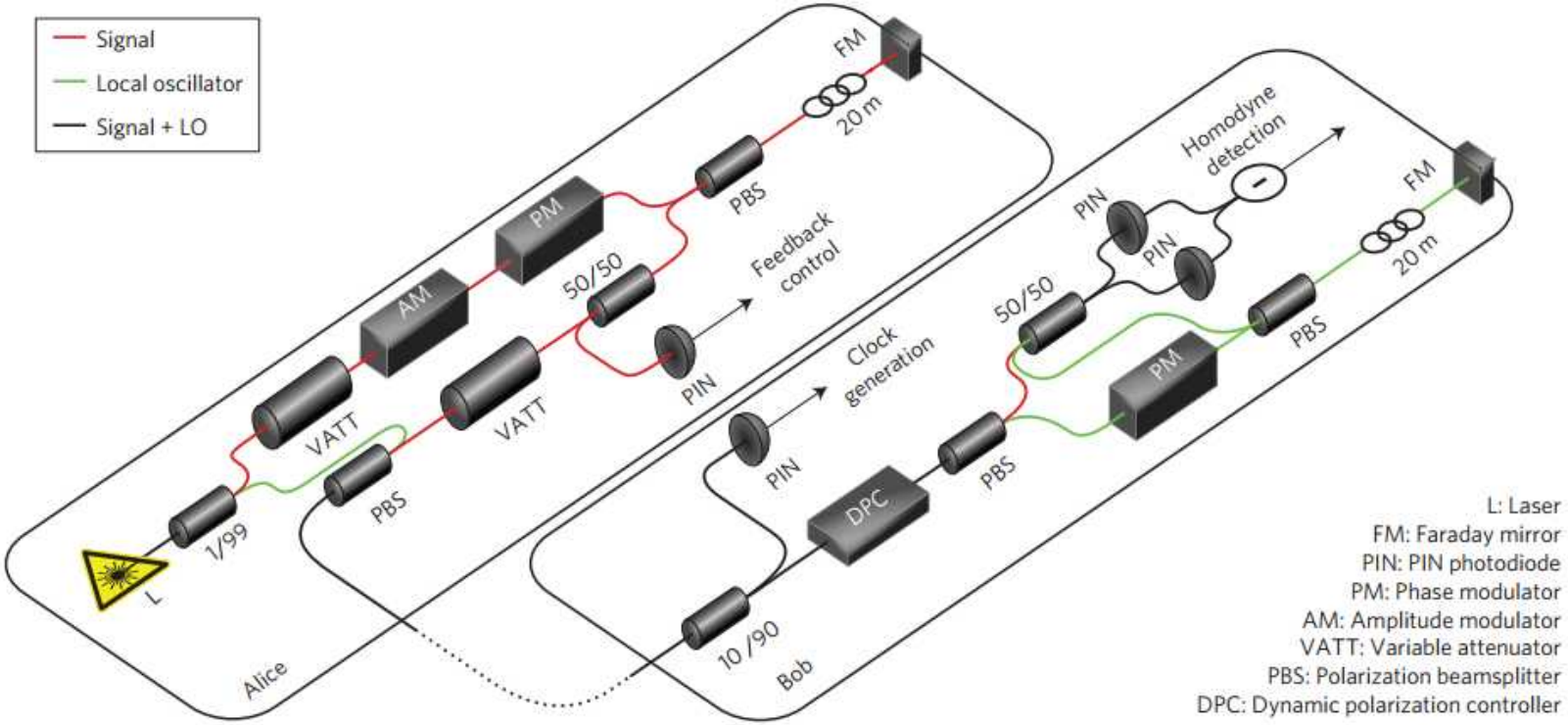
TDC Gate Width Histogram





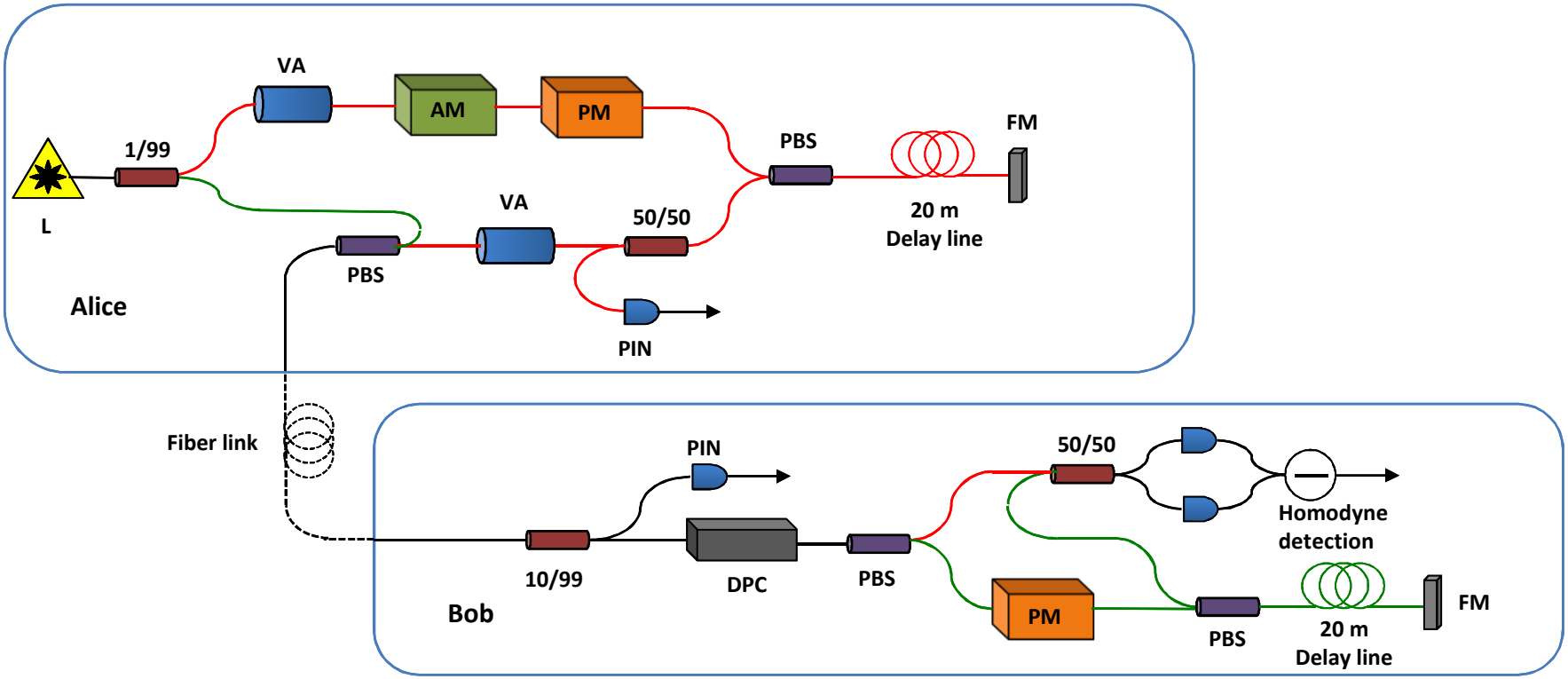
Bench-top CV-QKD link

Recent Publication using
COTS fiber optics.



P. Jouguet, S. Kunz-Jacques, A. Leverrier, P. Grangier, and E. Diamanti. Experimental demonstration of long-distance continuous-variable quantum key distribution. Nature Photonics, 7(5):378–381, 2013.

CV-QKD fiber test bed



- Coherent source is a CW laser.
- Bob randomly chooses measuring quadrature by phase-shifting the local oscillator.
- Eve randomly chooses measuring quadrature by phase-shifting the local oscillator.
- Eve's quadrature measurement squeezes the light (reduces the noise) in measured quadrature, but greatly increases the noise in the other quadrature (uncertainty principle).
- Local oscillator is temporally multiplexed and transmitted in the same fiber.

InP to Si Waveguide Grating Coupling

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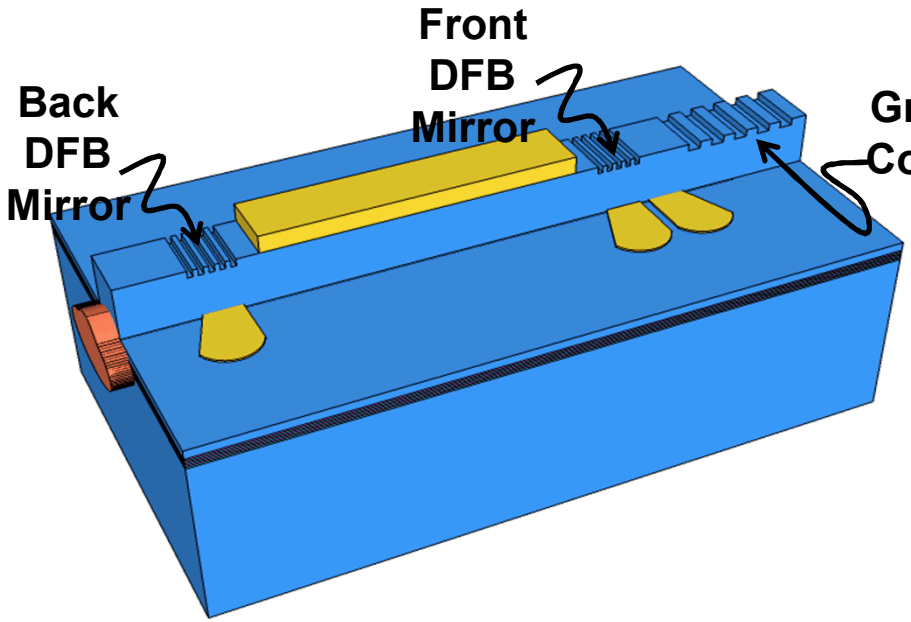
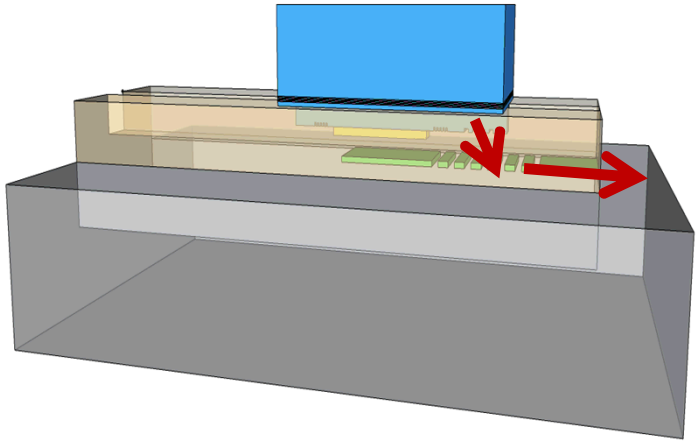
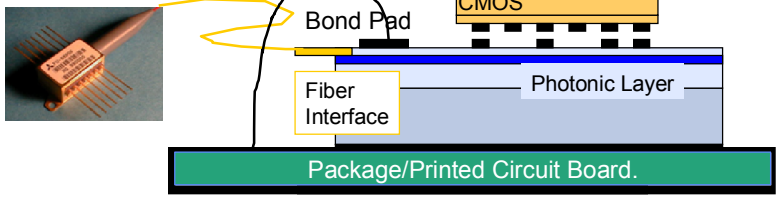
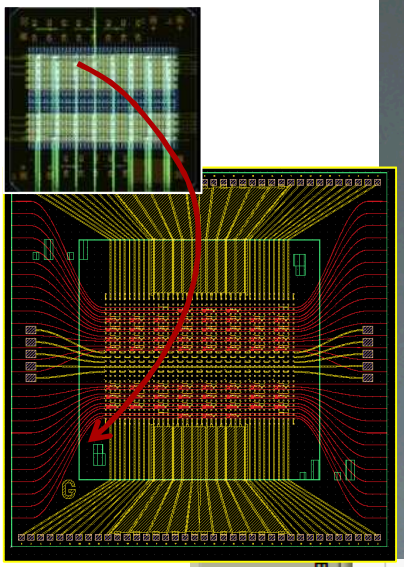
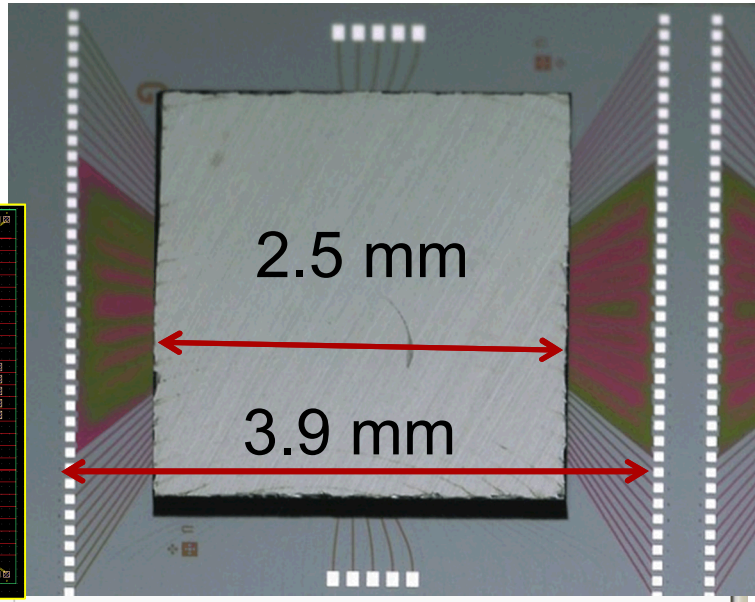




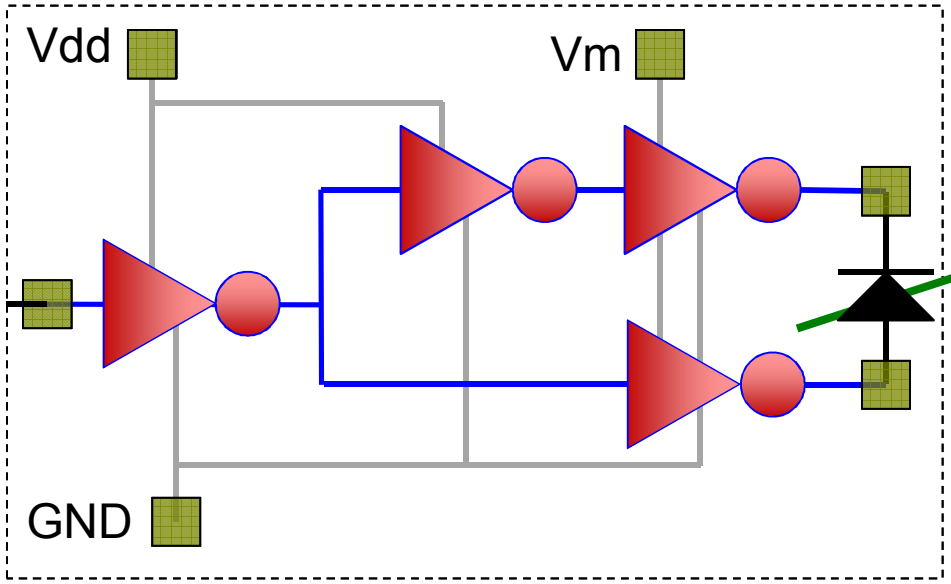
Electronic-Photonics Integration

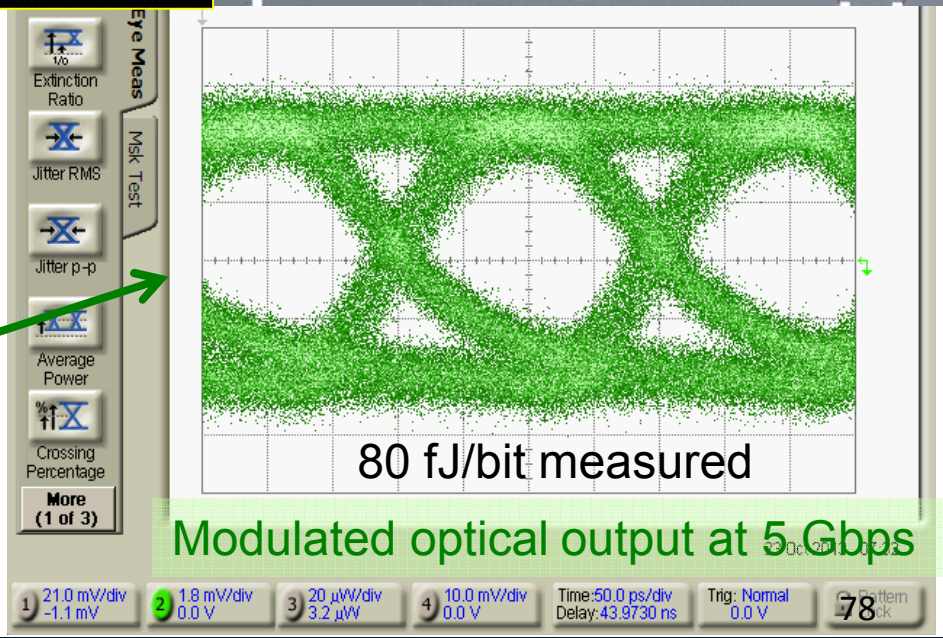




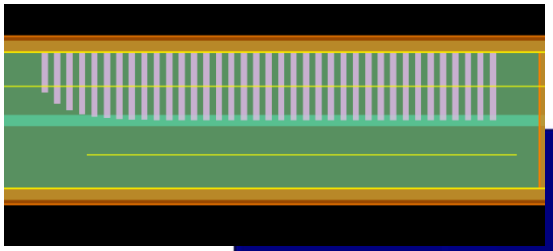


- Heterogeneous integration
  - Independent optimization of electronics & photonics
  - Challenge: Need high yields and small bond size

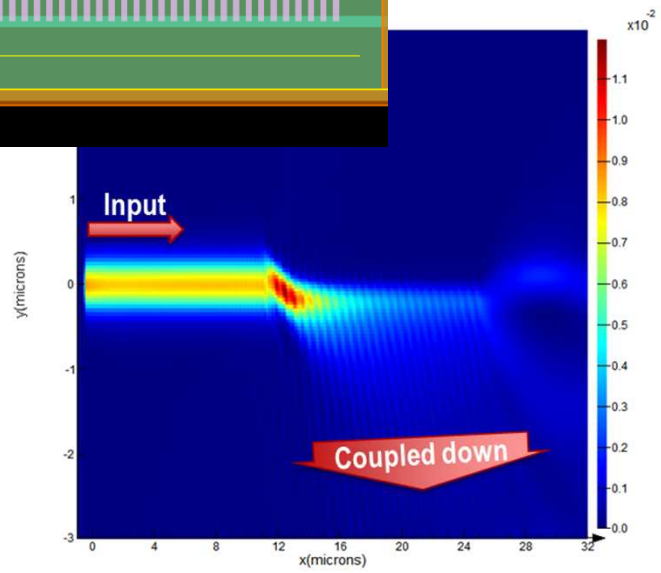




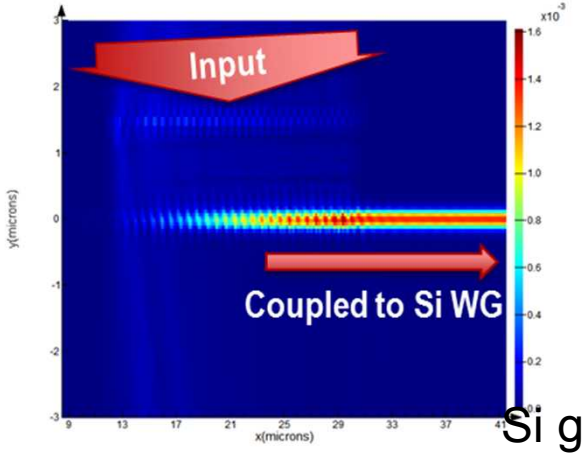
InP-to Si Grating Simulations

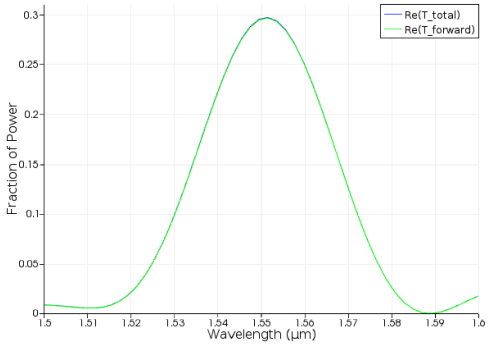


InP coupler



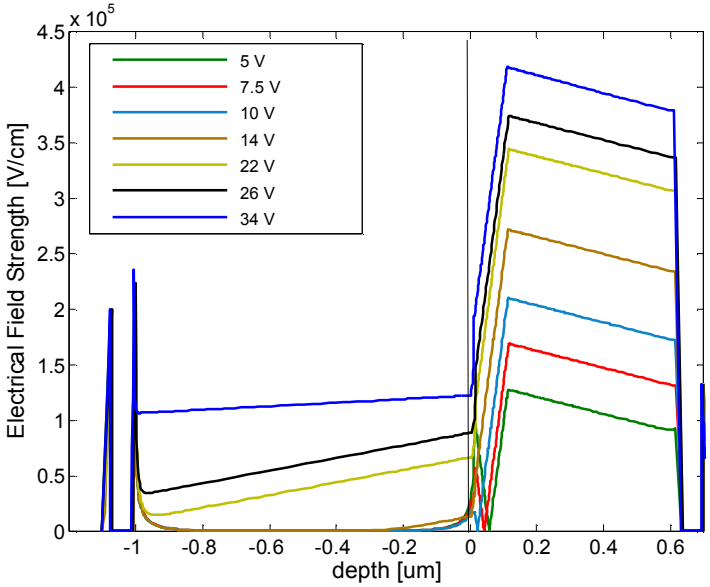
- InP coupler design
  - > 52% power coupled down
  - < 5° farfield angle
- Si coupler design
  - Input the InP coupler mode field
  - ~30% is coupled into the Si WG
- Next step
  - Combine InP and Si simulations
    - Will allow more design optimization

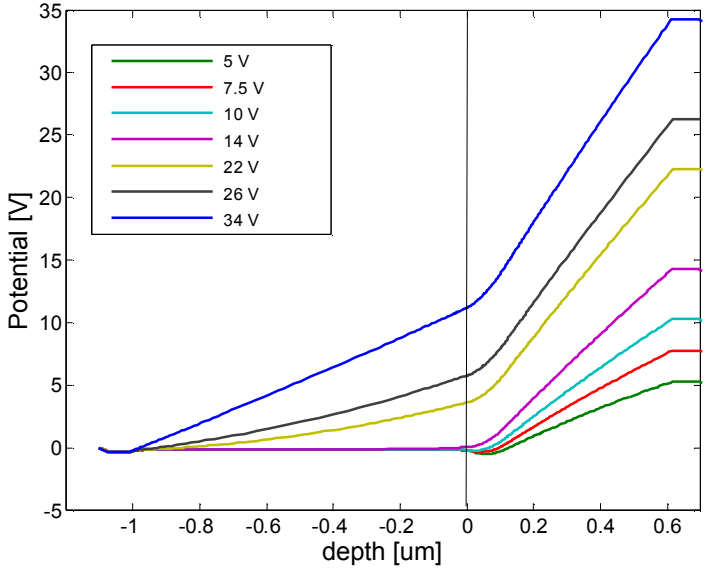


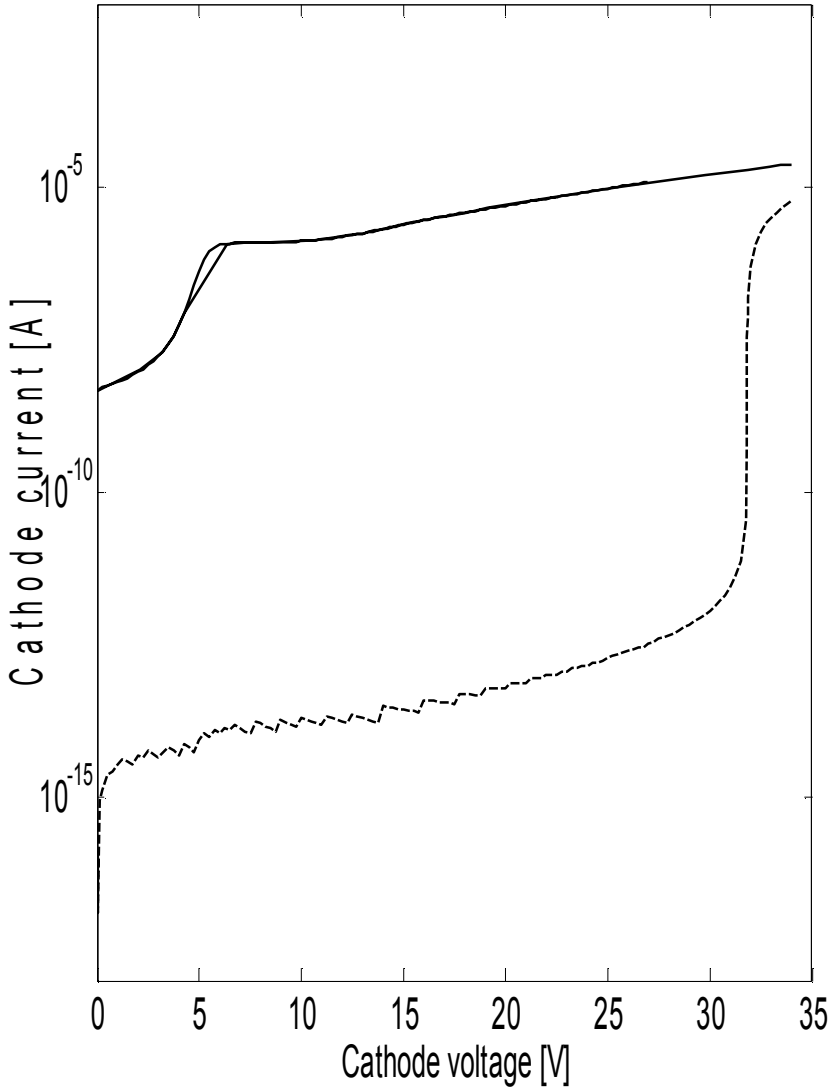


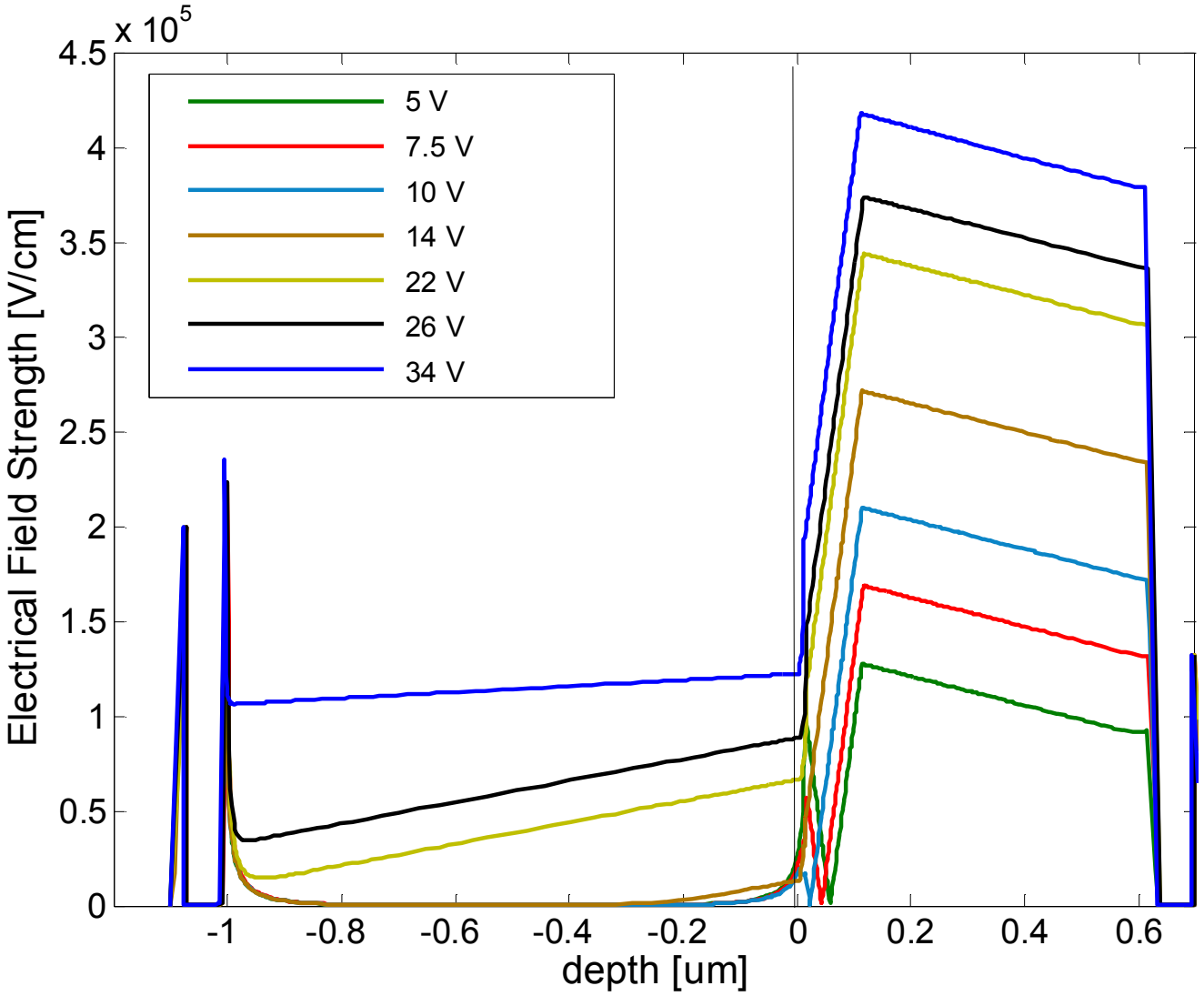
Si grating coupler

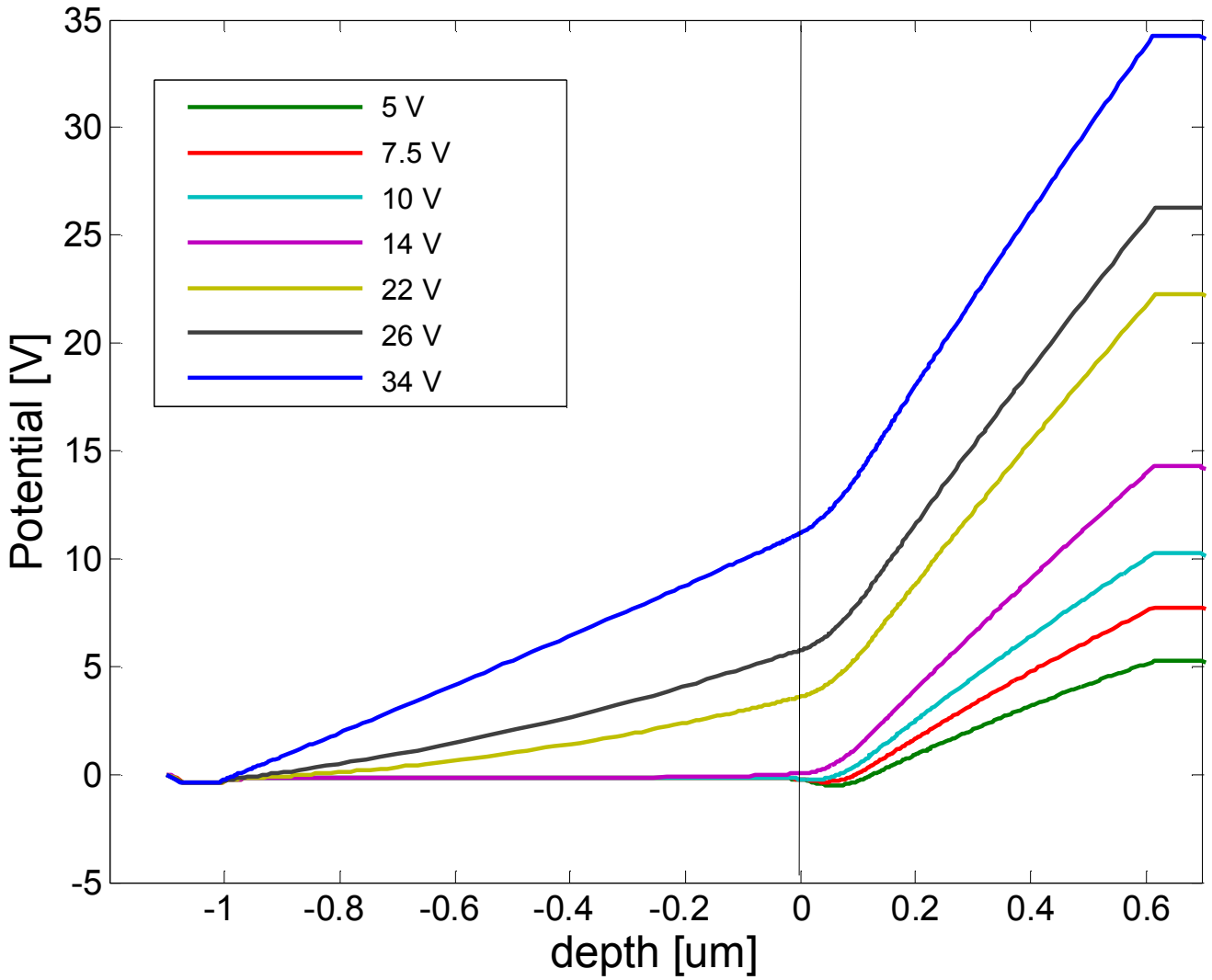
Device Simulations

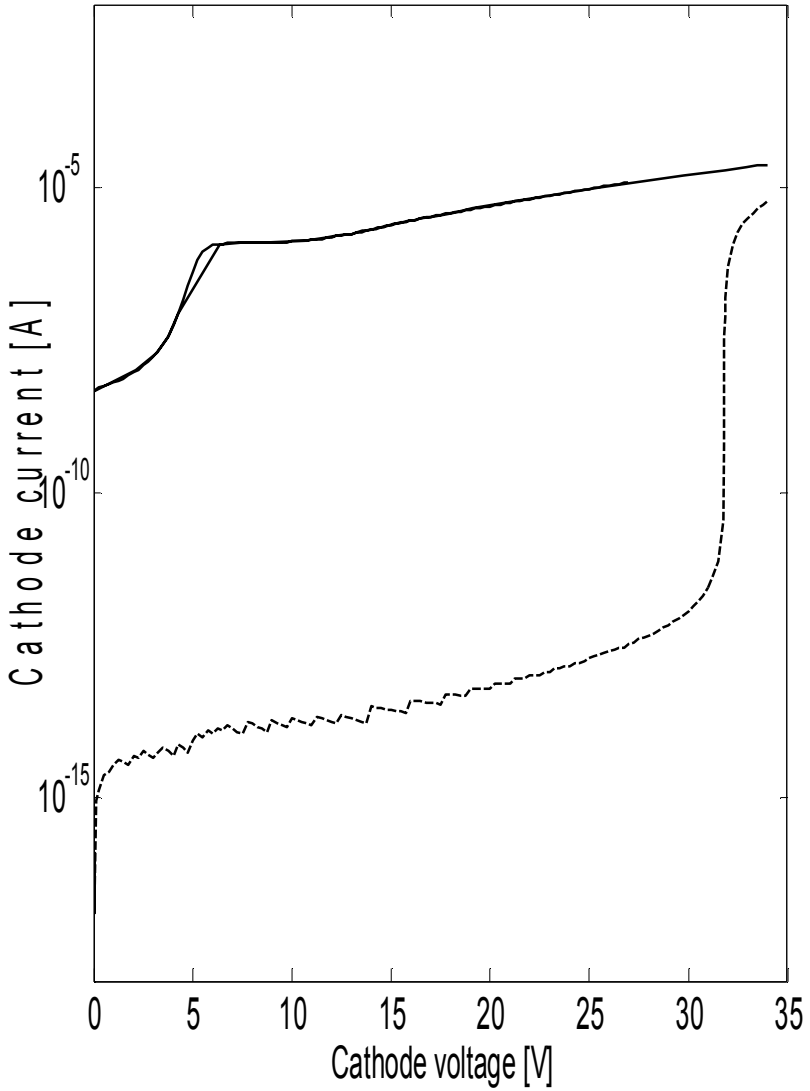




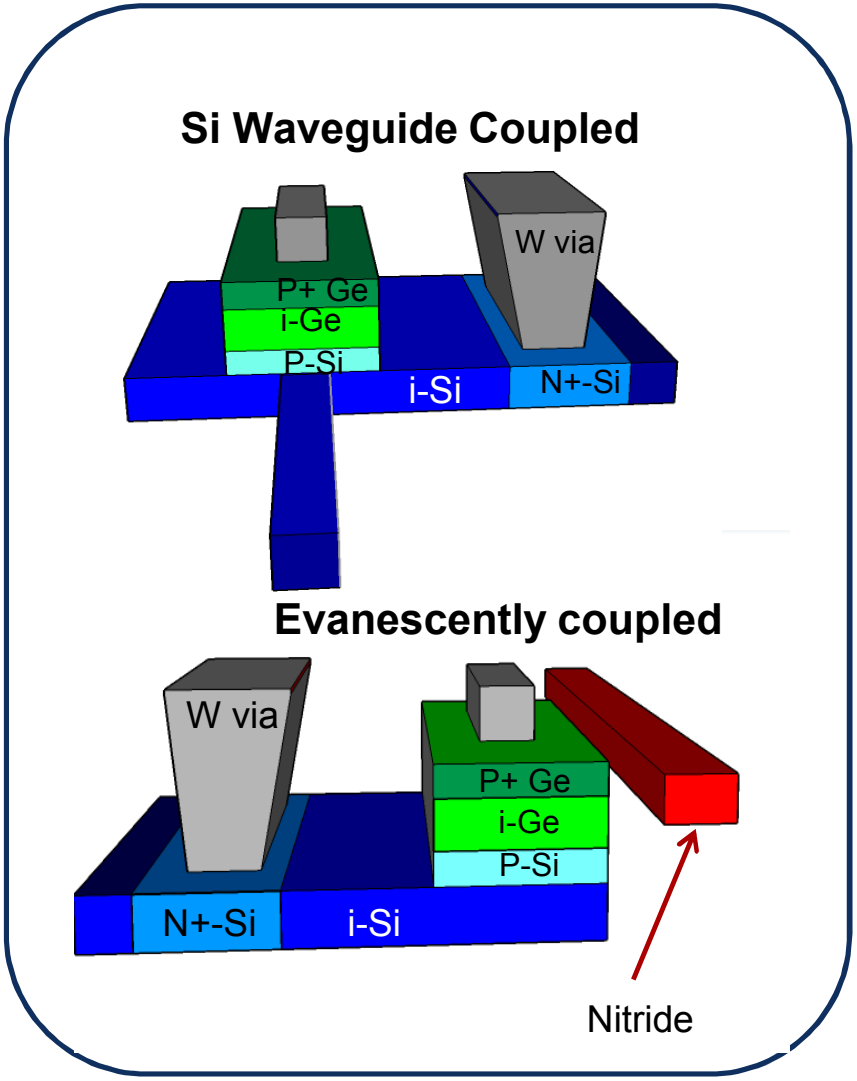



x 10^5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
Electrical Field Strength [V/cm]
5 V
7.5 V
10 V
14 V
22 V
26 V
34 V
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
depth [um]

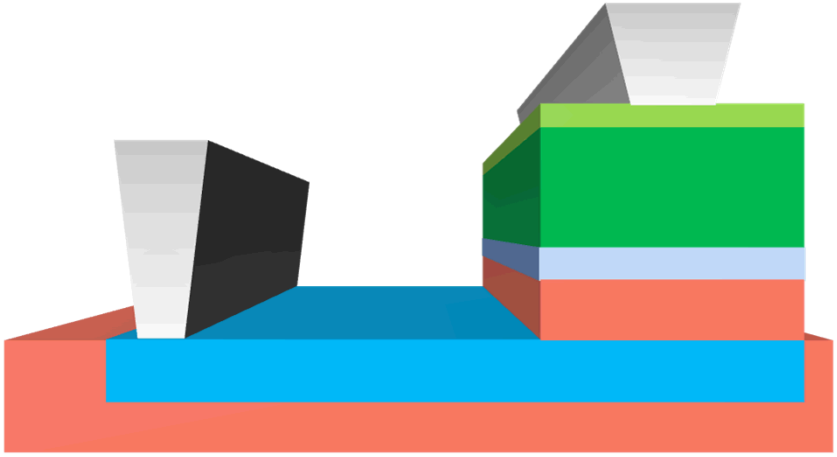

5 V
7.5 V
10 V
14 V
22 V
26 V
34 V
Potential [V]
depth [um]
35
30
25
20
15
10
5
0
-5
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6

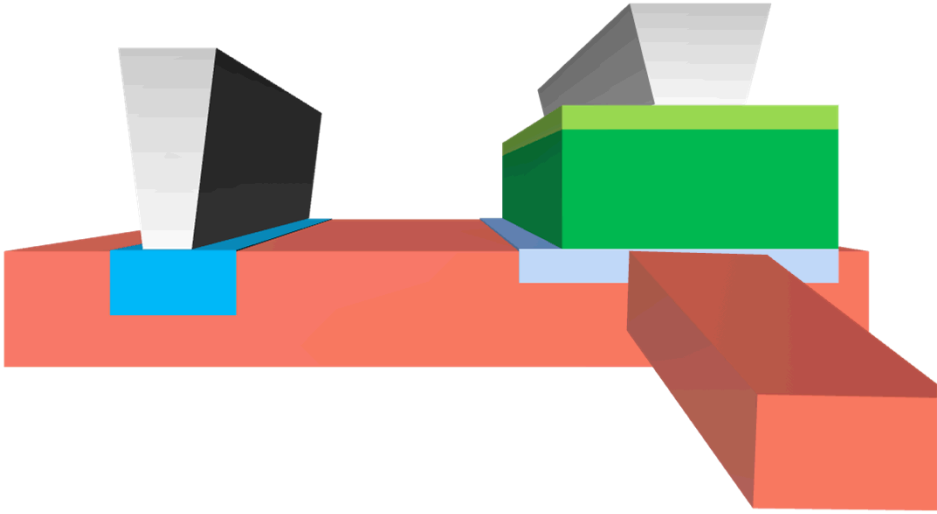

Cathode current [A]
10^-5
10^-10
10^-15
0
5
10
15
20
25
30
35
Cathode voltage [V]

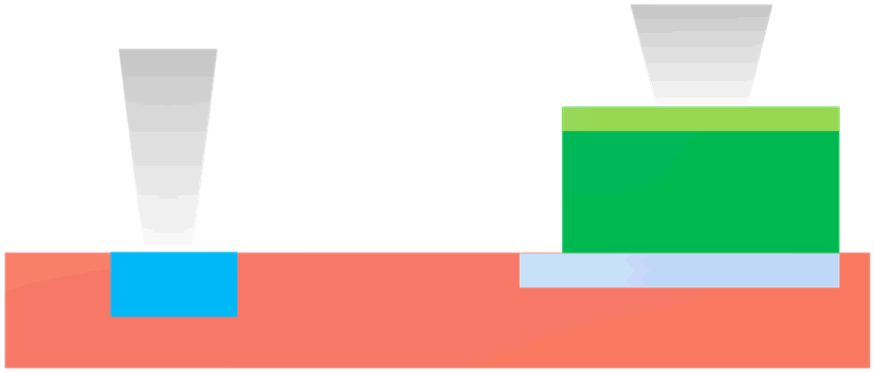
Integrated Waveguide Coupled SPAD



- ***Separate absorption and charge multiplication APD***
- Lateral and Vertical (not shown) APD designs.
- Selective Ge on Si Epitaxial growth.
  - Vertical design uses Si selectrive epitaxial growth.
- Waveguide-Coupling
  - Si end-fired
  - Nitride waveguide evanescent coupled







P+ Ge

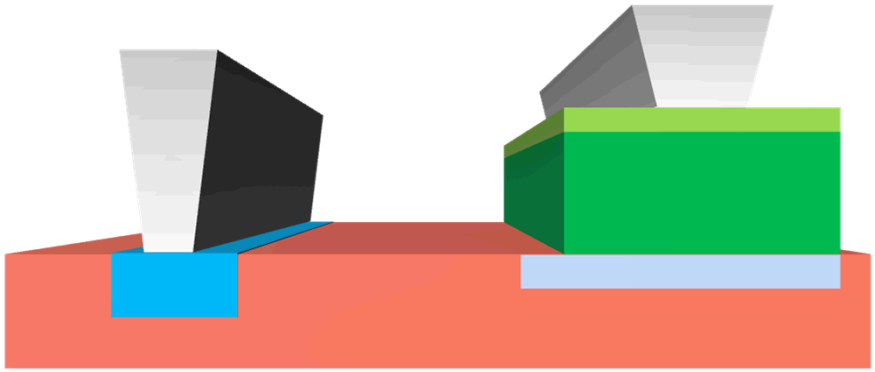
Ge

Si

P-Si

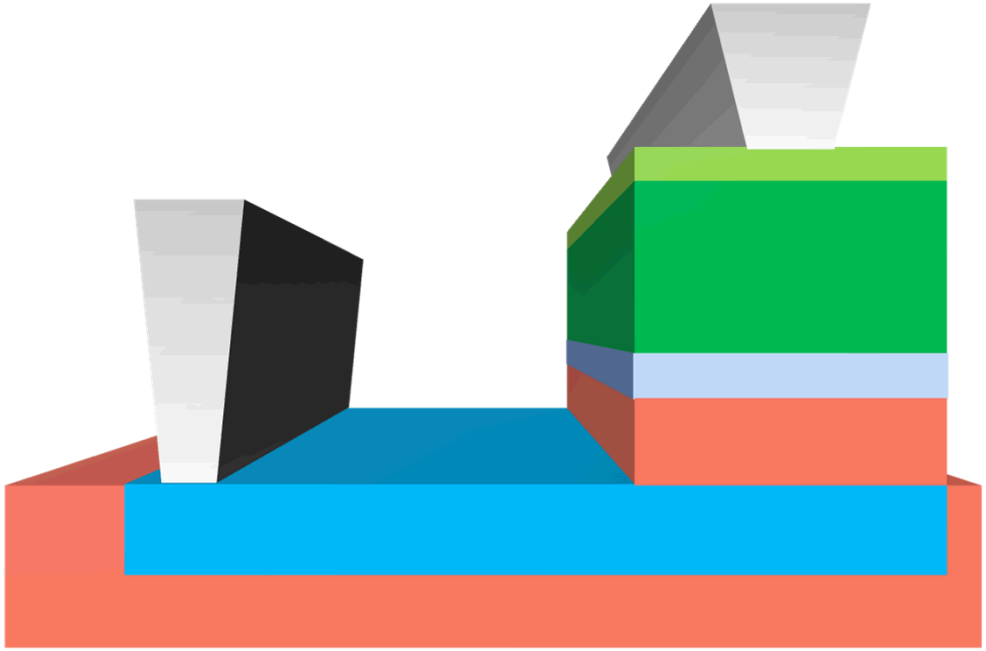
N+ Si

Integrated lateral APD results



Top down view shows variation of multiplication
Width and p-Charge layer overlap.

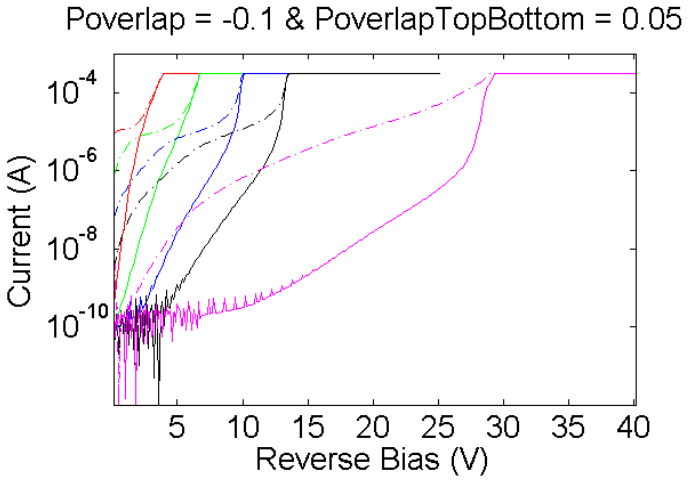
Together with implant doses we vary these parameters.

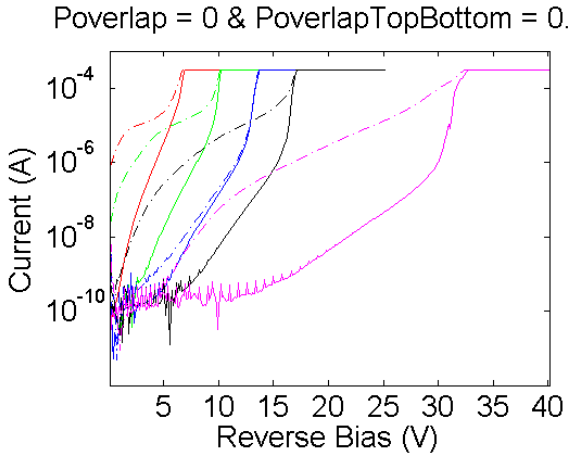


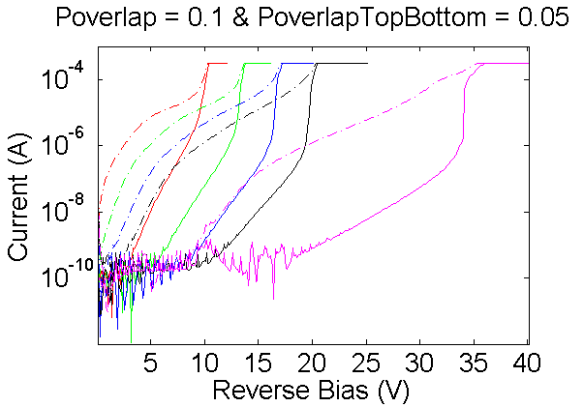
Top down view shows variation of multiplication Width and p-Charge layer overlap.

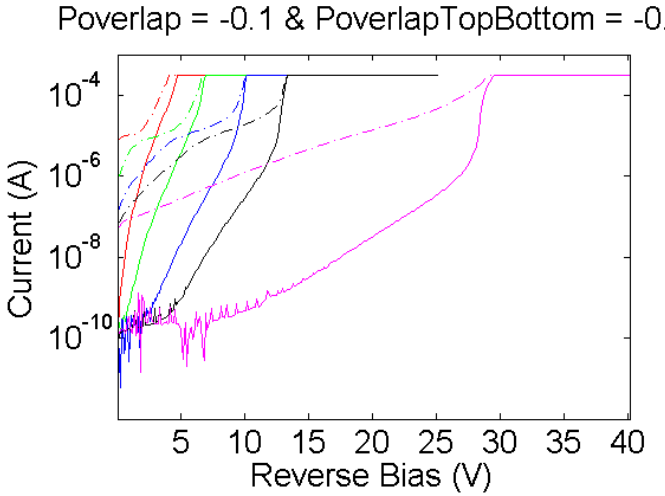
Together with implant doses we vary these parameters.

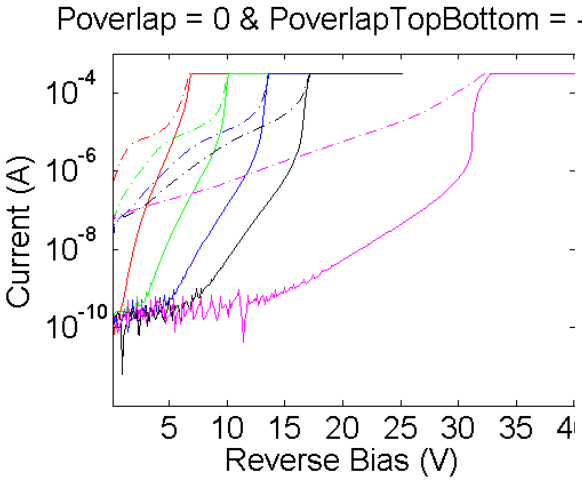
Light On (Dashed Curve) L = 16

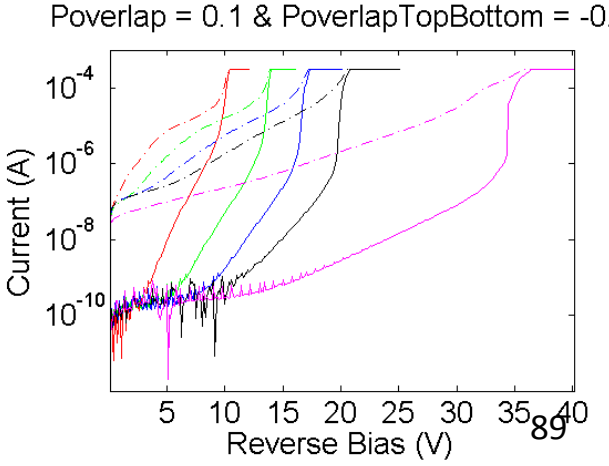




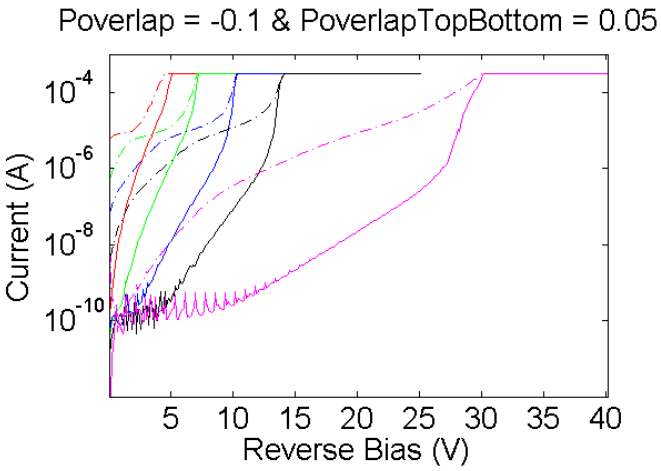


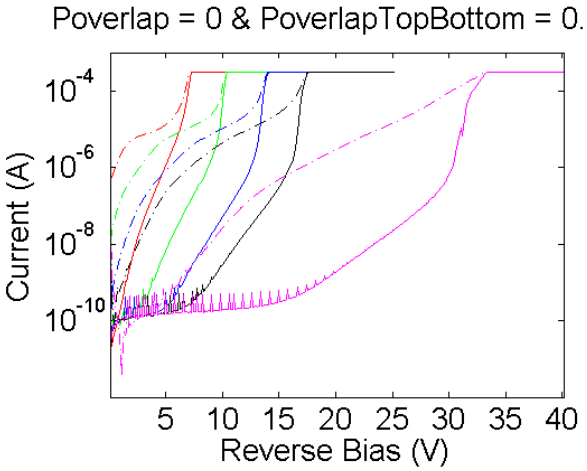


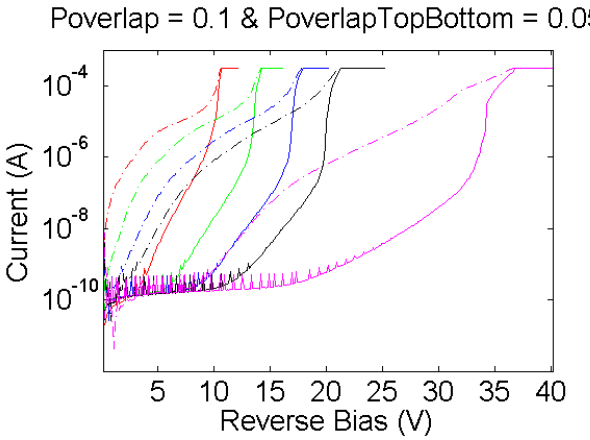


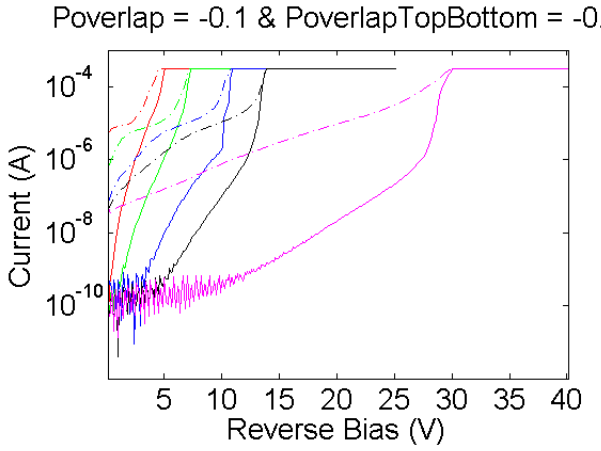


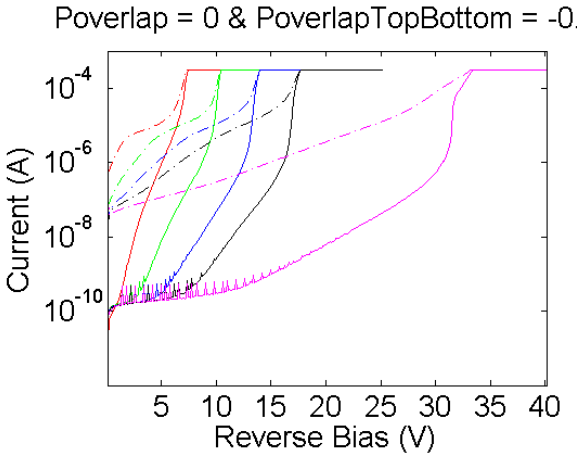
Light On (Dashed Curve) L = 8

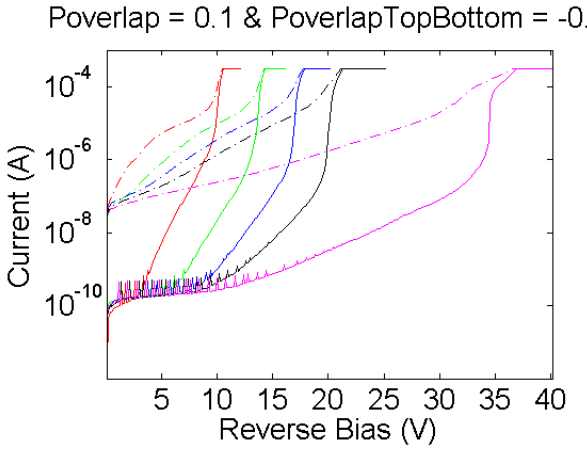




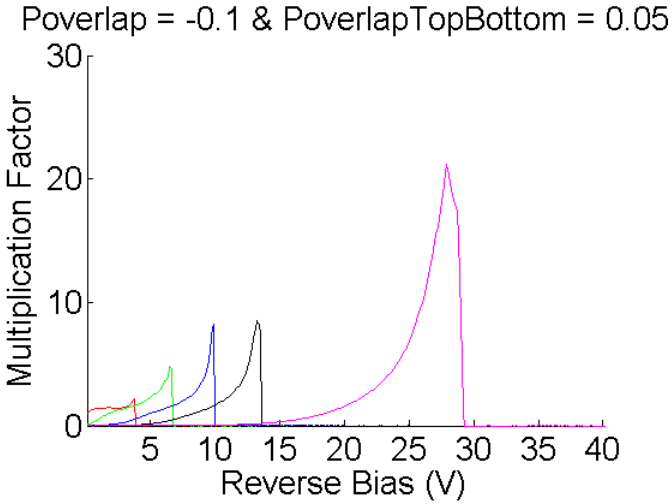


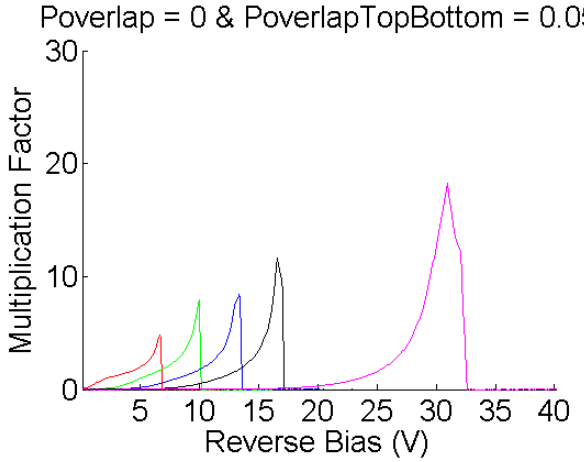


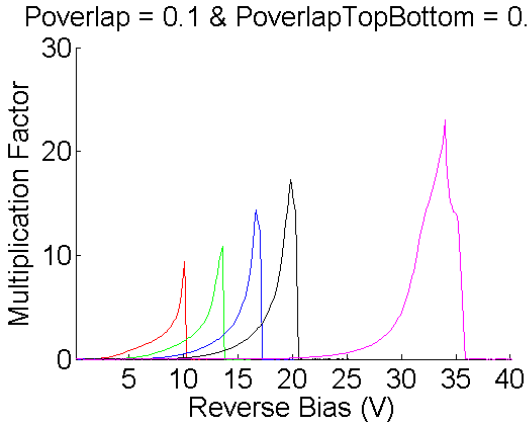


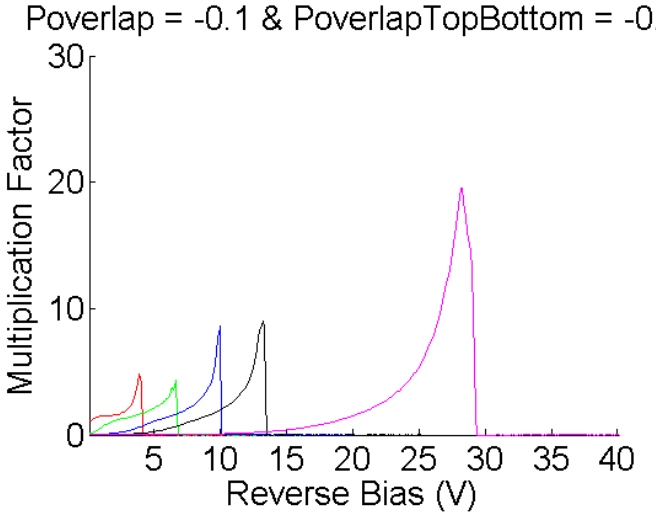


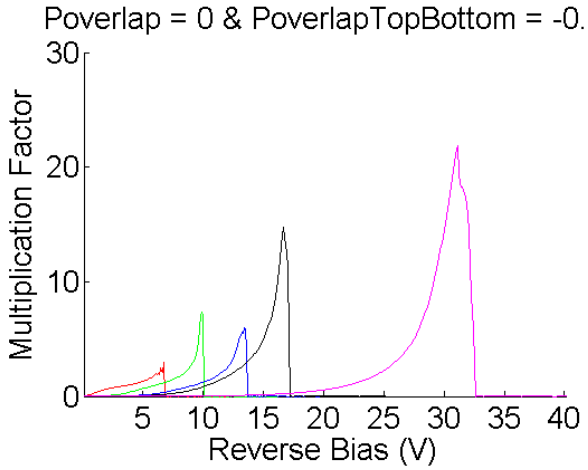
Multiplication L = 16

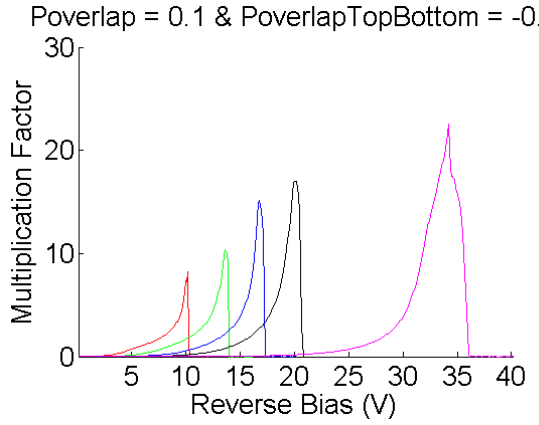




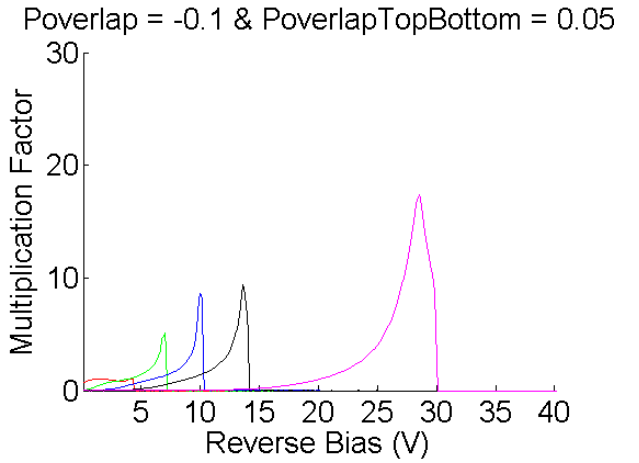


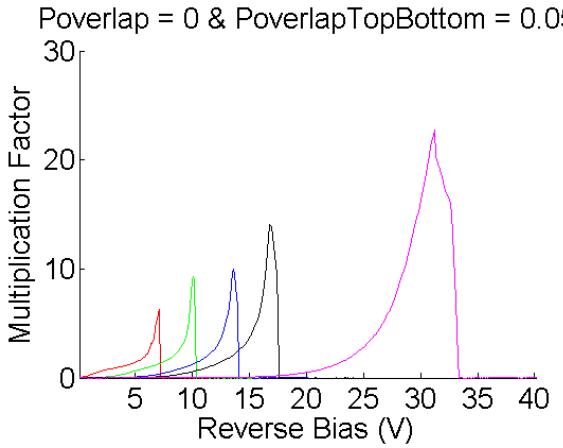


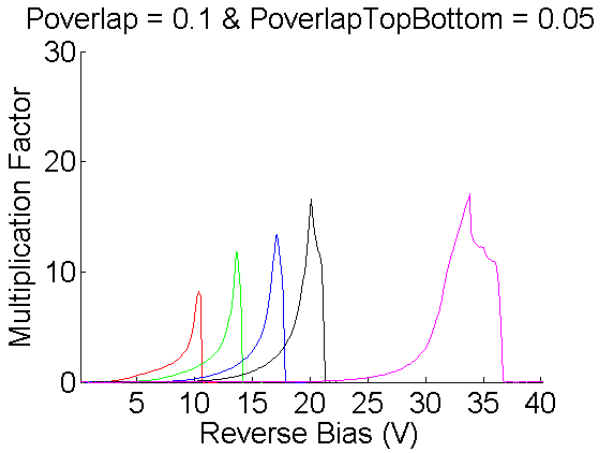


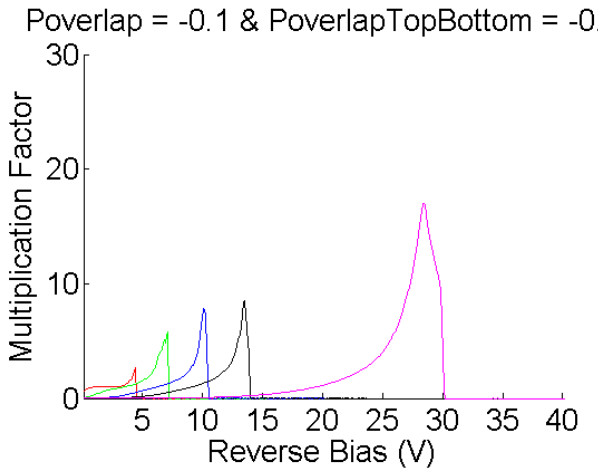


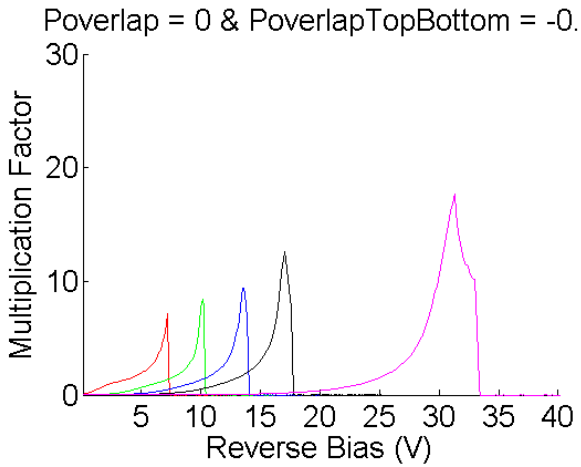
Multiplication L = 8

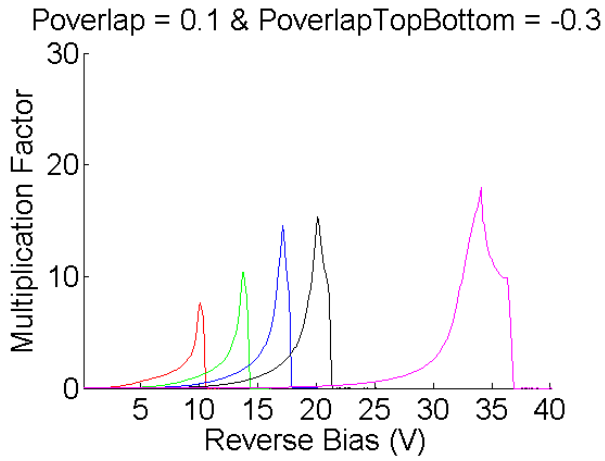










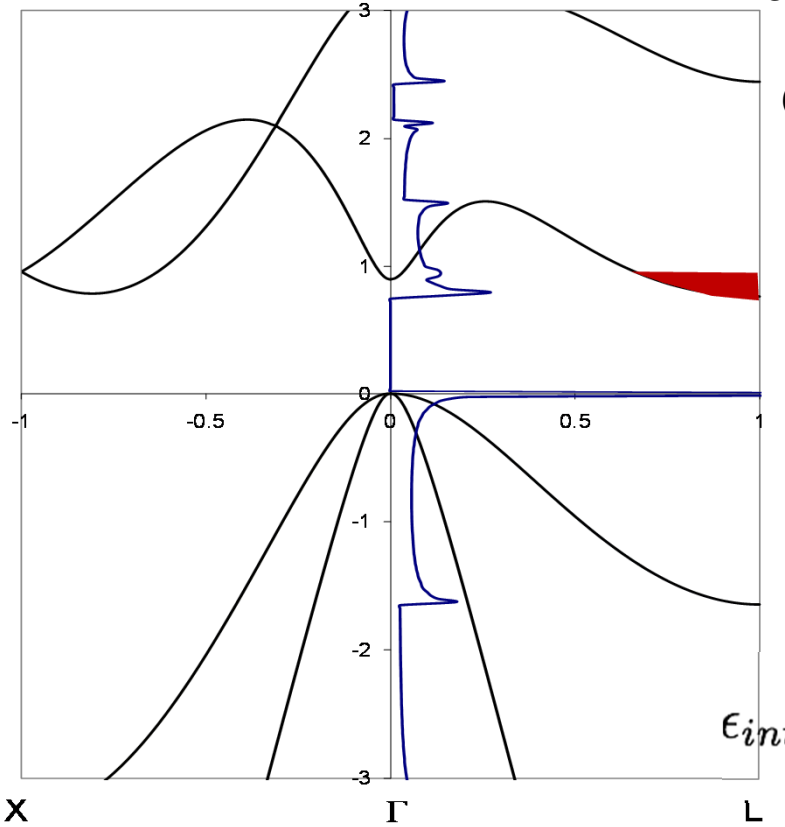


Initial Passive Quenched GM

Optical Properties of Doped Ge

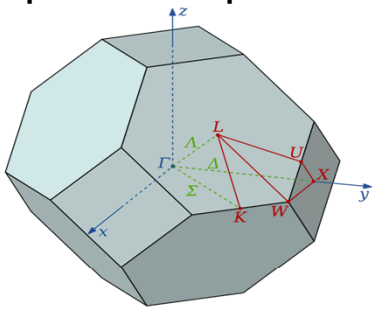
Sandia National Laboratories

Tight binding band-structure



Can we determine validity of band-filling and strain models for PL & EL signatures?

Optical Properties of Heavily Doped Semiconduc



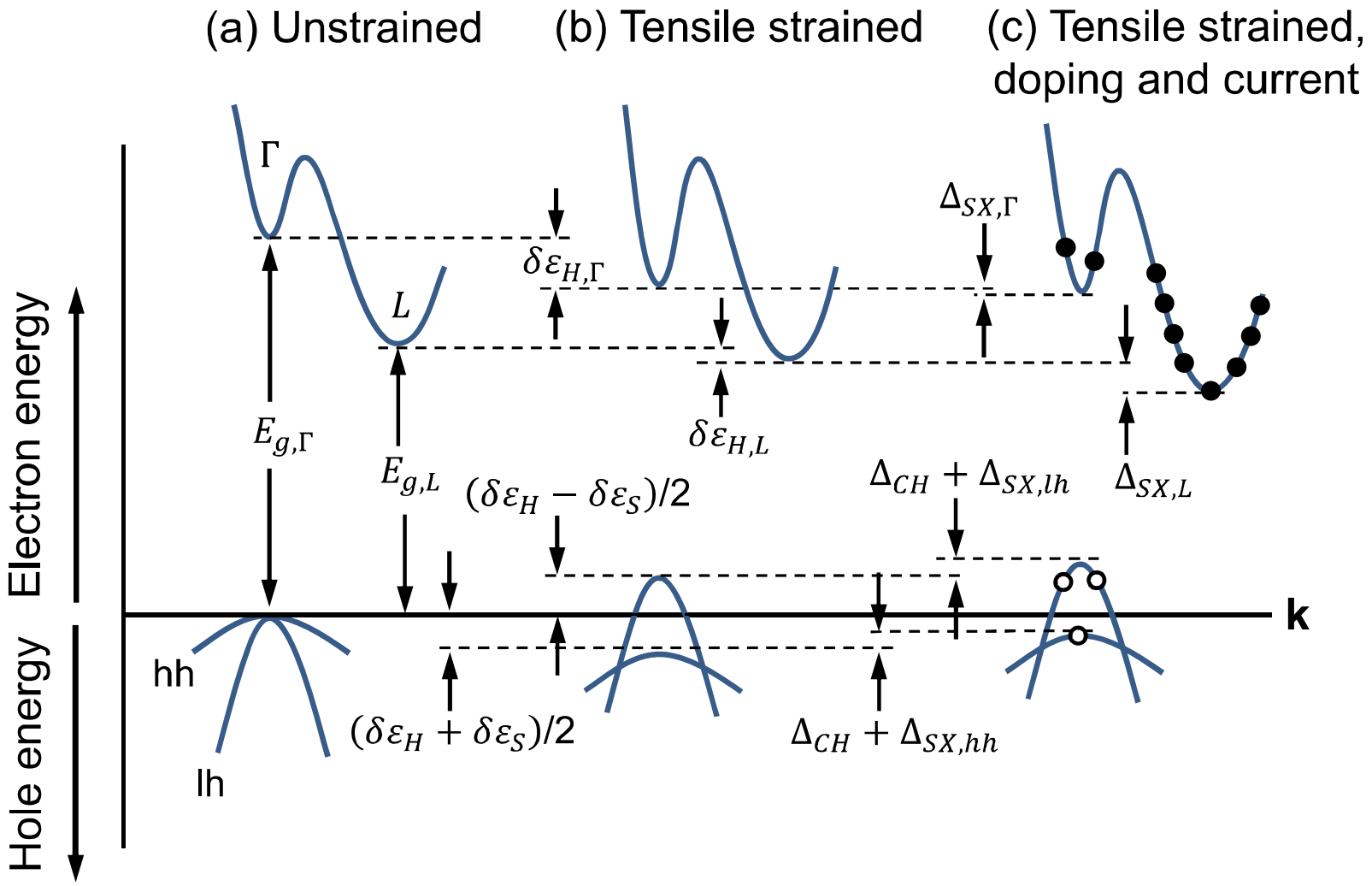
J. Jung, T. G . Pederson, JAP,113,114904,(2013)

$$\epsilon(\omega) = \epsilon_{inter}(\omega) + \epsilon_{intra}(\omega)$$

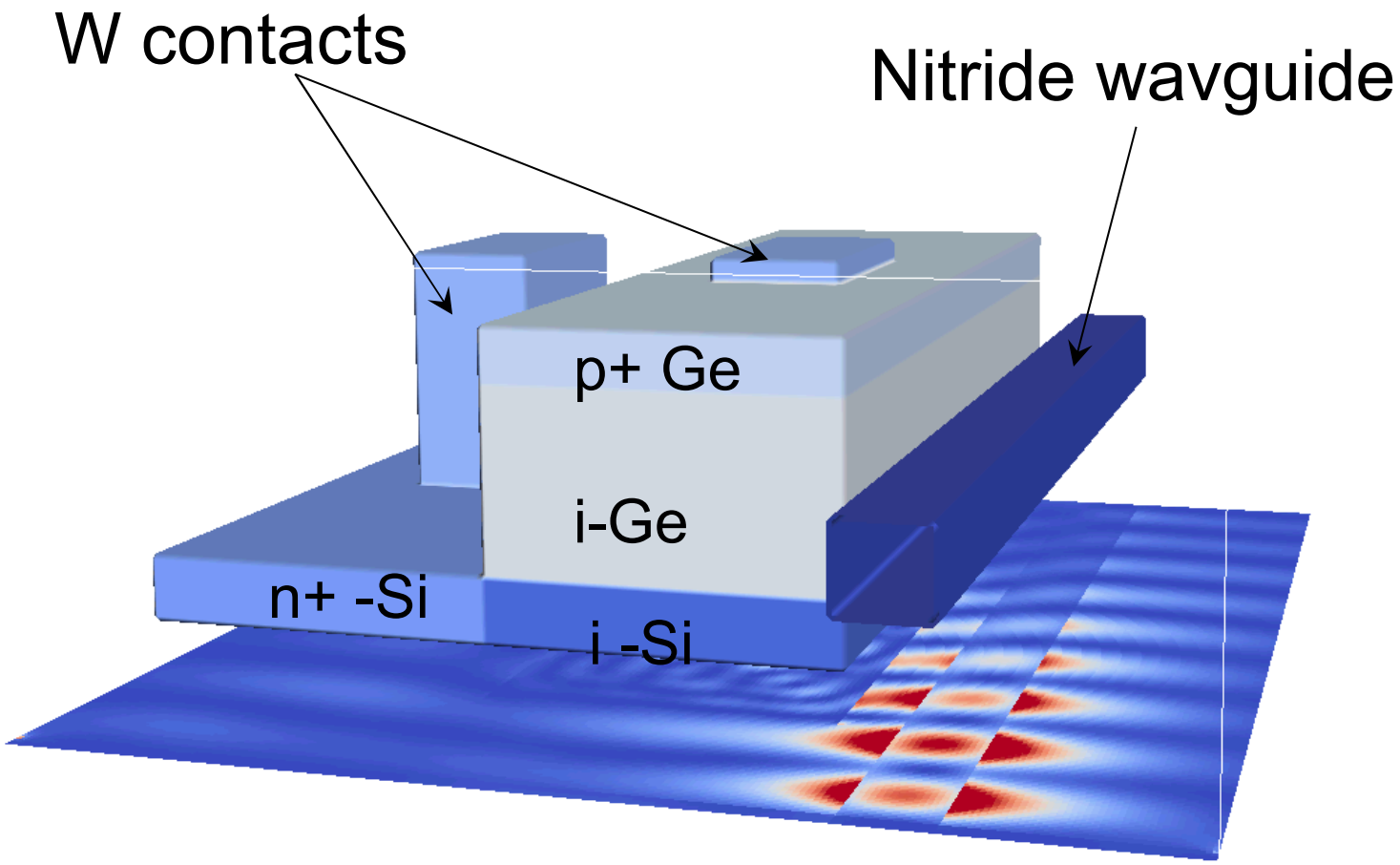
$$\epsilon_{intra}(\omega) = \frac{e^2}{8\pi^3\epsilon_0\hbar^2\omega^2}\sum_n \int \frac{\partial E_{n\mathbf{k}}}{\partial \mathbf{k}} f'(E_{n\mathbf{k}})d\mathbf{k}$$

$$\epsilon_{inter}(\omega) = 1 + \frac{e^2\hbar^2}{8\pi^3\epsilon_0 m^2}\sum_{n\neq m} \int \frac{f(E_{n\mathbf{k}}) - f(E_{m\mathbf{k}})}{E_{m\mathbf{k},n\mathbf{k}}[E^2_{m\mathbf{k},n\mathbf{k}} - (\hbar\omega)^2]} M_{m,n}(\mathbf{k})d\mathbf{k}$$

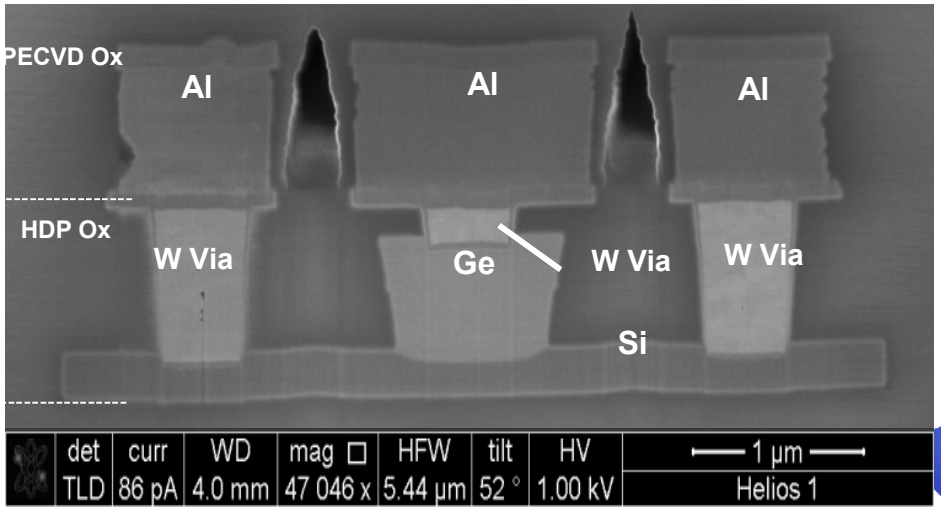
Indirect Bandgap in Strained Ge



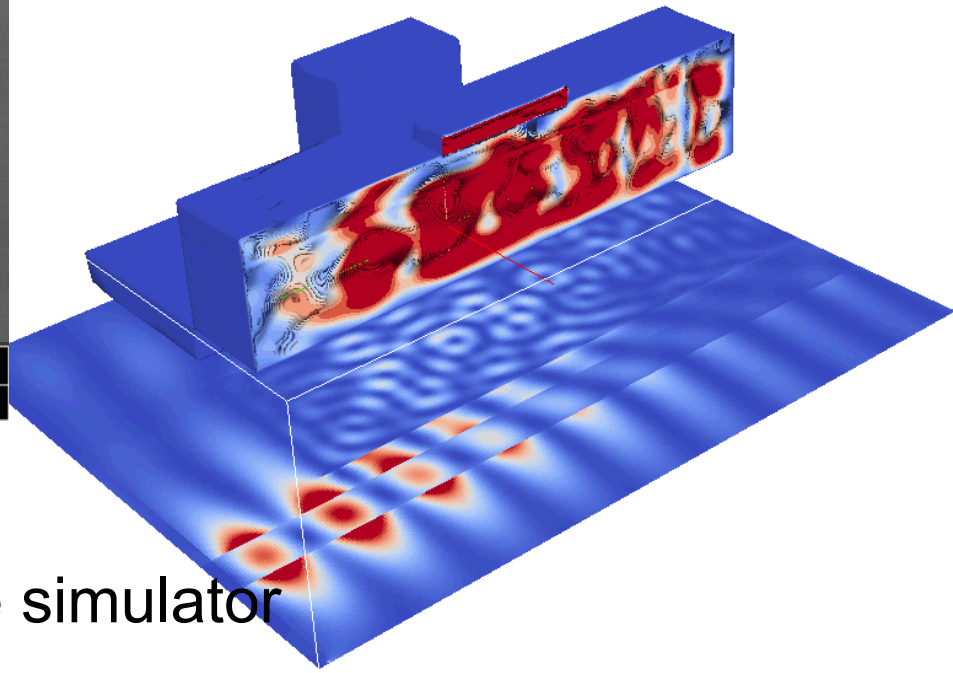
Waveguide Coupled SPAD



Ge Photodetector Development

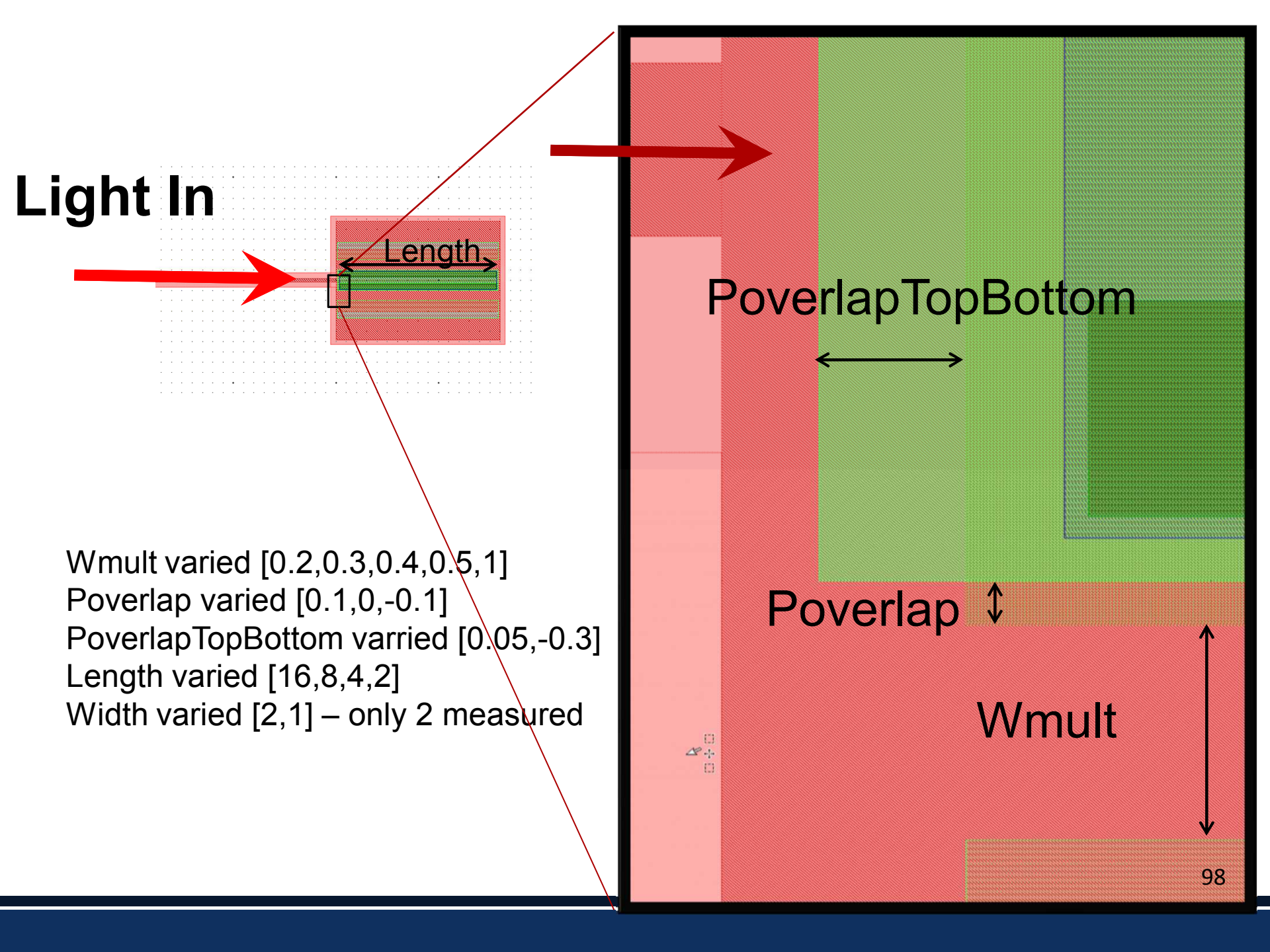


Generation rate

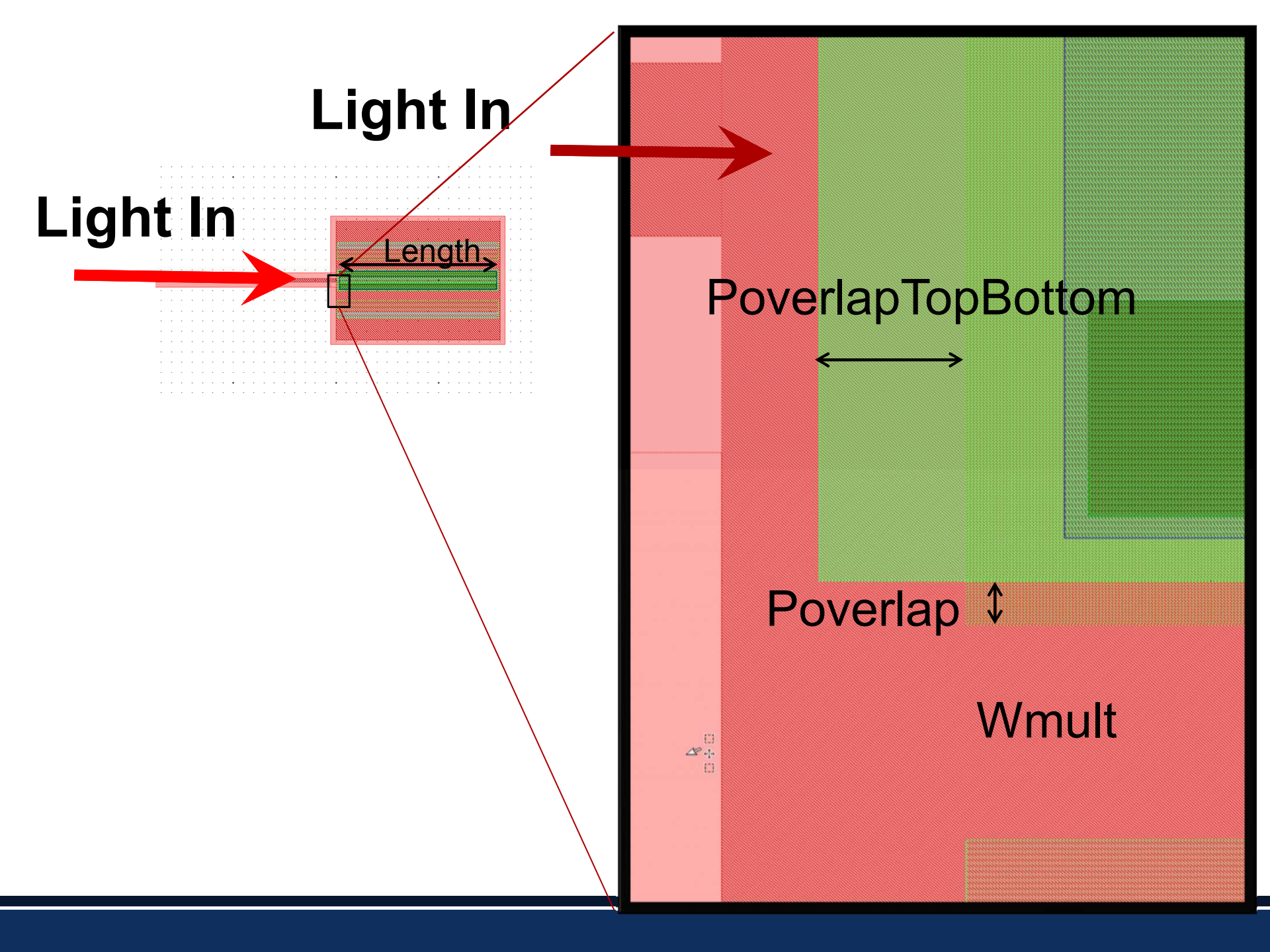


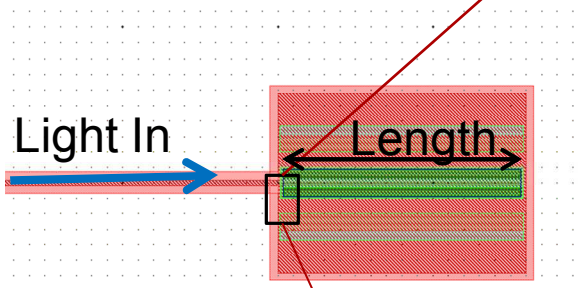
Input Generation rate into Device simulator
Synopsis drift-diffusion.
APD simulations currently underway.

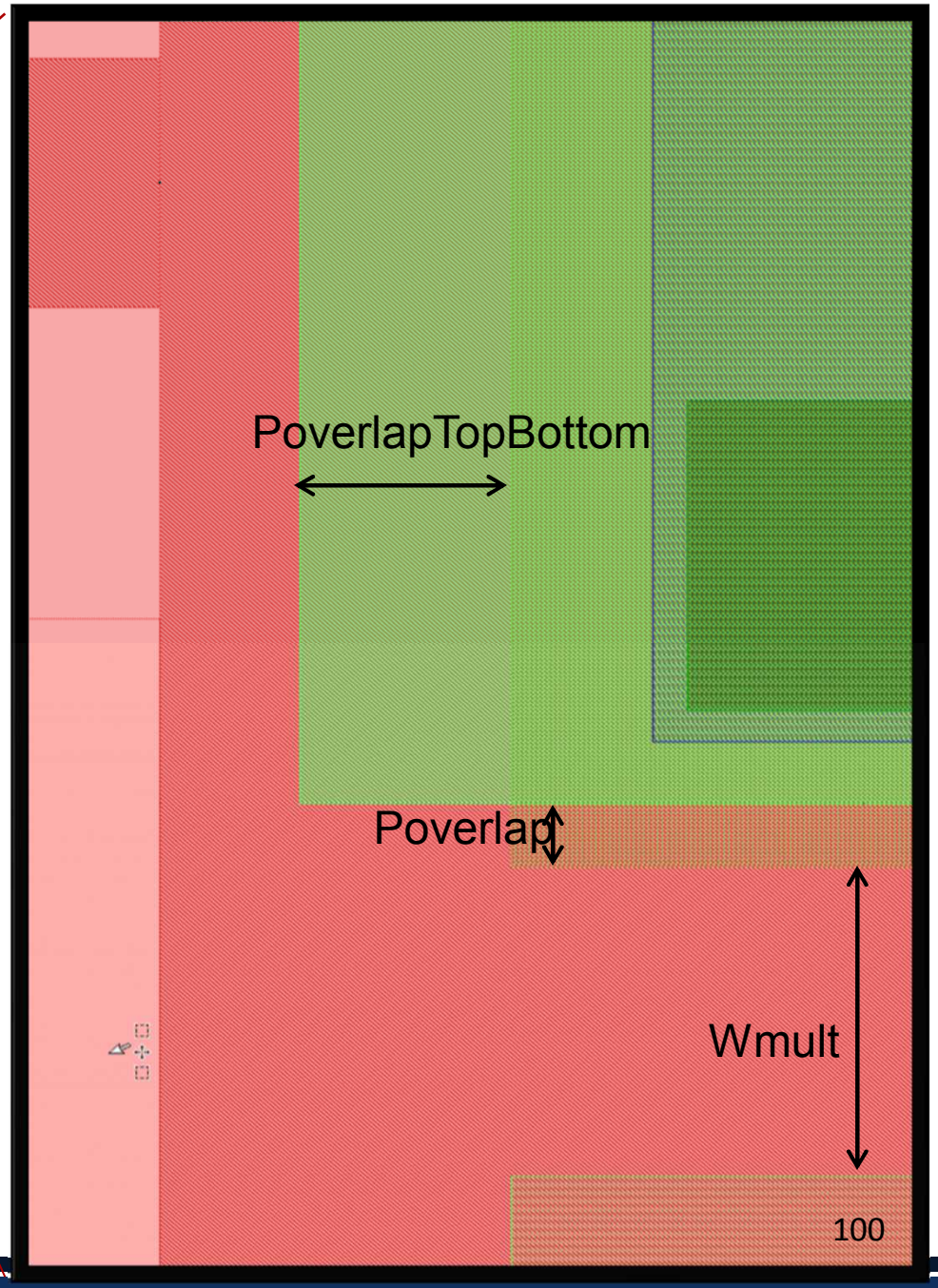
C. T. DeRose, D. C. Trotter, W. A. Zortman, A. Starbuck, M. Fisher, M. R. Watts, and P. S. Davids, "Ultra compact 45GHz CMOS compatible Ge waveguide photodiode with low dark current," *Optics Express*, vol. 19, no. 25, p. 24897, 2011.



Wmult varied [0.2,0.3,0.4,0.5,1]
Poverlap varied [0.1,0,-0.1]
PoverlapTopBottom varried [0.05,-0.3]
Length varied [16,8,4,2]
Width varied [2,1] – only 2 measured


Light In
Light In
Length
PoverlapTopBottom
Poverlap
Wmult





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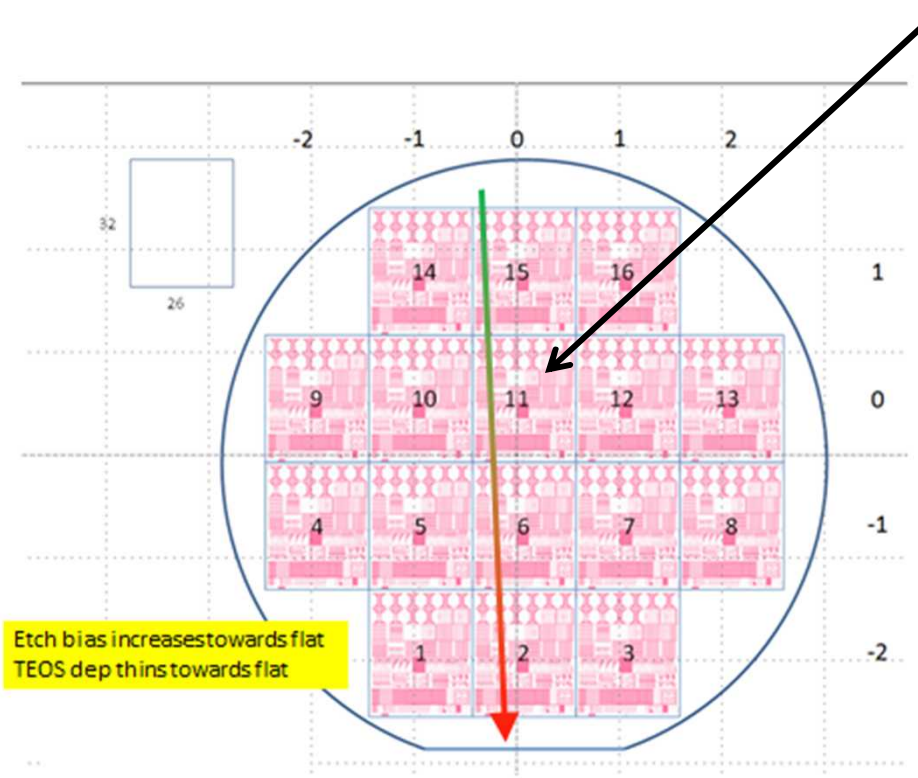
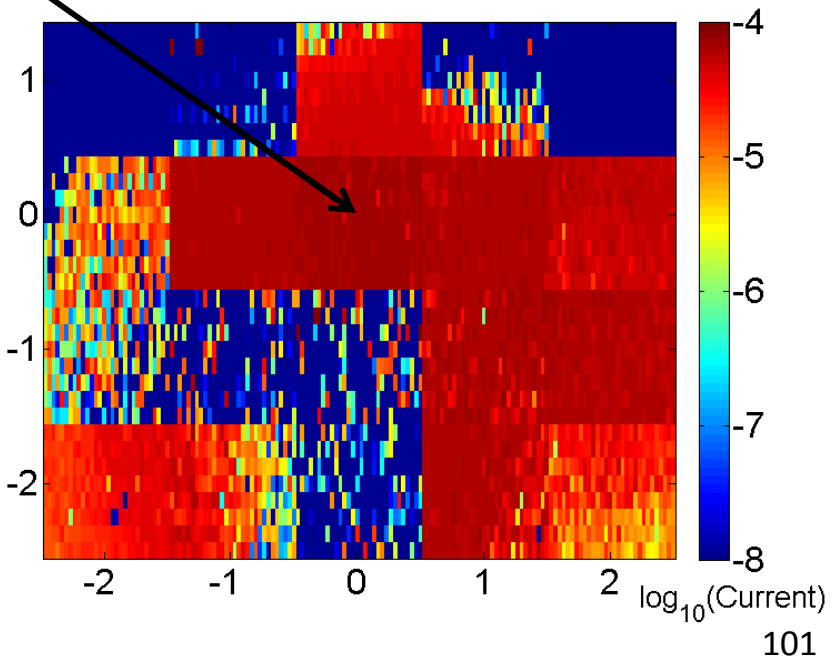
Length varied [16,8,4,2]
Width varied [2,1] – only 2 measured

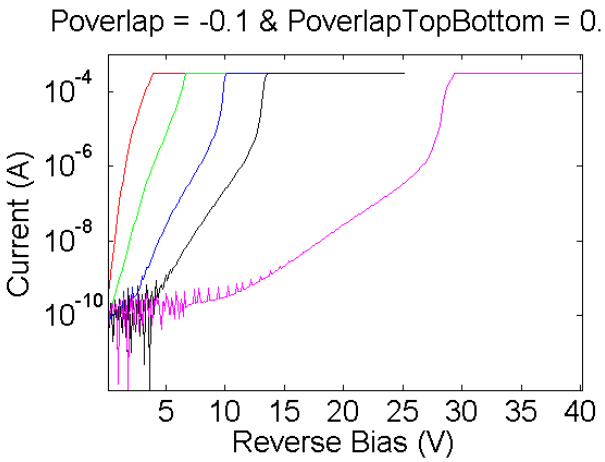
Die Map

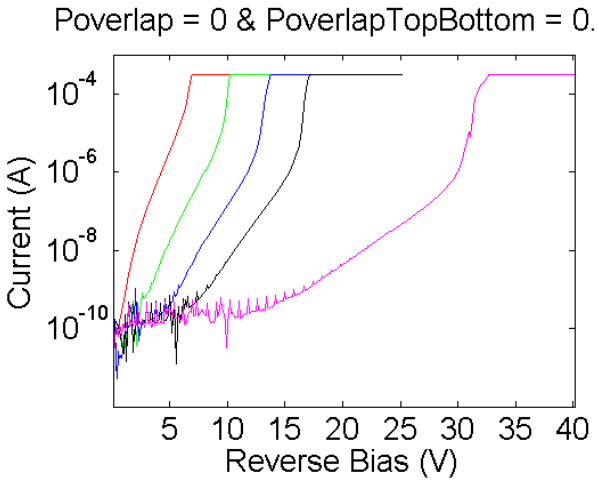
- All measurements presented here were on 1051A W2 Die (0,0)

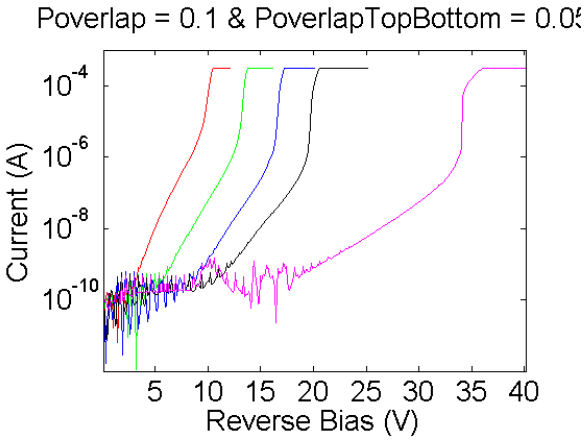


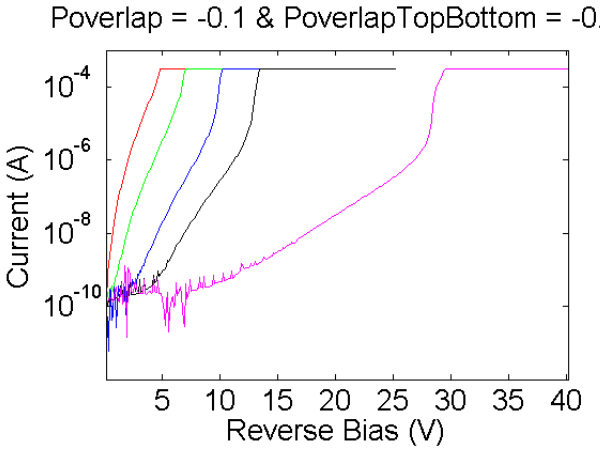


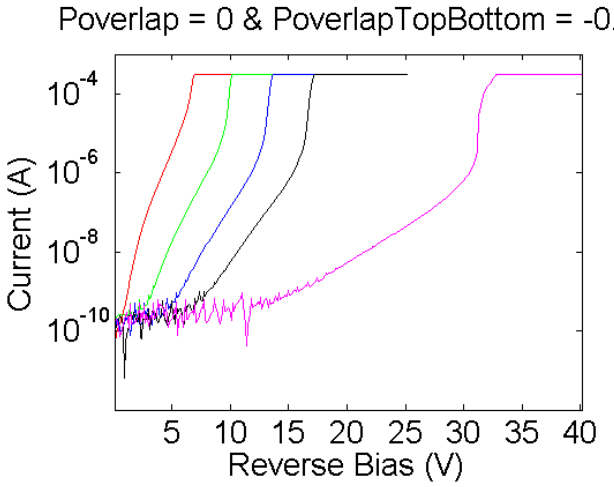
Dark Characteristics L = 16

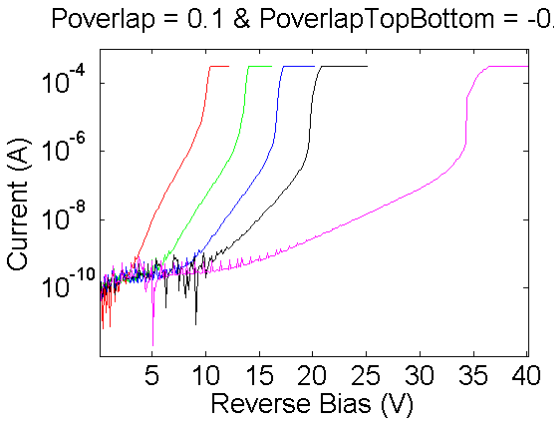




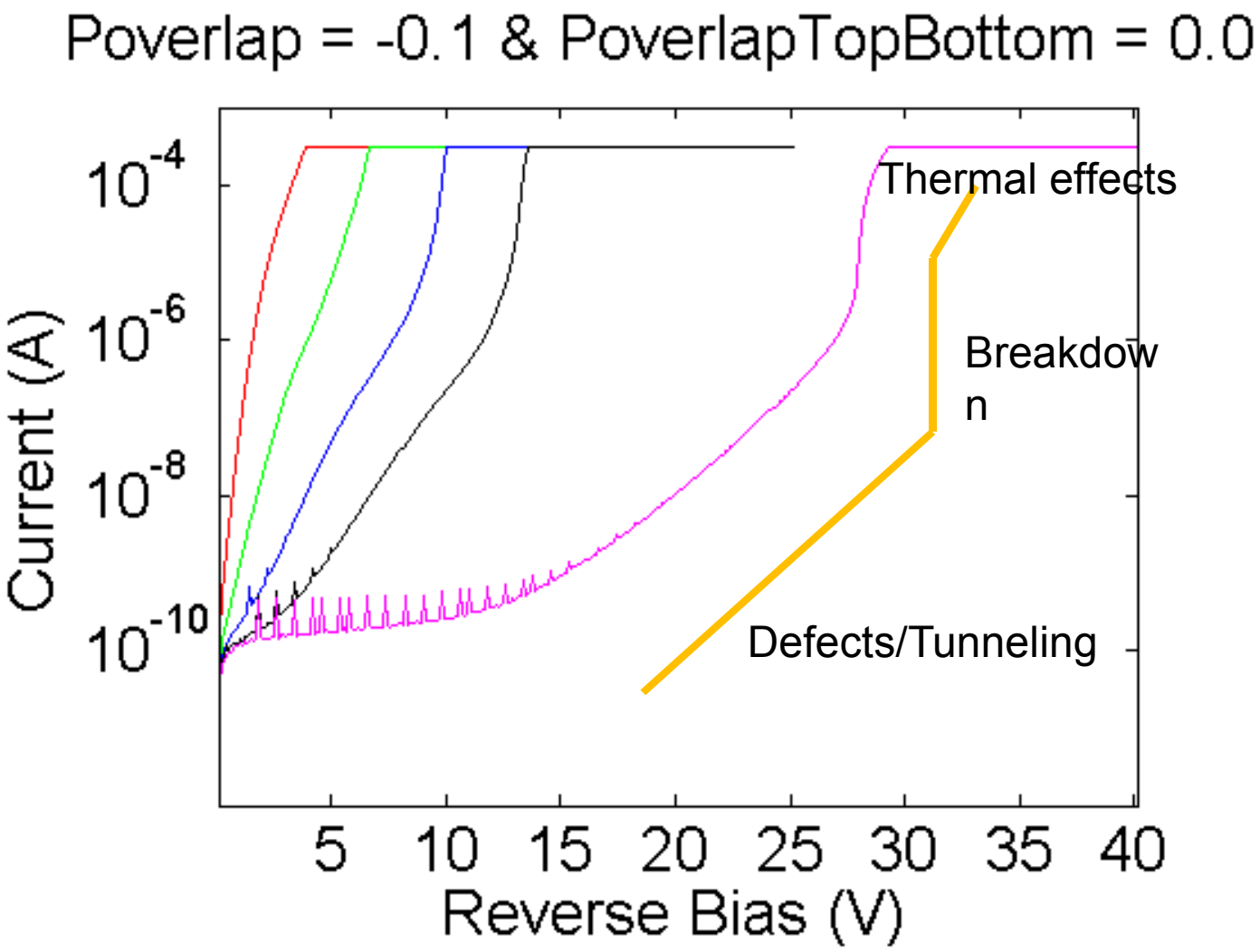




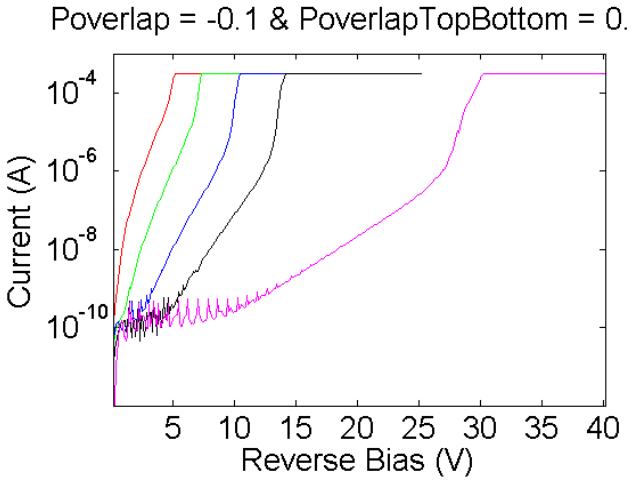


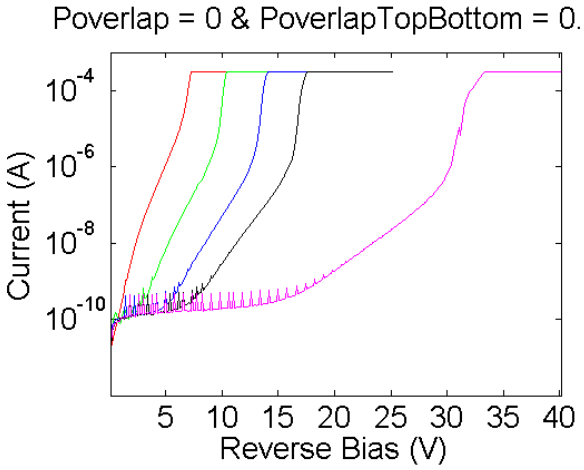


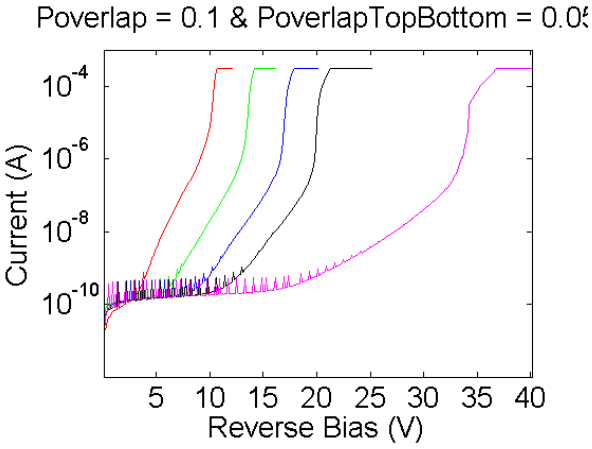
A closer look at the dark current

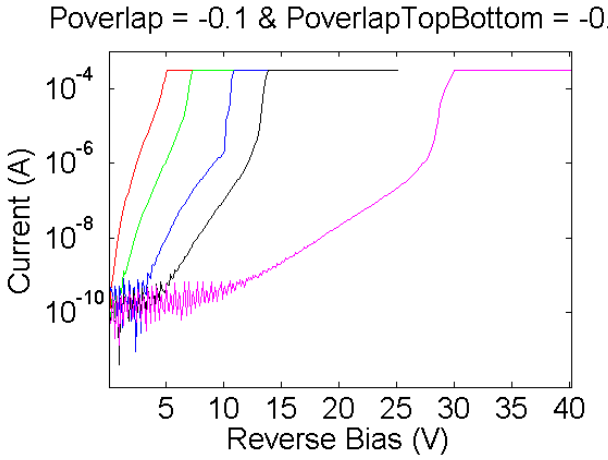


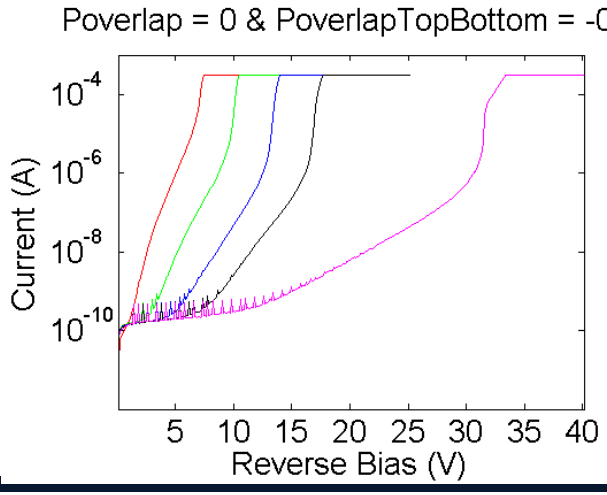
Dark Characteristics L = 8

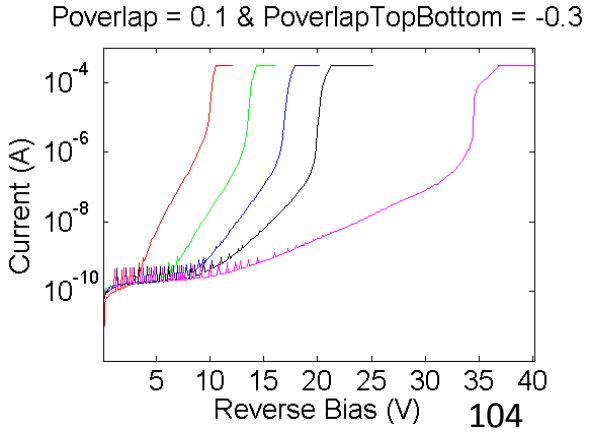




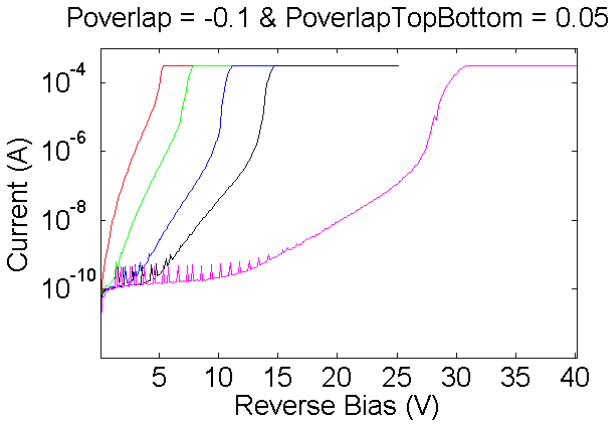


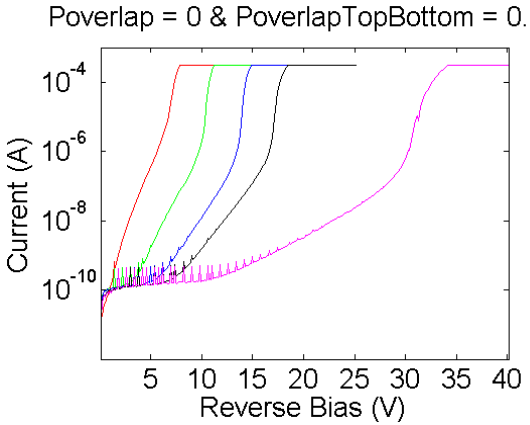


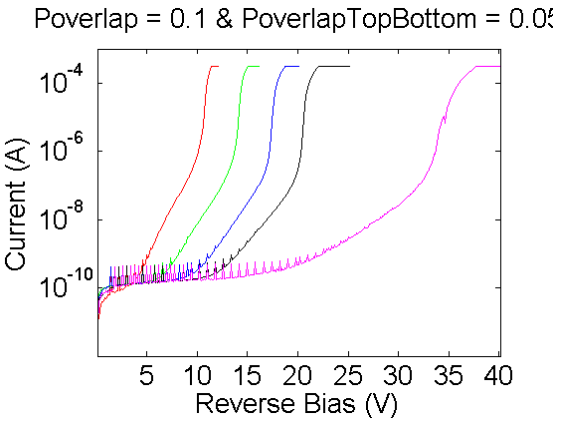


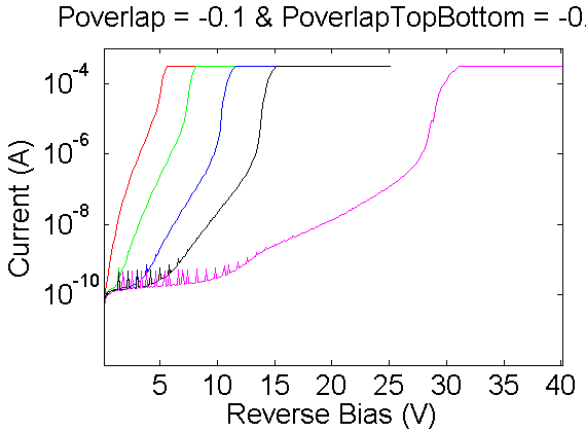


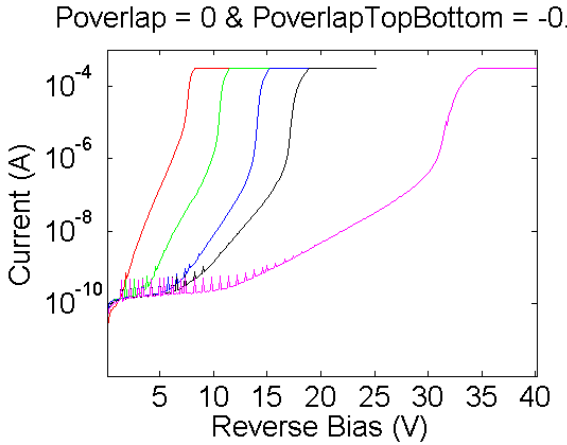
Dark Characteristics L = 4

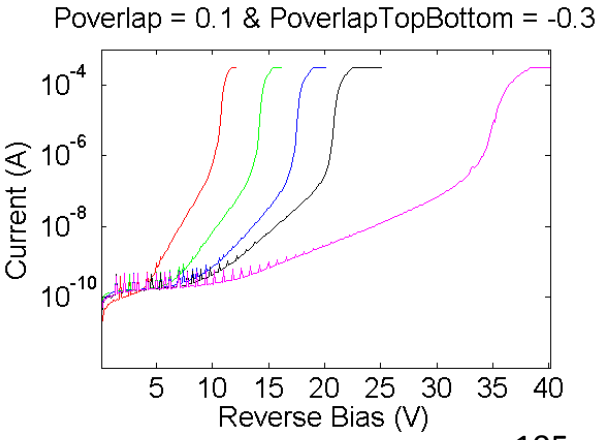




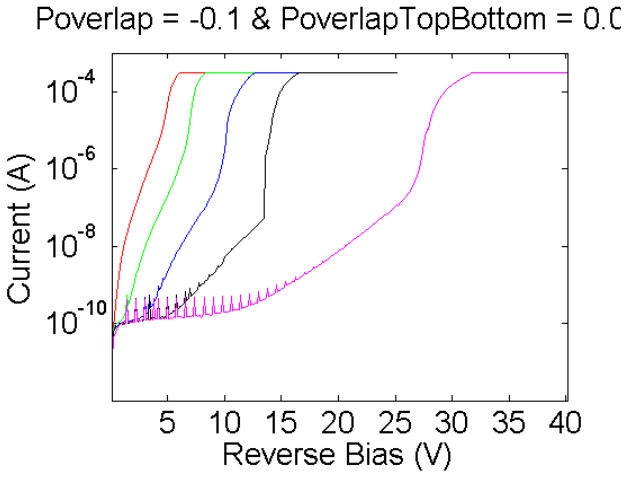


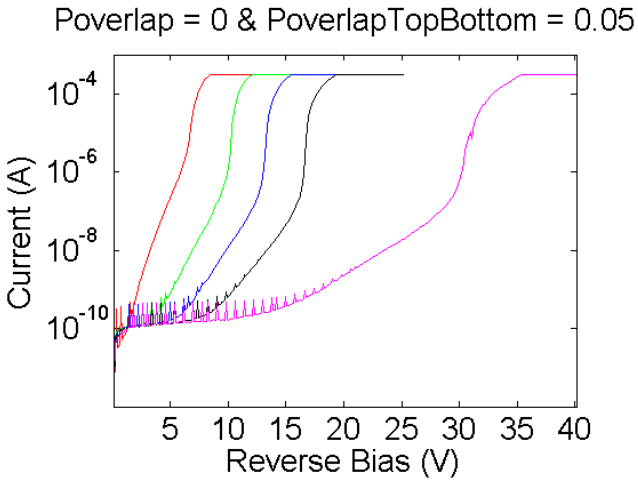


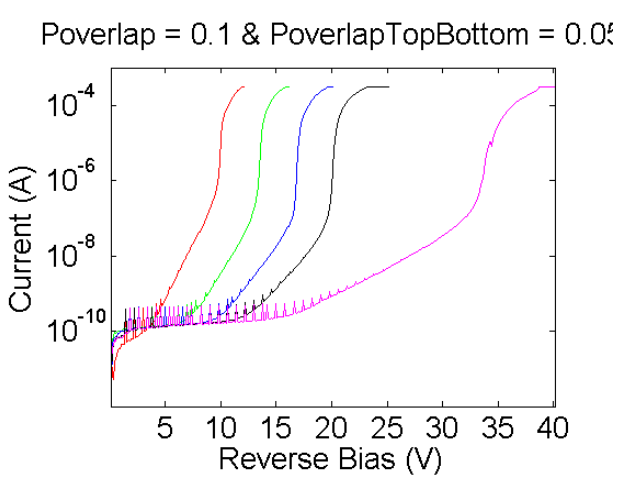


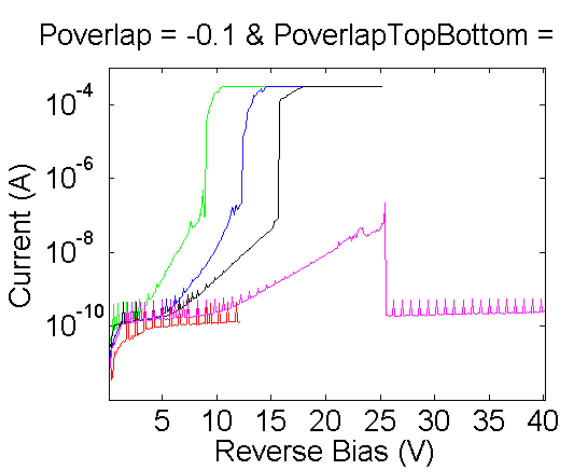


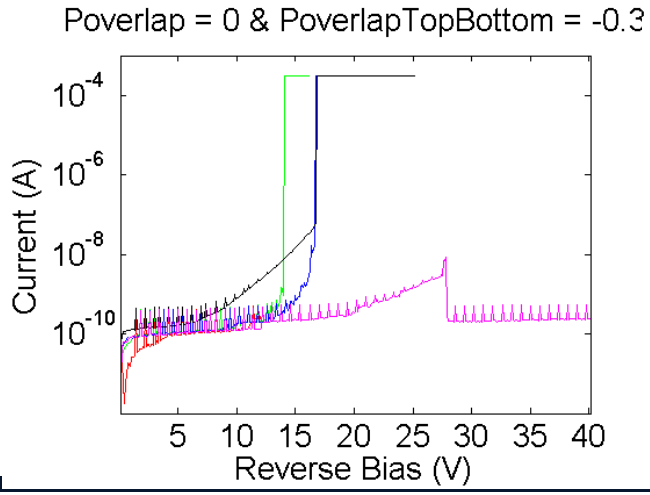
Dark Characteristics L = 2

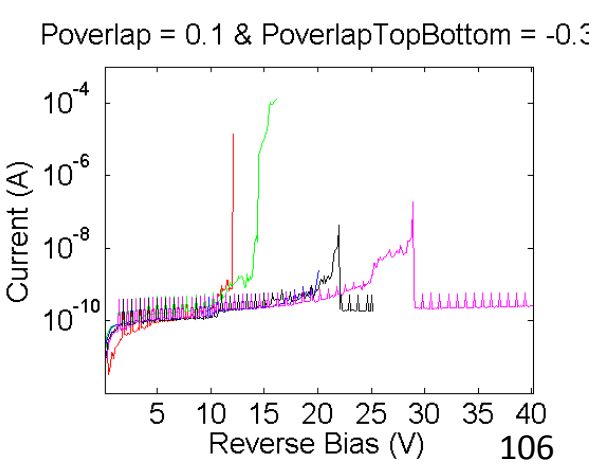






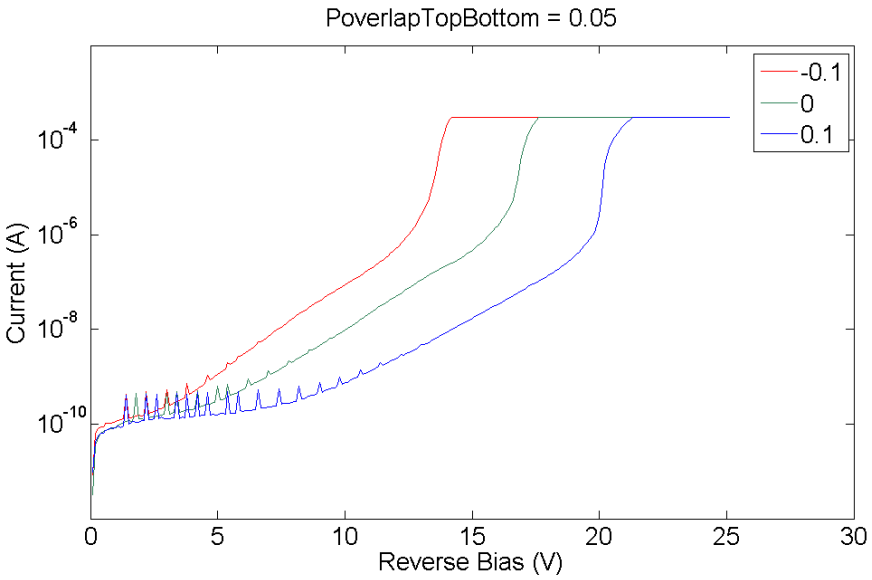


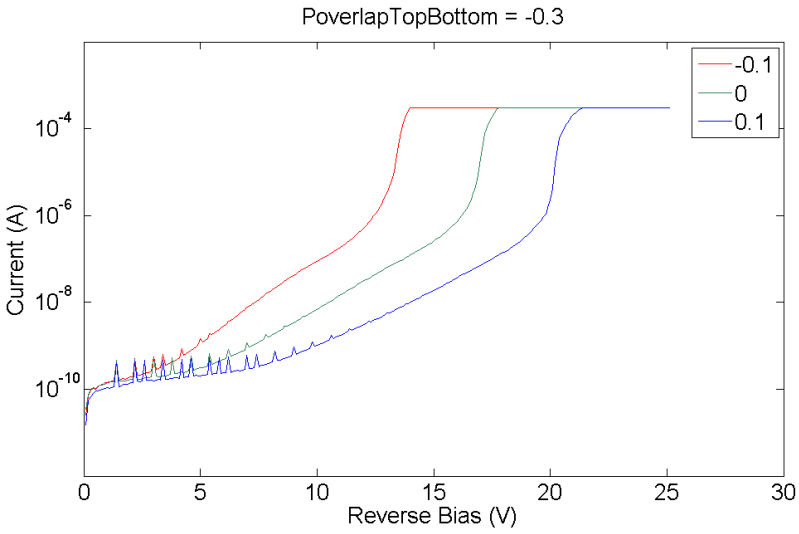




Effect of Poverlap

8um long 0.5 um Wmult

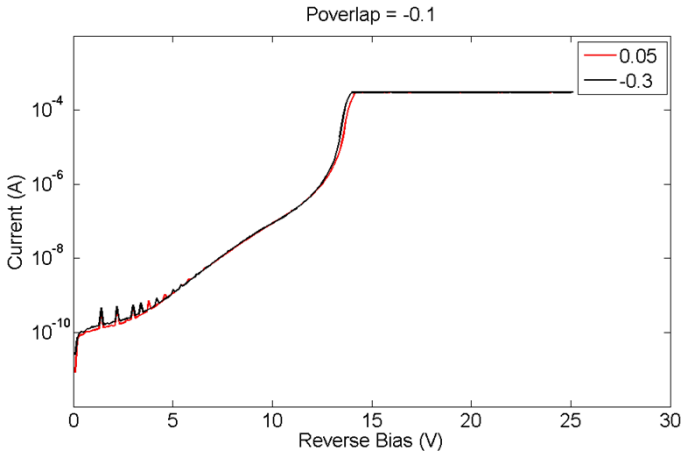


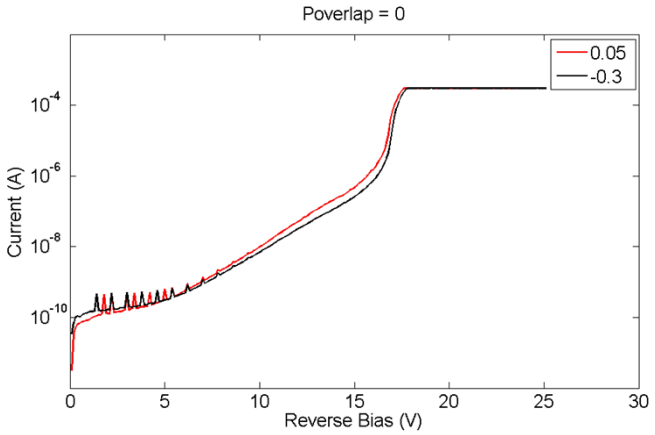


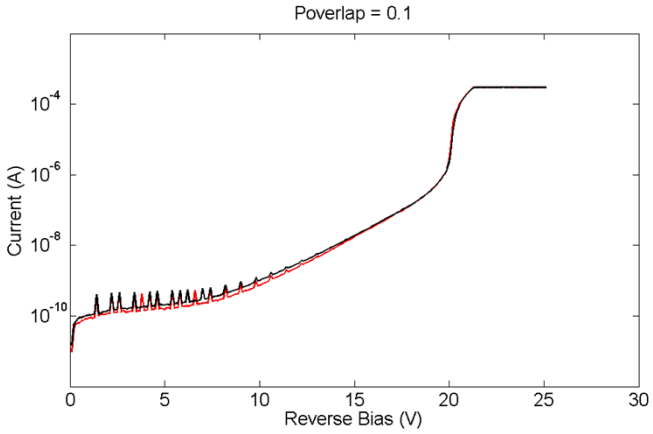
Increasing Poverlap pushes breakdown out due to widening depletion region

Effect of PoverlapTopBottom

8um long 0.5 um Wmult



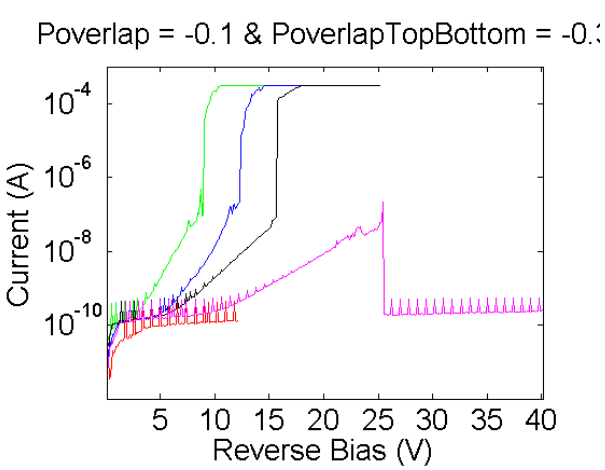


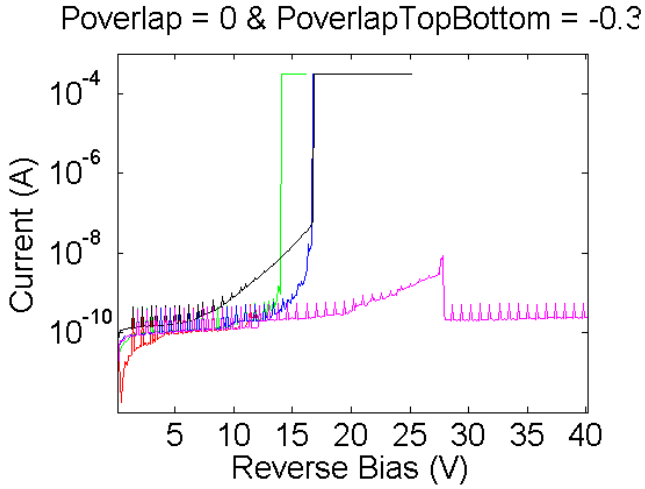


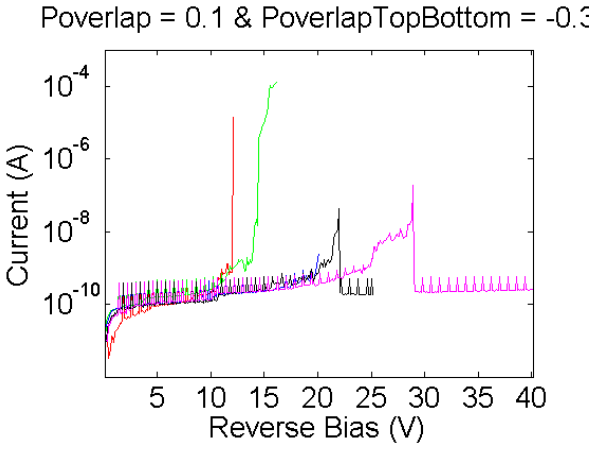
Little effect seen with PoverlapTopBottom in 8um device

Effect of PoverlapTopBottom

2 um long device





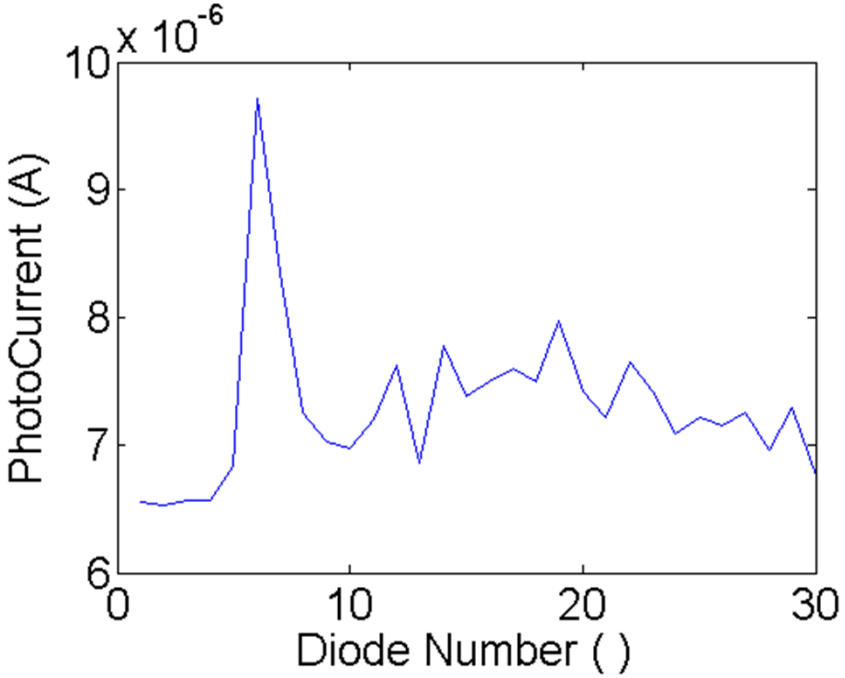


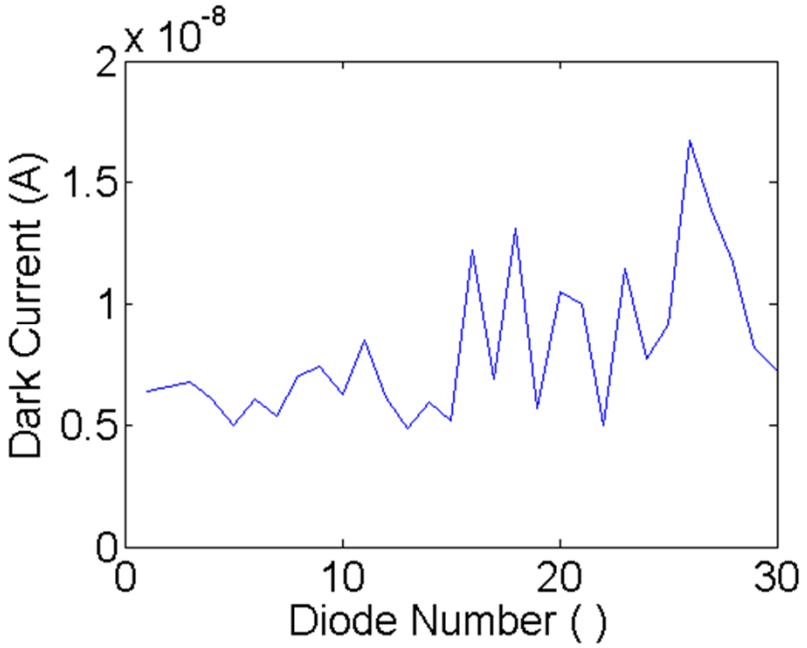
Reverse curves with reduced overlap are poor – now a significant portion of device le

Light On Measurements

- Done with 100 uW incident on grating coupler
- Wavelength set to 1540 nm.
- Estimate ~ 8 uA photocurrent in equivalent PIN structure.
- Fiber array position optimized for each measurement.

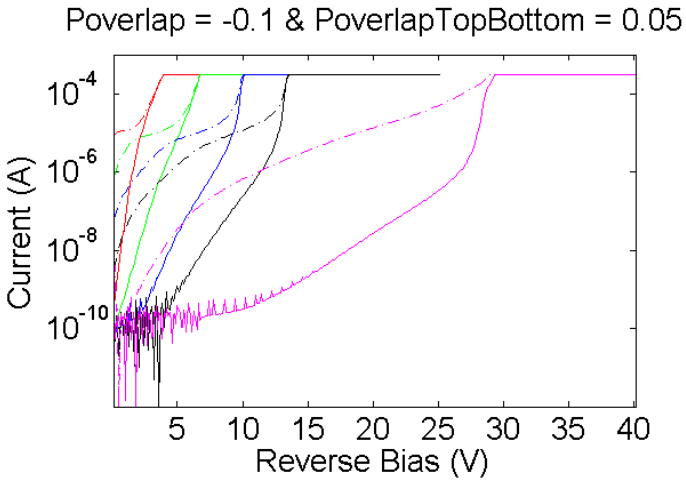
Photodiode Measurements

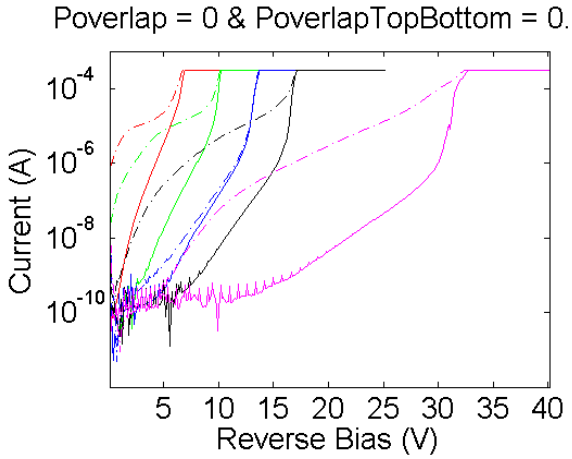


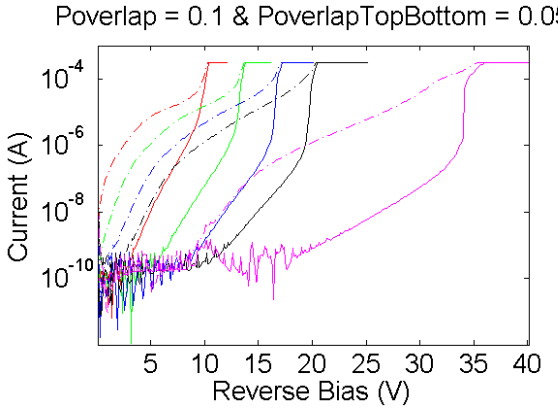


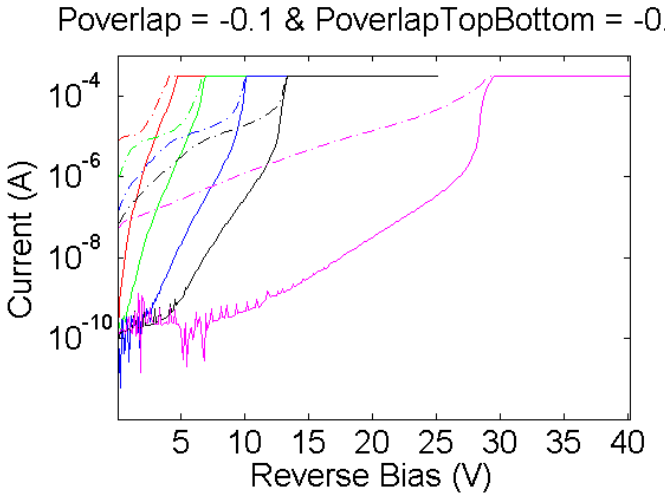
Measured photo and dark currents in 30 1.3x8 um photodiodes in the adjacent die the average photocurrent was 7.3uA and the average dark current was 8.1 nA. I used 8 uA as unit gain in the APD analysis.

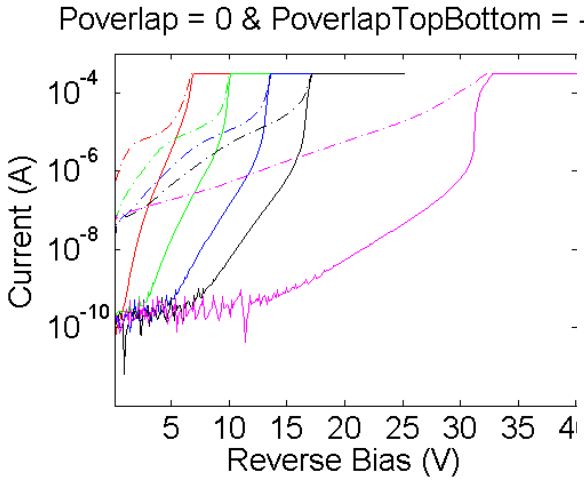
Light On (Dashed Curve) L = 16

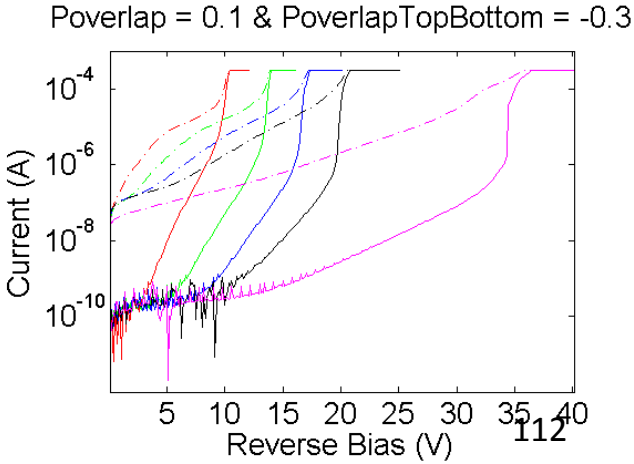




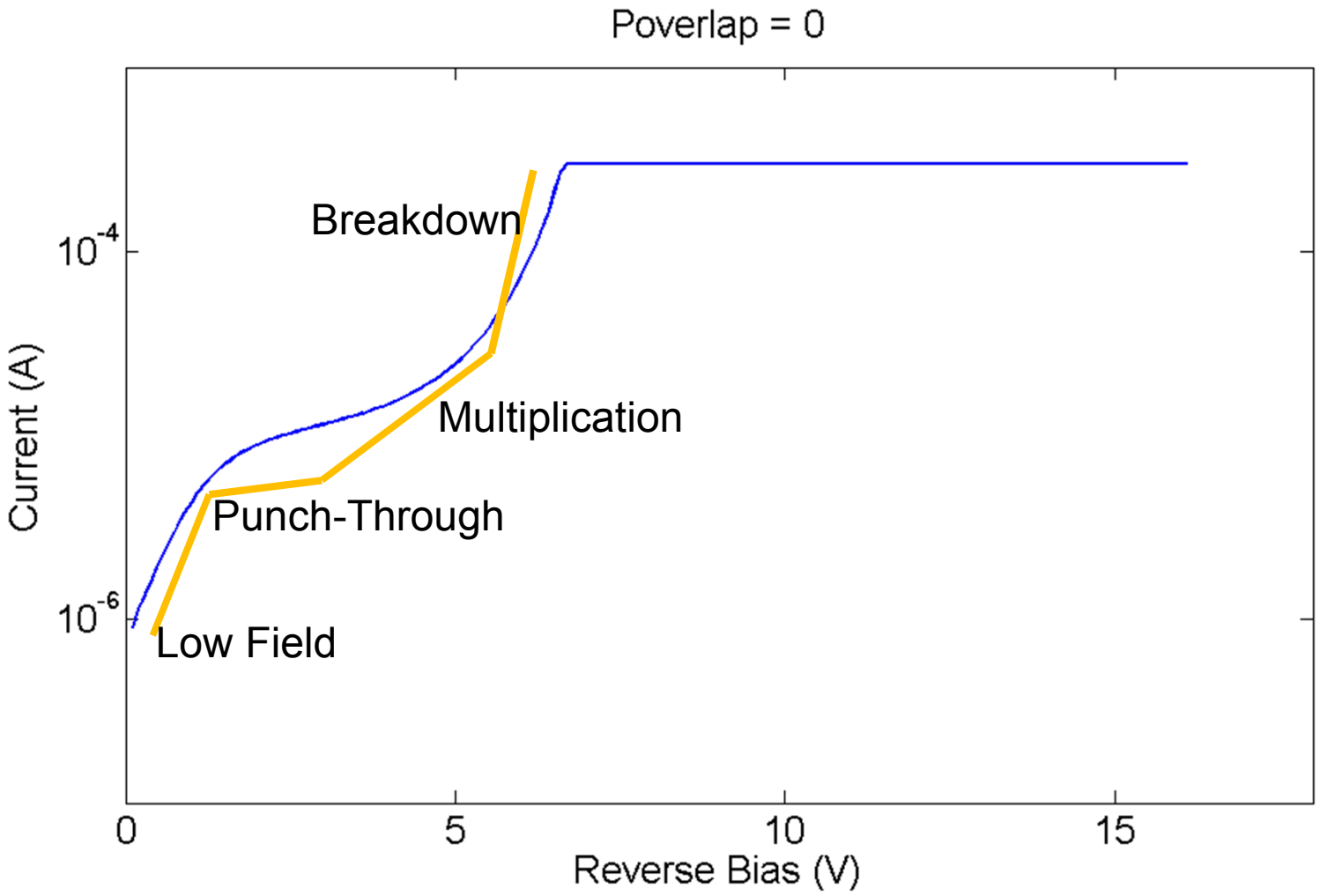




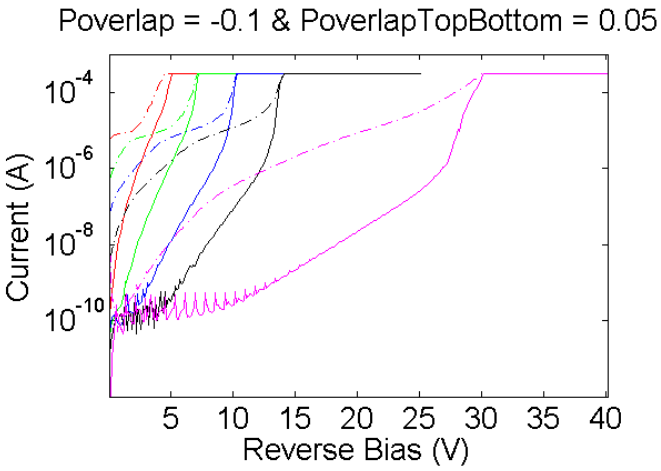


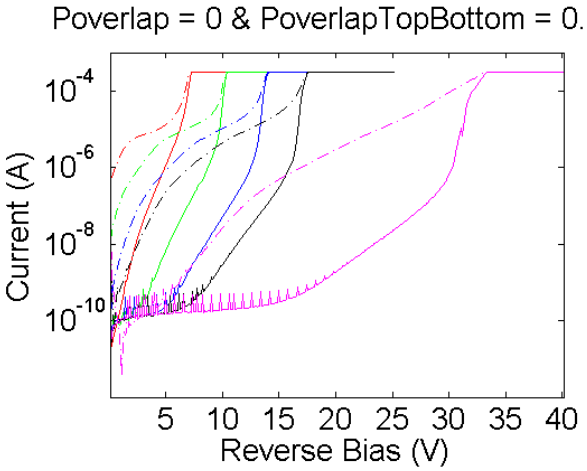


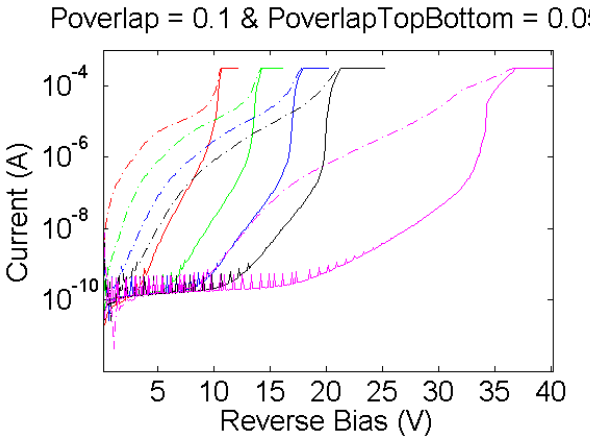
A closer look at photocurrent

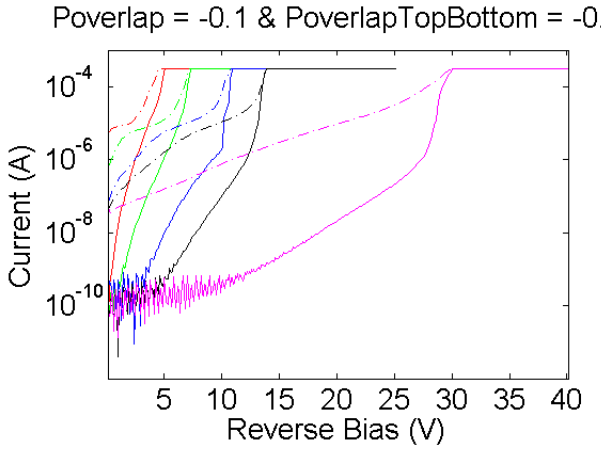


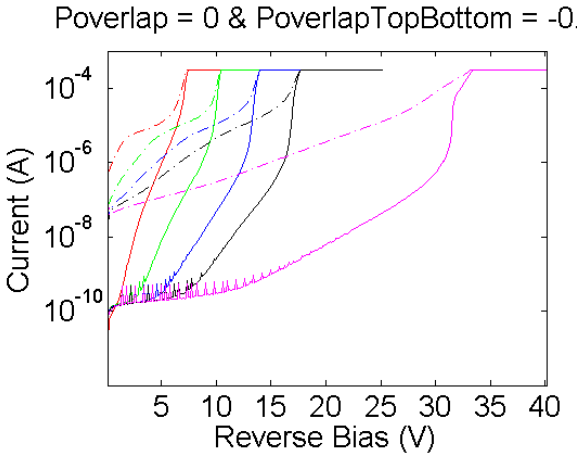
Light On (Dashed Curve) L = 8

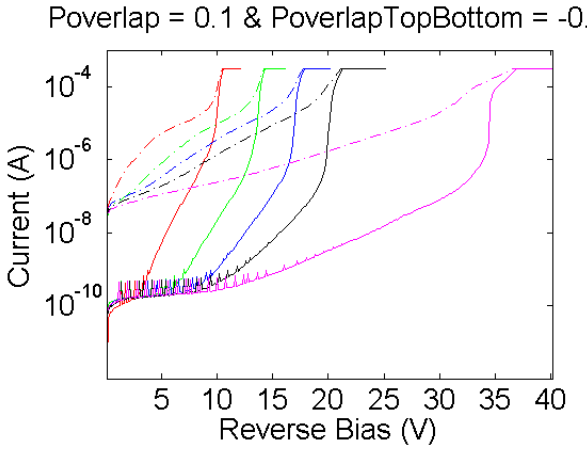












Light On (Dashed Curve) L = 4

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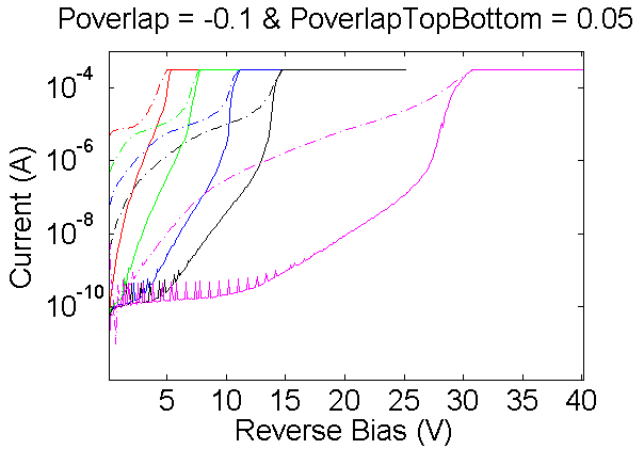
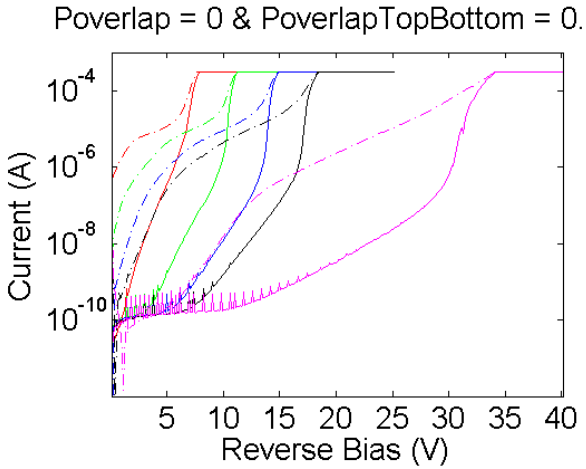
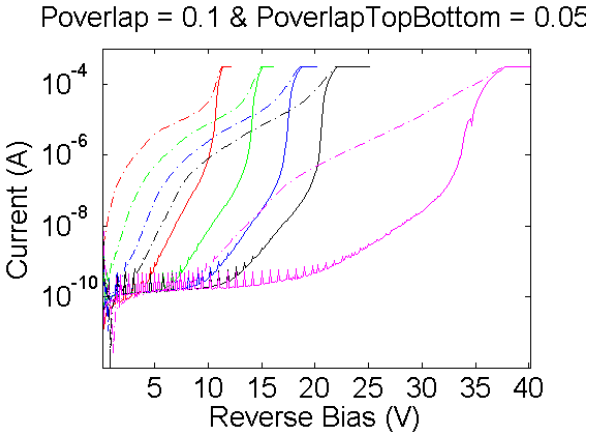
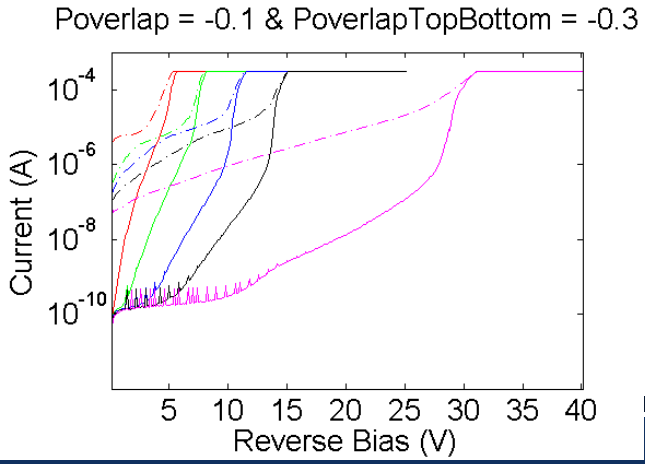
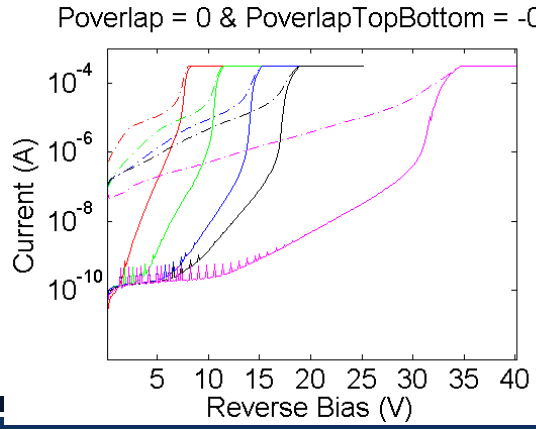
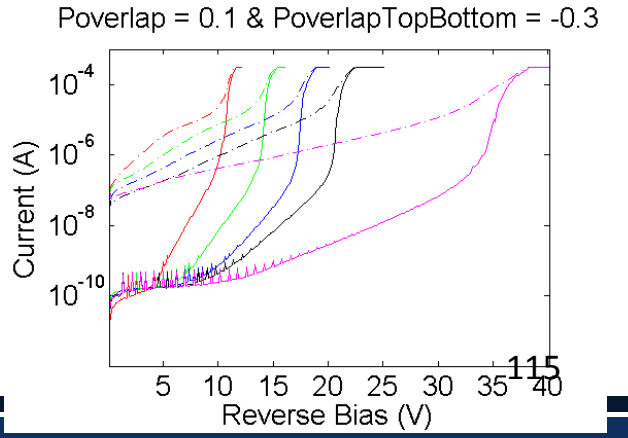




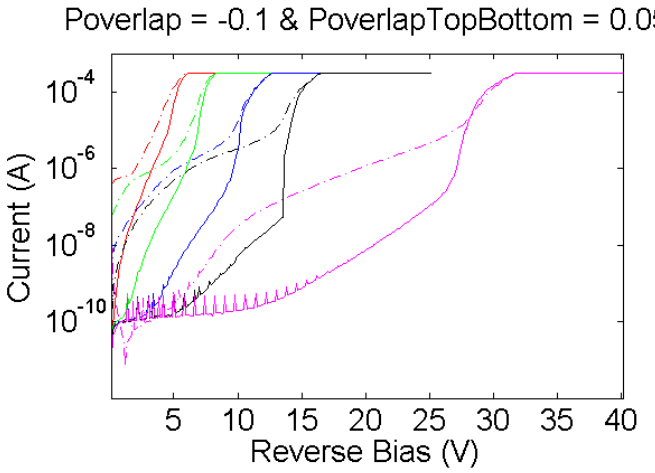


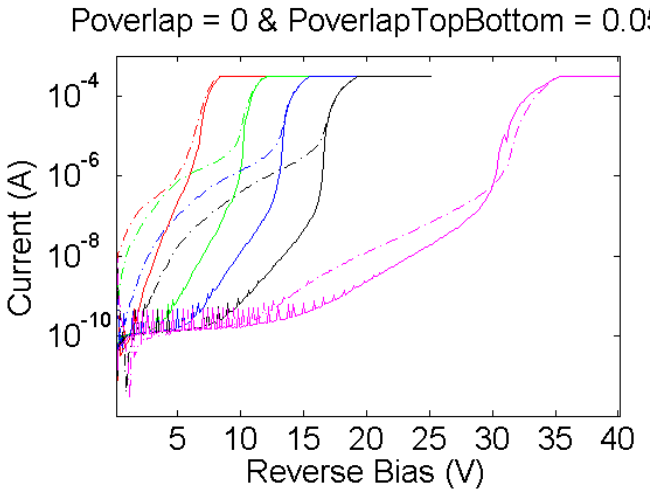


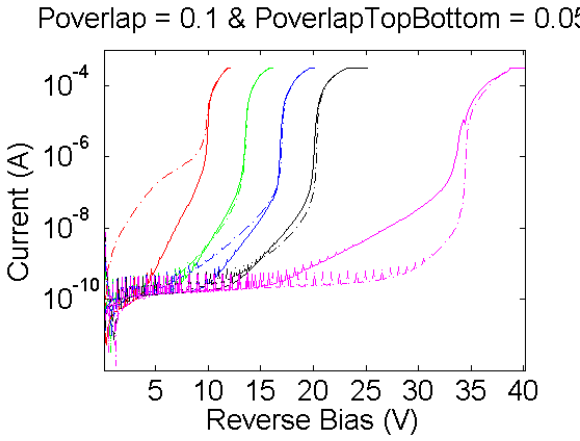


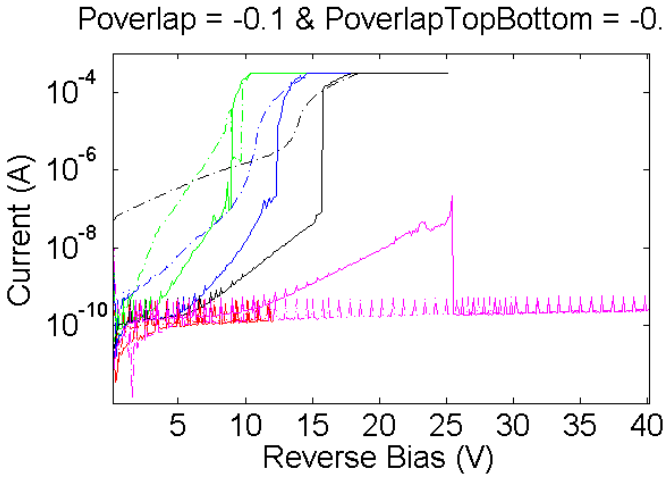


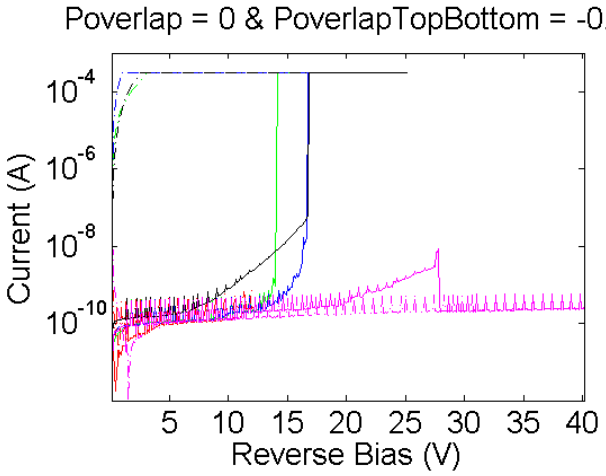
Light On (Dashed Curve) L = 2

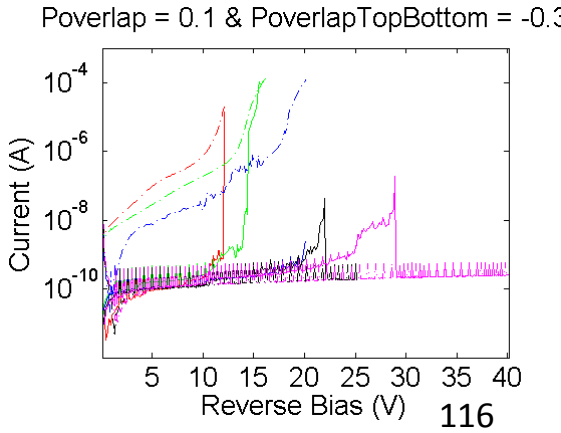




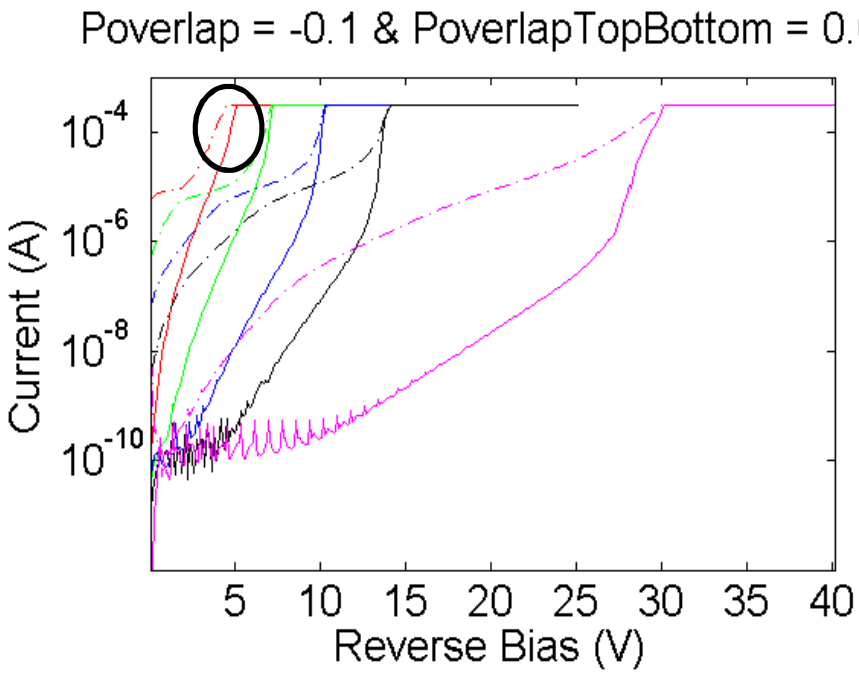


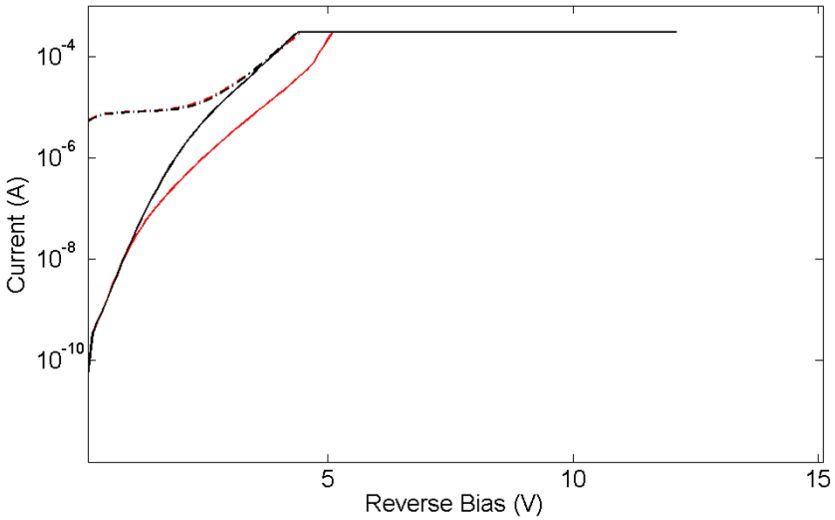






Permanent change in device?



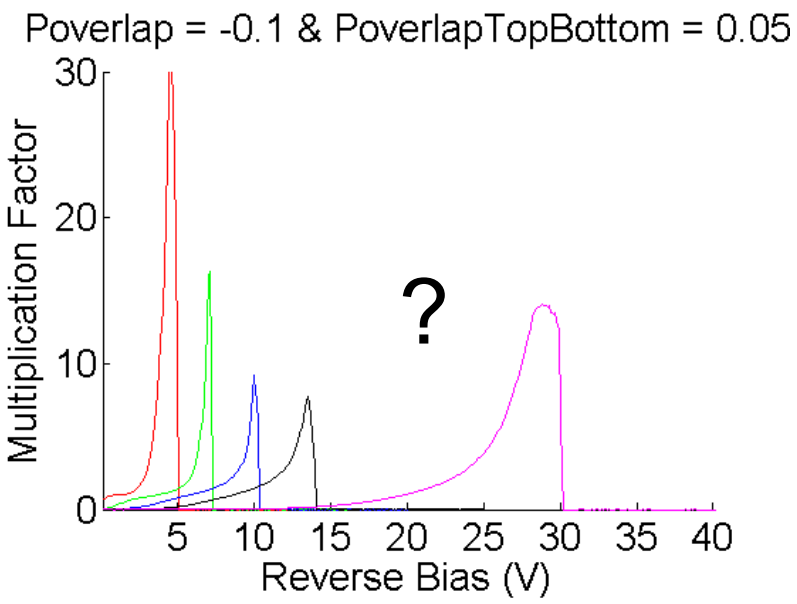


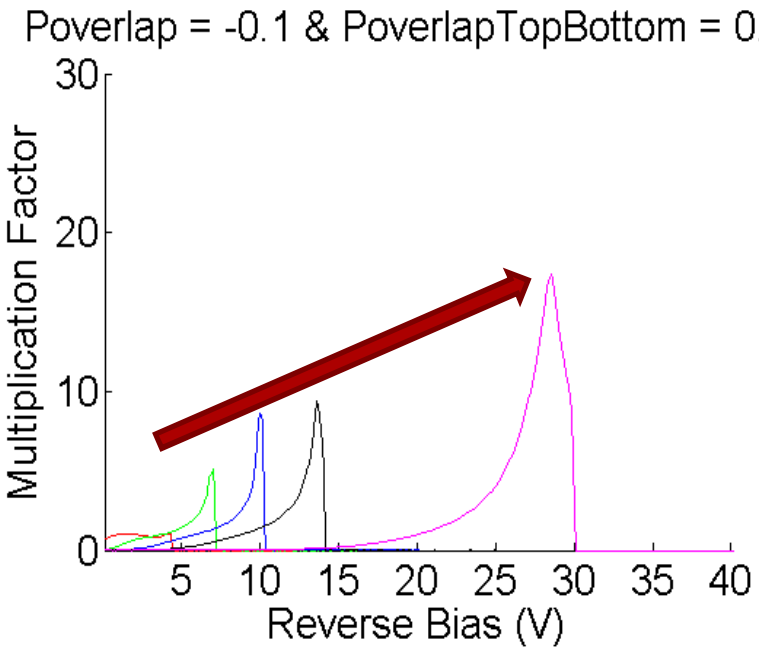
Some devices look particularly good. But…

…measuring the same device we see a hyster
effect on the dark current

A clear gain picture emerges

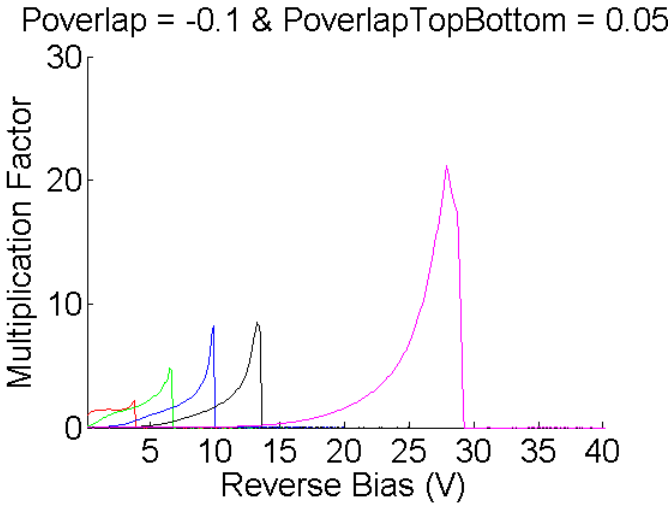
$M = (i_{light} - i_{dark})/8uA$

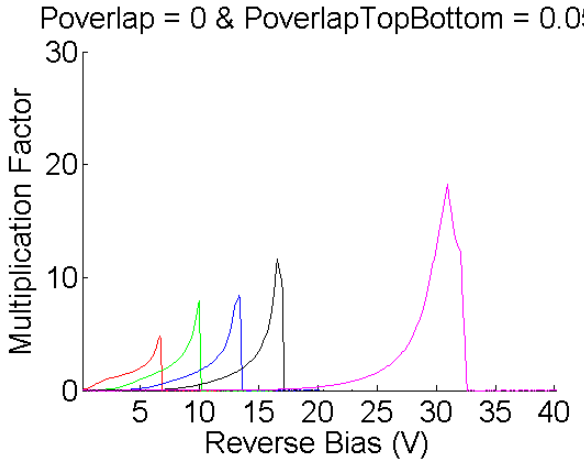


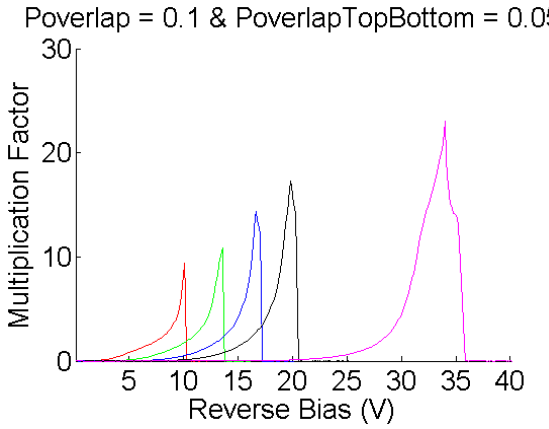


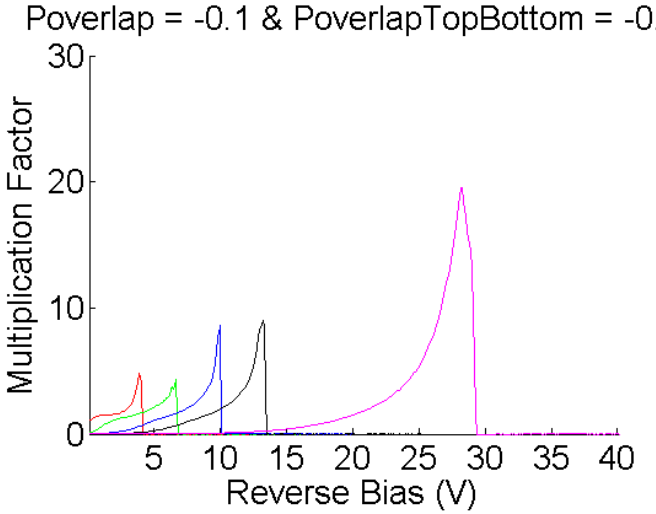
We expect that the avalanche multiplication gain is proportional to the size of the gain region. After hysteresis/burn-in is taken into consideration a very clear gain dependence on width of the avalanche region appears.

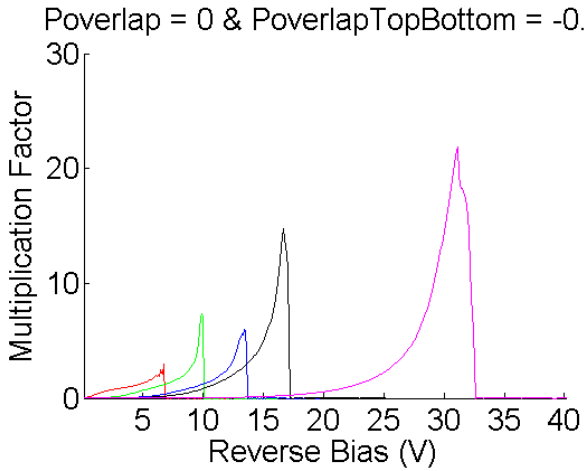
Multiplication L = 16

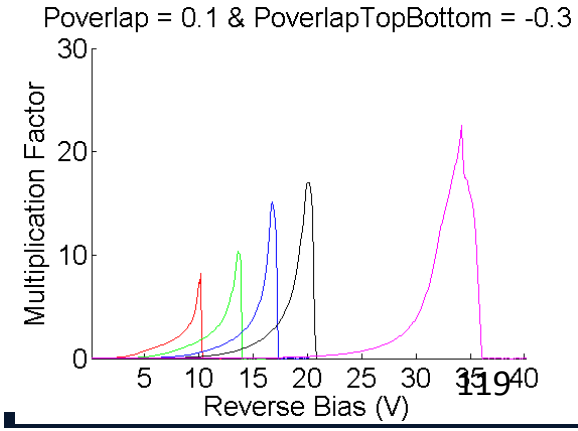












Multiplication L = 8

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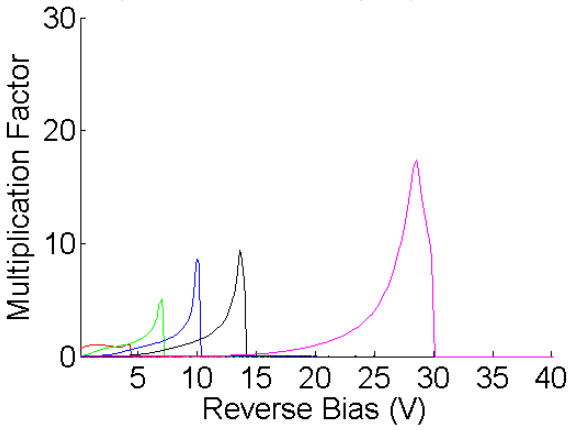
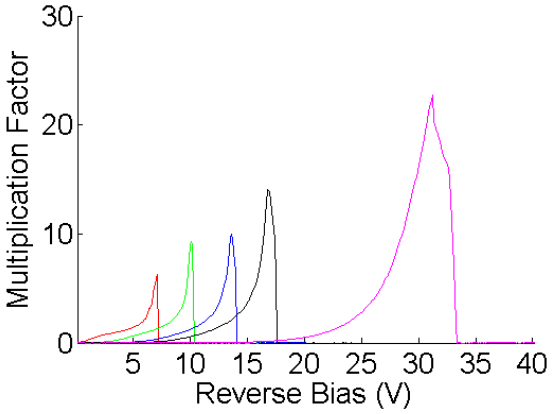
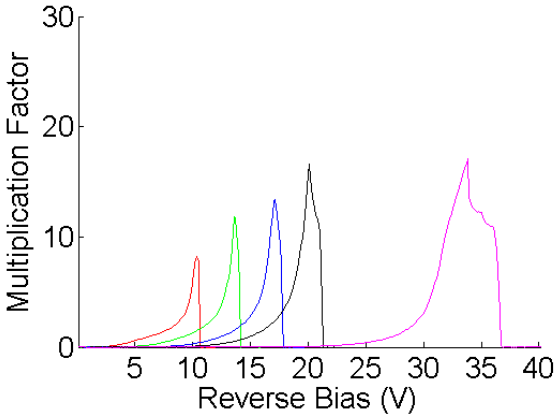
Poverlap = -0.1 & PoverlapTopBottom = 0.05



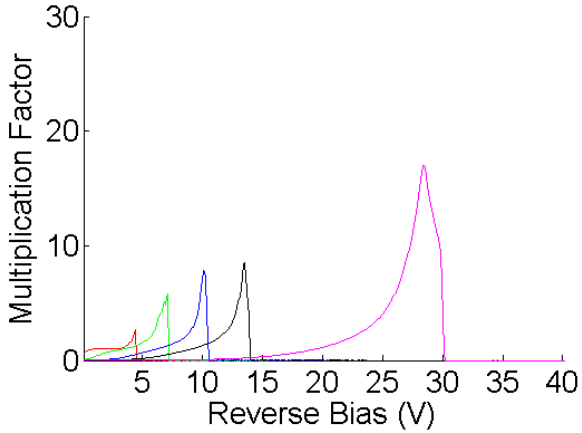
Poverlap = 0 & PoverlapTopBottom = 0.05



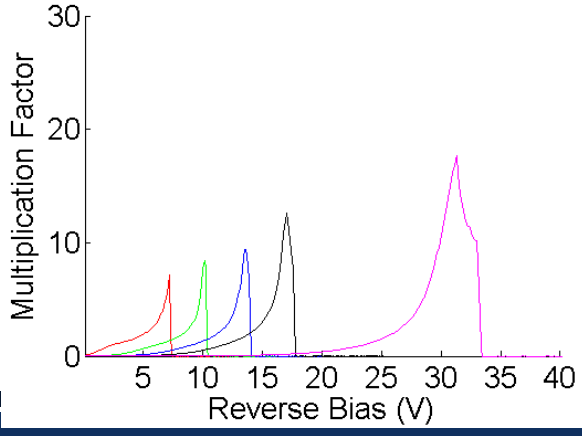
Poverlap = 0.1 & PoverlapTopBottom = 0.05



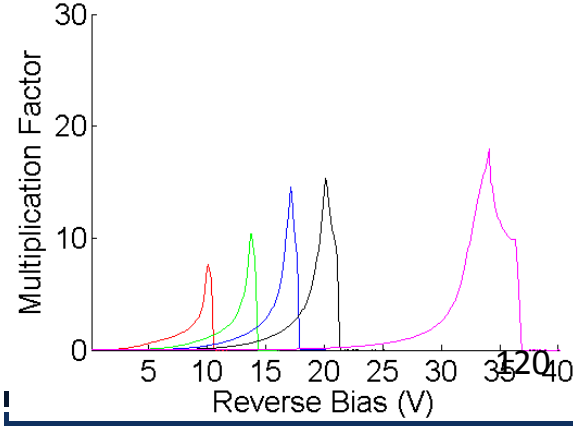
Poverlap = -0.1 & PoverlapTopBottom = -0.3



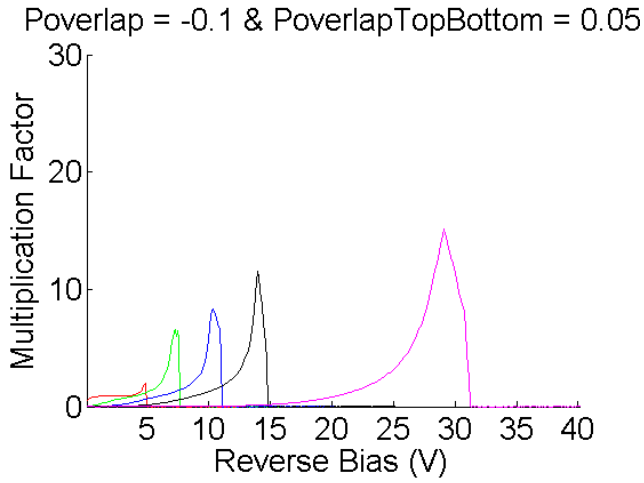
Poverlap = 0 & PoverlapTopBottom = -0.3

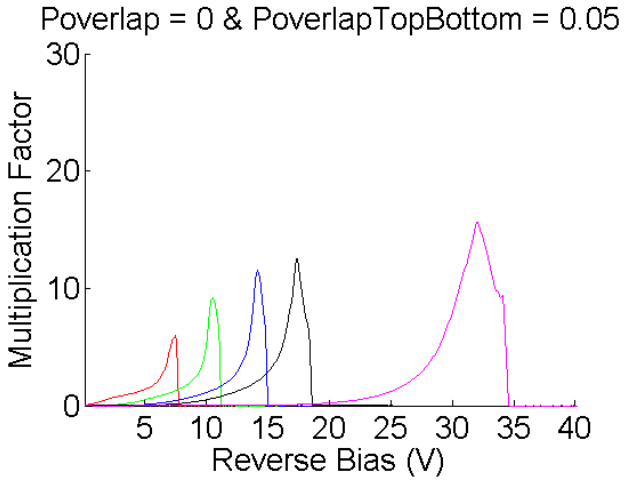


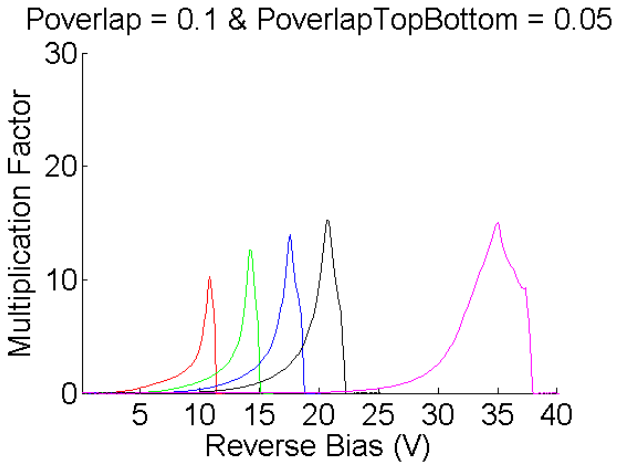
Poverlap = 0.1 & PoverlapTopBottom = -0.3

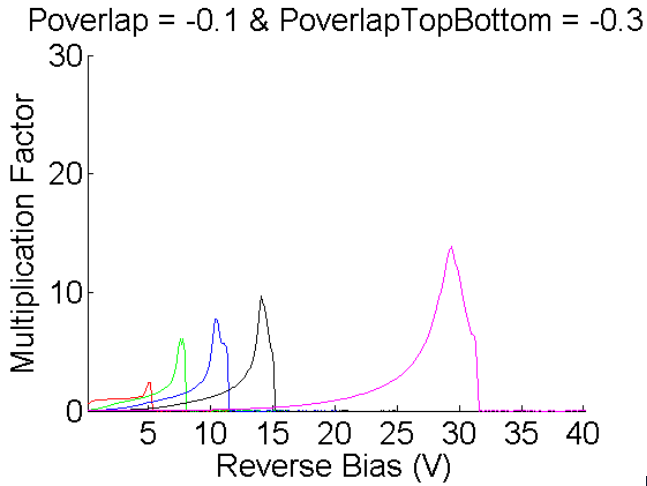


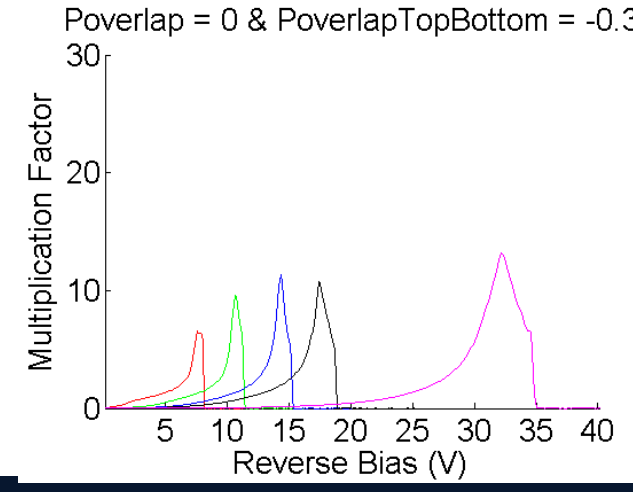
Multiplication L = 4

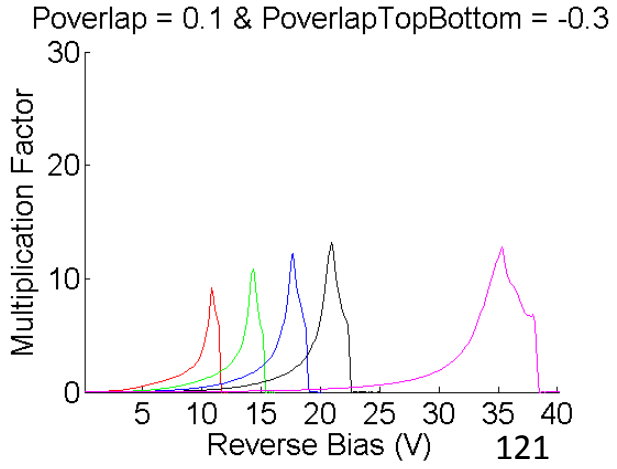




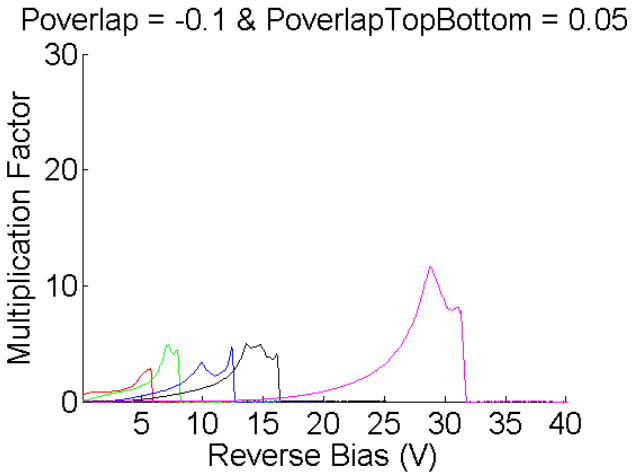


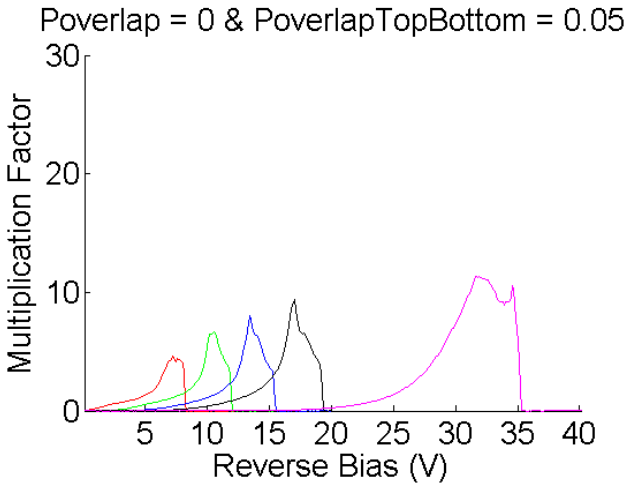


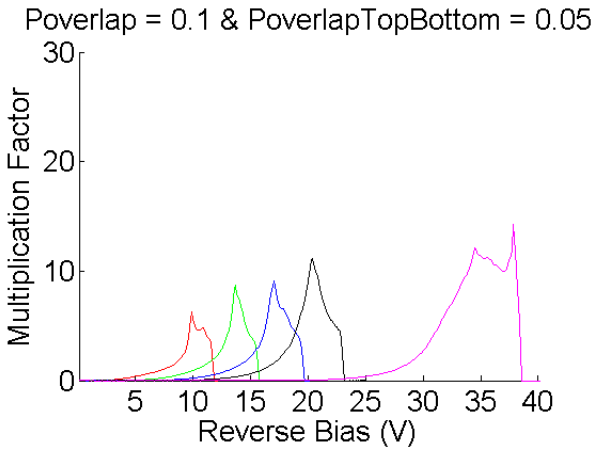


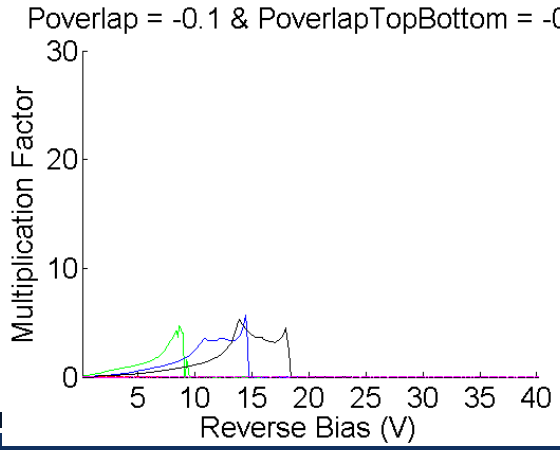


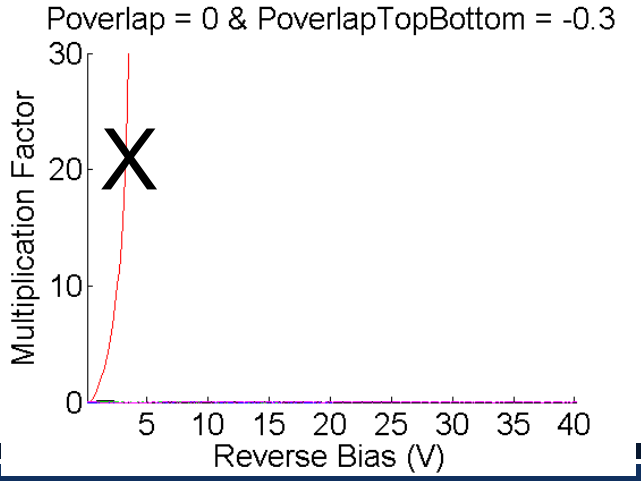
Multiplication L = 2

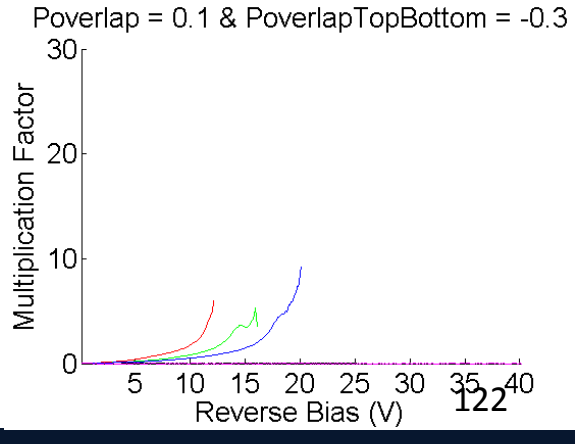






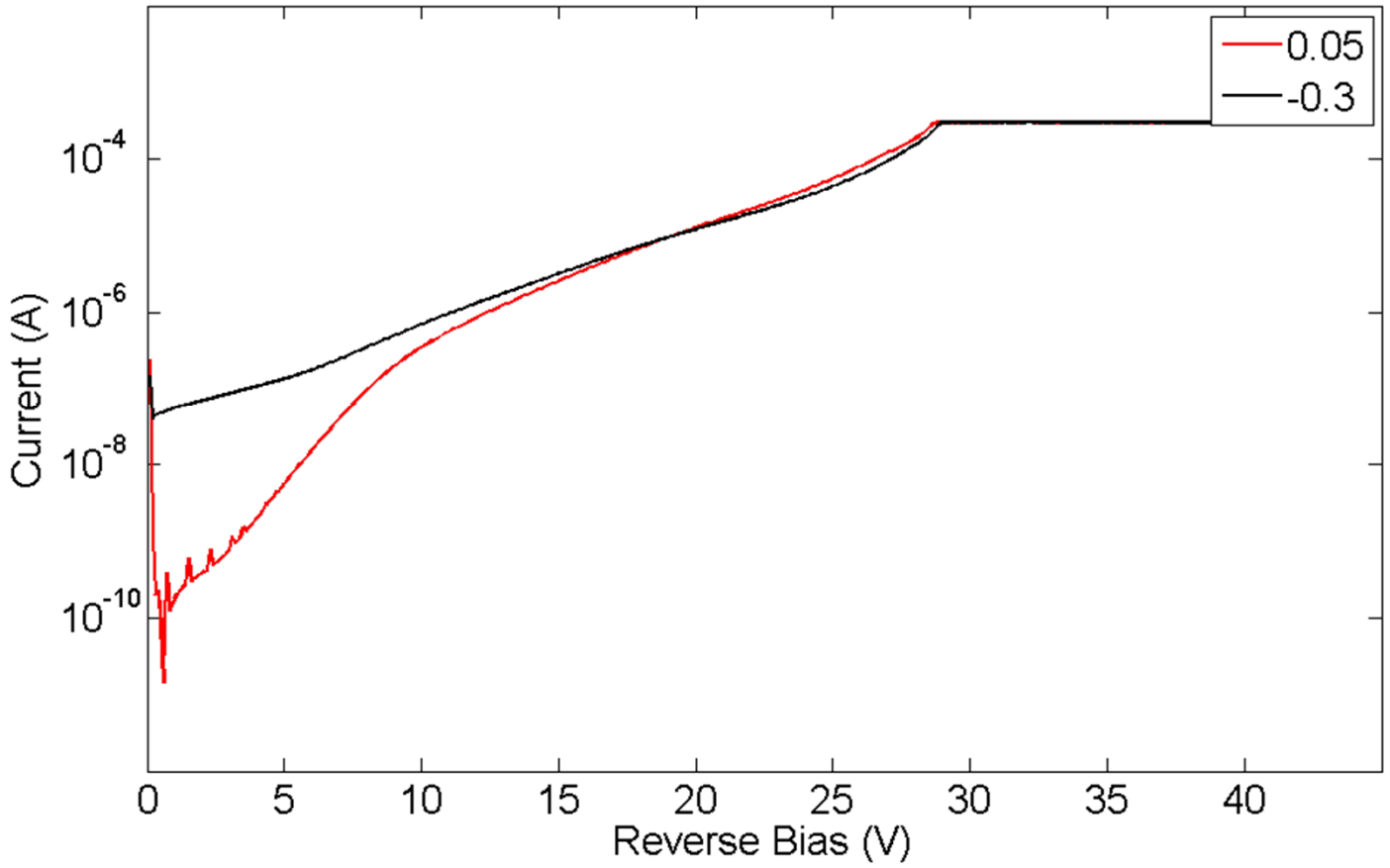




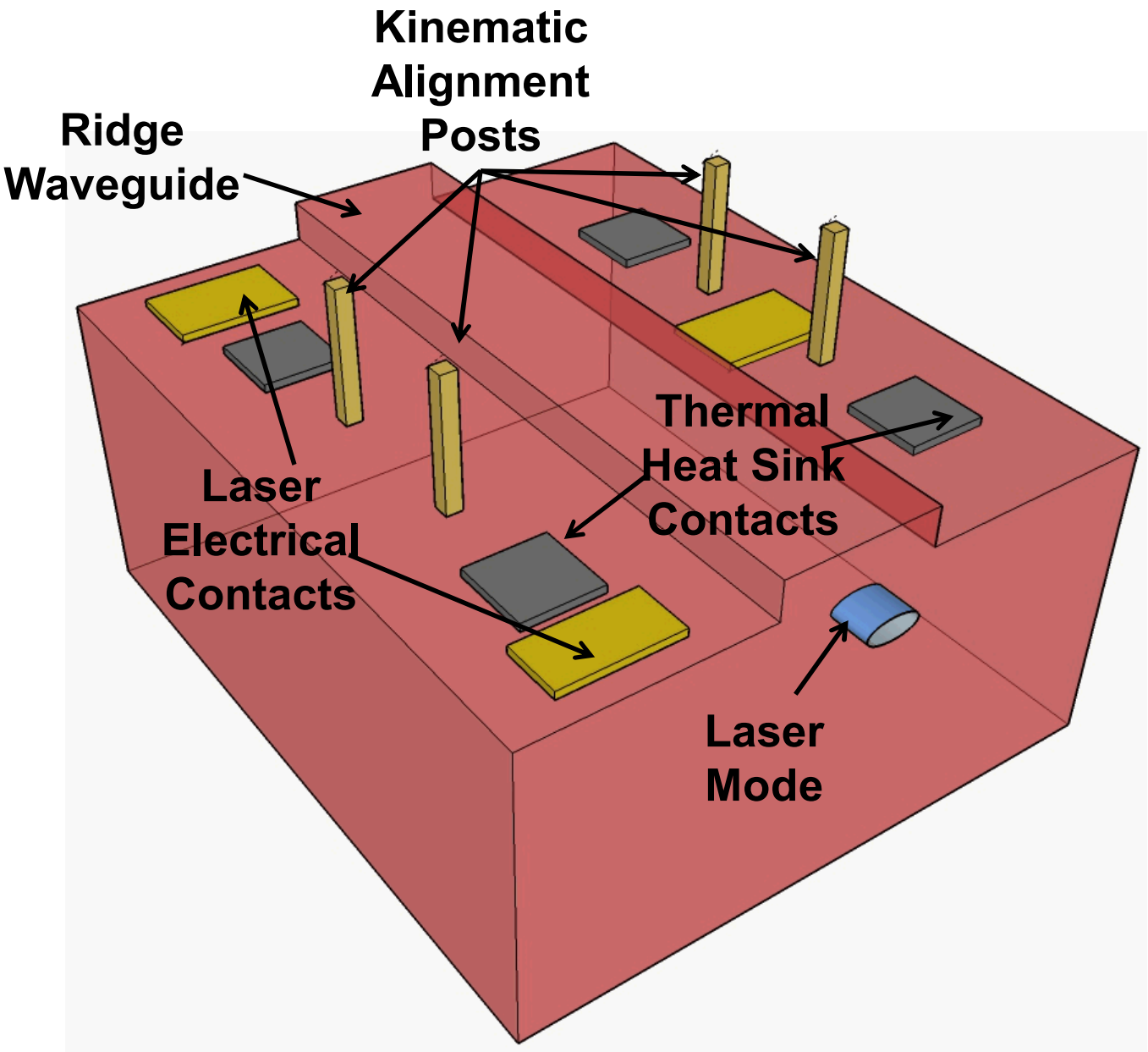


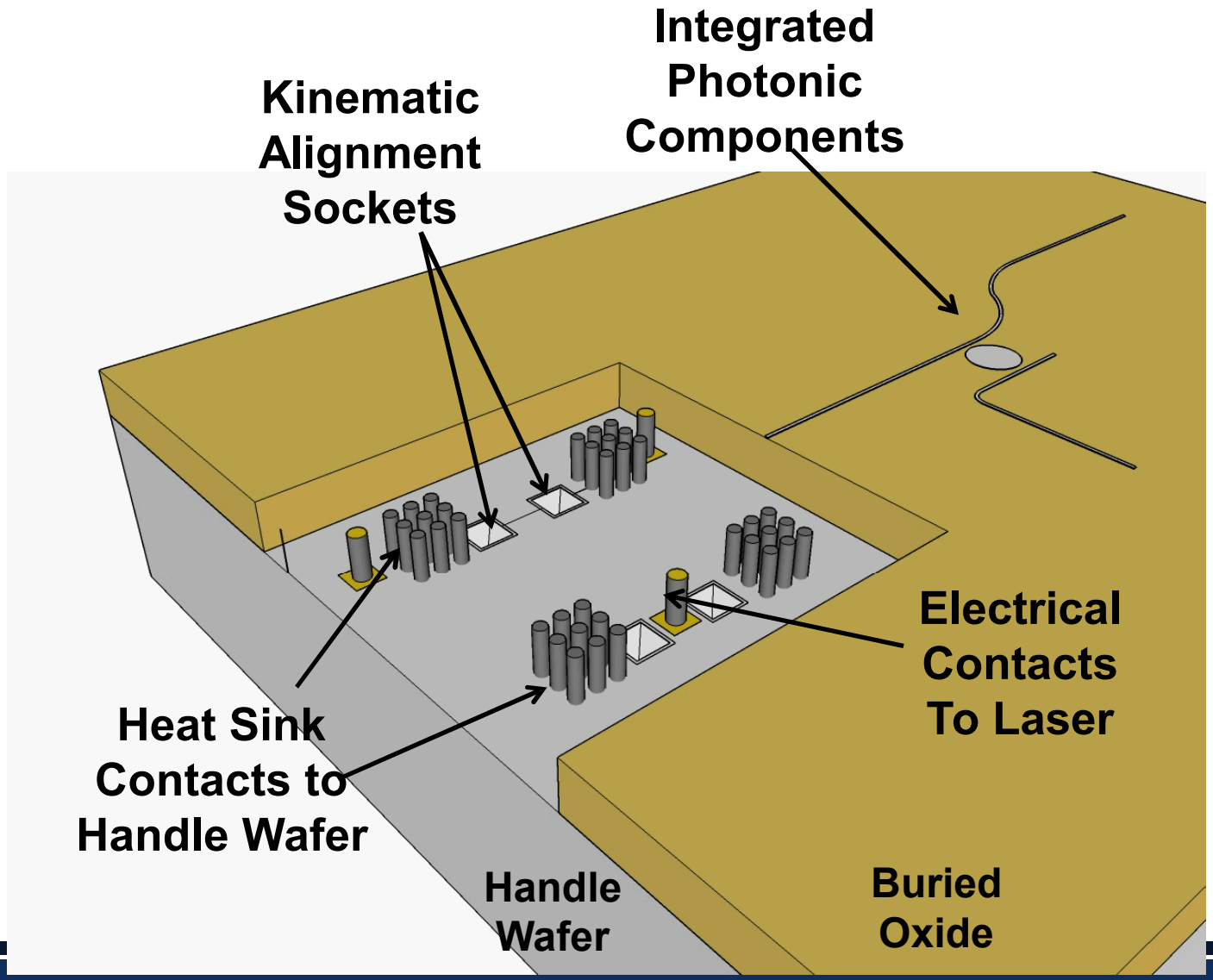
Effect of PoverlapTopBottom

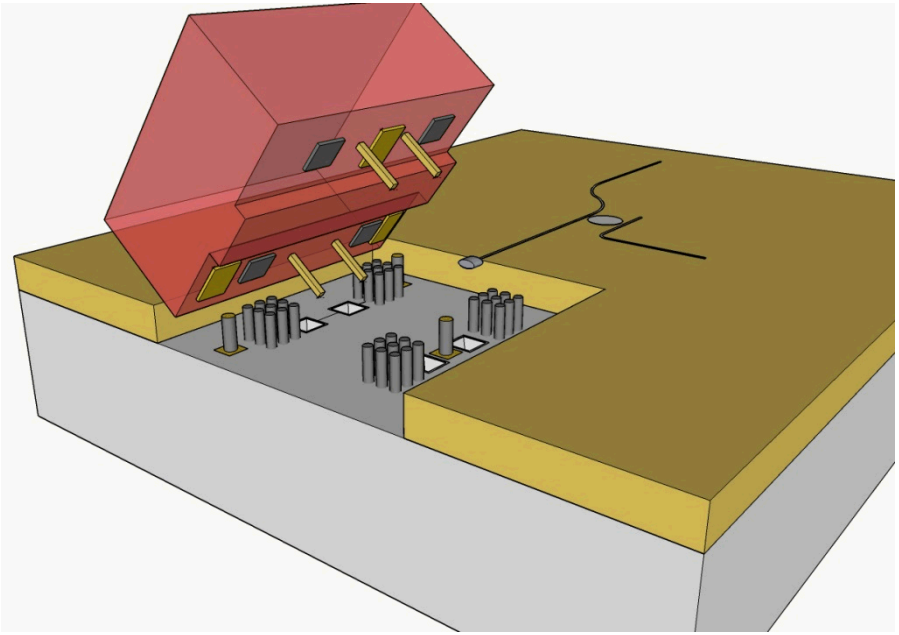
16um long 1.0 um Wmult, Poverlap = -0.1

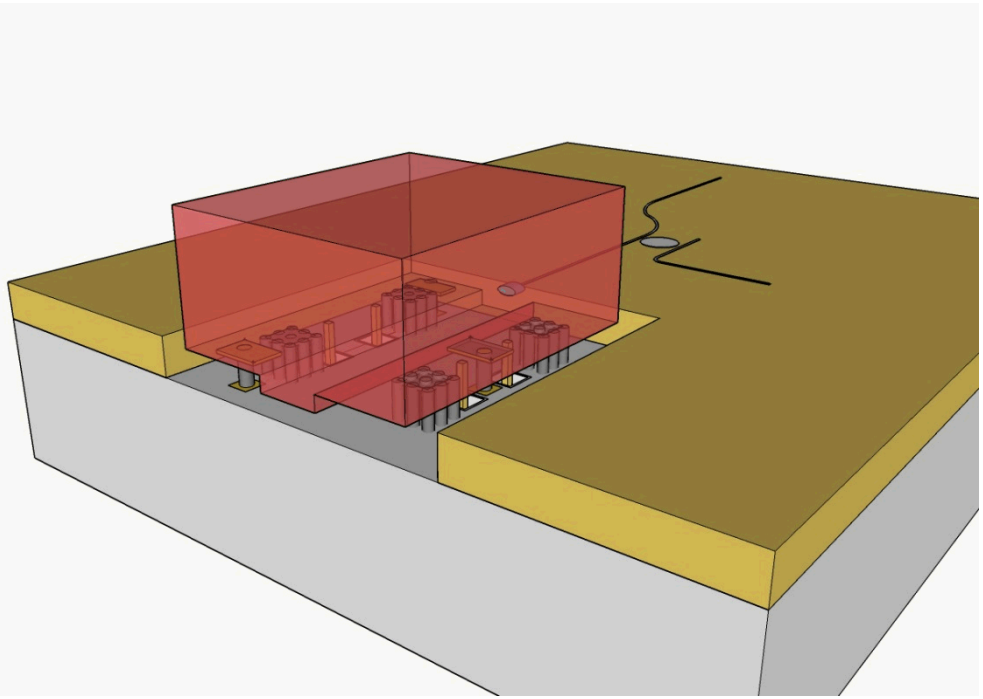


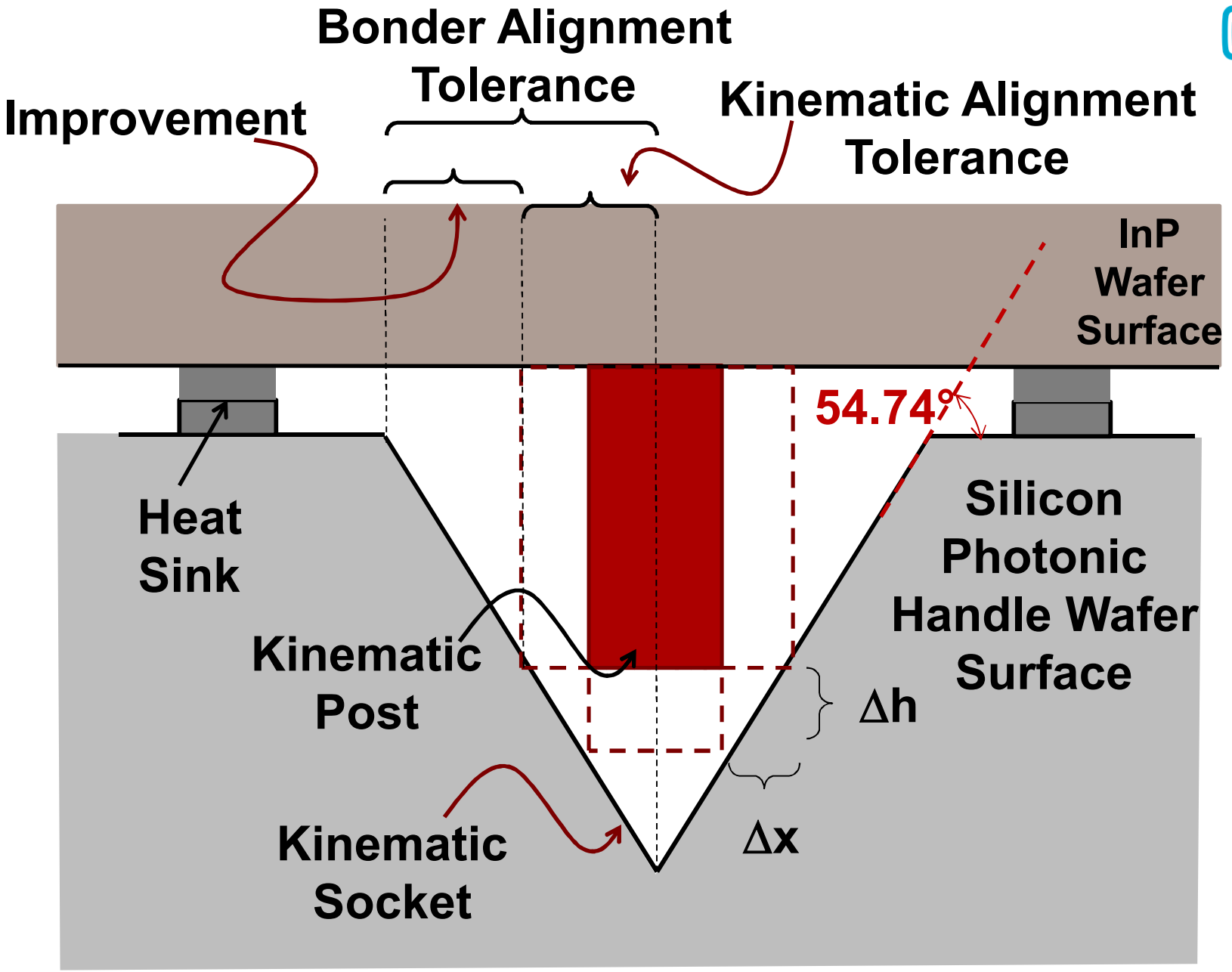
Photovoltaic mode observed at low voltages with reduced PoverlapTopBottom

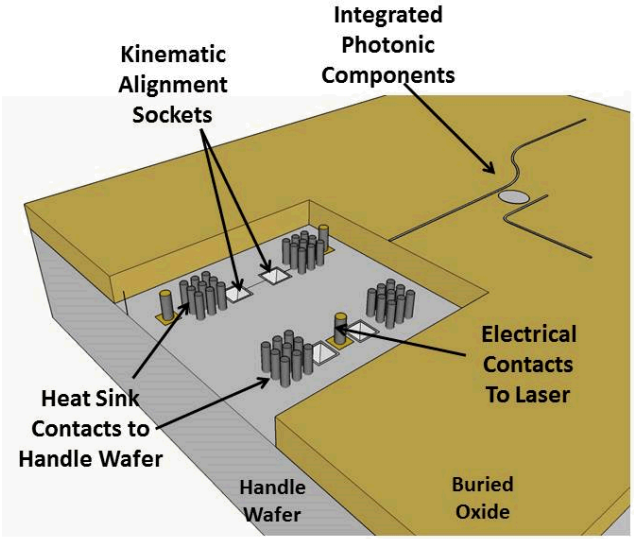

Kinematic
Alignment
Posts
Ridge
Waveguide
Thermal
Heat Sink
Contacts
Laser
Electrical
Contacts
Laser
Mode

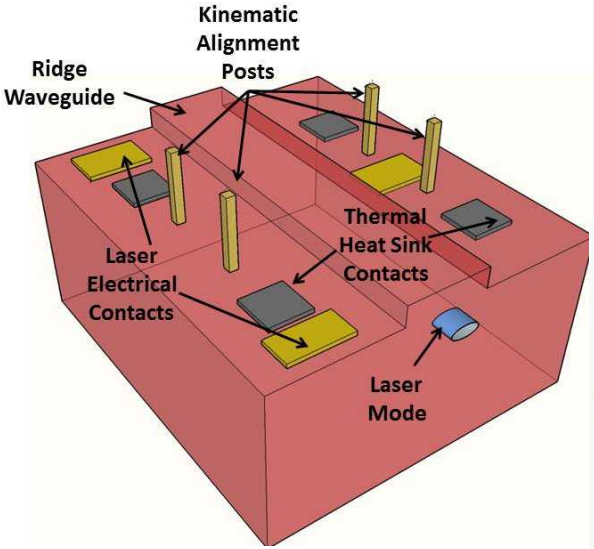

Integrated
Photonic
Components
Kinematic
Alignment
Sockets
Electrical
Contacts
To Laser
Heat Sink
Contacts to
Handle Wafer
Handle
Wafer
Buried
Oxide

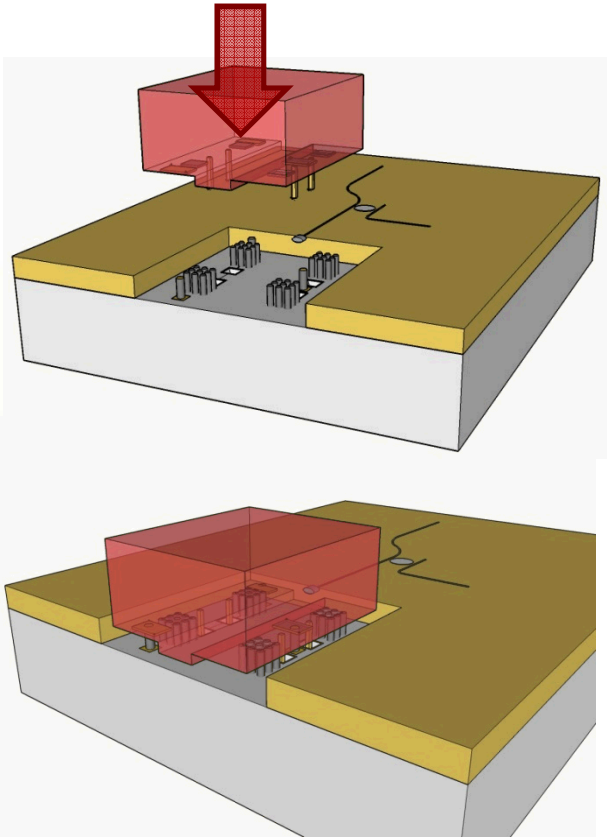





Bonder Alignment Tolerance
Improvement
Kinematic Alignment Tolerance
InP Wafer Surface
54.74°
Heat Sink
Silicon Photonic Handle Wafer Surface
Kinematic Post
Δh
Kinematic Socket
Δx


Integrated
Photonic
Components
Kinematic
Alignment
Sockets
Electrical
Contacts
To Laser
Heat Sink
Contacts to
Handle Wafer
Handle
Wafer
Buried
Oxide


Kinematic
Alignment
Posts
Ridge
Waveguide
Thermal
Heat Sink
Contacts
Laser
Electrical
Contacts
Laser
Mode



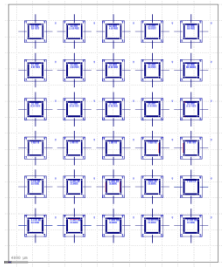
A.

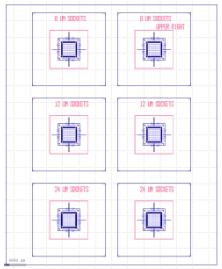
B.

C.

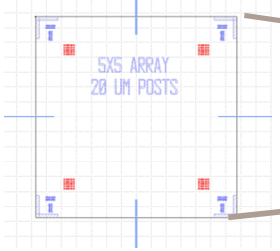
Sandia National Laboratories

Post Reticle Socket Reticle

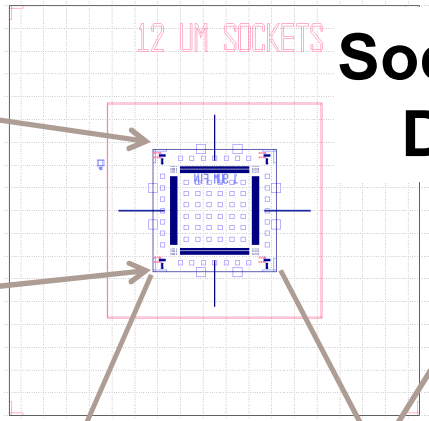




flip over

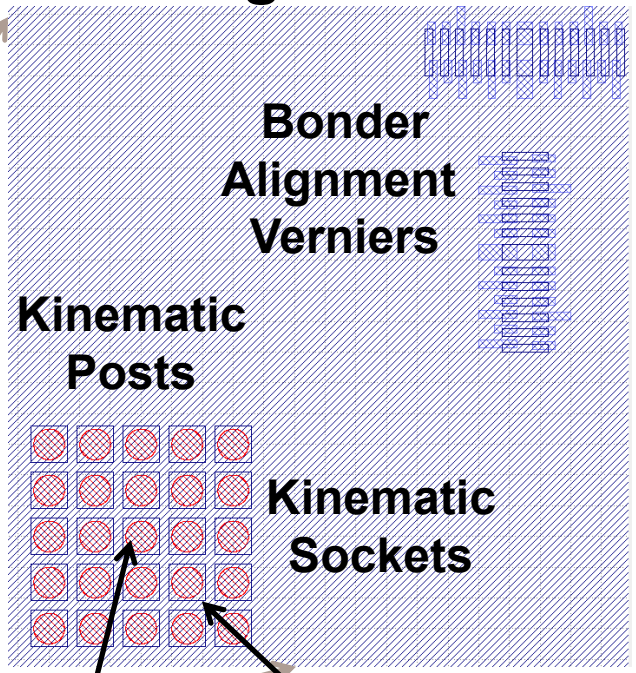


Post Die

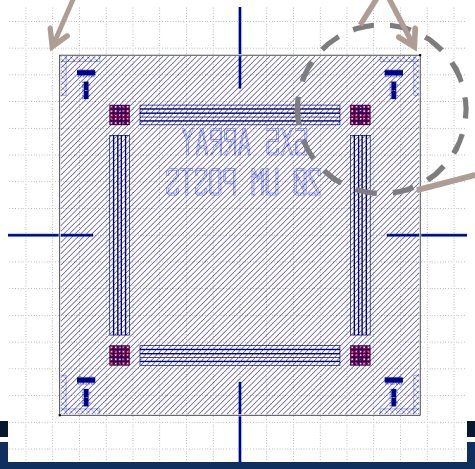


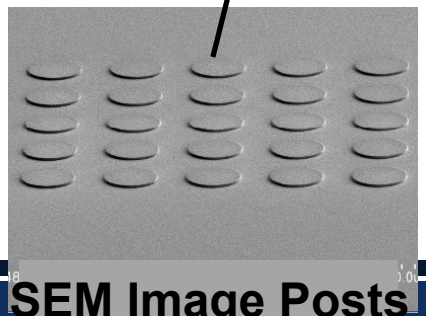
Socket Die

High Mag GDS Kinematic Alignment Features

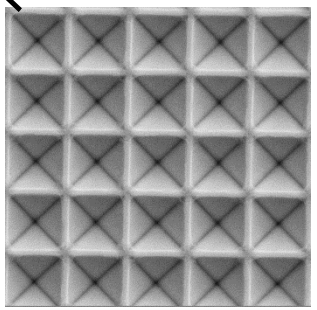


Bonded Socket-Post Die

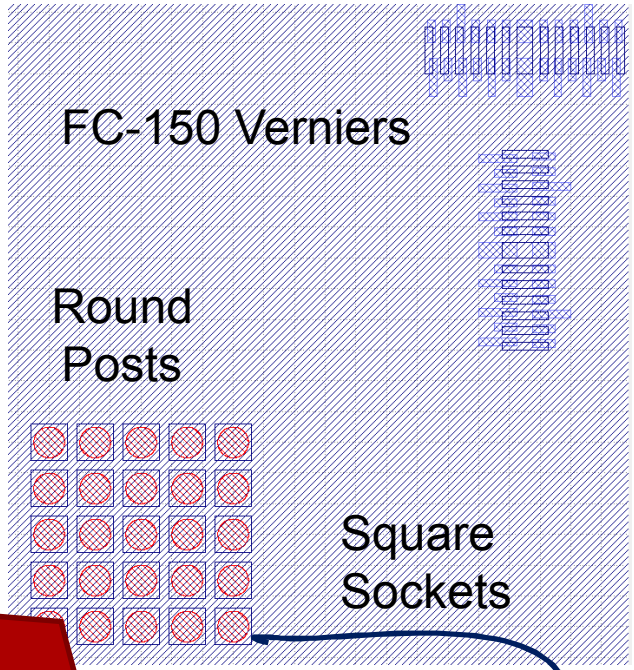




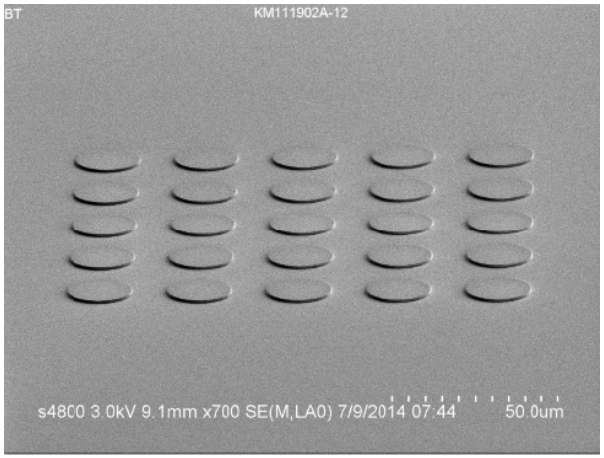
SEM Image Posts



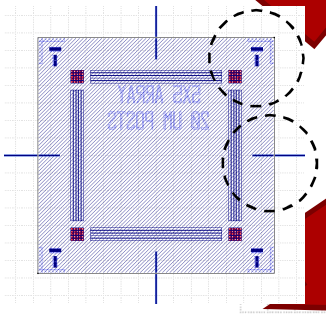
SEM Image Sockets

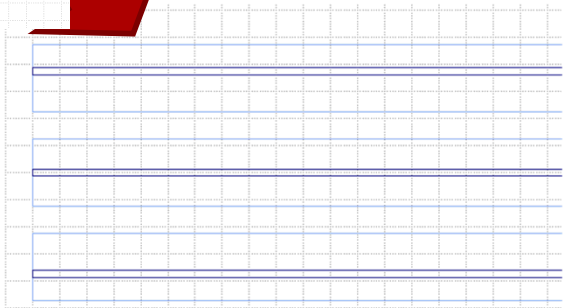


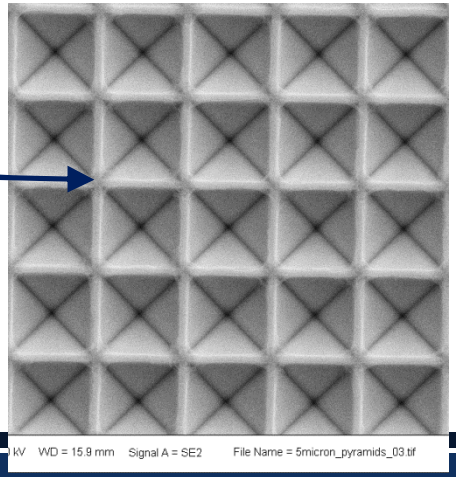
5 x 5 Post Array



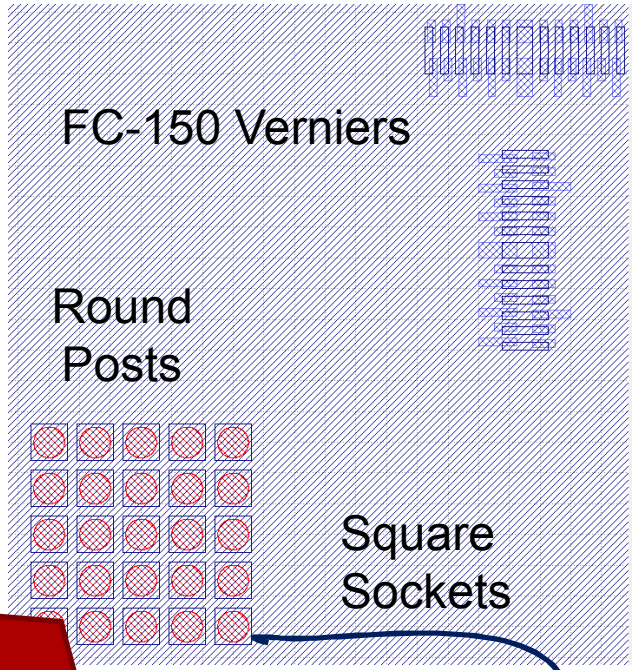
Note low aspect ratio



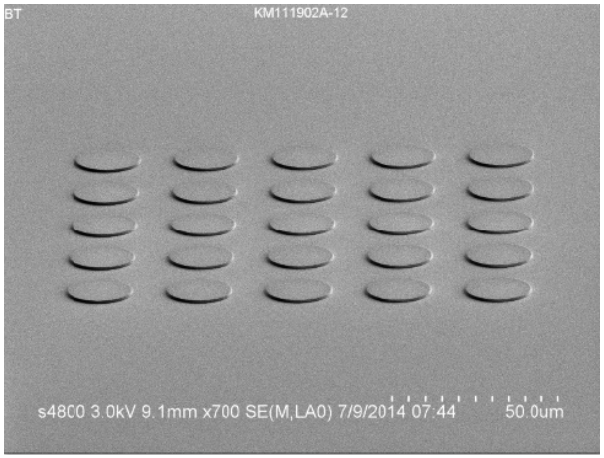


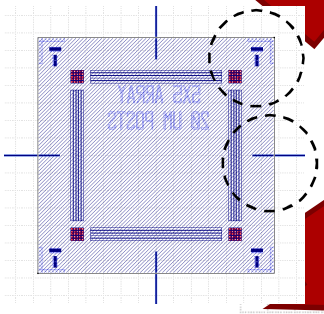


5 x 5 Socket Array

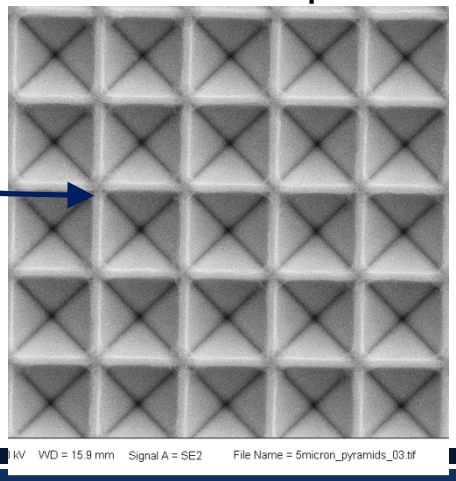


5 x 5 Post Array

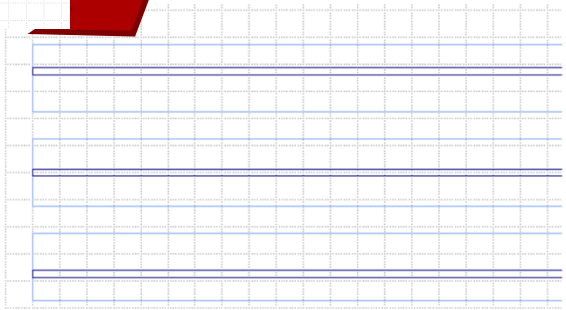




Note low aspect ratio

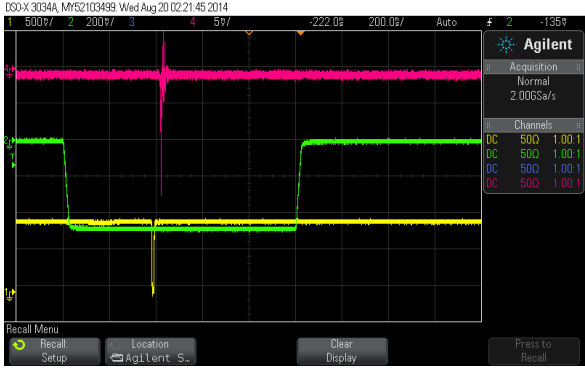


5 x 5 Socket Array



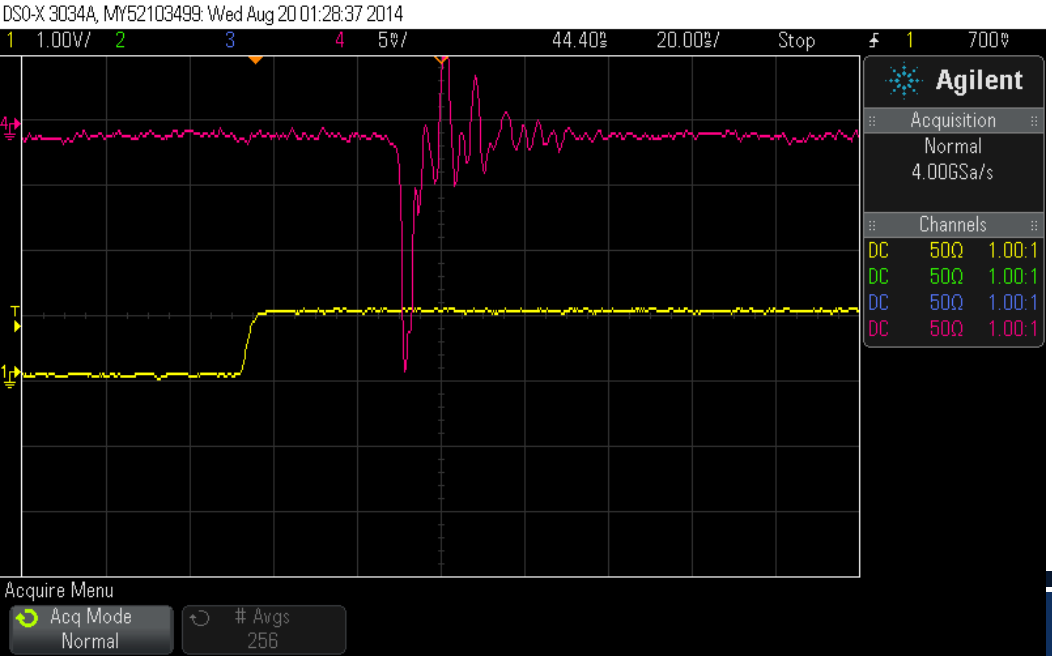
3-Element Vernier (3-Element Tauke-Pedretti)

Using Delay Generator for both Electrical and Light pulsing
Note differential spike on green trace due to DG



Using Agilent for electrical pulse
Agilent is plugged into RF of Bias Tee

Pink Trace: Signal
Green Trace: Electrical pulse
Yellow Signal: Modulated Light Pulse



Signal was taken with light on, biased ~V_B