SAND2016-1224C

Seebeck Enhancement via Quantum Confinement in MOSFET's: Towards Monolithic On-Chip Cooling

Key Team Members:

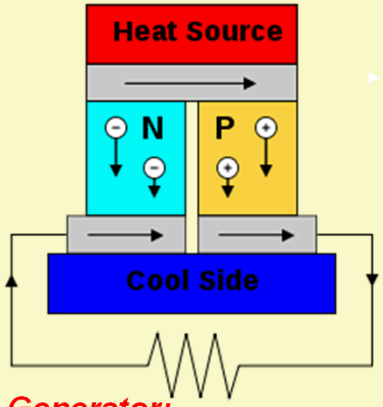
PI:
- Ihab El-Kady

Design & Experimental Measurements:
- Charles Reinke (Probe Station)
- Brian Swartzentruber (Cryostat)
- Aaron Katzenmeyer (Post Doc.)

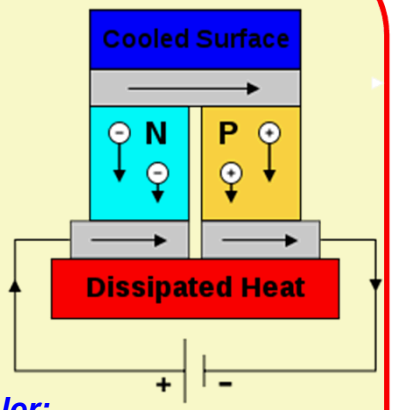
Transport Theroy:
- Erik Nielsen

Fabrication:
- Tom Hill (STD. MOSFET-Fab)

TE Peltier Effect:



Generator:
Heat gradient ➔ current flow



Cooler:
Apply DC voltage ➔ heat moves from cold-side to hot-side

Performance: Quantified by the dimensionless quantity ZT

- Figure of merit : $Z = S^2\sigma/\kappa$
- S: Seebeck coefficient ($\Delta V/\Delta T$)
- σ: Electrical conductivity
- κ: Thermal conductivity ($= \kappa_e + \kappa_{ph}$)

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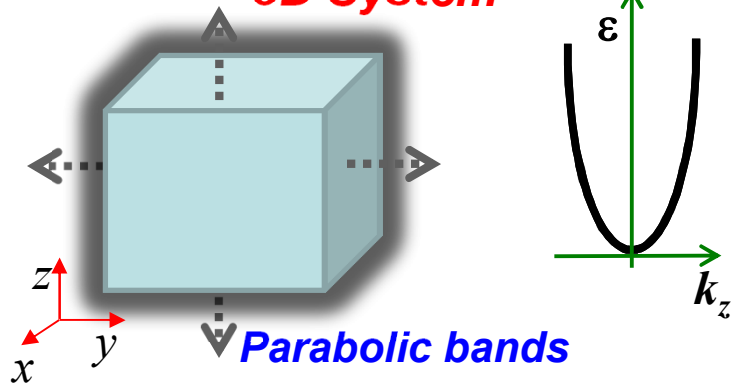
Objective:
Increasing S via Quantum Confinement

- **According to the Mott[1,2] and Wood [3] ⇒ Thermodynamically S∝ Entropy per carrier**
- **Hicks and Dresselhous [4,5] ⇒ Reduced dimensionality ⇒ Increase the Entropy share of each carrier**

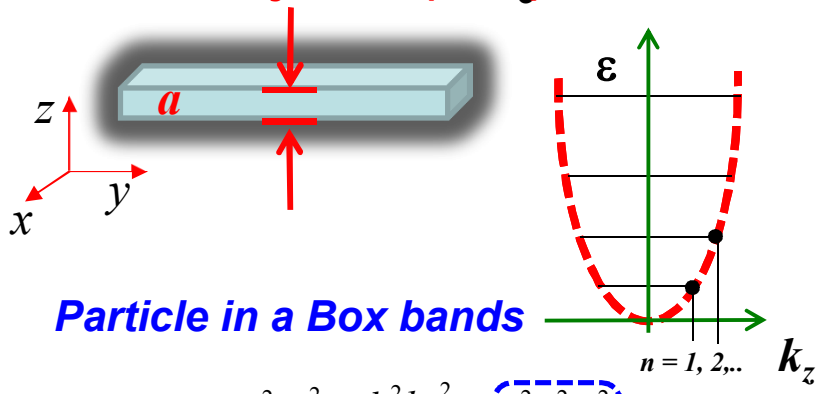
3D System



Parabolic bands

$$\varepsilon(k_x,k_y,k_z)=\frac{\hbar^2 k_x^{\,2}}{2m_x}+\frac{\hbar^2 k_y^{\,2}}{2m_y}+\frac{\hbar^2 k_z^{\,2}}{2m_z}$$

2D System ($a \le \lambda_e$)



Particle in a Box bands

$$\varepsilon(k_x,k_y,k_z)=\frac{\hbar^2 k_x^{\,2}}{2m_x}+\frac{\hbar^2 k_y^{\,2}}{2m_y}+\frac{n^2\hbar^2\pi^2}{2m_z a^2}$$

- **Following the derivation of the thermoelectric transport coefficients [4,5]:**

$$S_{3D}=-\frac{k_B}{e}\left(\frac{5F_{3/2}(\mu)}{3F_{1/2}(\mu)}-\frac{\mu}{k_BT}\right)$$

$$S_{2D}=-\frac{k_B}{e}\left(\frac{2F_1(\mu)}{F_0(\mu)}-\frac{\mu}{k_BT}+\frac{n^2\hbar^2\pi^2}{2m_z a^2 k_BT}\right)$$

Electronic contribution to S

Electrochem. contribution to S

Effect of quantized dimension

Reduced order by ½ due to quantized missing dimension

Thermodynamics:

$$dU = TdS - PdV + \sum_i \mu_i dN_i$$

$$TdS = dU - \sum_i \mu_i dN_i$$

$S \leftrightarrow$ *Entropy / carrier*

- ***$F_i(\mu)$:*** *Is the Fermi-Dirac Distribution function*
- ***μ:*** *is the Chemical potential*

Challenges to the Quantum Confinement Approach

Creation of a 2D quantum system:

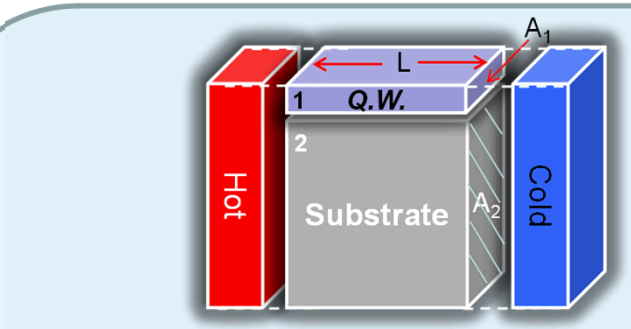
1. *Traditionally done by ALD ➔ "nm" layer thicknesses ➔ Superlattices*
   - ➔ *Difficult to integrate*
   - ➔ *Hard to scale-up*
   - ➔ *We will create a 2D electronic QW at the top layer of a 3D slab by using an electric field*

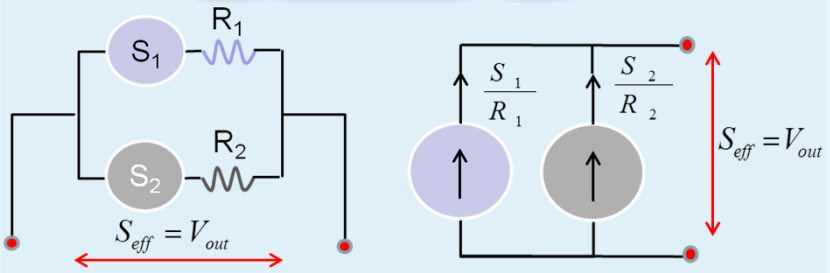
Eliminating the substrate effects:

2. *Because we will now have a "substrate"*
   - ➔ *Substrate will compete with our QW for transport!*
   - ➔ *Rather than eliminate the substrate ➔ we will isolate it electrically to reduce its influence*

Practicality Challenge:

3. *How much energy can we move through the QW as oppose to the substrate?*
   - ➔ *Force enough of the energy to move though the QW*
   - ➔ *Calculate performance metrics*
   - ➔ *Evaluate potential integration schemes*





$$\sigma_{eff} = \frac{A_1 \cdot \sigma_1 + A_2 \cdot \sigma_2}{A_1 + A_2}, \qquad \kappa_{eff} = \frac{A_1 \cdot \kappa_1 + A_2 \cdot \kappa_2}{A_1 + A_2}$$

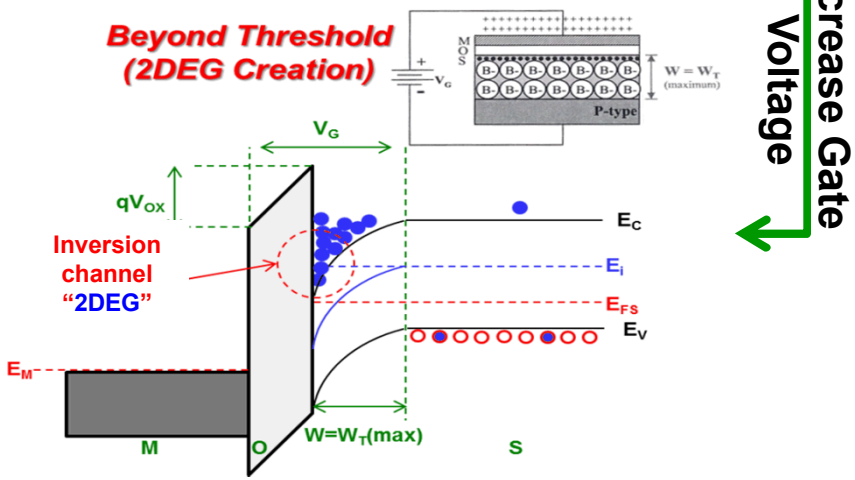
$$\& \qquad S_{eff} = \frac{(A_1 \cdot \sigma_1)S_1 + (A_2 \cdot \sigma_2)S_2}{(A_1 \cdot \sigma_1) + (A_2 \cdot \sigma_2)}$$

To <u>minimize/eliminate</u> the substrate influence we need:

- ➔ $\sigma_1 \geq (A_2/A_1)\sigma_2$ ***or***
- ➔ σ_2 ➔ ***zero! or***
- ➔ ***Isolate substrate electrically***

Creation of an electrically defined 2D QW

MOS Capacitor Under Inversion



Is the inversion channel narrow enough?

Book Chapter preprint, C. Hu

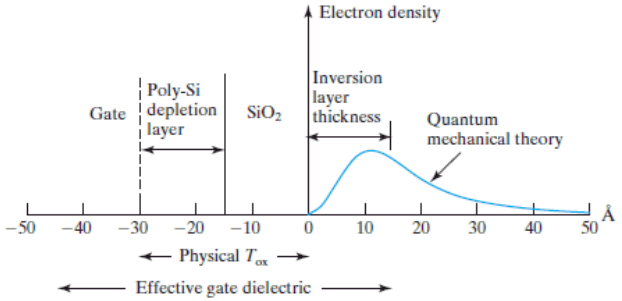


FIGURE 5–24 Average location of the inversion-layer electrons is about 15 Å below the Si–SiO_2 interface. Poly-Si gate depletion is also shown.

[8] Yang. K., Y-C. King, C. Hu, Technical Digest of Symposium on VLSI Technologies, p.77-78, (1999)

[10] IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 44, NO. 11, NOVEMBER 1997

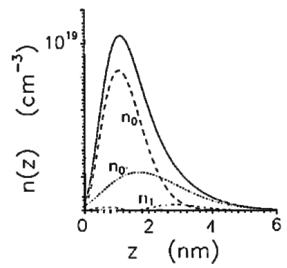


Fig. 1. Total electron concentration as a function of the distance from the silicon-SiO_2 interface (solid line) and electron concentrations contained in the three lowest subbands (dashed lines). Long dashed lines correspond to the two ellipsoids perpendicular to the interface in a transistor with a (100)-oriented substrate. Short dashed lines correspond to the four parallel ellipsoids. Doping concentration: $5 \cdot 10^{17}$ cm^{-3}. Electron density per unit area: 10^{12} cm^{-2}.

[9] Andreas Wettstein, "Quantum Effects in MOS devices", (2000)

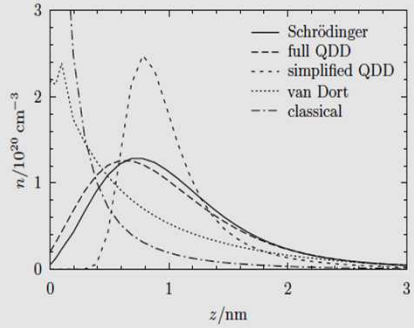


Figure 5.4.: *Density distribution in the device of Fig. 5.2 in deep inversion ($U_G = 4$ V)*

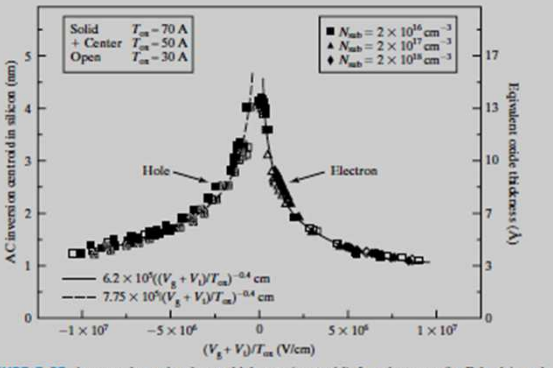


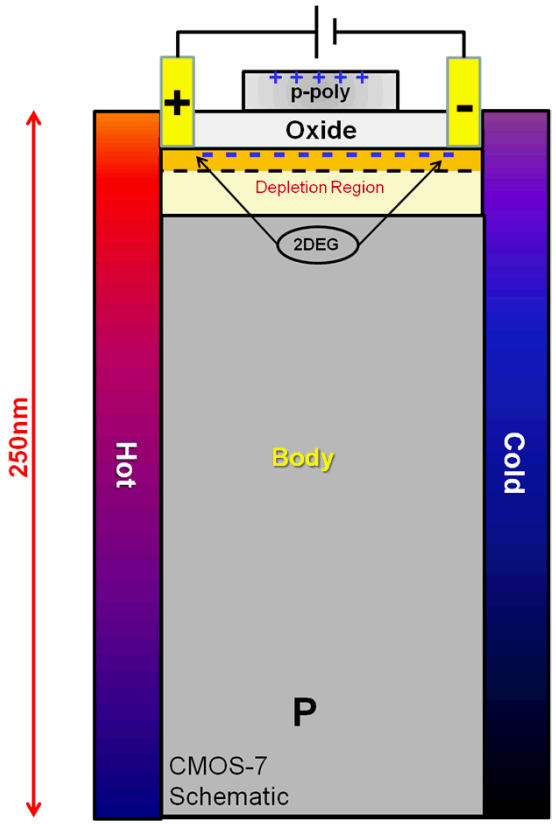
FIGURE 5–25 Average inversion-layer thickness (centroid) for electrons (in P body) and holes (in N body). (From [3]. © 1999 IEEE.)

- ***SiGe-NW 11-25nm (2DHG defined by gate voltage): increase in S with increasing gate voltage*** [11 Jaeyun Moon, et. al., Nano Lett., dx.doi.org/10.1021/nl304619u (2013)]

Eliminating the substrate effect via MOSFET structure

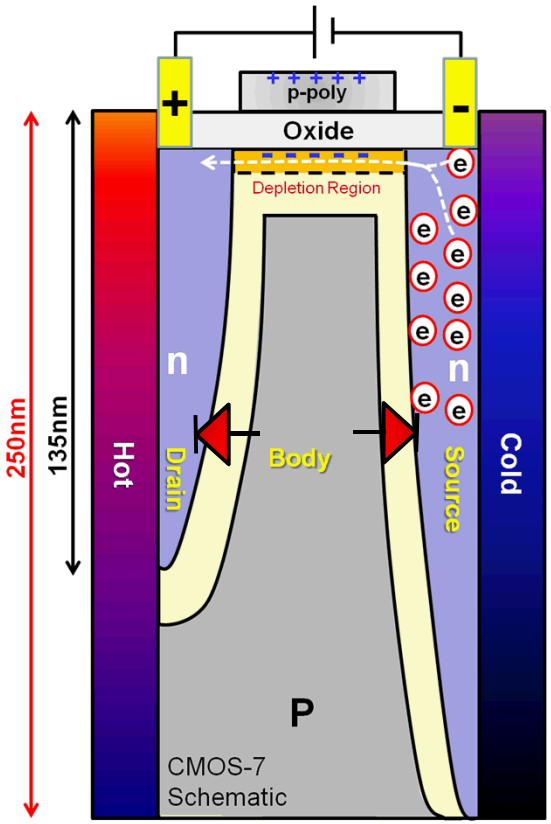
Delaminating the Electrical and Thermal paths

MOSCAP



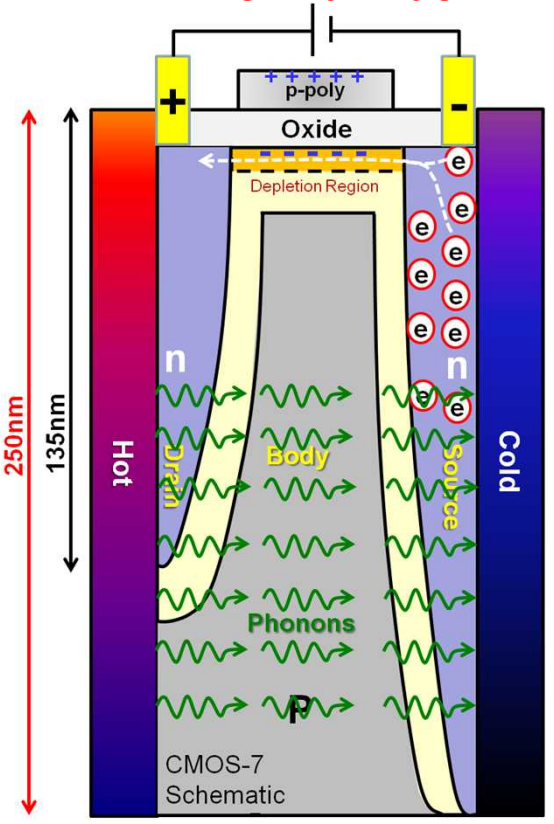
The most likely electric path is through 2DEG
Body still competes

MOSFET



The only possible electric path is through 2DEG
Body electrically isolated

Thermal Path



Dominant thermal path will be through the body

$$S_{eff} \approx S_{2DEG}, \quad \sigma_{eff} \approx \sigma_{2DEG} \quad \& \quad \kappa_{eff} \approx \kappa_{Body}$$

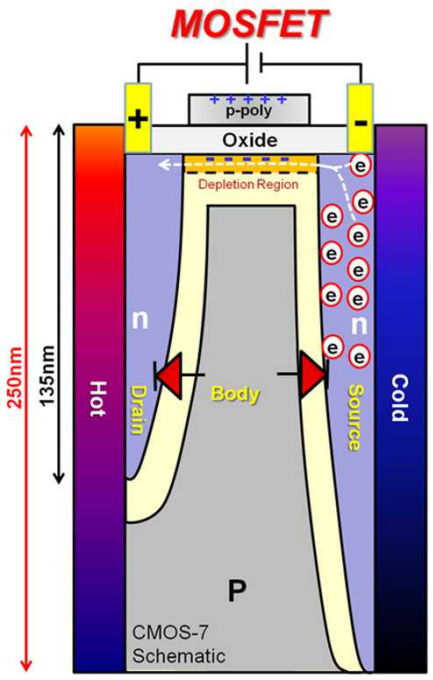
Our Approach:
Electronic as opposed to Physical Confinement

Creation of a 2D quantum system:

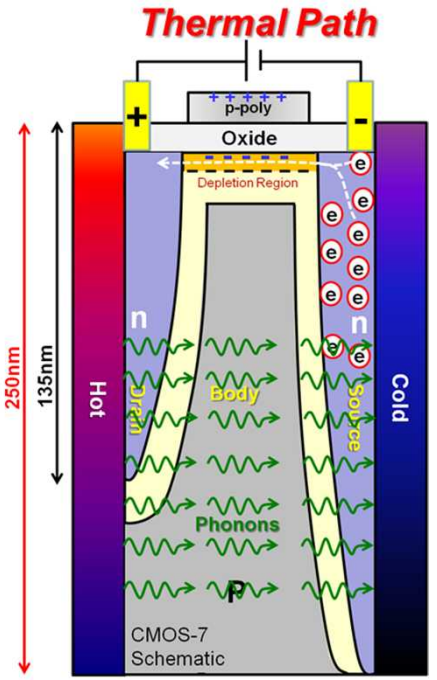
1. *Traditionally a physically thin layer: (e.g. "nm" Superlattices, Graphene, …etc.)*
   - ➔ *Difficult to handle, integrate and scale-up*
   - ➔ *We will create a 2D electronic QW at the top layer of a 3D slab by using an electric field*

Minimizing the substrate effects:

2. *Because we will now have a "substrate"*
   - ➔ *Substrate will compete with our QW for transport!*
   - ➔ *Rather than eliminate the substrate ➔ we will isolate it electrically to reduce its influence*



*The **only possible** electric path is through 2DEG*
Body electrically isolated



***Dominant** thermal path will be through the body*

$$S_{eff} \approx S_{2DEG}, \quad \sigma_{eff} \approx \sigma_{2DEG} \quad \& \quad \kappa_{eff} \approx \kappa_{Body}$$

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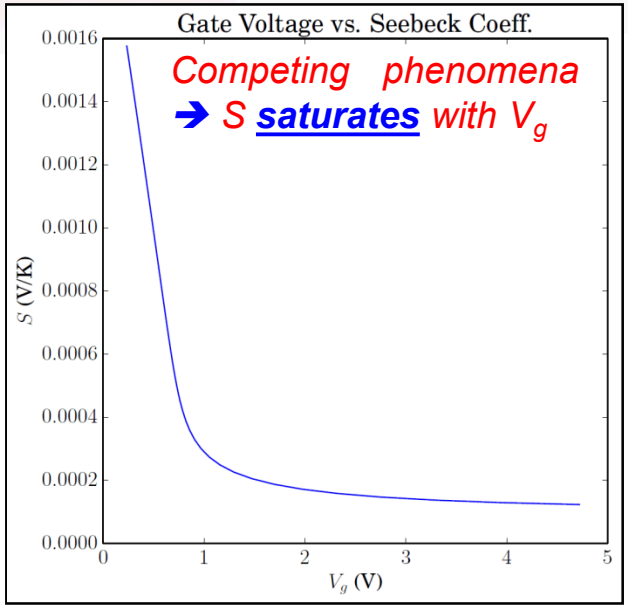
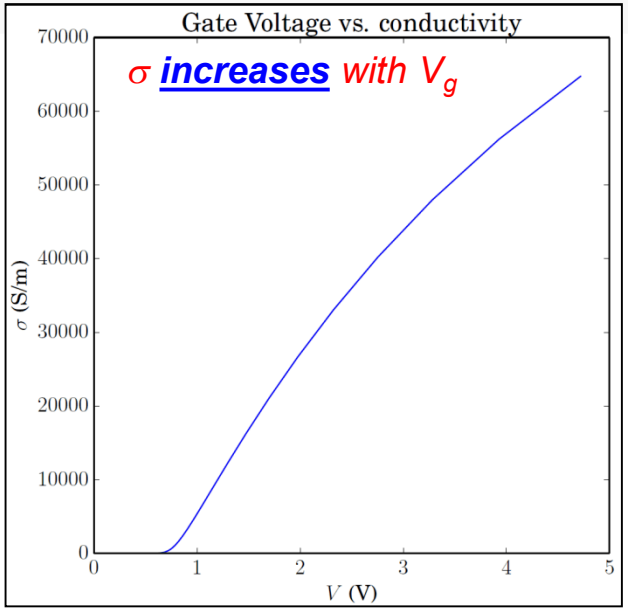
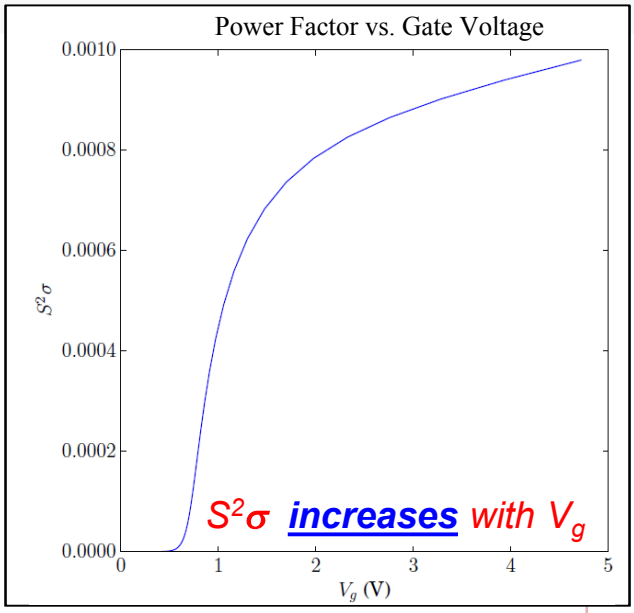
Quantum Confinement Effects-Theoretical Predictions

Quantum versus Classical TE Behavior

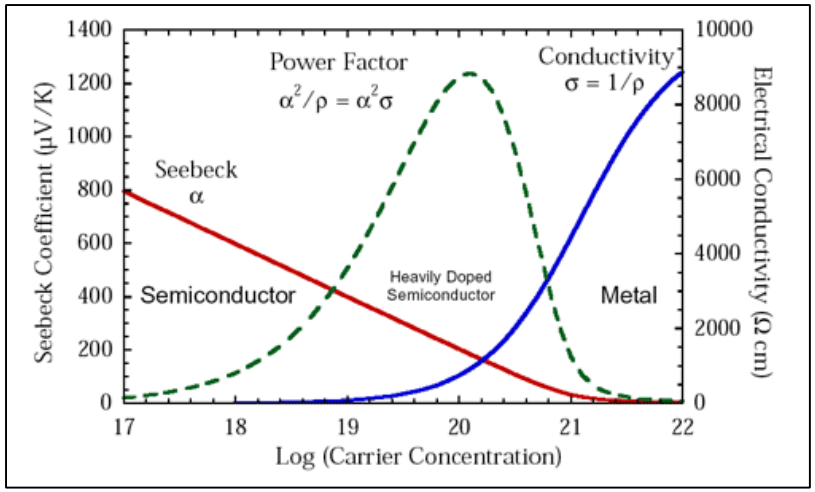
Predicted Behavior







Classical Behavior



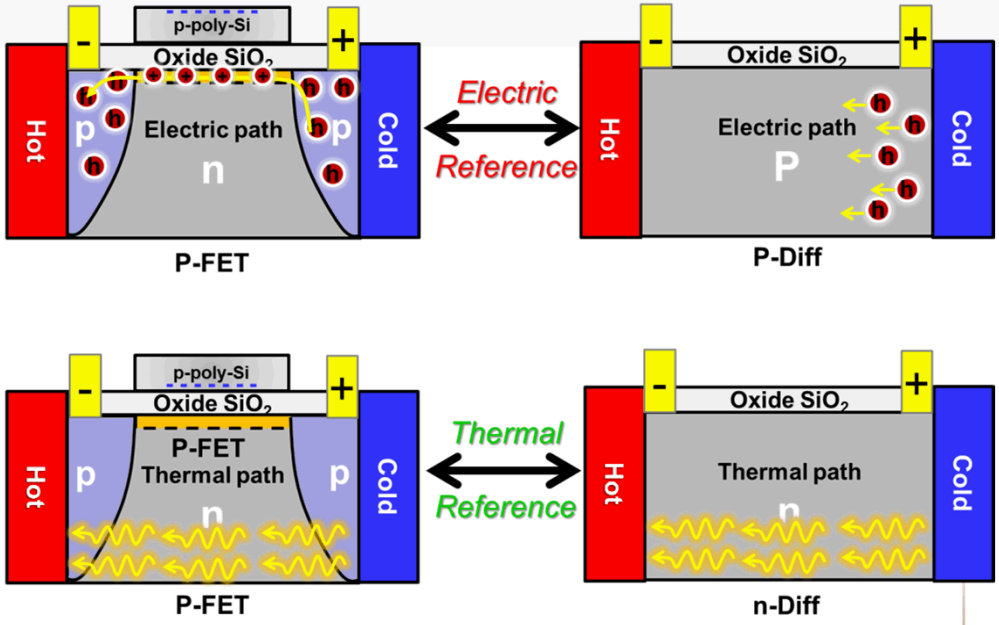
- ***Recall that $V_g \propto N$ (carrier concentration)***
- ***Given:***
  - ***Enhancement in channel conductivity compared to body***
  - ***Size of channel***

  ➔ Carrier concentration in the FET channel >> $10^{21}cm^3$!
- ***Expected behavior is non-classical!***

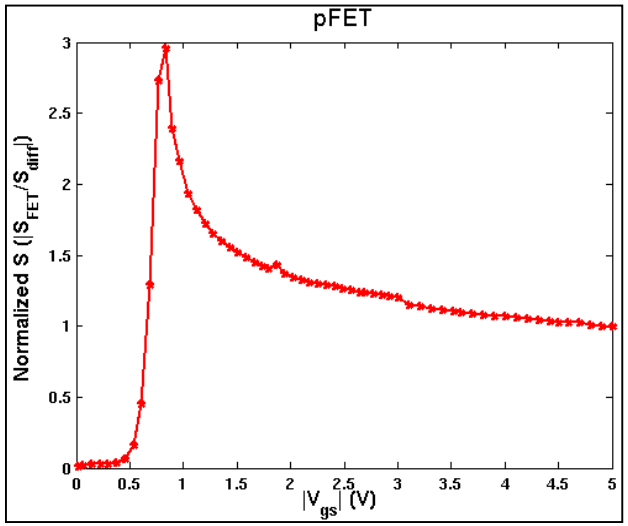
Experimental Measurements
P-MOSFET MPW111102E-W01

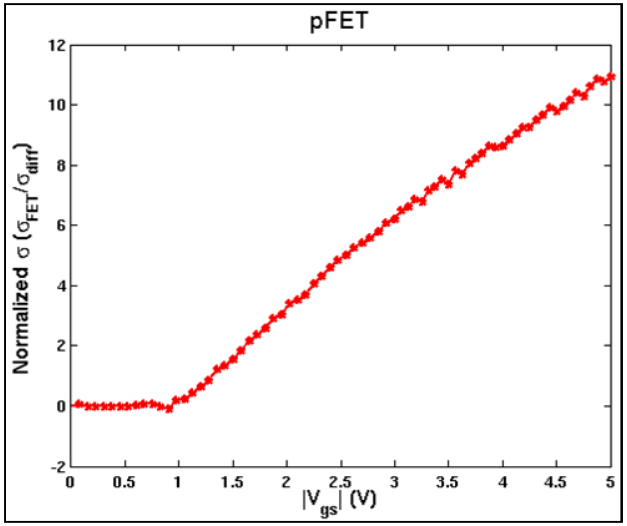
To avoid any systematic errors:

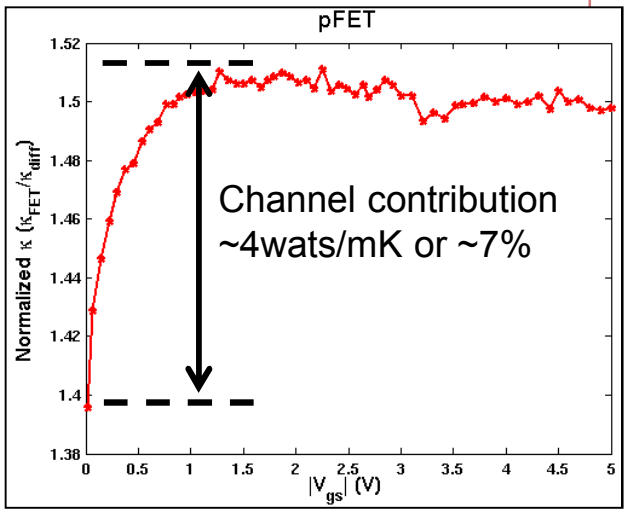
- Normalize electric measurements (σ & S)
- Intrinsic properties independent of size
- **p-FET** to **p-diffusion**
  - Doping determines threshold voltage (channel formation)
  - Channel characteristics are determined by carrier type and mobility
- Normalize thermal conductivity κ
- **p-FET** to **n-diffusion**
  - Thermal conductivity is dominated by body



Electric Measurements:



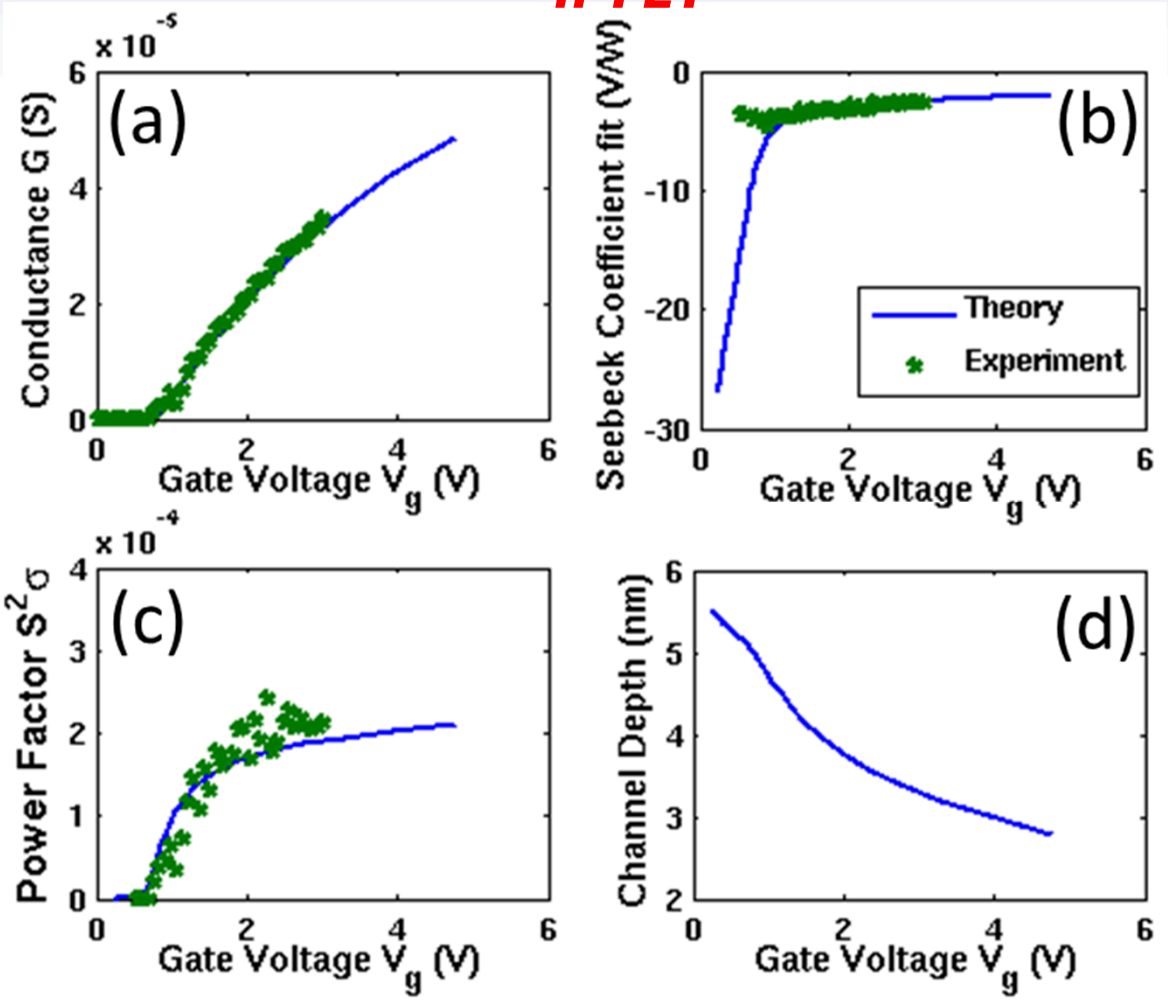




Theory Versus Experiment

How Does the theory Compare with the Experiment?

n-FET



Caveat:

- *Qualitative agreement only at this point*
- *Don't have exact doping numbers*
- *Values scaled until match was found*

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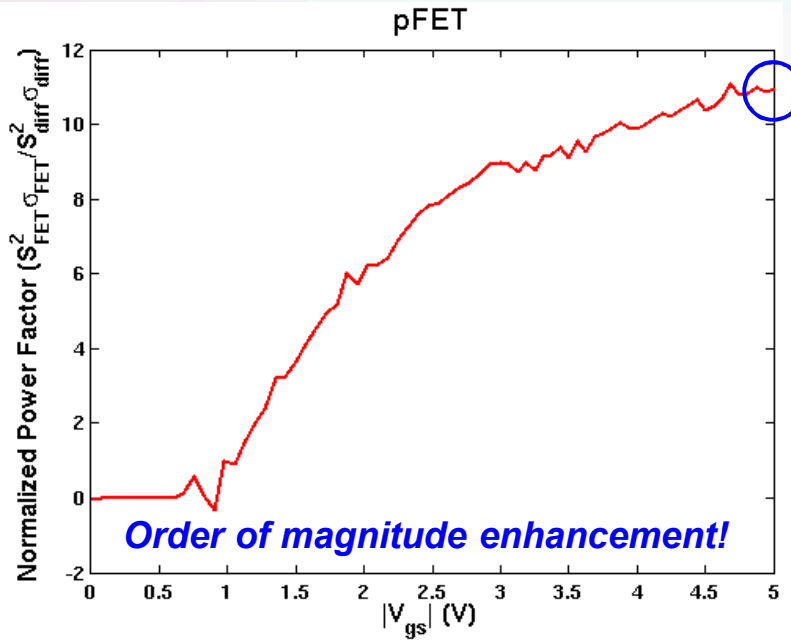
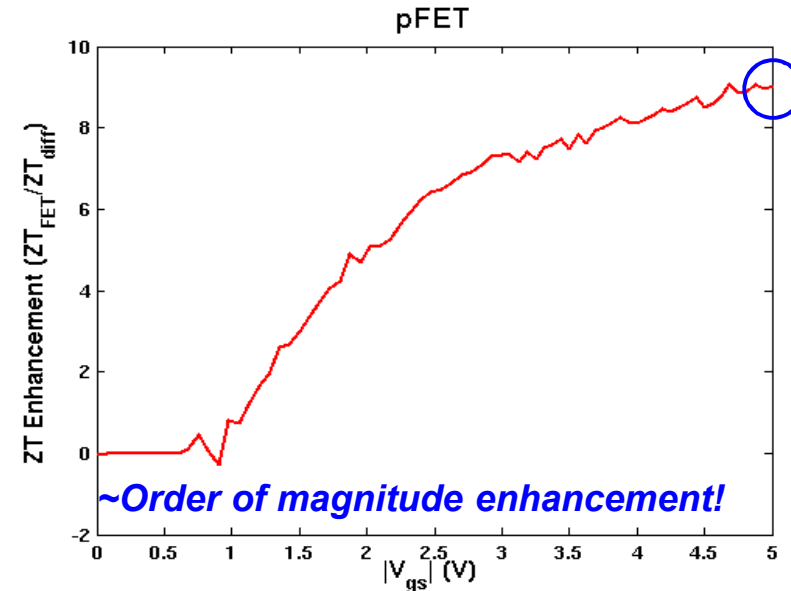
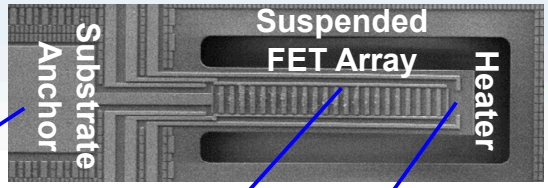
ZT & Power Factor

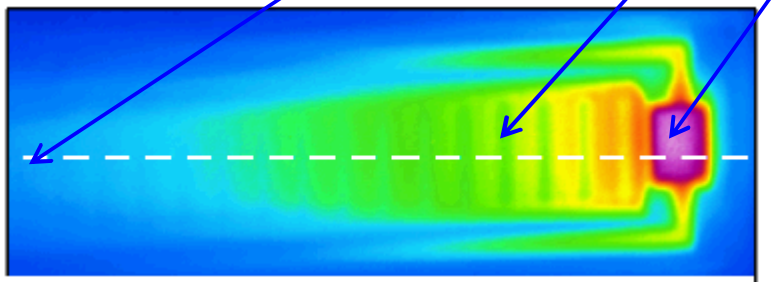
Experimentally Predicted

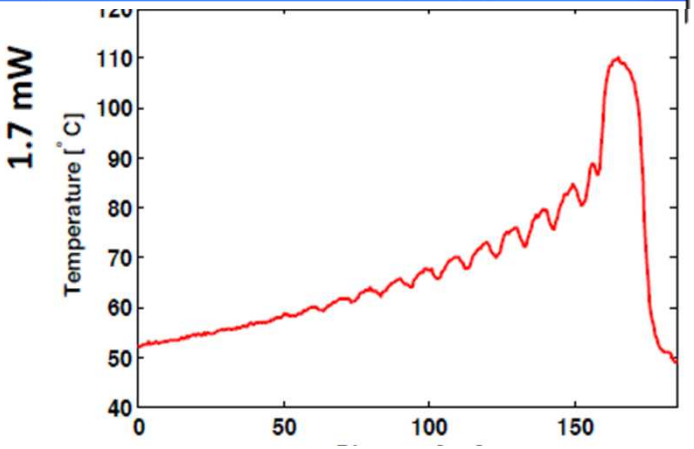




IR-Thermography







Quantitative Measurements:

- *250nm SOI Si-CMOS7*
- *S_{QC} = 400μV/K*
- *κ = 40 W/mK*
- *σ = 5.74e4 S/m*
- *ZT_{room} = 0.08 ↔ $ZT_{Si\text{-}max}$~0.008!*
- *No wafer thinning yet!*

Potential Designs

Possible Temp Control and Cooling Demos

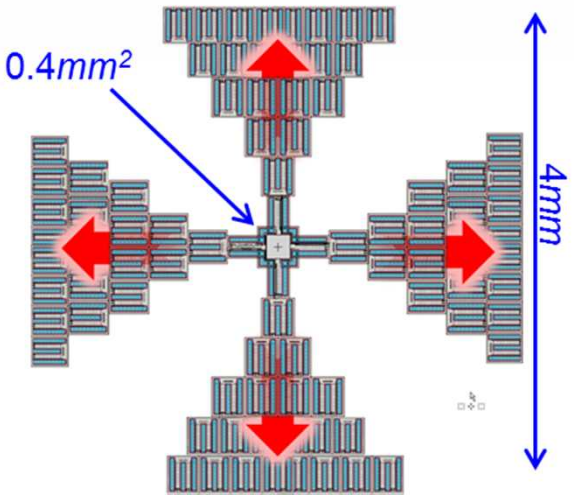
Ongoing Demo Circuits for T (ΔT=0) Control:

- *Resistor Element*
- *Single Diode*
- *Band Pass filter (RC circuit)*
- *Bandgap Reference circuit*
- *Balanced Differential Amplifier circuit*

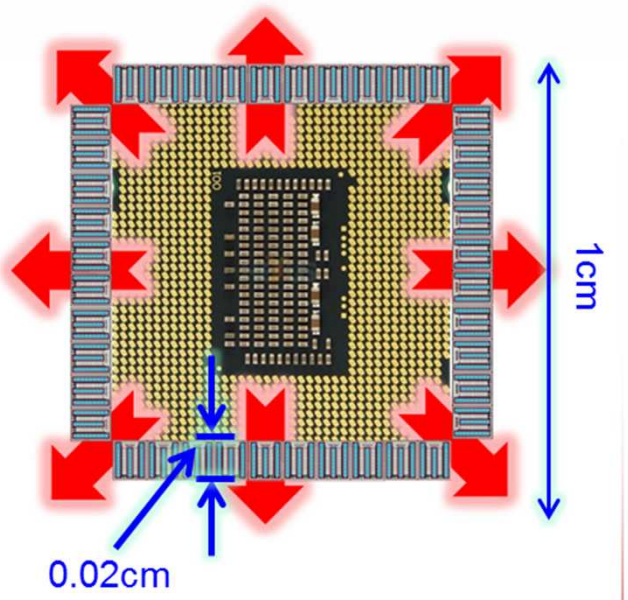
Potential Applications:

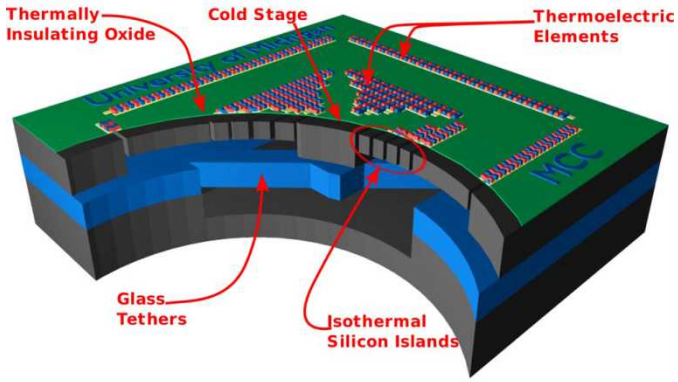
- *Precise T control of islands for memristor applications, e.g. Vanadium Oxide*
- *Uniform T or constant ΔT across a ROIC*
- *Chip Cooling*
- *Energy Generation and Scavenging*

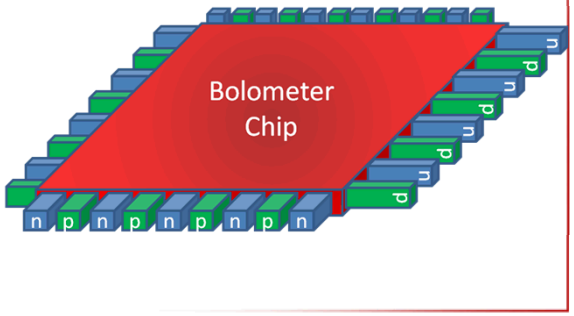
Max ΔT Layout



Heat Pump (ΔT=0) Layout







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Summary & Conclusions

- Measured data confirms QC effects
- ***Non classical*** TE behavior observed for first time!
- Observed ***order of magnitude enhancement*** in Power Factor
- Observed ~***order of magnitude enhancement*** in ZT
- The realization of a new class of TE devices in CMOS compatible platforms including for the ***first time*** Si-based TE devices enabling monolithic integration of TE coolers and scavengers.
- ***First direct demonstration*** of deterministic engineering and optimization of the Seebeck coefficient in a semiconductor material.