In collaboration with MUSIQC

Scalable micro-fabricated ion traps for Quantum Information Processing

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Abstract

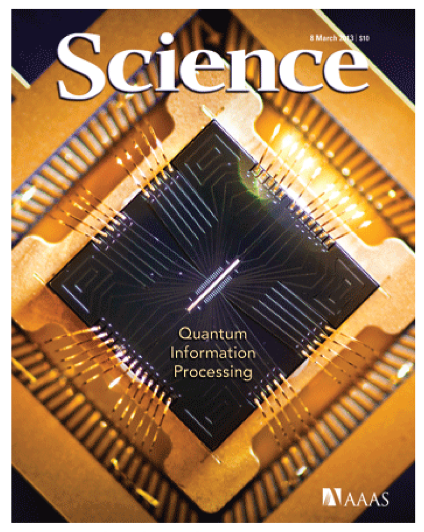
Trapped atomic ions are one of the most promising candidates to realize a quantum information processor. In this bottom up approach to quantum information processing the availability of reliable and scalable trap structures is essential to scale trapped ion quantum information processing to larger systems.
At Sandia National Laboratories, standard silicon fabrication technologies are being used to produce surface ion trap structures.

Here, we present a new chip trap design with excellent optical access both parallel to the surface and perpendicular to the surface. The trap is also optimized to generate high secular frequencies and to provide full control of the principal axes of the trap. Furthermore, we are employing segmented control electrodes close to the ion to achieve sharp control potentials to facilitate separation and combination of ion chains. We present and characterize voltage solutions for single ions, long chains of ions and the splitting and combining of chains of ions.

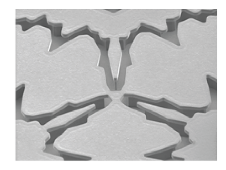
.1mm x50 SE 6/5/2014 1.00

Microfabricated traps for QIP

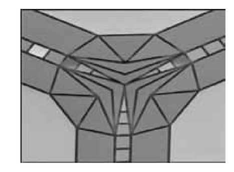
Scalable traps require a two-dimensional array of trapping sites.
Microfabrication is necessary to fabricate scalable traps.
Two-dimensional arrays of traps require junctions and multi-level metallization.



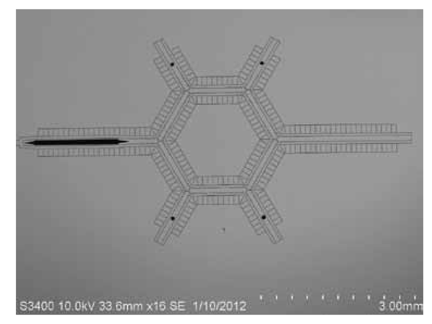
Thunderbird Trap



Y-Junction

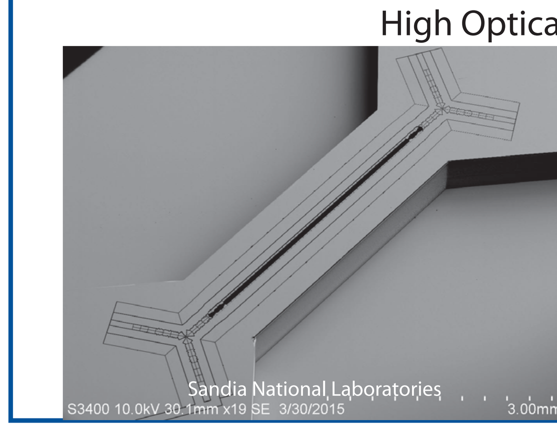


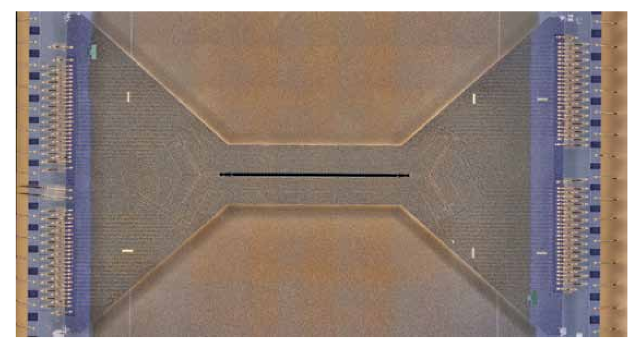
Switchable junction



Y-circulator trap

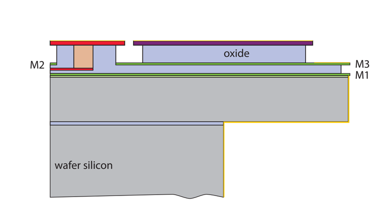
High Optical Access trap (HOA-2)

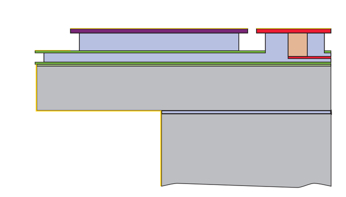


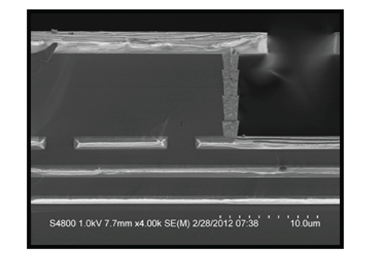


Trap fabrication capabilities

Silicon based fabrication capabilities at Sandia
Four level metallization

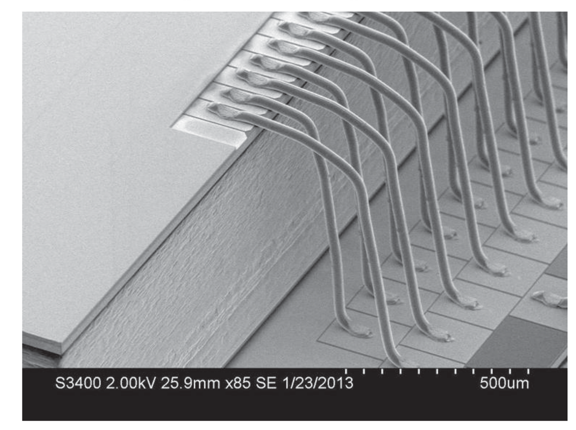




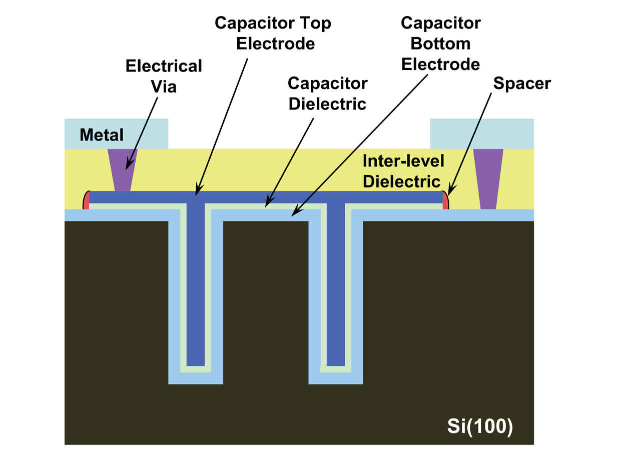


By routing of DC electrodes through lower metal layers, we achieve the following:
- Simplified routing as wiring can now cross in different metal layers
- More complex, islanded trap structures, such as circulators and rings, can be wired
- Eliminates the need to model effects of electrode leads on the trap

Low-profile wire bonds
- Maximal optical access
- Minimizes light scattering

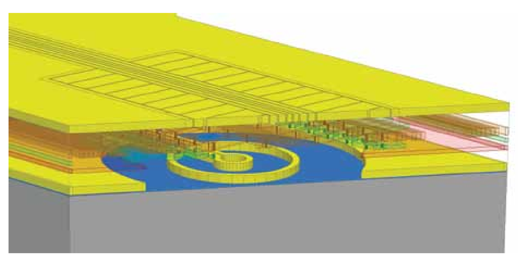


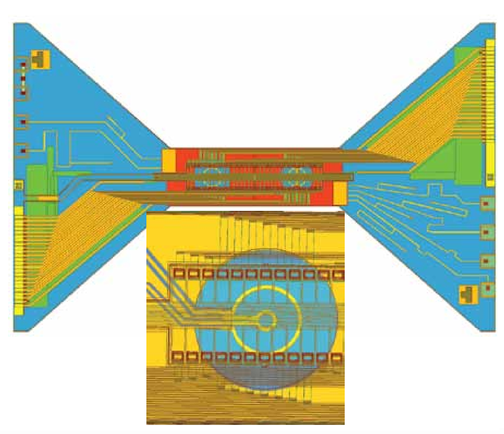
An Interposer chip is used to route the control voltages from two sides of the bowtie shaped trap to the pads of the standard CPGA carrier. Trench capacitors are integrated on the interposer to reduce rf pickup.

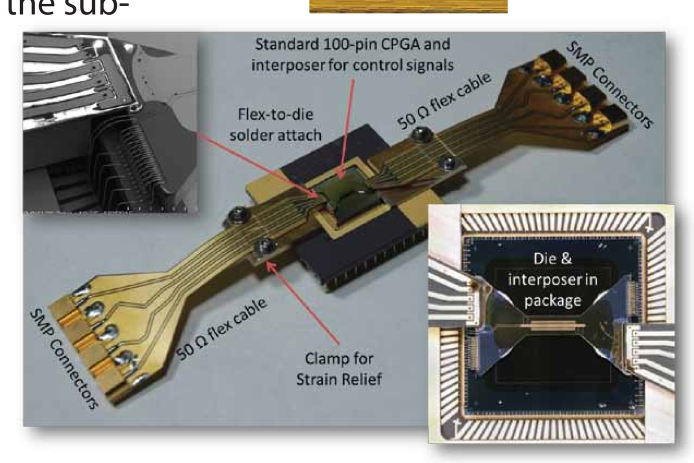


Microwave integrated trap

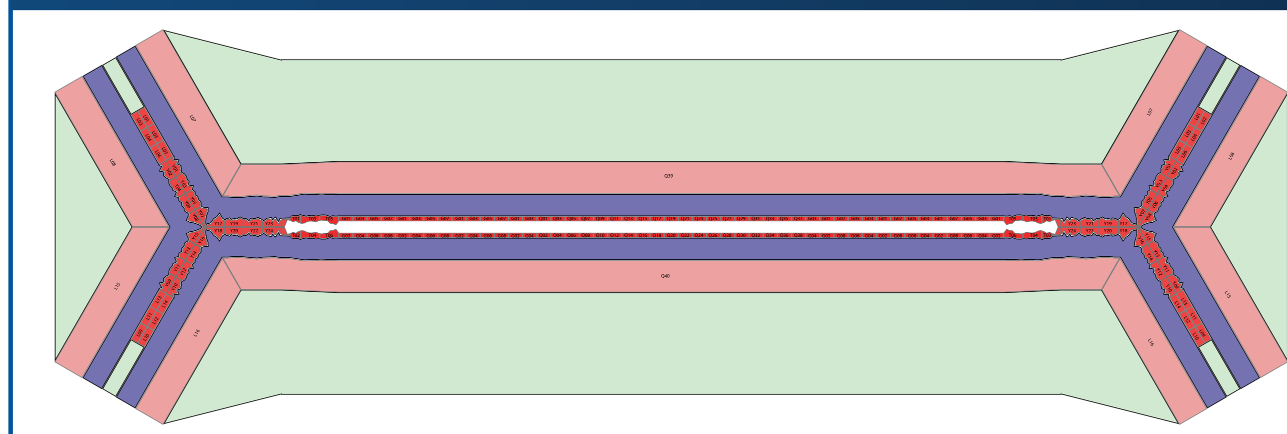
- Microwave structures integrated into the trap without disrupting the top metal.
- Concentric loops enable homogeneous fields as well as gradient fields
- Ion trap structures can be built above microwave structures.
- Magnetic fields couple through slots in the upper metal structures, without line of sight.
- Approach achieves about 60% of magnetic field of bare loops.
- Microwave traces are placed next to the substrate for heat dissipation







High Optical Access Trap



- Linear section and junctions to enable scaling
- High optical access skimming the surface (NA 0.11) as well as through central slot (NA 0.25).
- Transition between slotted and un-slotted regions (2D scalability)
- High trap frequencies to facilitate ground state cooling and quantum gates. Characteristic distance 140µm, closest electrode 96µm.

Trap tested and characterized using Ytterbium and Calcium
- Very good trap performance: lifetime up to 96 h in Ytterbium while taking data
- Lifetime without cooling > 5 min
- Trap frequencies in ytterbium up to 2.6 MHz
- Low heating rates approx. 100 quanta/second
- Shuttling in and out of the slotted area demonstrated

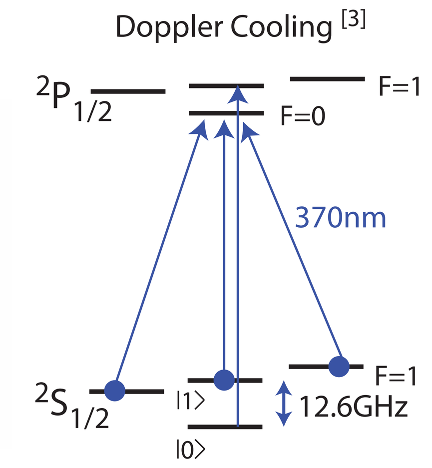
Surface trap with exceptional performance

Gate Set Tomography

The $^{171}Yb^{+}$ qubit

$$\langle\langle E_k | F_i G_l^{2^n} F_j | \rho \rangle\rangle$$

Doppler Cooling [3]

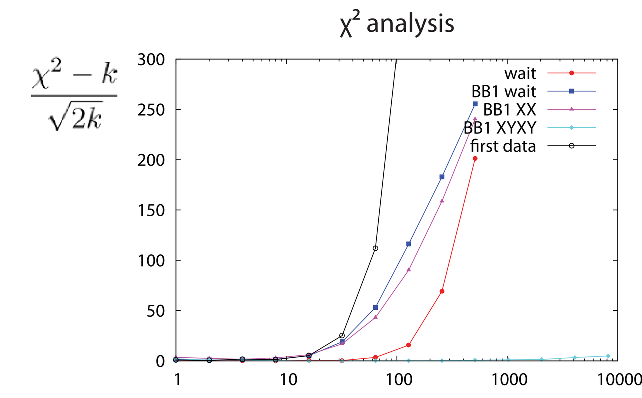


qubit stored in hyperfine clock states

Gate Set Tomography
- No assumptions on gates
- Self-consistent analysis
- Many repetitions of gates enables high precision
- Germs to amplify all possible errors in the process matrix

Gate	Process Infidelity	Trace Dist.	Frobenius Dist.
Gi	0.000063	0.000173	0.000073
Gx	0.000059	0.003411	0.001307
Gy	0.000066	0.003237	0.001191

χ^2 analysis

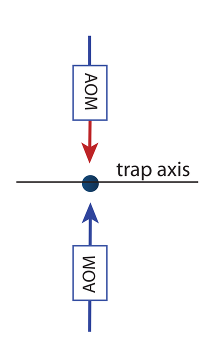


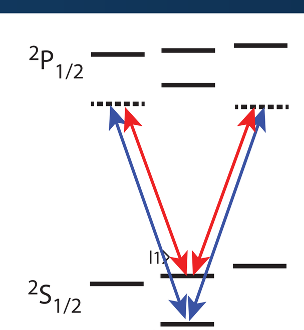
χ^2 analysis (right) shows that GST can fit sequences of any length very well.
This demonstrates that the model of a single qubit describes the experiment very well.

Set	Gates	Identity	Infidelity I	Infidelity G_x, G_y	Trace distance
First ever	direct	wait	7×10^{-4}	2.9×10^{-3}	3×10^{-2}
wait	direct	wait	3×10^{-4}	5×10^{-4}	1×10^{-2}
BB1 wait	BB1	wait	1.7×10^{-3}	2×10^{-4}	0.12
BB1 XX	BB1	XX	1.5×10^{-3}	1.2×10^{-4}	2×10^{-2}
BB1 XYXY	BB1	XYXY	6.2×10^{-5}	6.5×10^{-5}	2.9×10^{-3}

Motional Transitions

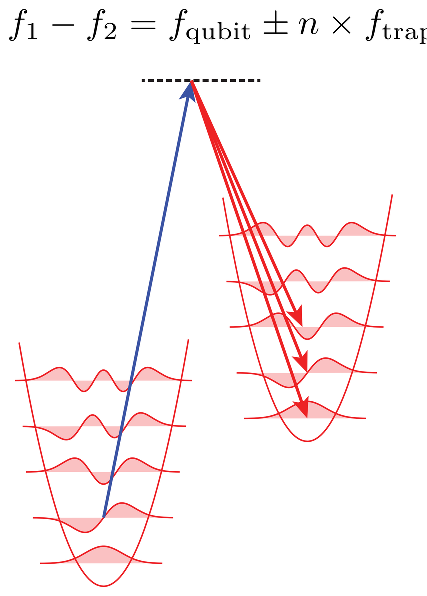
To address the motion of a single ion, the optical frequency comb is split into two beams and sent through the AOMs to tune the relative offset of the two combs.

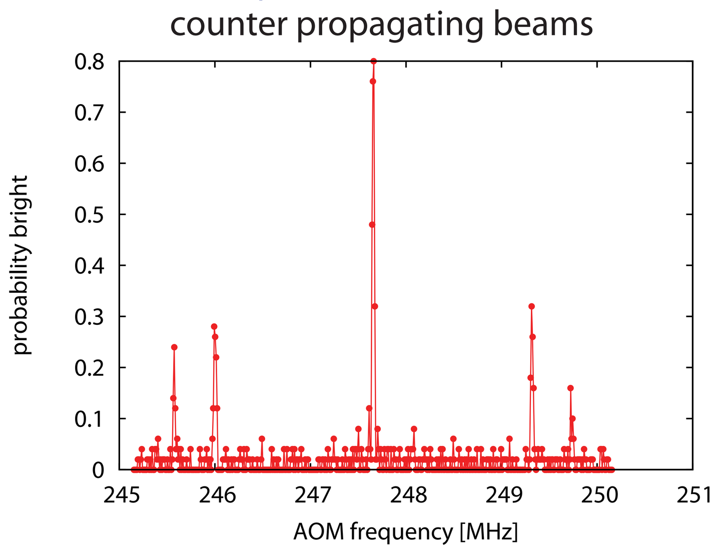




counter propagating beams

$$f_1 - f_2 = f_{\text{qubit}} \pm n \times f_{\text{trap}}$$

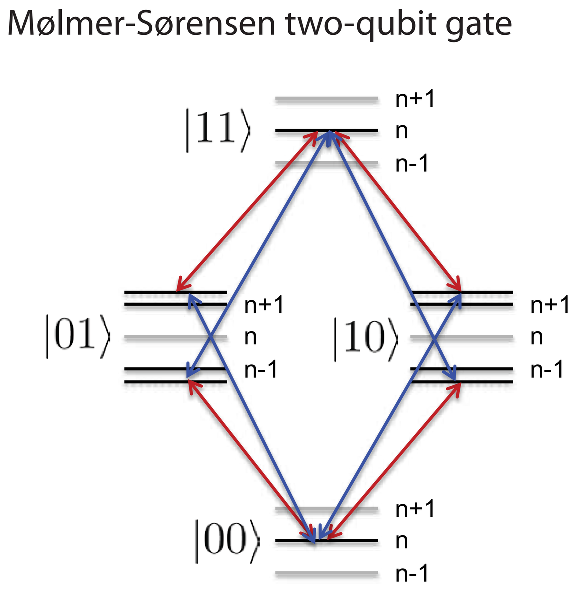




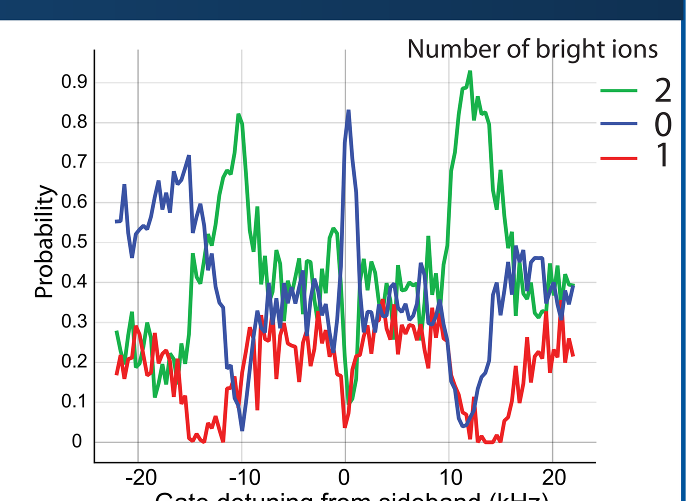
We clearly observe motional transitions at ±1.66 MHz and ±2.06 MHz

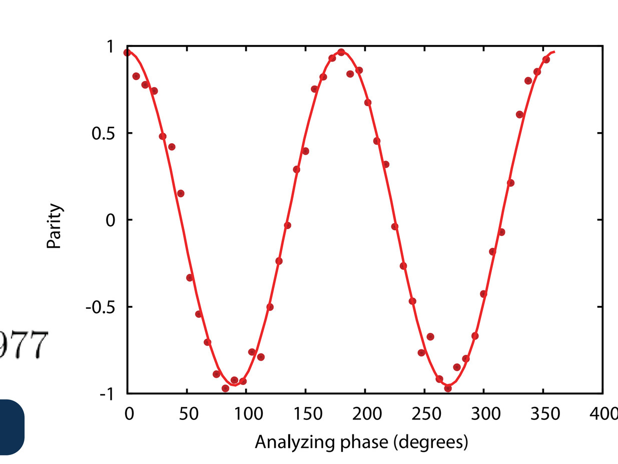
Two qubit gate

Mølmer-Sørensen two-qubit gate



$$|00\rangle \rightarrow |00\rangle + |11\rangle$$





$$\mathcal{F} = \frac{1}{2}(P(|00\rangle) + P(|11\rangle)) + \frac{1}{4}c = 0.977$$

Best gate fidelity in any scalable surface trap

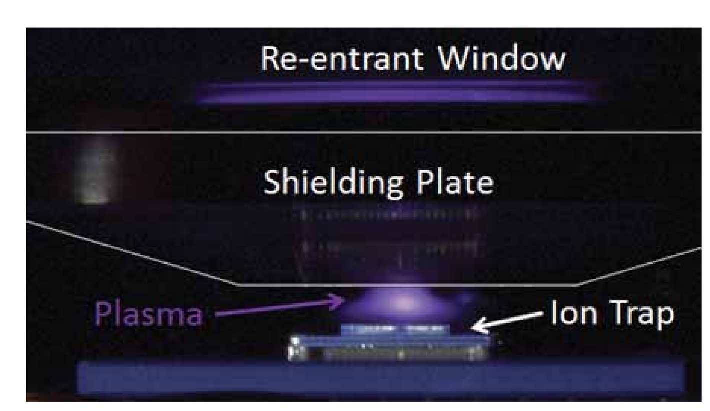
Conclusion & Outlook

Realized and delivered scalable surface traps with exceptional performance

Demonstration of two-qubit gates:

- Shows that traps are ready for quantum information processing applications.
- Demonstrates to performers that they can obtain the trap and the knowledge to operate it successfully for their cutting edge QIP demonstrations
- Allows us to detect and characterize the limitations of the device. This essential knowledge will allow us to further improve the device.
- Collaboration between Sandia's fabrication experts and Sandia's experimental ion trapping experts will lead to further improvements to the devices.

Currently working on:
- Plasma treatment to reduce anomalous heating rate of devices
- Surface pre-treatment (annealing) to reduce heating
- Results will enable trap with lower anomalous heating rates which will be available to IARPA performers.



LDRD LABORATORY DIRECTED RESEARCH & DEVELOPMENT
IARPA BE THE FUTURE

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