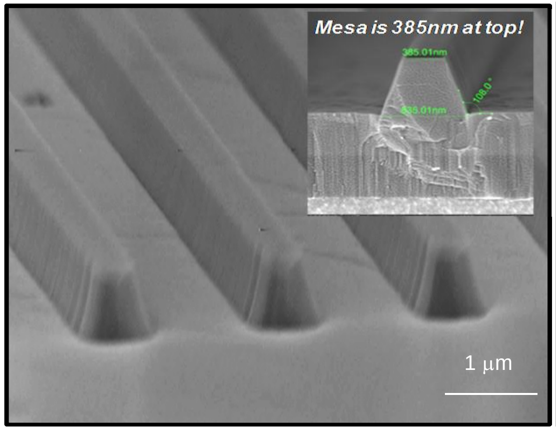
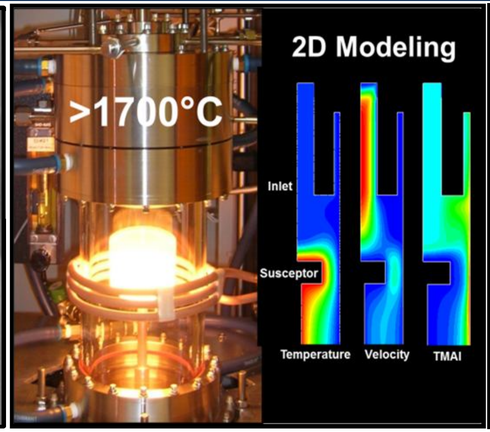
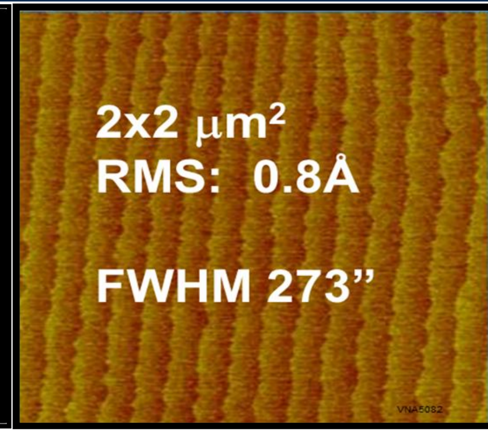
SAND2016-1159PE

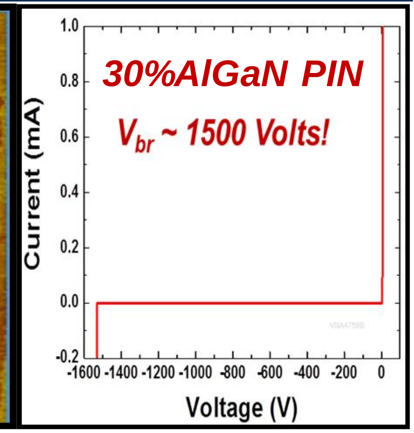
Exceptional service in the national interest

Sandia National Laboratories









Challenges in Epitaxy of Vertical GaN Power Electronics

UWBG ULTRAWIDE BANDGAP POWER ELECTRONICS

Andrew Allerman

Sandia National Laboratories

U.S. DEPARTMENT OF ENERGY | NNSA National Nuclear Security Administration

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

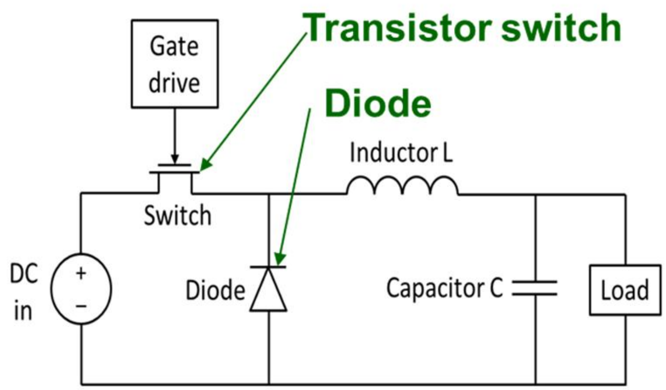
Outline

- **Key devices ➡ Diodes and Transistor Switches**

- **Junction Diodes**
  - Higher voltage
  - Compensation doping
  - Morphology

- **Transistor Switches**
  - Same as diodes
  - P-regions (regrowth, implant)

- **AlGaN PIN diode**



Step-down (Buck) DC-DC converter

Recent GaN PIN Diode Demonstrations

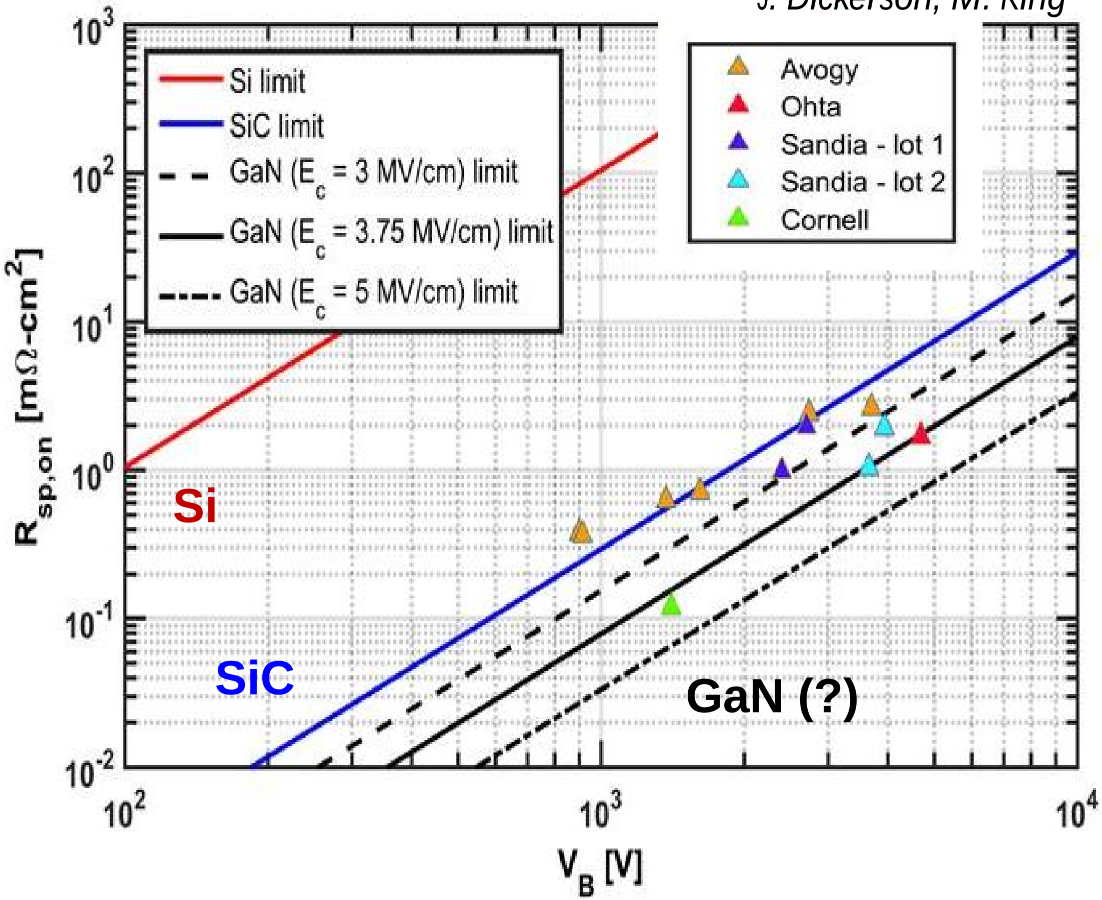
GaN PIN Diodes:

- **Breakdown voltages: 4 - 5kV**
  - Hitachi (4.7 kV)
  - Avogy (> 4 kV)
  - Sandia (3.9 kV)

- **Currents to hundred's of Amps**

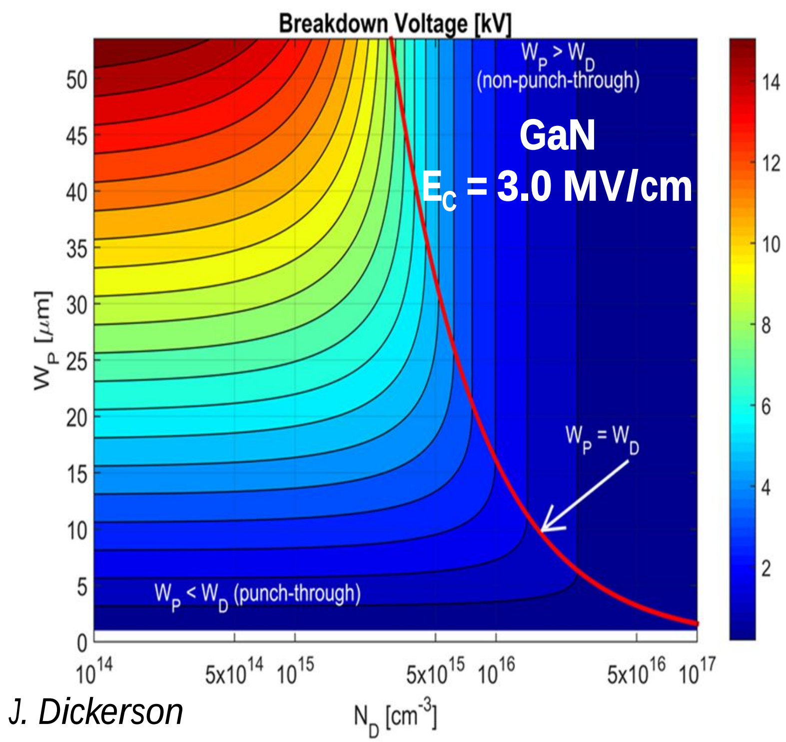
- **Robust avalanche breakdown**

J. Dickerson, M. King



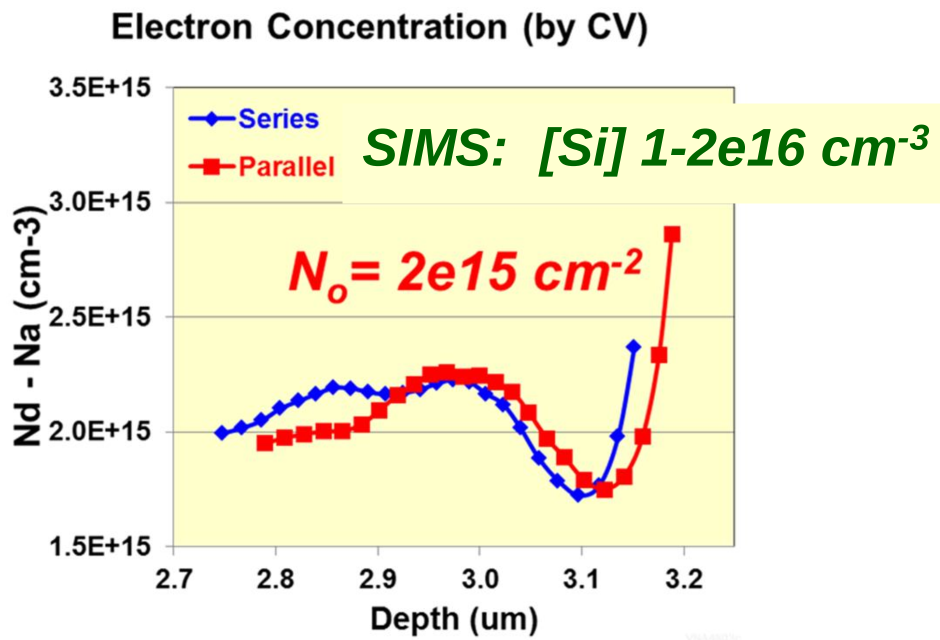
➡ **Early demonstrations of GaN diodes are promising**

Achieving Higher Breakdown Voltages



J. Dickerson

- **Low carrier density (~ 10^{15}) and thick (> 40 μm) drift layers are required for > 5kV breakdown**

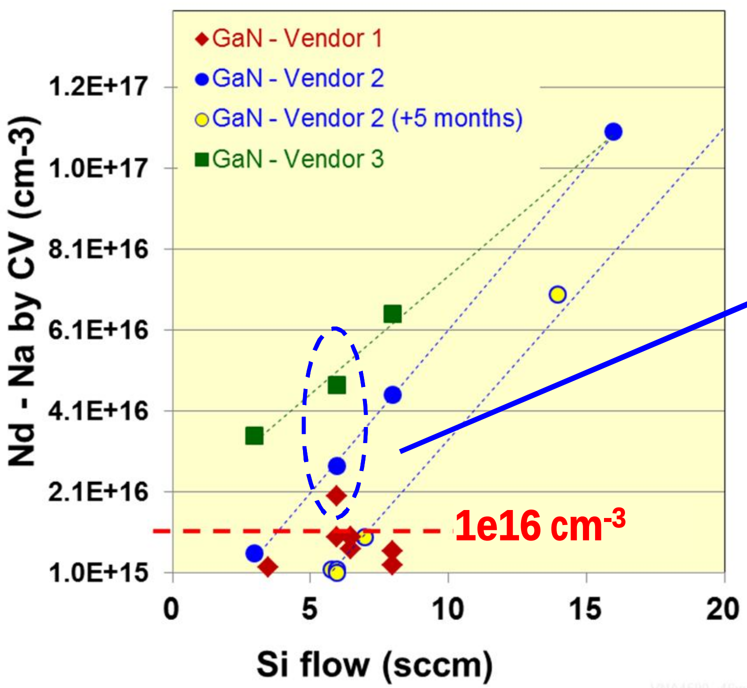


- **High levels of donor compensation.**
  - ➡ **Hard to control $N_o < 1\times10^{16}$ cm^{-3}**
  - ➡ **Variation in diode performance**

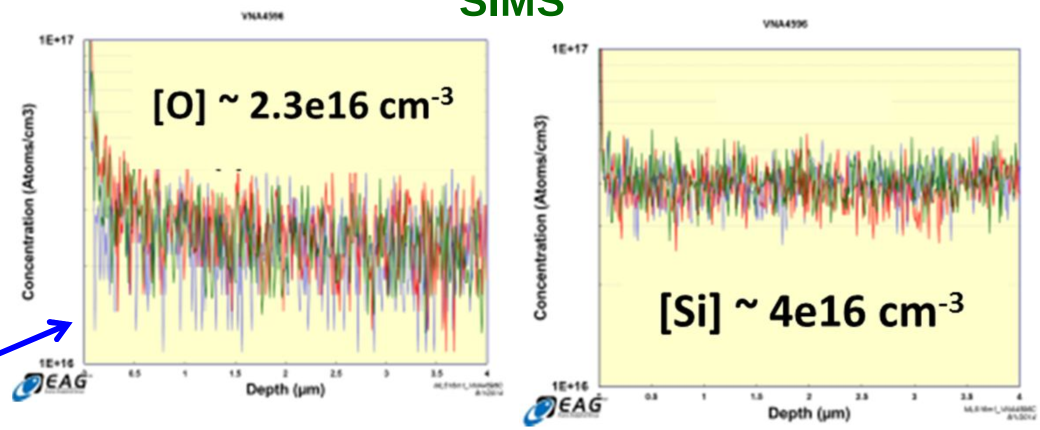
Q: What is responsible for donor compensation?

GaN Substrates and Electron Concentration

Electron concentration vs Si flow

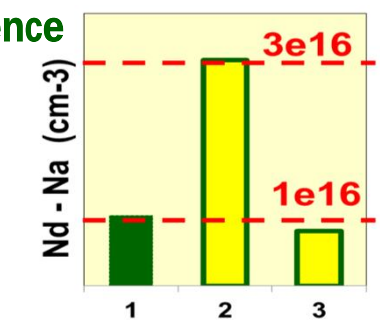


SIMS



- [O] and [Si] are the same for each substrate
- No impurity out-diffusion from substrate

- Three wafers from the same vendor grown in sequence

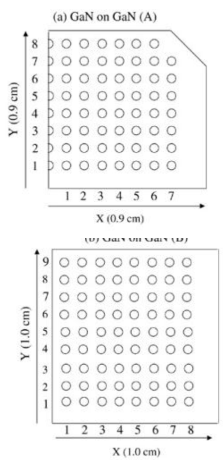


- Linear dependence of N_D-N_A on Si flow but:
  - ➡ Curve depends on vendor of GaN substrate and sometimes varies wafer to wafer from the same vendor

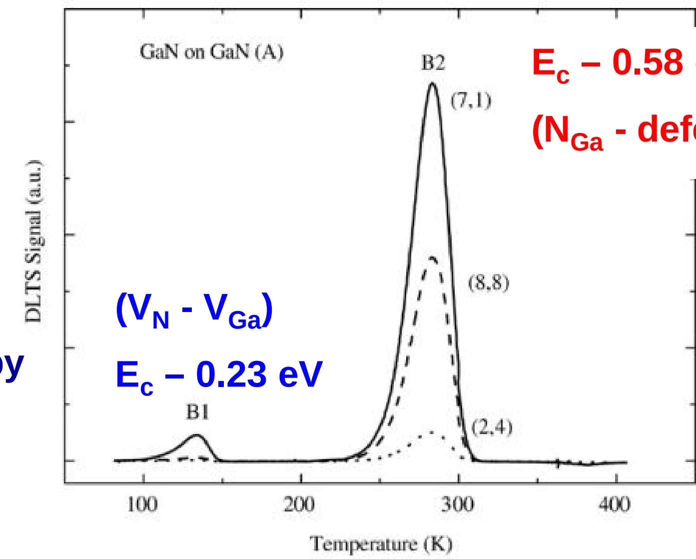
➡ **GaN substrate influences compensation in epi.**

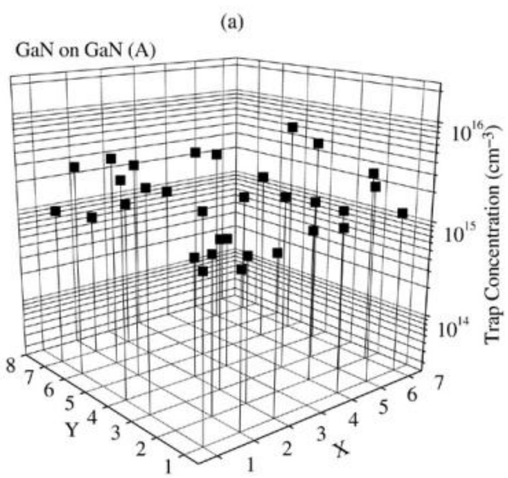
GaN Substrates and Electron Traps

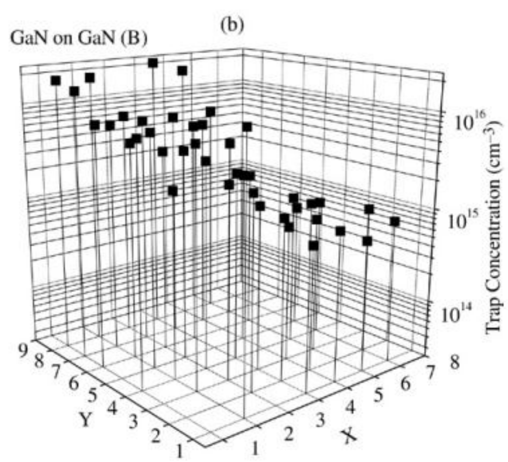
Tokuda, Superlattices and Microstructure 2006



- **5 μm Si GaN (N_o= 5X10^{16} cm^{-3}) grown on GaN substrates from two vendors**
  - **Always observed 2 electron traps by DLTS and the concentration varied. (also in GaN on sapphire)**



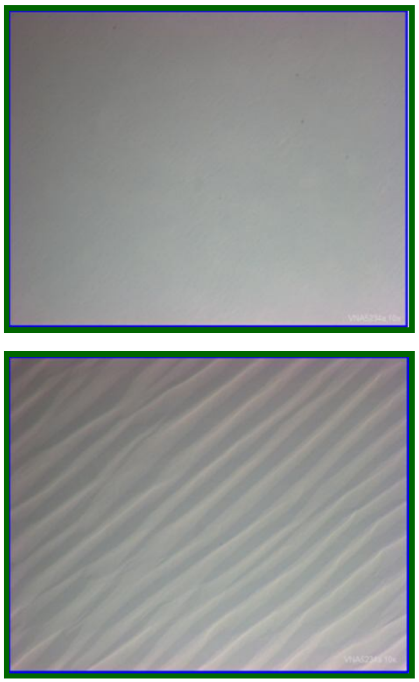




- **[B2] ranged 10^{14} – low 10^{16} cm^{-3}**
- **[B2] varied spatially**

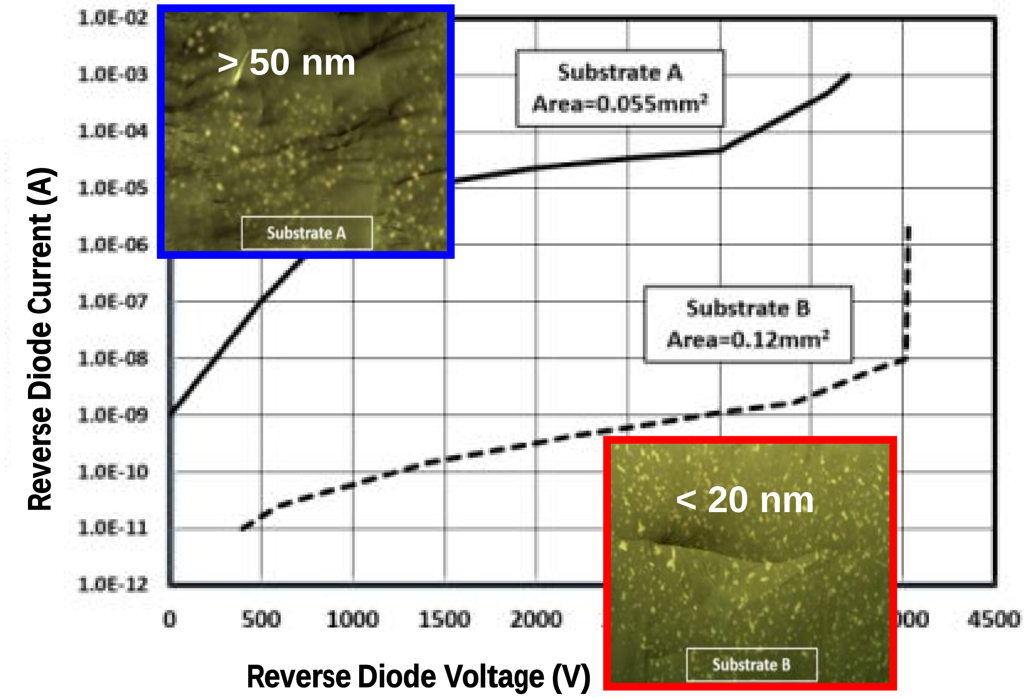
GaN Substrates and Electron Concentration

Nomarski DIC, 10x (SNL)



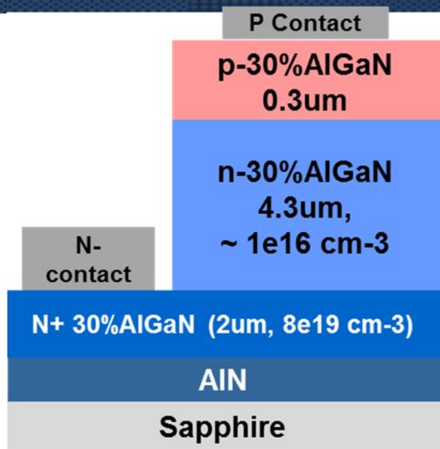
Reverse Diode IV

Kizilyalli (Avogy) EDL 2015

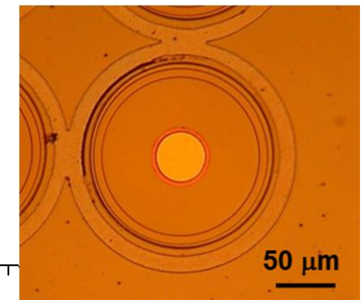


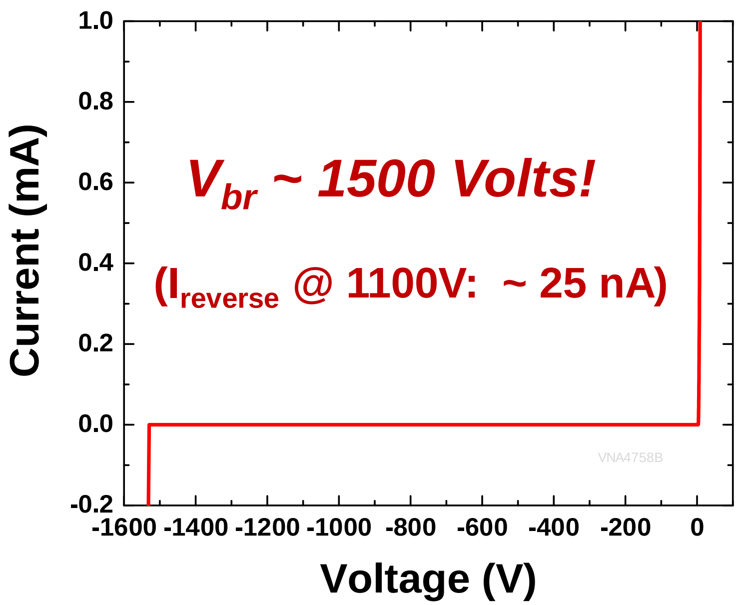
- **Surface morphology epi layer can vary across wafer & wafer to wafer. (SNL)**
- **Rough surfaces and hillocks result in higher reverse leakage current. (Avogy)**
  - ➡ **Wafer mis-cut & growth process are critical for device yield**

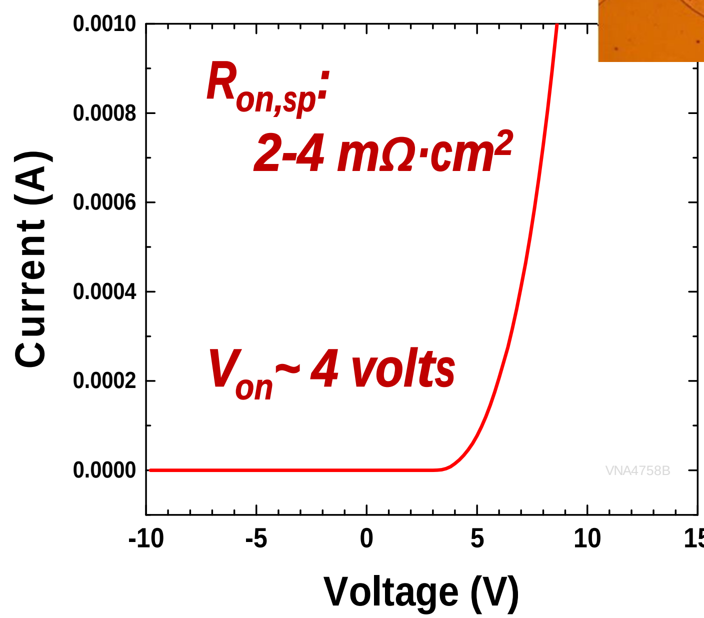
“Quasi-Vertical” $Al_{0.3}Ga_{0.7}N$ PIN diode on sapphire



- Implanted junction edge termination around p-contact
- Drift region: 4.3 μm, N_o~ 1e16 cm^{-2}, μ ~ 150 cm^2/Vs
- Dislocation density: 1-2e9 cm^{-2}
- On wafer testing in Fluorinert (150 μm dia.)

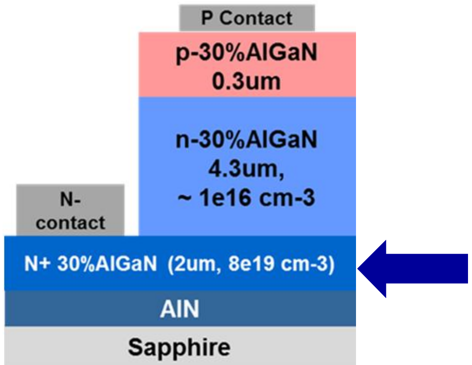






➡ First report of kilovolt class AlGaN PIN diode

"Quasi-Vertical" $Al_{0.3}Ga_{0.7}N$ PIN diode on sapphire



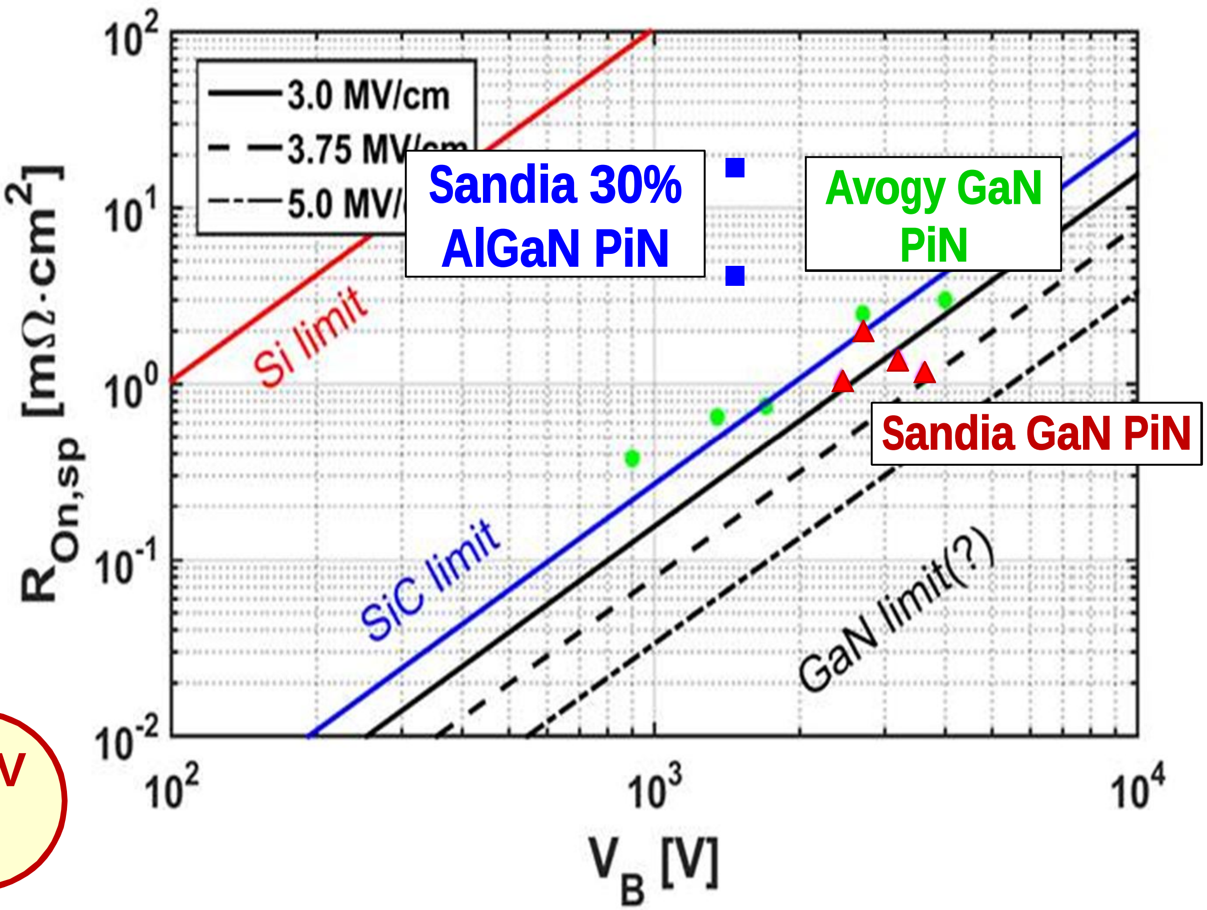
- **On resistance is high due to thin current spreading layer**
- **For N_d = 1e16 cm^{-2}, 4.2 μm**

GaN: V_{br} ~ 1200 – 1500 V

($3.0 < E_{crit} < 3.7$)

➡ $Al_{0.3}Ga_{0.7}N$ with V_{br} ~1500V is near limit for GaN

Unipolar Figure of Merit:
Specific on resistance vs breakdown voltage



Summary

- **GaN substrates need to improve ➡ device yield & performance**
  - Spatial uniformity and wafer-to-wafer
  - Control of mis-cut and epi-morphology
  - Breakage

- **Understand origins of donor compensation**
  - Role of substrate
  - Growth conditions and impurities