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Heterogeneous Integration of III-V Photonics and Silicon Electronics for Advanced Optical Microsystems

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Abstract: *The dense integration of compound semiconductor photonics and silicon microelectronics leads to significant reductions in system size, weight, and power, while simultaneously yielding performance improvements and new functionality. This paper describes several advanced optical microsystems developed at Sandia National Laboratories that combine custom III-V semiconductor optoelectronics with silicon microelectronics, and discusses the relevant integration technologies in detail.*

Keywords: heterogeneous integration; photonics; microelectronics; compound semiconductors; flip-chip; VCSEL; interconnect; optical microsystems.

Introduction

Optical microsystems represent the miniaturization of conventional electro-optical systems through hybrid integration techniques. Notable applications of interest to government customers include optical sensing and high-speed communications. While silicon is a critical material for advanced microelectronics, most high-performance active photonics devices (i.e., lasers, modulators, and detectors) are based on compound semiconductors. Hence, optical microsystems typically require hybrid packaging to realize the benefits of microscale system integration.

This paper addresses heterogeneous integration processes developed at Sandia National Laboratories to combine electronics and photonics technologies, and highlights recent examples of optical microsystem prototypes created from III-V semiconductor photonics and silicon CMOS circuits. In particular, we describe the integration and performance of a low-power optical interconnect prototype designed to boost bandwidth density by an order of magnitude for future high-performance systems. The system combines GaAs vertical-cavity surface-emitting lasers (VCSELs), InGaAs photodiodes on InP, and advanced silicon CMOS circuits through die-level hybrid integration.

Electronic/Photonic Integration

Almost all optical systems that combine semiconductor-based optoelectronics with silicon circuitry (for control, drive, or read-out functions) can be improved by higher integration density. Most photonics applications are sensitive to cost, size, weight, and power, and system designers have begun moving from component packaging at the circuit board level to more aggressive 2D assembly techniques. However, even with custom interposers and advanced packaging, optical systems still typically place silicon microelectronics and compound semiconductor photonics merely "near" one another, using conventional 2D layouts to achieve modest reductions in wiring lengths. Denser 3D heterogeneous integration is seen as the next step to achieve higher levels of system performance.

Heterogeneous Integration Methods: We have developed several approaches to high density integration of photonics and electronics, both at the wafer scale and at the die level. At the wafer level, monolithic integration has been used to combine silicon photonic components with electronics using our in-house CMOS and silicon photonics capabilities [1]. Sandia also fabricates advanced compound semiconductor photonic integrated circuits (PICs) which combine active and passive optical and electrical elements through a monolithic fabrication process on InP [2]. Hybrid integration on the wafer scale has been performed using dielectric bonding to combine silicon CMOS electronics with silicon detector arrays [3], and to combine silicon and III-V materials for multi-junction solar cells.

At the die and chip level, we create hybrid photonic microsystems using high-density flip-chip bonding processes. This flexible approach to 3D integration allows the use of state-of-the-art CMOS circuitry (often obtained in die form from 12" wafers) without necessitating customization of the CMOS process flow or access to full wafer runs. Our tight pitch flip-chip techniques were originally developed for infrared focal plane array (FPA) assembly, in which 2D compound semiconductor detector arrays are attached to silicon read-out integrated circuits (ROICs) on a per-pixel level. In a similar fashion, one can

attach high-speed optoelectronic devices such as modulators, VCSELs, and photodiodes directly to silicon electronics using solder microbumps, effectively eliminating the electrical transmission lines needed in conventional 2D packaging. This approach allows higher integration density, faster data rates, and lower power consumption.

Integration process steps are generally performed following standard CMOS and photonic fabrication is complete. Solder dams, underbump metallization, and microbump definition can take place at the wafer level, or on individual die following singulation. Figure 1 shows an array of ~10µm microbumps on a silicon IC prior to integration. Depending on the application, microbump material choices include gold, indium, eutectic alloys, and various lead-based and lead-free solders. Underbump barrier layers are employed to prevent the formation of unwanted intermetallics.

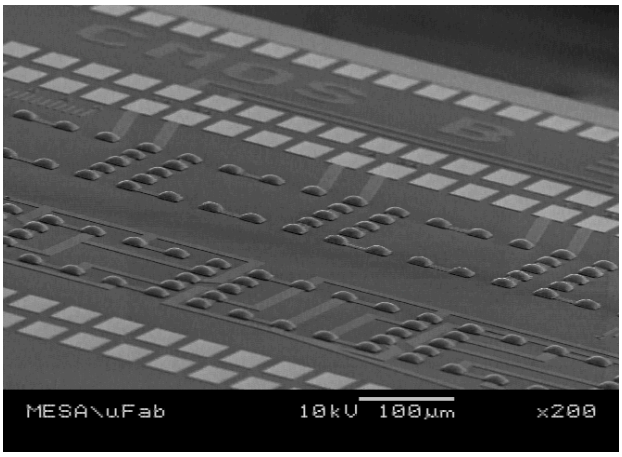


Figure 1. Silicon test chip with gold-tin microbumps prior to flip-chip integration. The bump pitch is 50µm.

Custom photonic devices are designed, fabricated, and diced in-house for flip-chip bonding to active circuitry. Waveguide devices and bottom-emitting/backside-illuminated components are commonly employed in order to place electrical connections and optical access on opposite sides of the die. Bonding accuracy is on the order of +/-1µm, but most microsystems have used bump pitches of 20µm or greater. This pitch allows high yields despite the differing coefficients of thermal expansion between silicon and III-V materials, and is typically similar in scale to the footprint of the optoelectronic devices.

Optical Microsystem Prototyping: Numerous national security applications call for custom photonics technologies, and hybrid microsystem integration can be critical to achieving target performance metrics. Areas that rely on III/V-Si hybrid integration include infrared imaging systems, photonic microsensors, and optical interconnects for data centers and computing systems. The accompanying presentation will discuss work in each area. Below, we focus briefly on the design and performance of a recent optical interconnect demonstrator, which serves as an exemplar electronic/photonic integrated system.

Low-Power High-Bandwidth Optical Interconnects

The explosive growth of internet traffic continues to drive the development of optical data communication technologies. High-speed silicon photonics transceivers [4] and parallel optics modules based on VCSEL components [5, 6] are used in data centers, servers, and high performance computers, where computation, data storage and switching, and interconnection are all critical tasks. Bandwidth density and energy dissipation are the key metrics that limit interconnect performance in these applications today. Here, we aim to boost interconnect bandwidth density by an order of magnitude over current levels using several technological innovations: 980-nm bottom-emitting VCSELs, flip-chip integration with 45-nm and 32-nm CMOS, and coupling to multi-core optical fiber arrays. Figure 2 shows a packaging schematic of the demonstration system, which places high-speed optical I/O directly on the CMOS IC using hybrid integration.

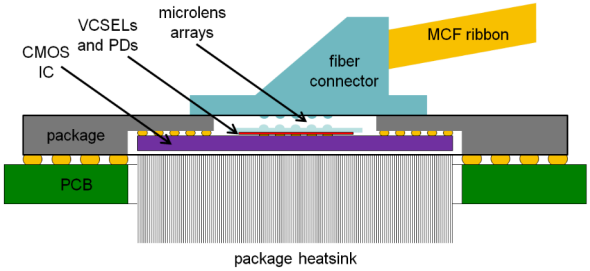
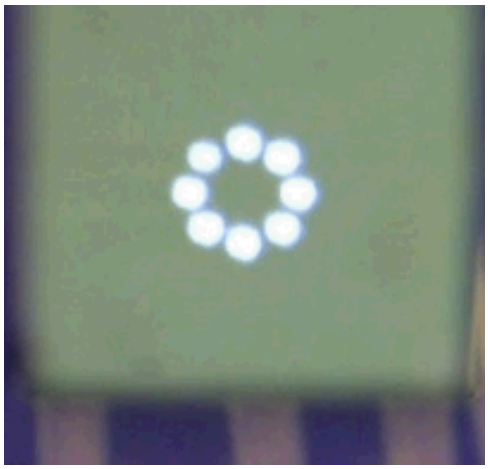


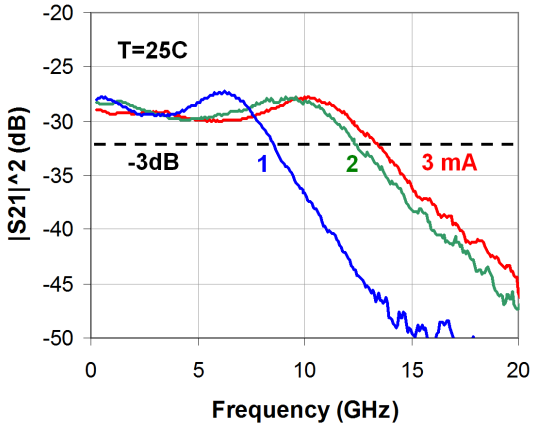
Figure 2. Package schematic of the optical interconnect demonstrator, which incorporates VCSELs, photodiodes, micro-optics, multi-core fibers, and advanced silicon CMOS.

Components and Integration: CMOS circuits, including VCSEL drivers and photodiode receivers, were designed and fabricated using 45-nm and 32-nm technology. Signaling rates of 10 and 20 Gbps were targeted, with a goal of simultaneously optimizing for energy dissipation and bandwidth density; higher bitrates come at the expense of greater power dissipation. Following CMOS fabrication, post-processing steps were performed to allow hybridization with III-V photonics.

980nm bottom-emitting VCSEL arrays fabricated on GaAs are used as optical transmitters. These components were laid out for flip-chip integration with CMOS and compatibility with multicore optical fibers. Devices incorporate strained InGaAs quantum wells for high bandwidths at low drive currents. Modified fabrication processes were used to achieve the required device and wiring density. Figure 3 shows an array of eight lasers following flip-chip integration, along with their frequency response at various drive currents.



(a)



(b)

Figure 3. (a) Laser emission from VCSELs within a bonded array. (b) VCSEL frequency response at low drive current.

InGaAs photodiodes were fabricated on InP with layouts similar to that of the VCSEL arrays. Figure 4 shows detectors prior to integration. Each element has independent anode and cathode connections to the CMOS circuitry through flip-chip bumps at the periphery. Device arrays are repeated on a 250µm pitch, permitting the use of 2D fiber arrays for highly parallel optical I/O. Following integration, detectors achieved ~90% quantum efficiency, sub-nA leakage, and >40 GHz bandwidth at 1V bias.

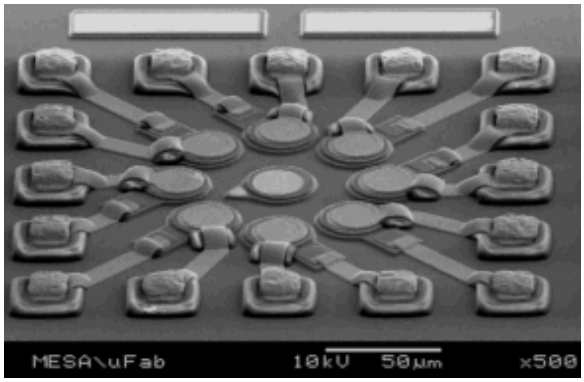


Figure 4. Backside illuminated InGaAs photodiodes on InP. Detectors are 20µm in diameter with topside contacts leading to flip-chip microbumps.

System Performance: Following heterogeneous integration, CMOS ICs were packaged for high-speed optical and electrical probing. Figure 5 shows an integrated receiver with InP chip attached to the silicon microelectronics. Transmitters and receivers were tested independently and together to quantify performance. Figure 6 shows receiver test results from the 45-nm CMOS design. Error-free (equipment-limited) operation up to 12.5 Gbps was demonstrated, with receiver energy dissipation measured to be only 260 fJ/bit at 10 Gbps.

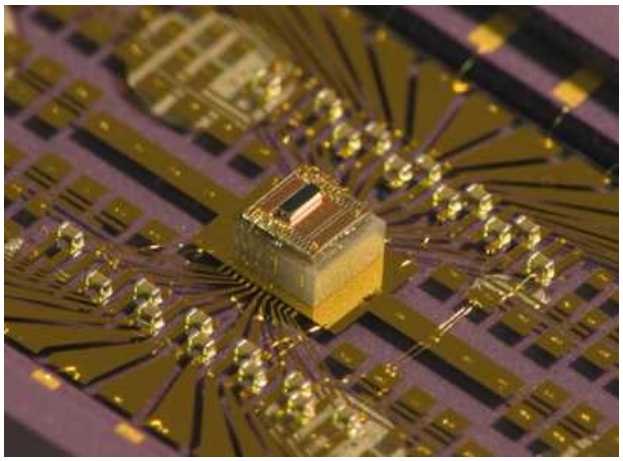


Figure 5. CMOS IC with integrated InGaAs photodiode arrays used for optical interconnect system testing. Only a small portion of the 4mm^2 IC is used to provide 24 optical channels, yielding high data bandwidth density.

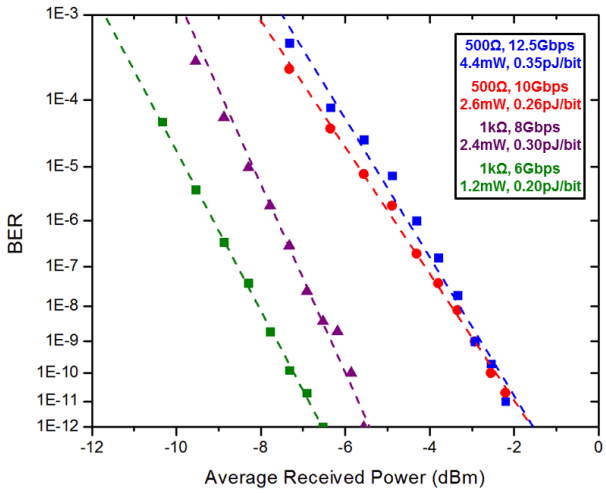


Figure 6. Measured receiver performance, demonstrating the low power dissipation that results from microsystem integration.

Summary

Heterogeneous integration of silicon microelectronics and III-V photonics will enable next-generation optical microsystems for national security applications. We address relevant integration details and resulting system operation of optical microsensors, infrared imagers, and optical interconnect demonstrators.

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