Establishing a Ti-Cu-Pt-Au Thin Film Conductor on Low-Temperature, Co-Fired Ceramic (LTCC) for High Temperature Electronics

P. Vianco, J. Rejent, M. Grazier, B. McKenzie, A. Allen, and A. Kilgo,

Sandia National Laboratories*
Albuquerque, NM 87185
Contact: ptvianc@sandia.gov

E. Guerrero and W. Price

National Security Complex
Kansas City, MO

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Introduction

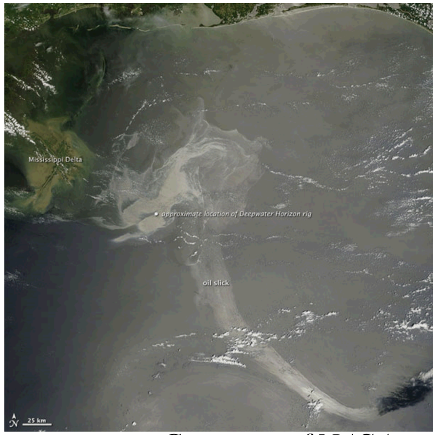
- The development and operational sustainment of down hole **renewable (geothermal)** and **non-renewable (fossil fuel)** energy resources will be subjected to increasingly higher costs factors:

Courtesy of Dept. of Energy

Site preparation ($B)

Courtesy of Dept. of Energy

Site operations ($M/day)



Courtesy of NASA

Liability ($B)

Introduction

- Placing sensor electronics directly down hole can significantly improve both the efficiency and the reliability of well production.

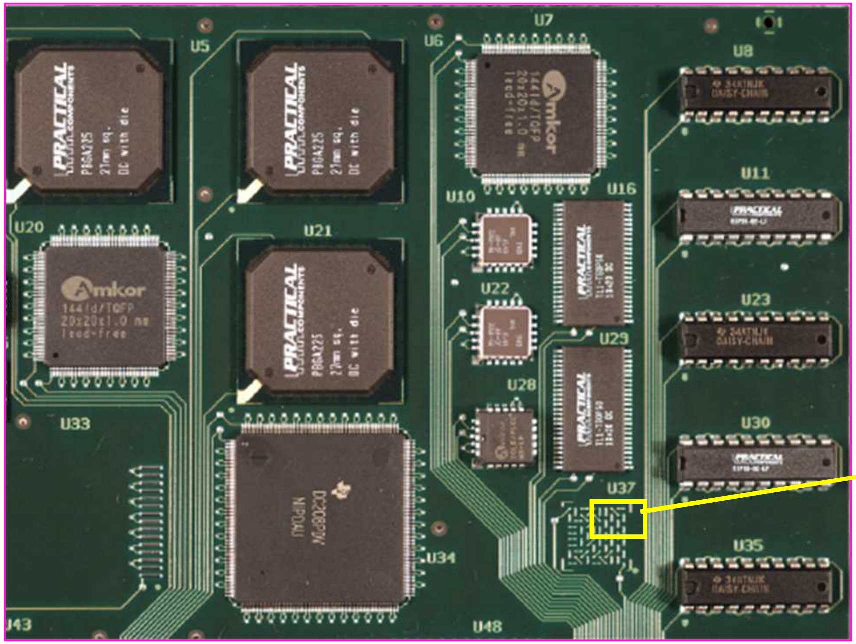
- Oil, gas, and geothermal wells present some of the harshest service conditions for electronics and electrical equipment.

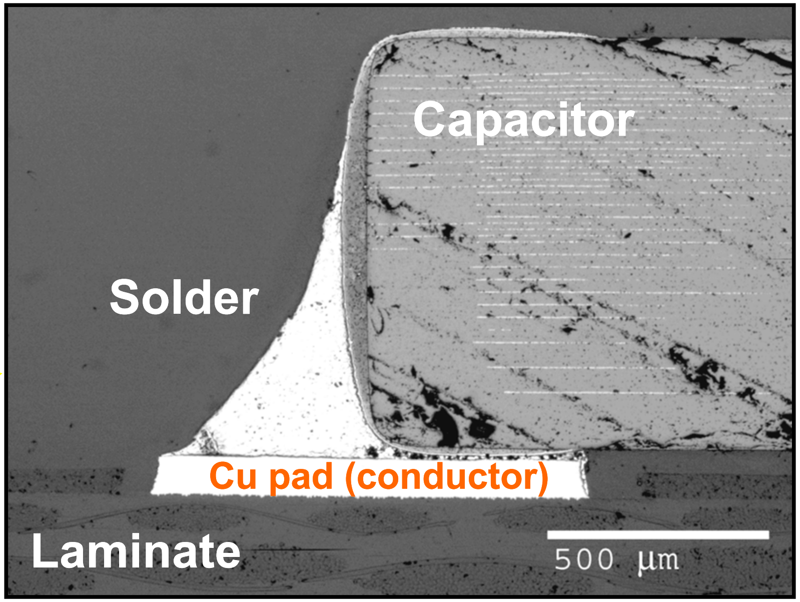
  - Temperatures: 300°C continuous; 350°C peak
  - Pressures: 15,000 to 30,000 psi
  - Vibration: PDS (g^2/Hz), 0.01 – 0.1 (0.6 – 3 kHz)
  - Corrosion: H_2S and H_2 gas, brine, and superheated steam.

Courtesy of Sandia National Labs.

Introduction

- **Electronic packaging is becoming the enabling technology for high temperature electronic systems.**

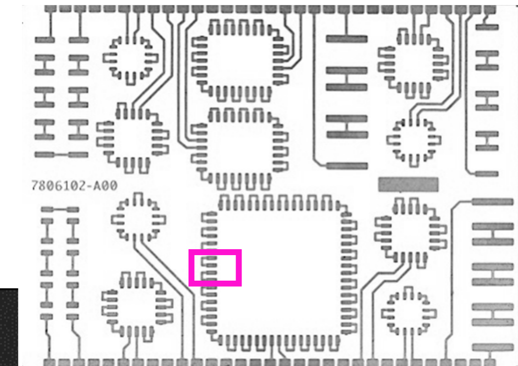


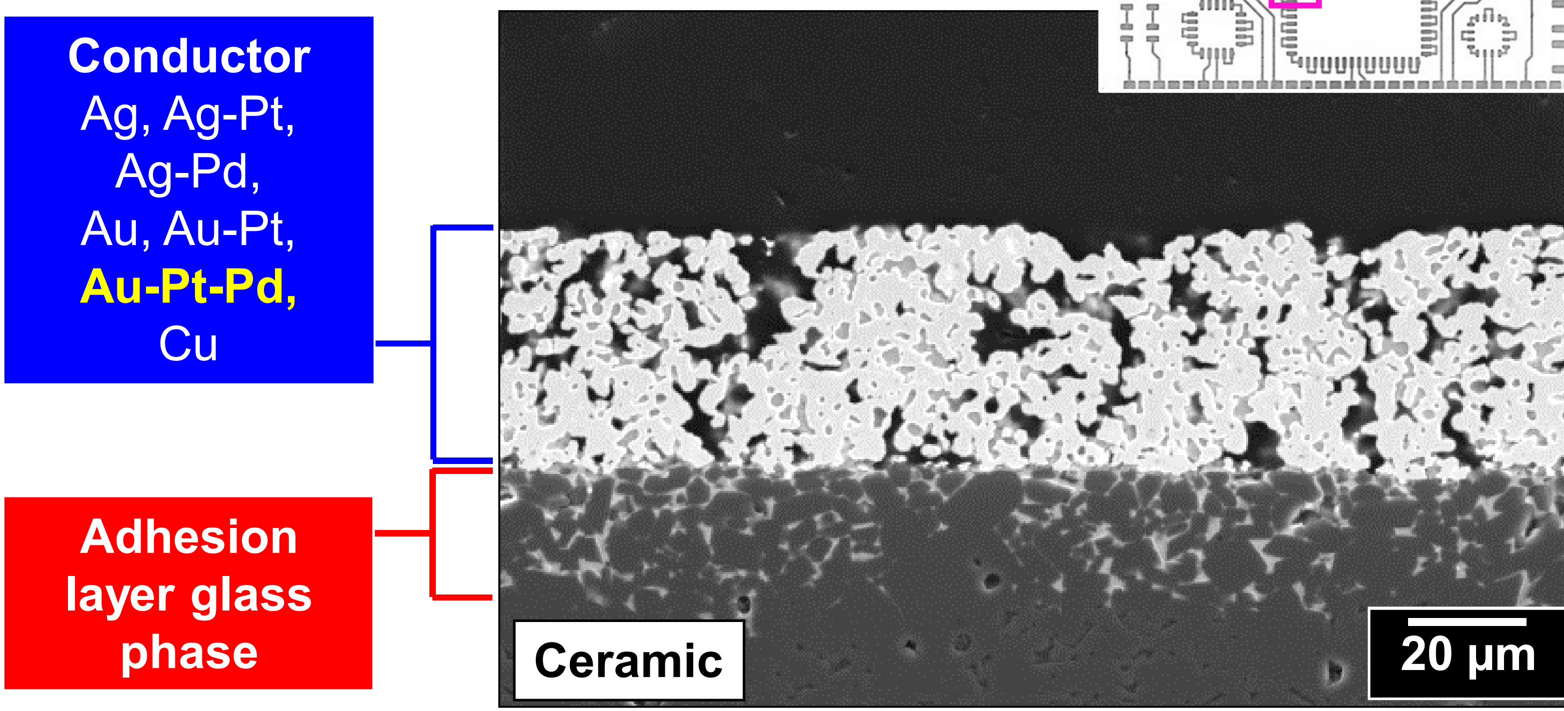


- **Organic laminate technologies are reaching their mechanical and temperature limitations under such operating conditions.**

Introduction

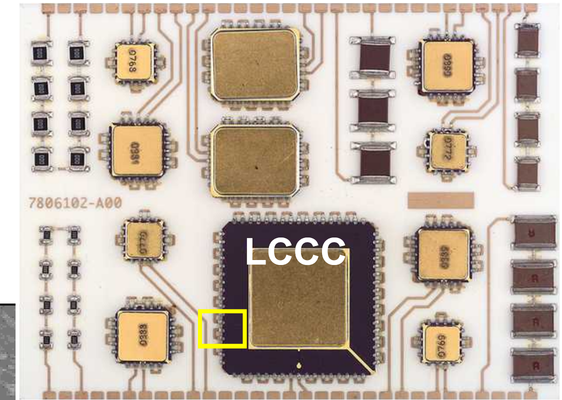
- **Ceramic substrates** have the capacity to extend the operational range of electronics into down-hole applications.
- **Hybrid Microcircuit (HMC)** assemblies are based on an **alumina ceramic substrate** and ***fired* thick film (conductor) circuit**.

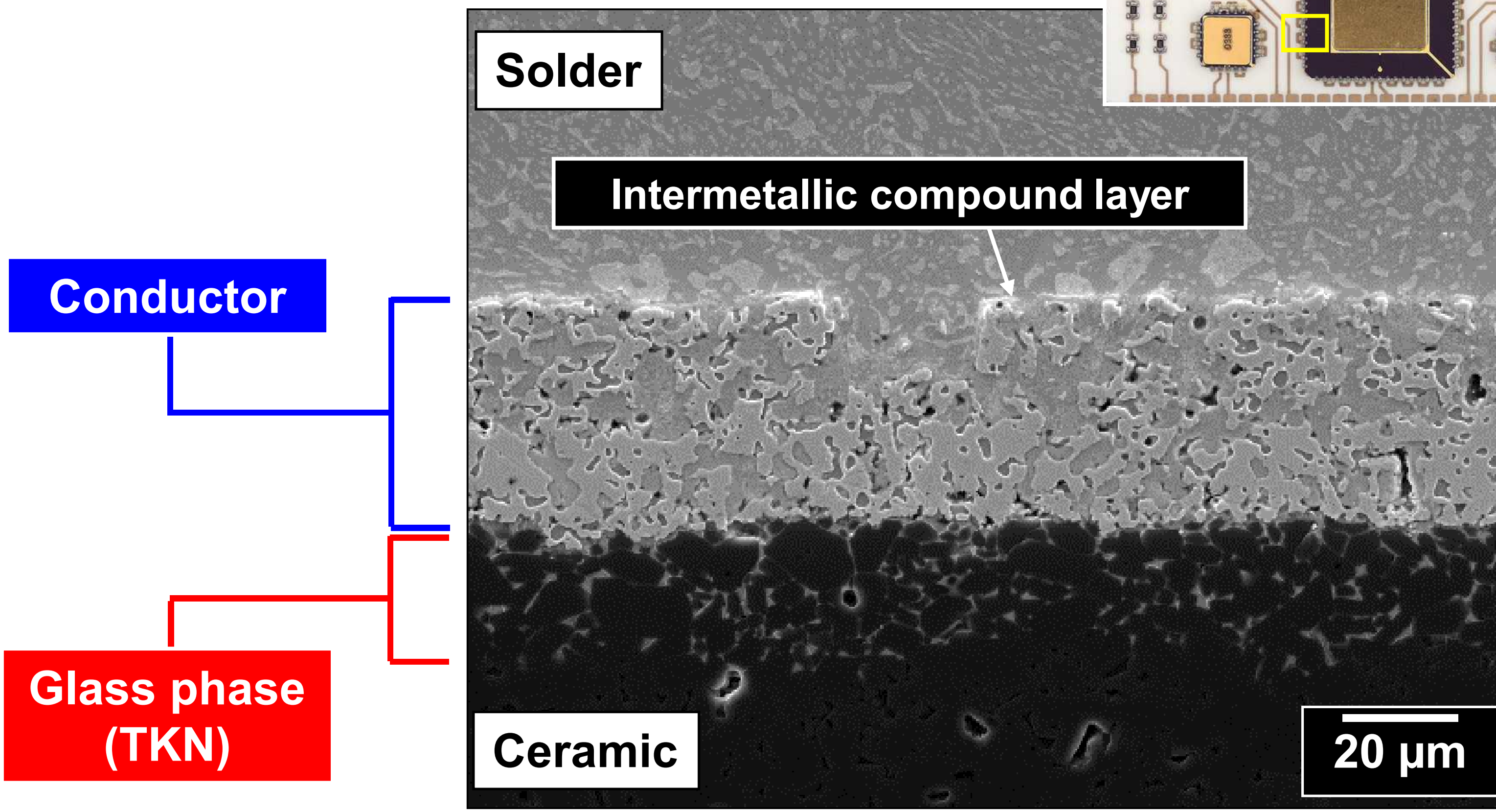




Introduction

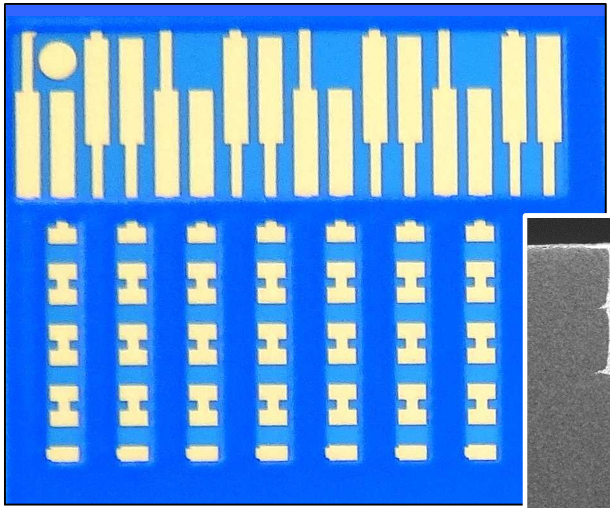
- The molten solder wets to, and penetrates the pores of, the thick film layer to form the interconnection.



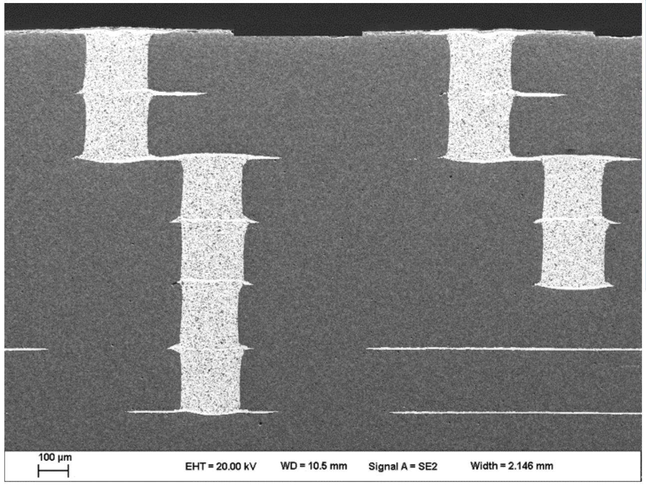


Introduction

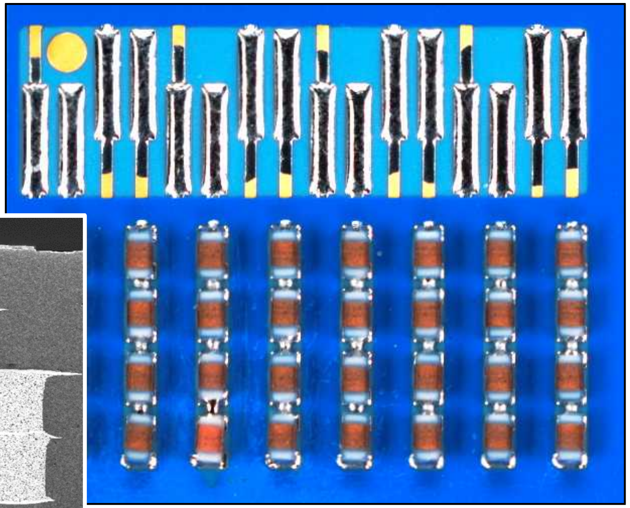
- The development of low-temperature, co-fired ceramic (LTCC) substrates provided the same *multi-layer* capability enjoyed by organic laminates.
  - Layer-by-layer, build-up technology places internal traces and vias into the LTCC substrate that can create highly complex circuits.



LTCC substrate



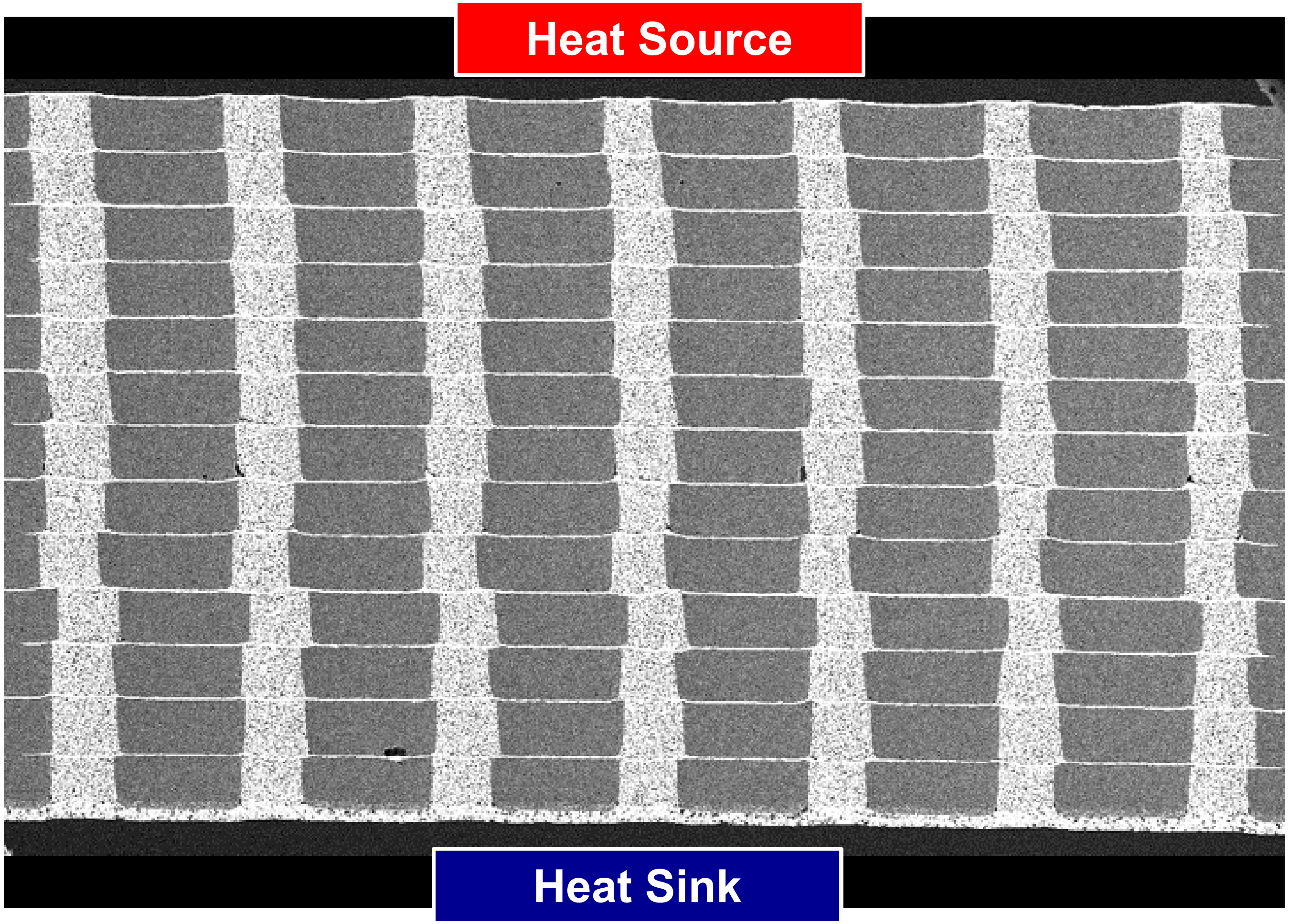
Signal traces and vias



Miniaturization of circuits

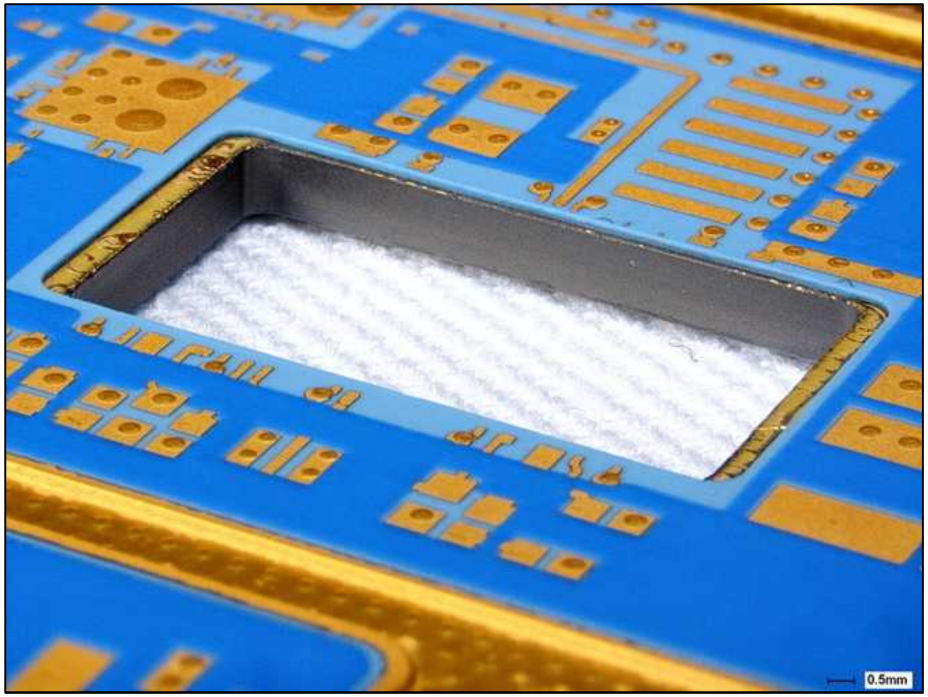
Introduction

- Special via-plus-trace designs can optimize **thermal management**.

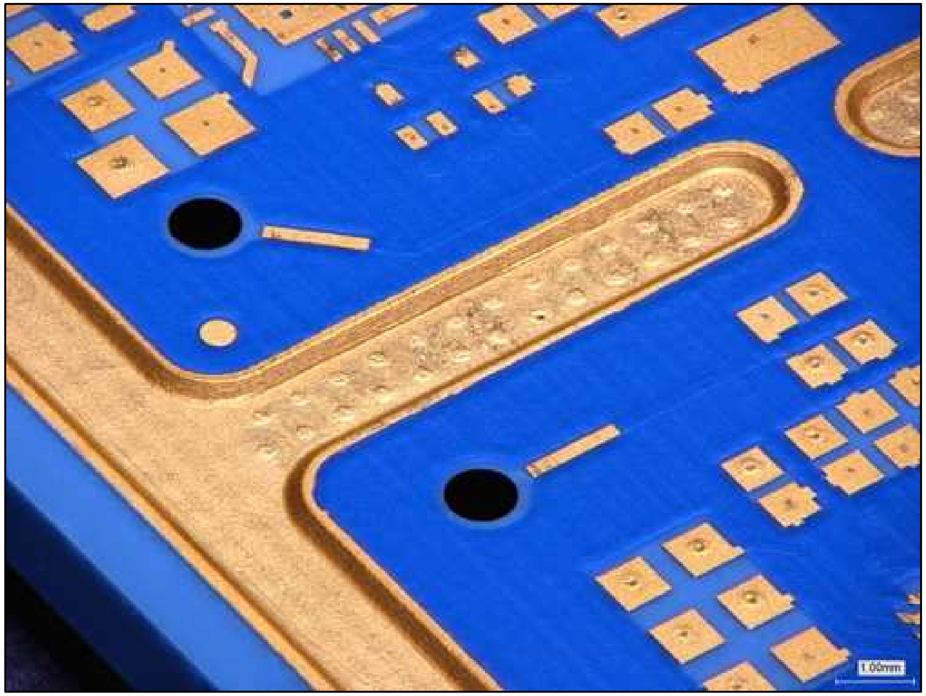


Introduction

- The LTCC build-up technology also allows for the creation of three-dimensional structures such as windows and cavities.



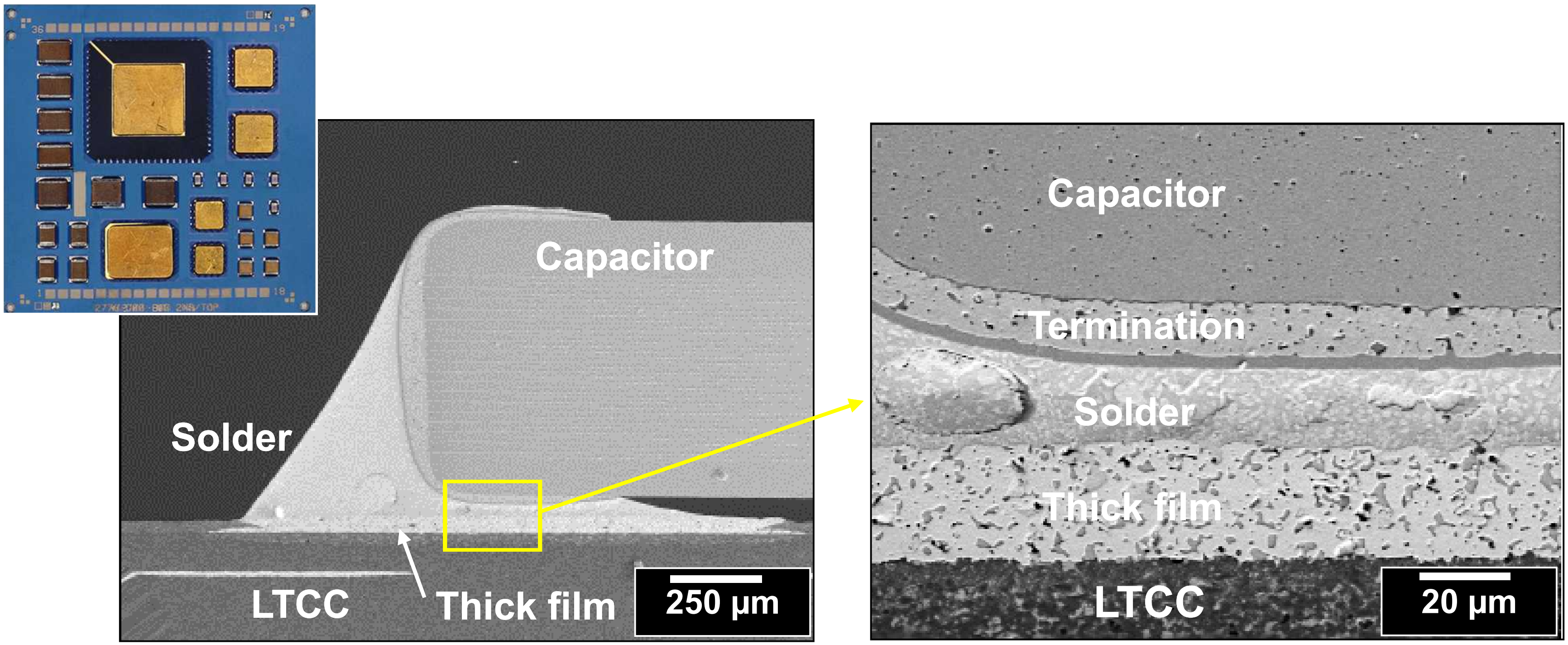
Window



Cavity

Introduction

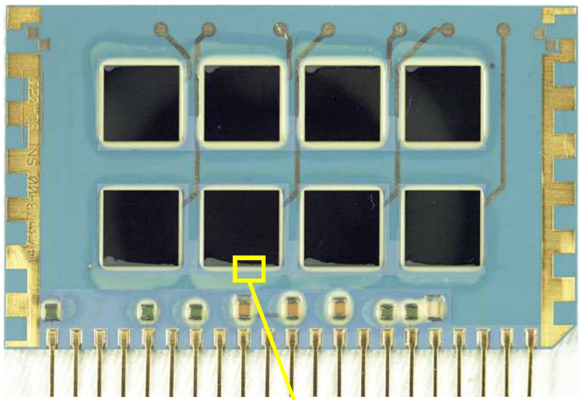
- The early development of HMC that incorporated LTCC, and numerous applications today, use thick film conductors.

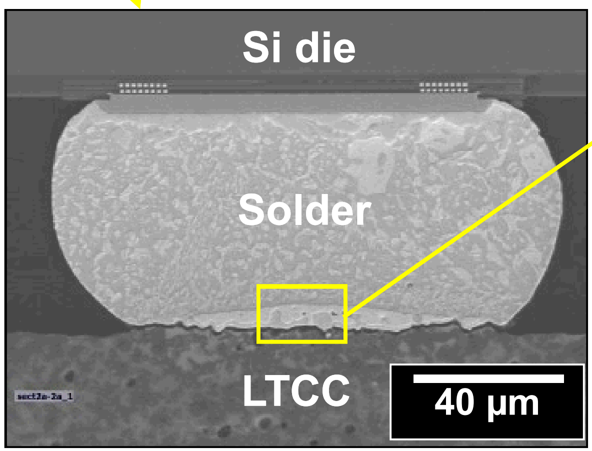


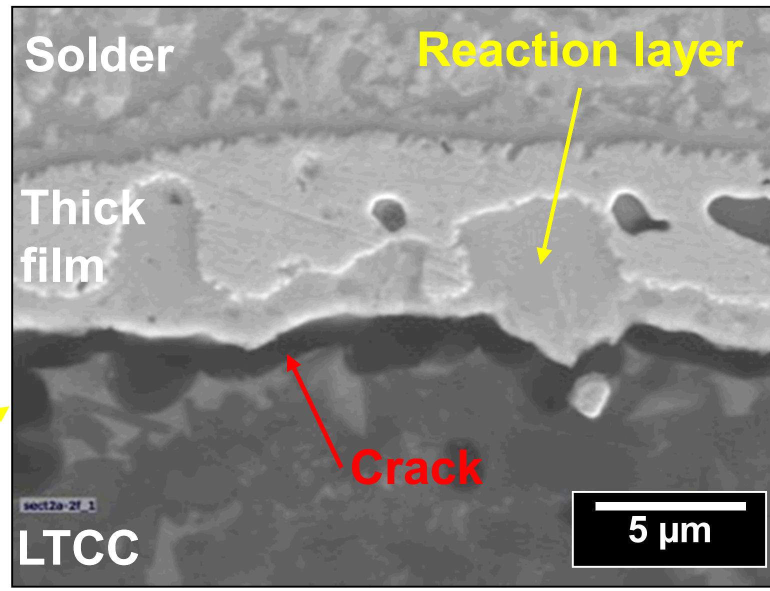
- Although such circuits could be very complex, “lines-and-spaces” did not pose particularly demanding requirements.

Introduction

- However, the miniaturization required by multi-chip modules (MCMs) *pushed the limits of thick film conductor technology*.



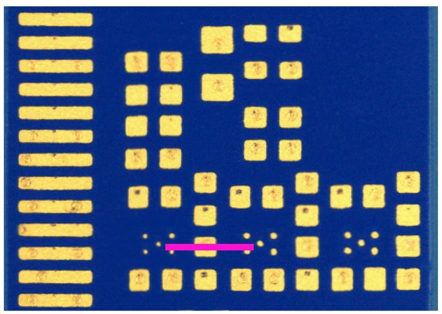




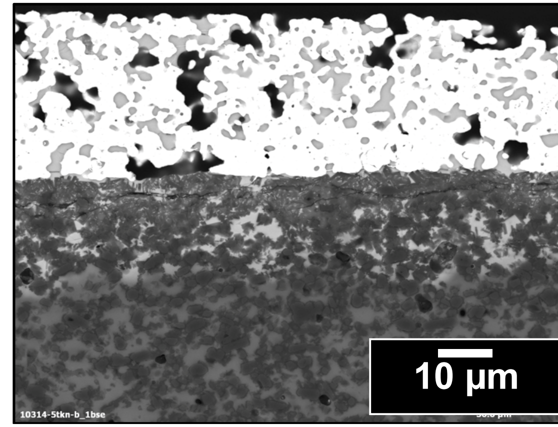
Unexpected material reactions can degrade the long-term reliability of the solder joints.

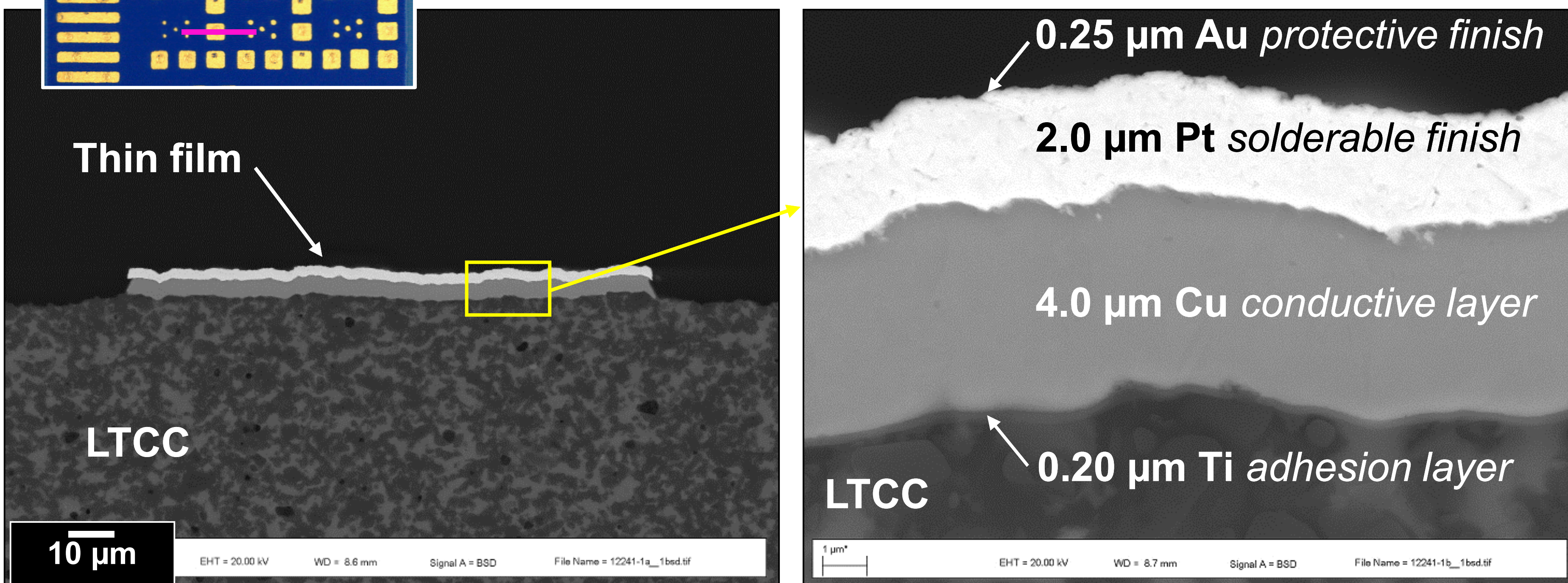
Introduction

- **The next step to improve functionality and miniaturization was replacing thick film conductors with thin film technology.**



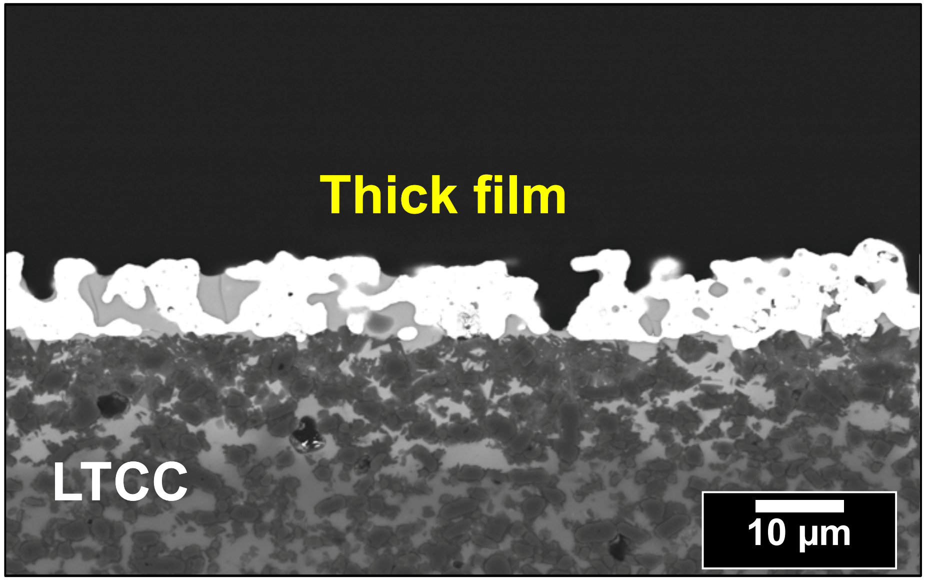
- **Photo imaging/plasma etch pattern definition**
- **Laser ablation *"erasing"***

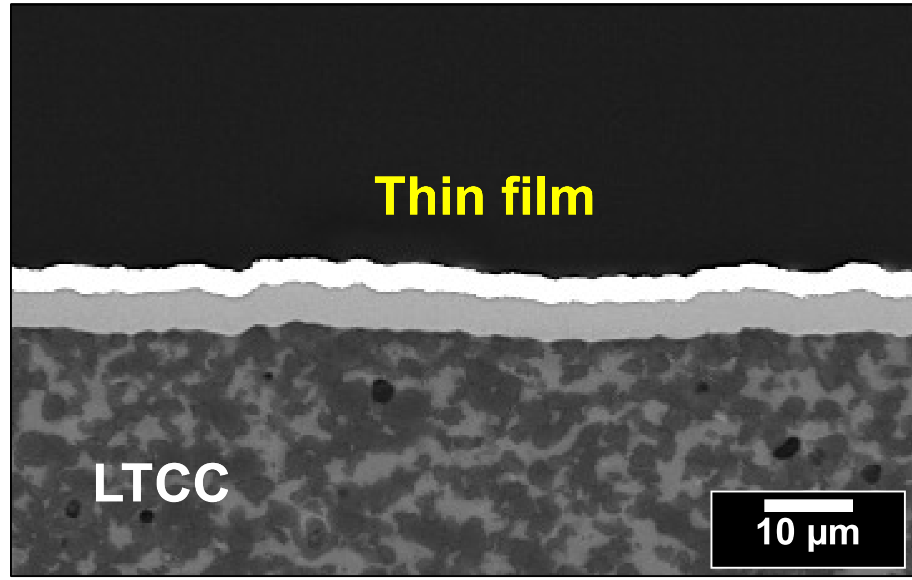


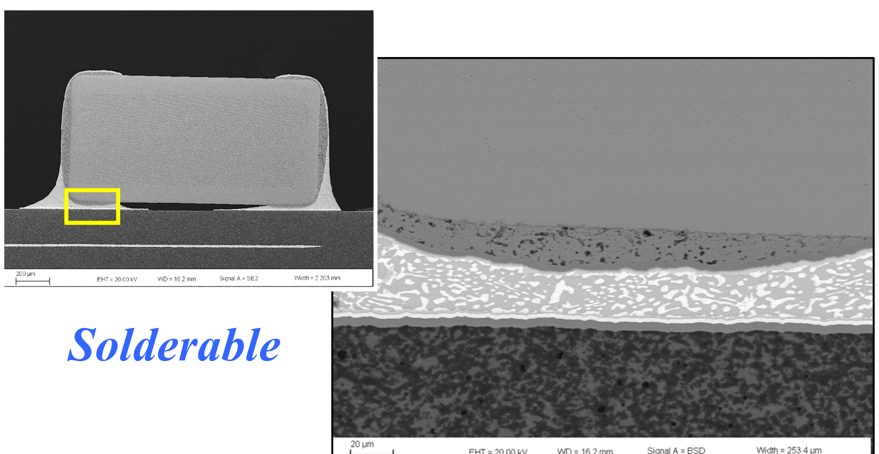


Introduction

- The **thin film technology** supports critical *functional* capabilities:

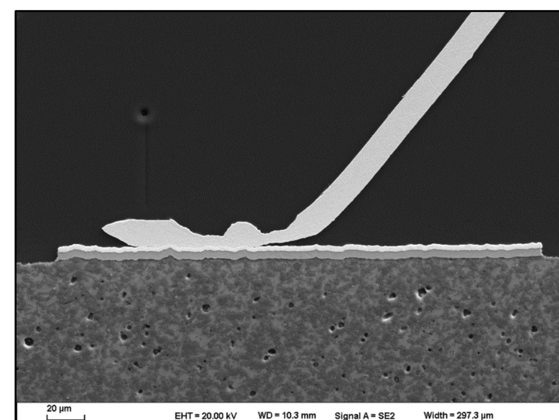






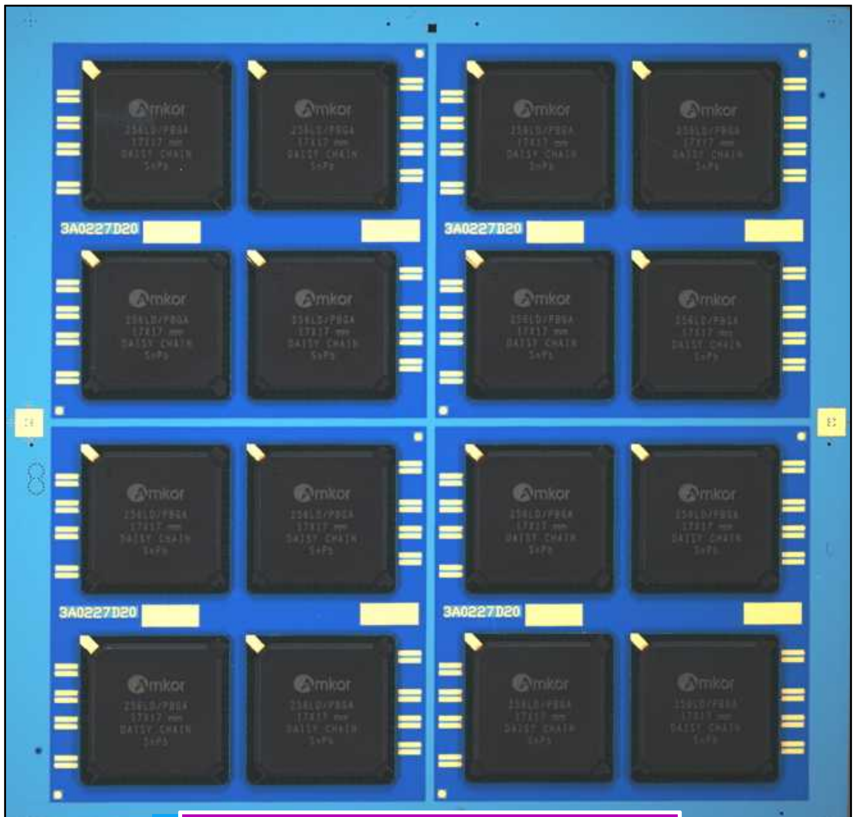
Solderable

Wire and ribbon bondable

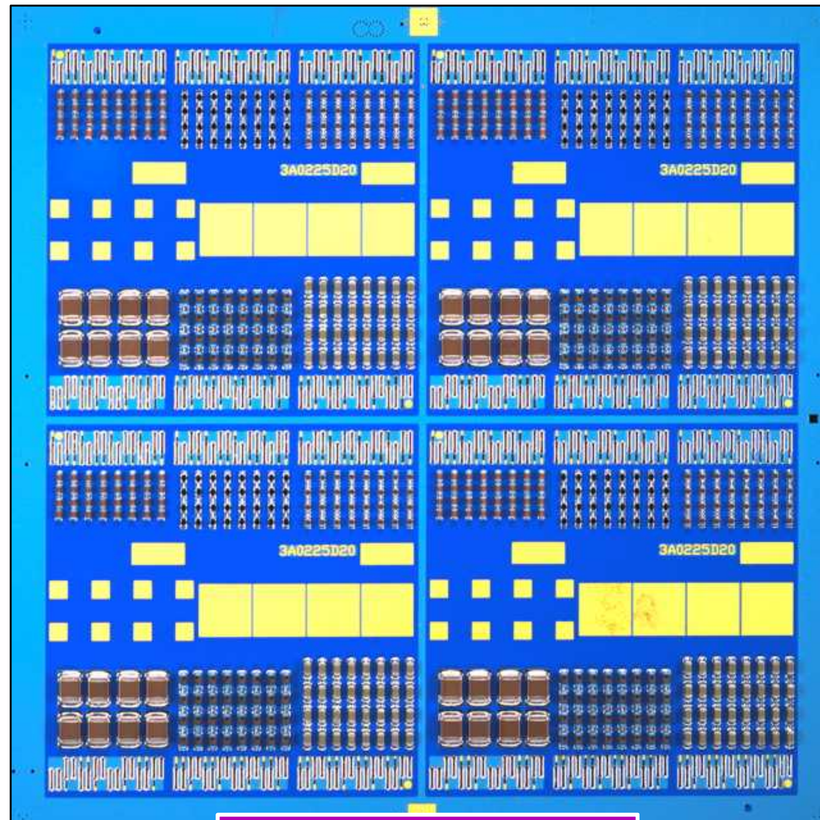


Introduction

- The LTCC-based, HMC technology using thin film conductors is illustrated by these accelerated aging test vehicles that readily incorporates 1.0 mm BGAs and 0402 passive devices.



Area-array packages



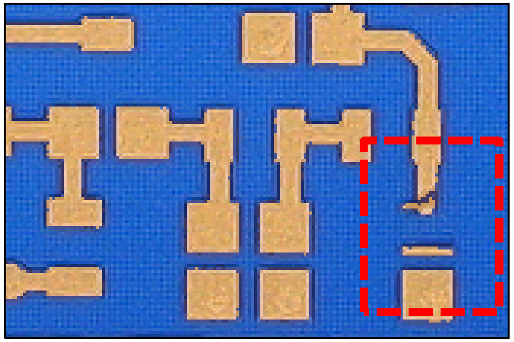
Passive devices

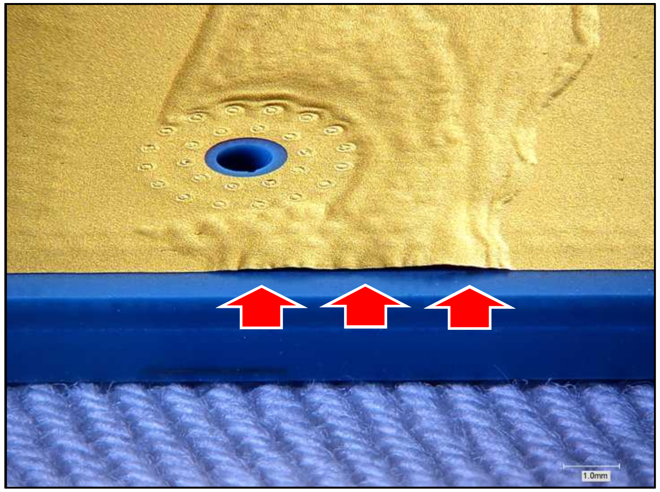
Path-Forward

- **Problem:**

  Thin film performance and reliability are sensitive to numerous factors:

  - **Choice of layers (the "stack")**
  - **Interphase adhesion**
  - **Surface contamination**





The potentially significant impact on product yield necessitates a means to identify root-cause from amongst multiple contributing factors.

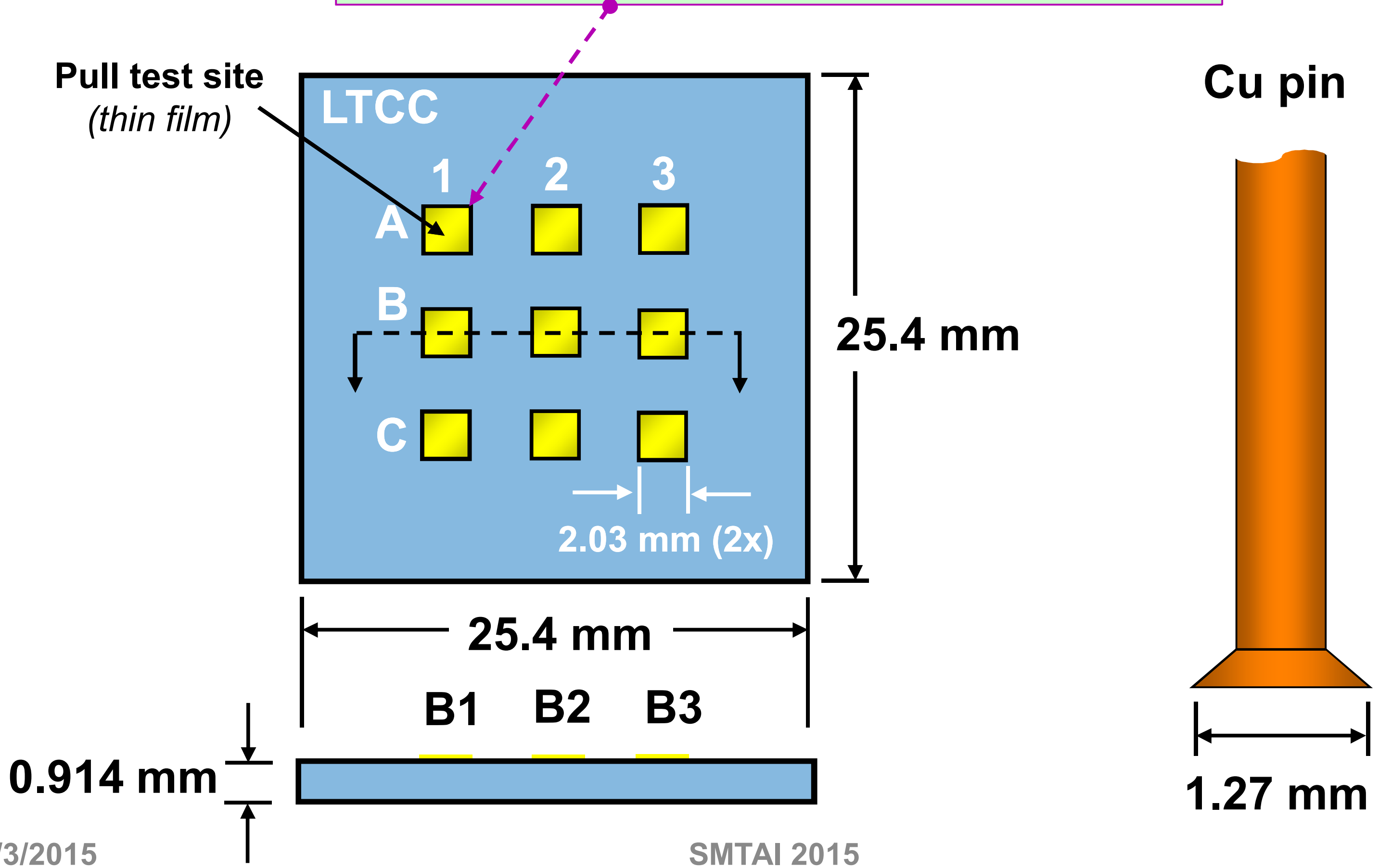
- **Objective:**

  Product optimization required a means to assess, at a more basic level, the strength of solder joints made to thin films on LTCC.

Experimental Procedure

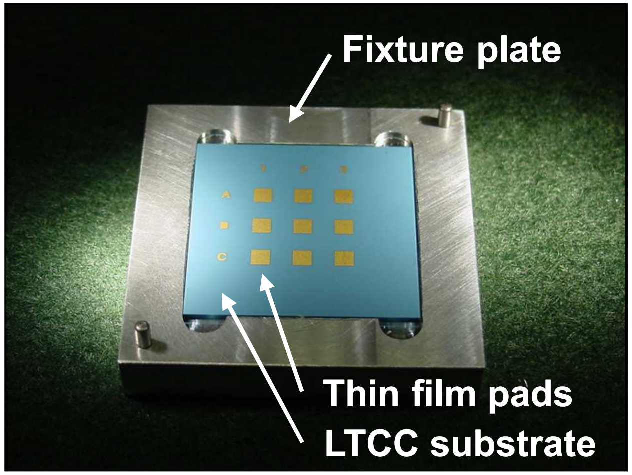
- A *pin pull test* was developed to measure the tensile strength of solder joints made to thin film conductors on LTCC substrates.

The pattern was created by evaporation of the thin film through an aperture mask.

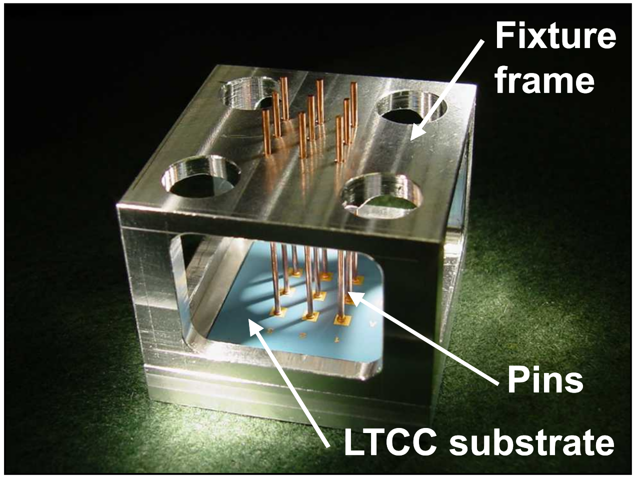


Experimental Procedure

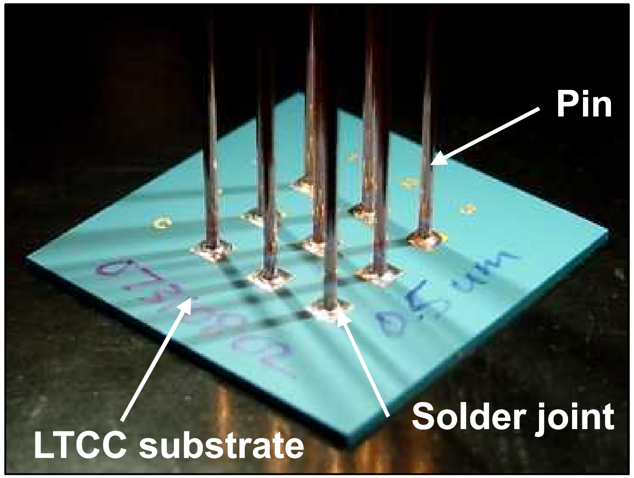
- The test assembly was fabricated by soldering a pin to each of the nine (9) thin film pads, using a conduction furnace.



Substrate is placed on the fixture plate.



Fixture frame and pins are put into place.



Completed test specimen

Experimental Procedure

- The low-temperature, co-fired ceramic (LTCC) substrate is fabricated from the DuPont™ 951 tape*
- The thin film is … 0.20 Ti - 4.0 Cu - 2.0 Pt - 0.25 Au (µm)
- The solder alloys (wt.%) … 63Sn-37Pb (Sn-Pb)
  … 95.5Sn-3.9Ag-0.6Cu (SAC396)
- Soldering times (seconds) and temperatures (°C):

	15s	60s	120s
215°C			
240°C			
260°C			
290°C			

Sn-Pb

	15s	60s	120s
240°C			
260°C			
290°C			

SAC396

* *DuPont™ is a registered trademark of E.I. DuPont de Nemours Corp., Wilmington, DE.*

Experimental Procedure

- The role of **solid-state aging** was evaluated for the **Sn-Pb joints**.

- The test samples were assembled using the two limiting cases of process variables … **215°C, 15s**

  … **290°C, 120s**

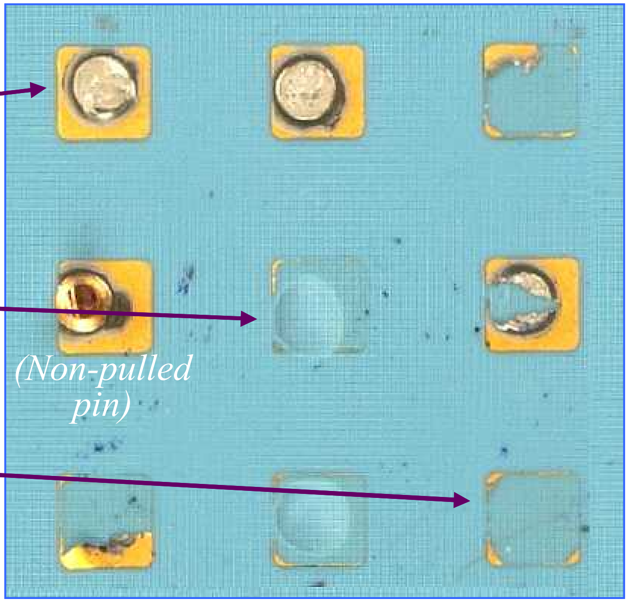
- Solid-state aging times (days) and temperatures (°C):

	5d	10d	25d	50d	100d	200d
215°C						
240°C						
260°C						
290°C						

Sn-Pb

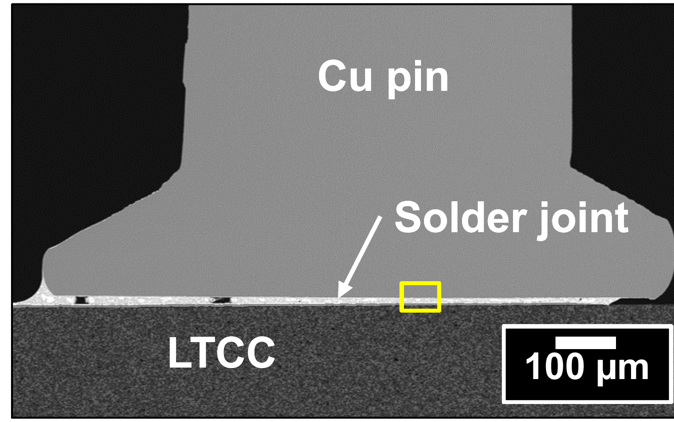
Experimental Procedure

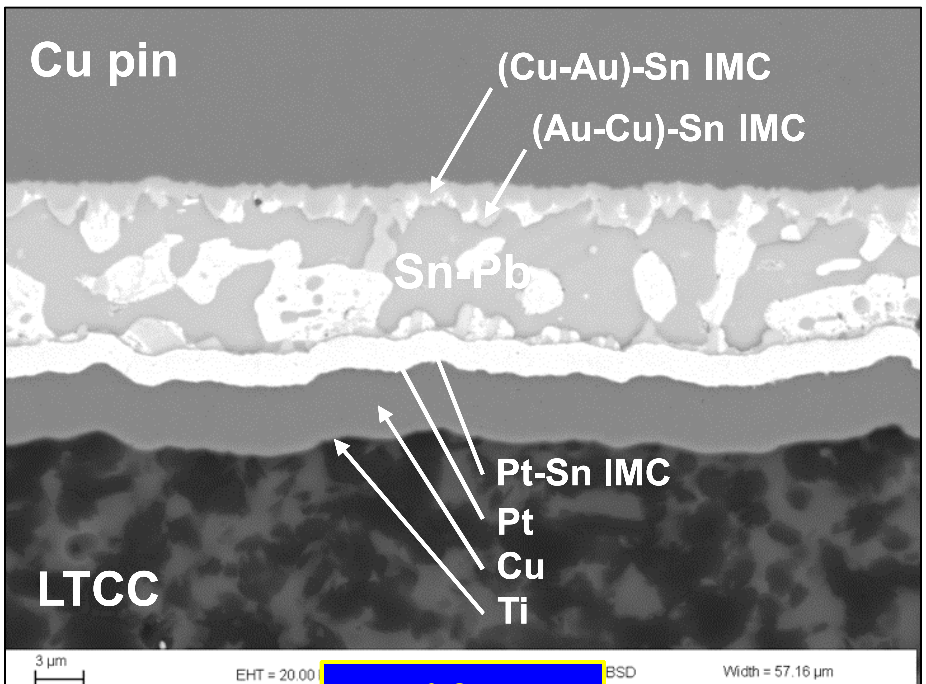
- **The pin pull test was performed at 10 mm/min.**
- **Eight (8) of nine (9) pins were pull tested on duplicate test specimens per condition, for a total of sixteen (16) data points.**
- **Fracture mode analysis is a *critical* step in this analysis.**
  - **There were three predominant failure modes:**
    - **Solder failure**
    - **Divot failure**
    - **Thin film delamination failure**



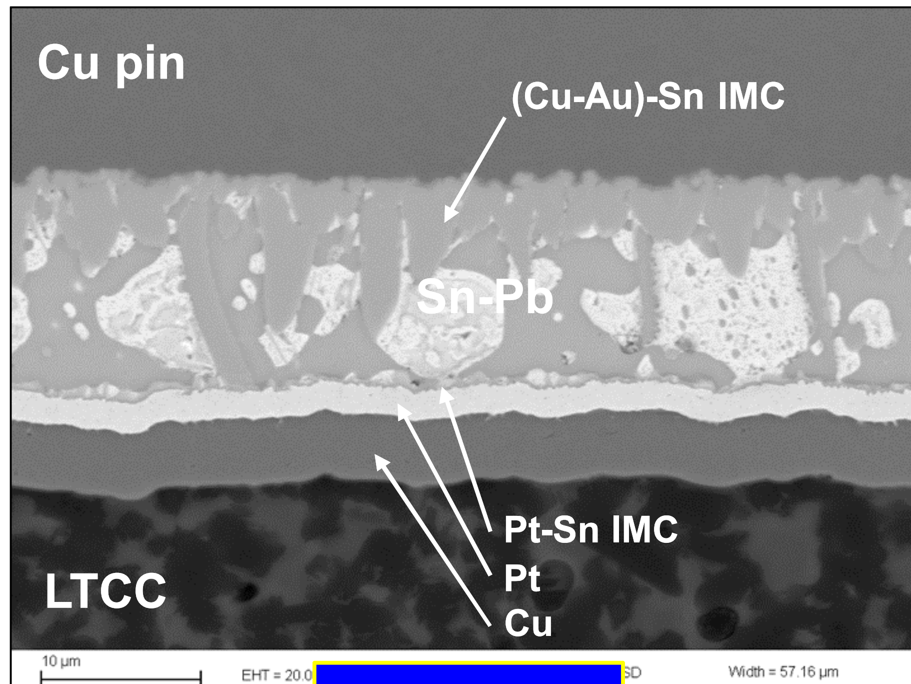
Results – Soldering Process Parameters

- The solder joint microstructures are shown for the Sn-Pb solder.
  - *Very minimal* reaction between the Sn-Pb solder and Pt solderable layer.
  - *Significant* IMC reactions occurred at the Sn-Pb / Cu pin interface.





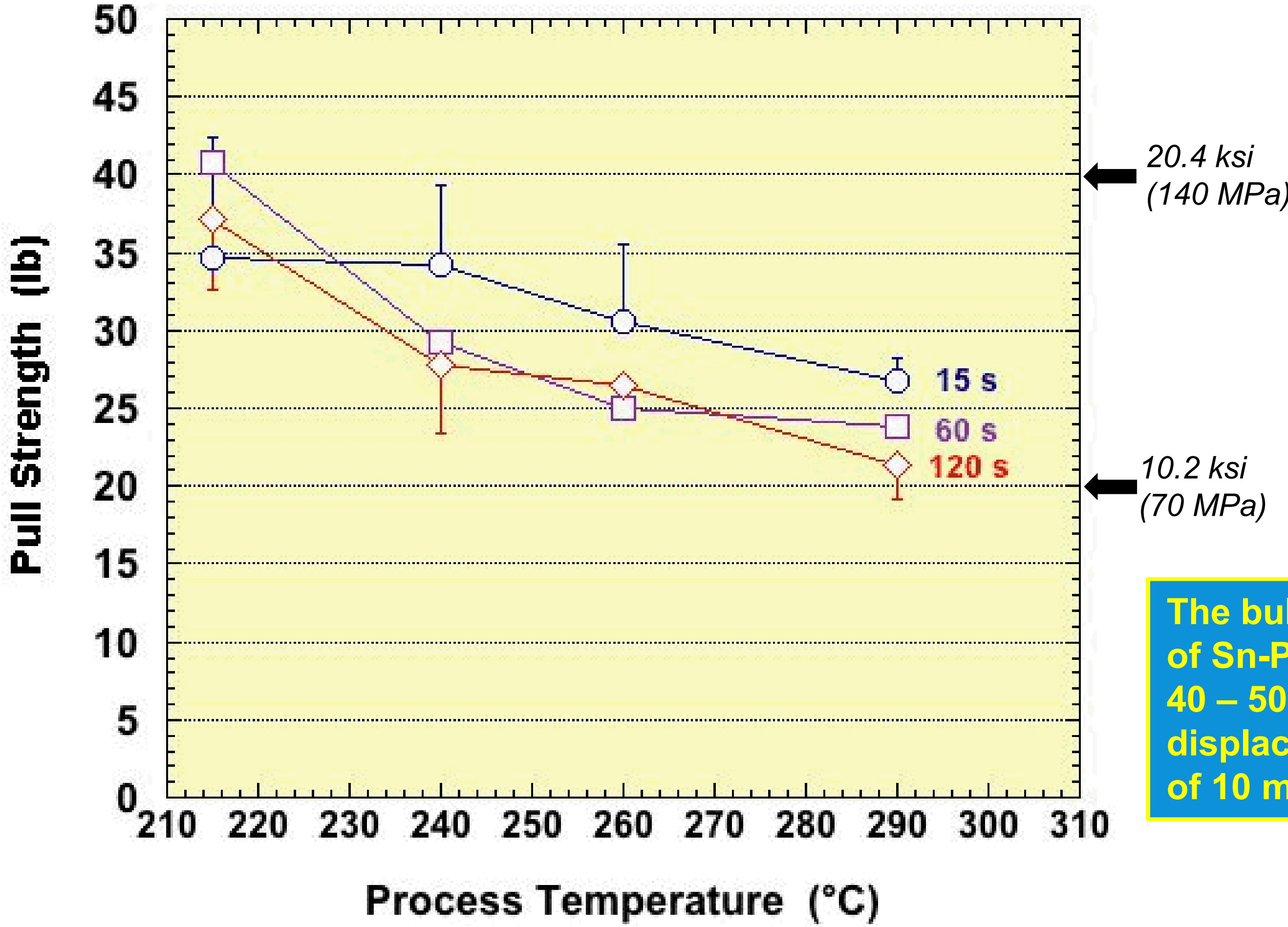
215°C, 15s



290°C, 120s

Results – Soldering Process Parameters

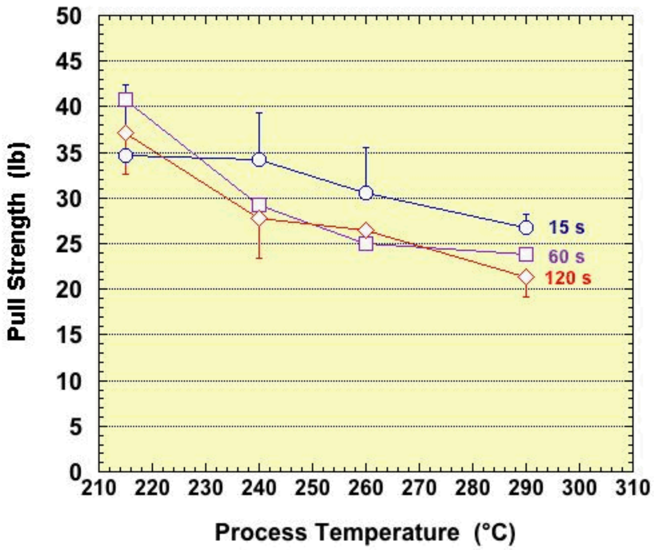
- The Sn-Pb solder pin pull test data are shown in this plot.

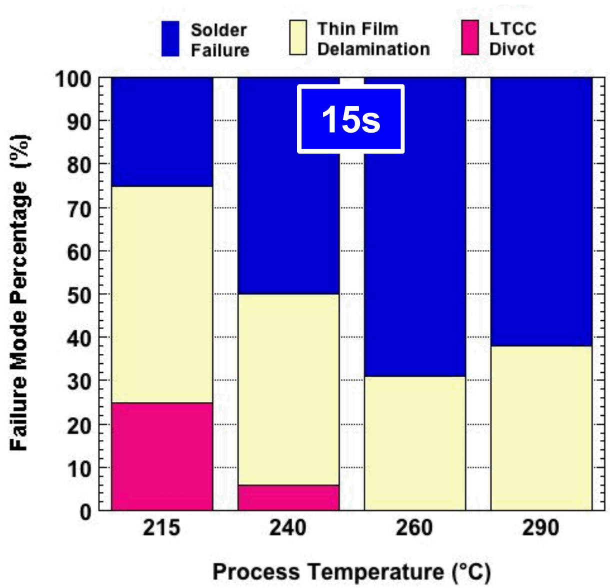


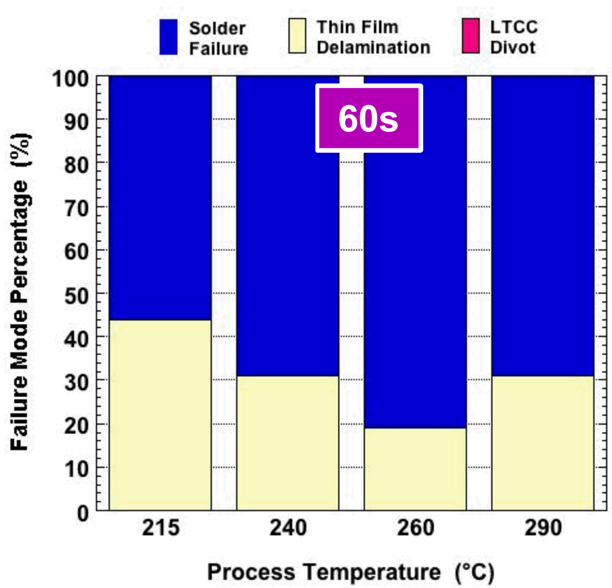
The bulk strength of Sn-Pb solder is 40 – 50 MPa at the displacement rate of 10 mm/min.

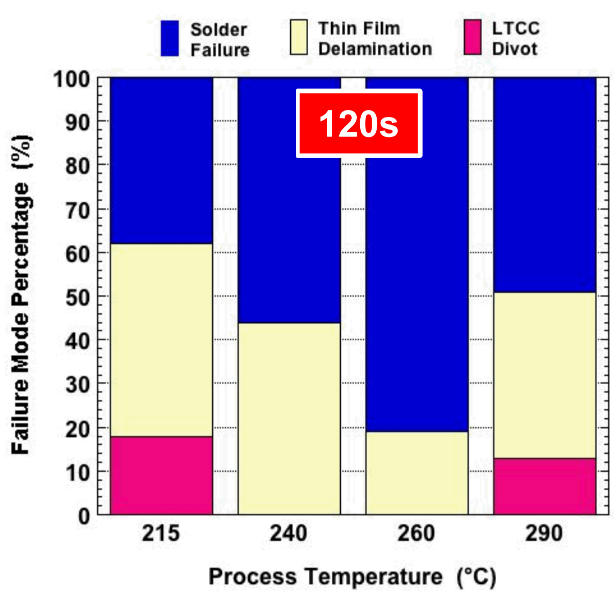
Results – Soldering Process Parameters

- The Sn-Pb solder failure mode data are shown for the three process times.
  - *215 – 260°C:* Increasing the process temperature caused delamination and divot failure modes to be replaced with solder failures.
  - *290°C:* The trend showed a slight reversal.



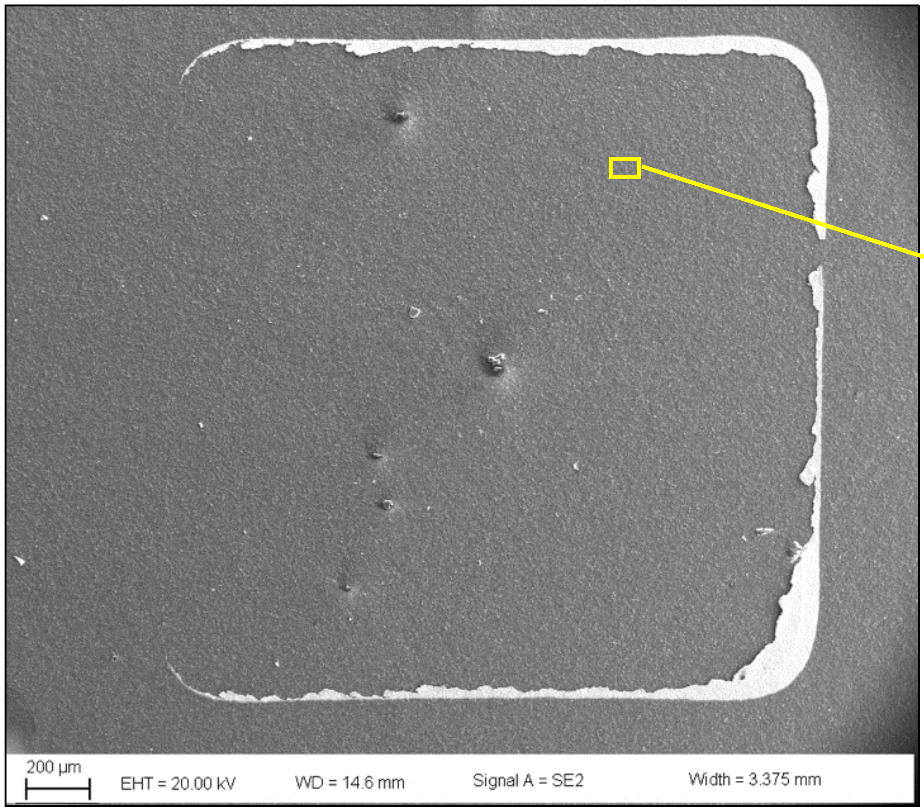


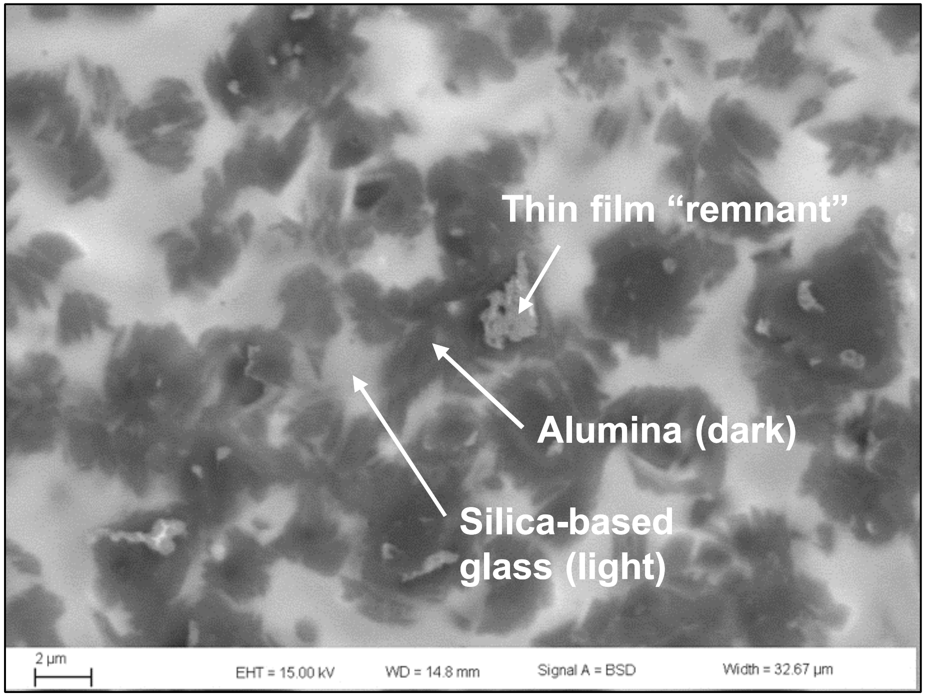




Results – Soldering Process Parameters

- The **thin film delamination failure** mode was characterized by separation at the *immediate* **Ti adhesion layer / LTCC** interface.

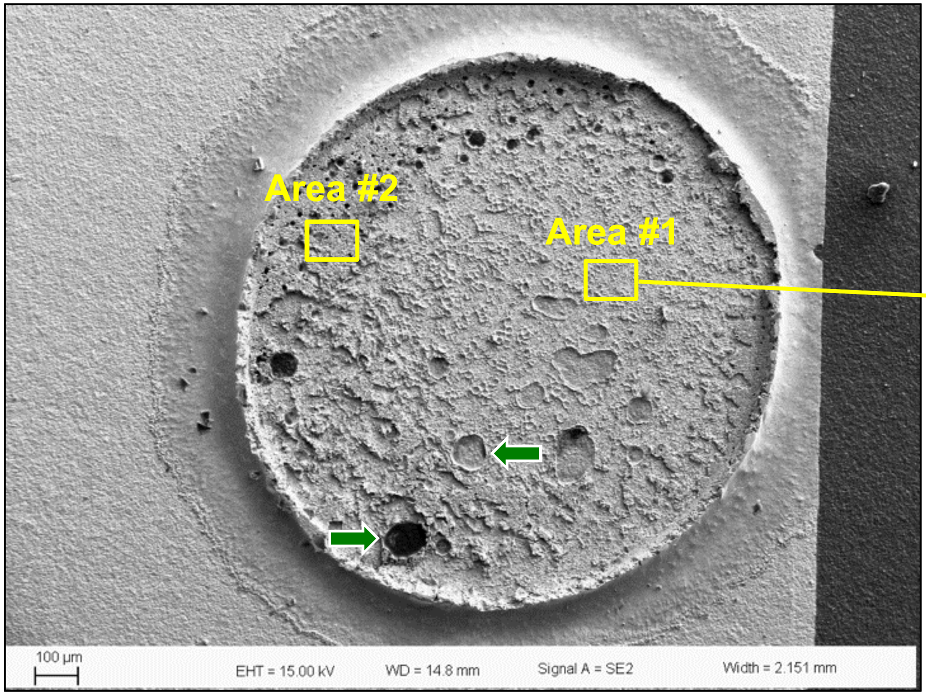


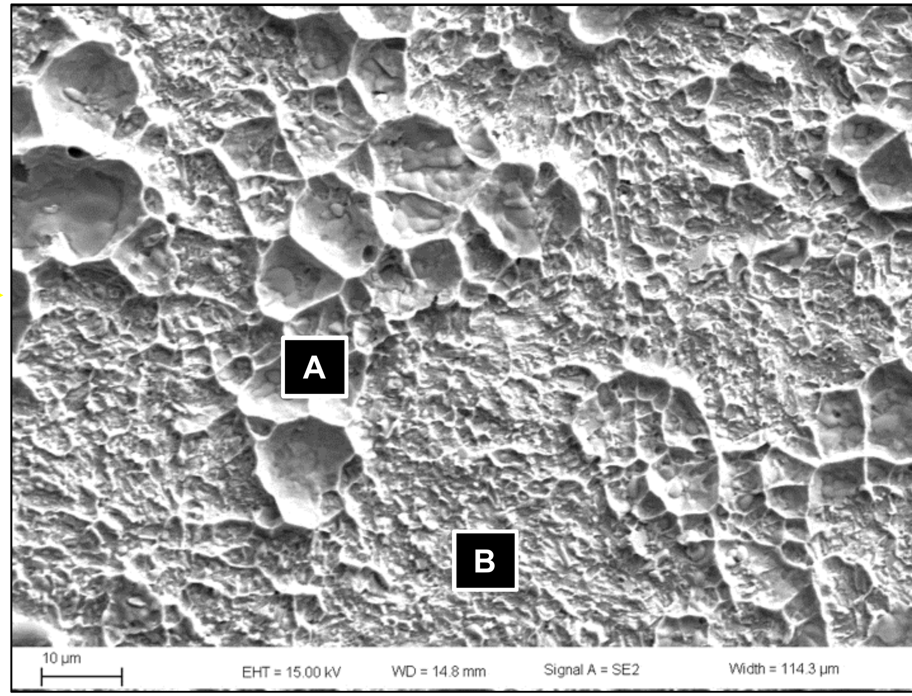


Sn-Pb solder; 215°C, 15s

Results – Soldering Process Parameters

◆ The **solder failure** mode exhibited multiple crack paths.





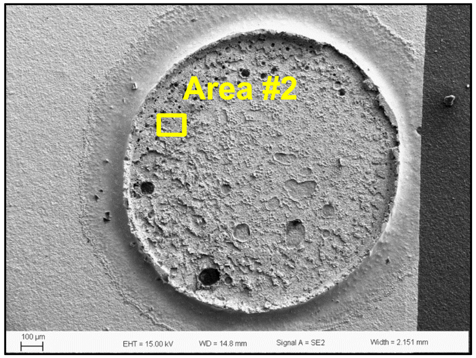
Sn-Pb solder; 215°C, 15s

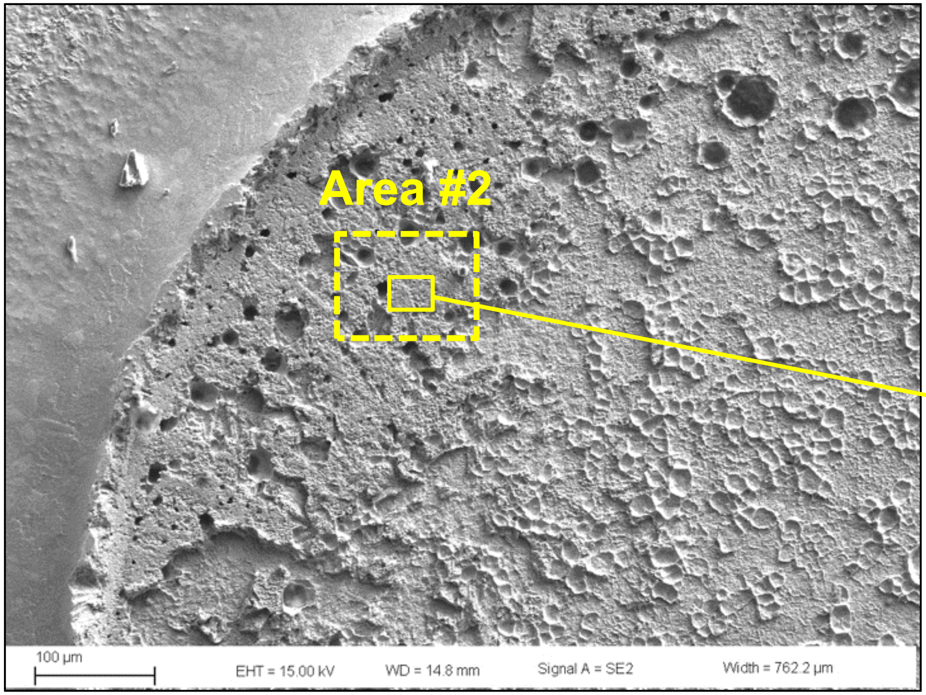
- Green arrows … minor voids
- Two fracture morphologies indicated by areas #1 and #2.

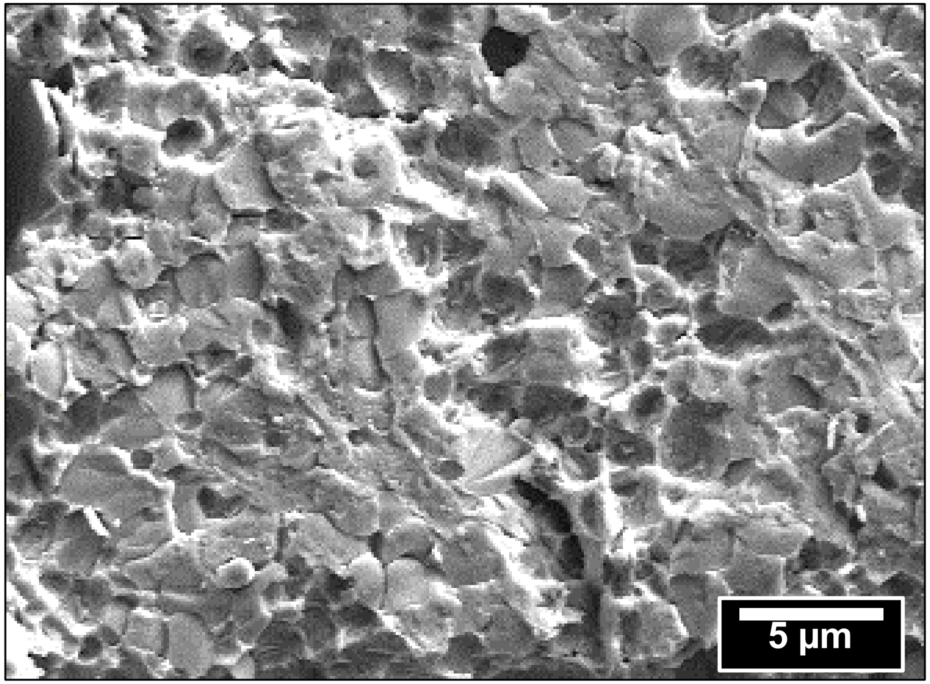
- Area #1:
  - "A" … ductile failure in the solder
  - "B" … Pt/Pt-Sn IMC interface failure

Results – Soldering Process Parameters

- **The area #2 morphology is examined, below.**
  - **Fracture surface … brittle, intergranular**
  - **EDX analysis … *high-Au,* (Au-Cu)-Sn IMC that formed at the solder / Cu pin interface.**



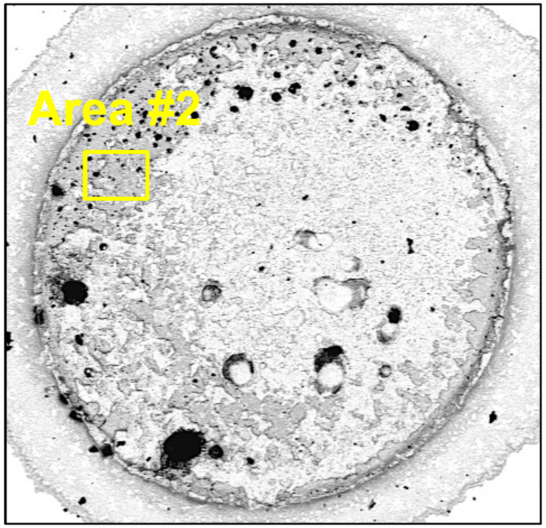




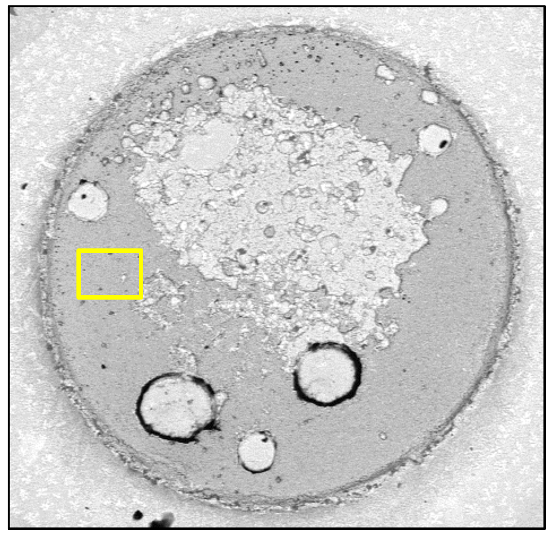
Sn-Pb solder; 215°C, 15s

Results – Soldering Process Parameters

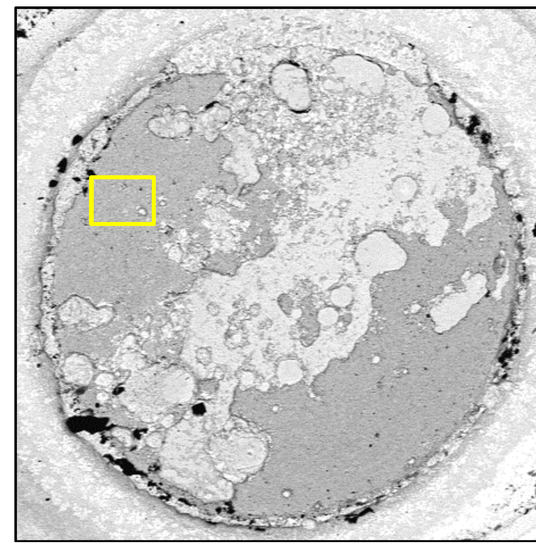
- The fracture surface changed with process parameter "severity."



215°C, 15s



260°C, 60s

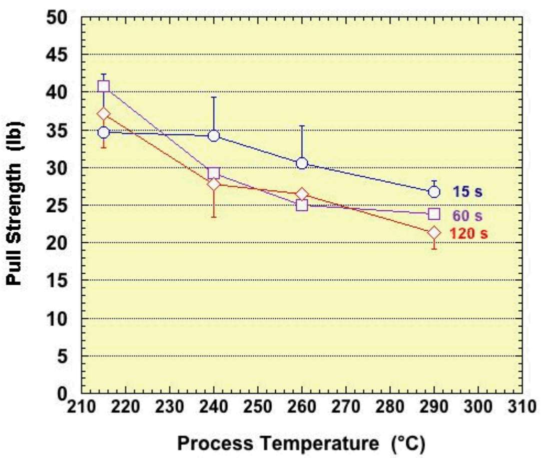


290°C, 120s

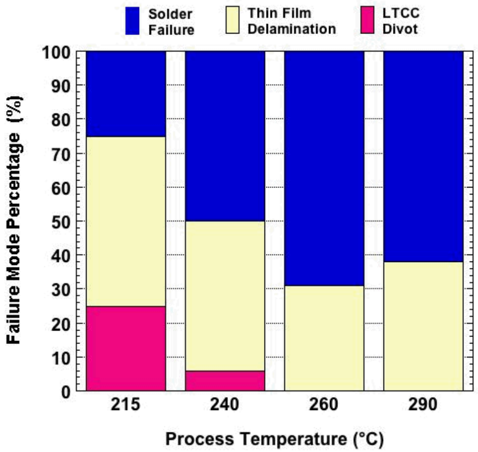
- The area #2 fracture surface increased with "severity."
- The **area #2** fracture surfaces of 260°C, 60s and 290°C, 120s progressed through the ***low-Au,* (Cu-Au)-Sn IMC.**

Results – Soldering Process Parameters

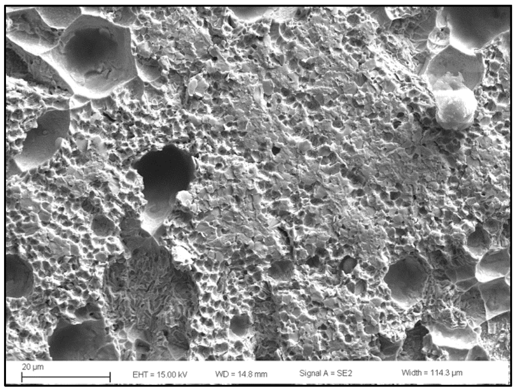
◆ **An analysis was made, based on all three data sources:**



Pull strength



Failure mode analysis

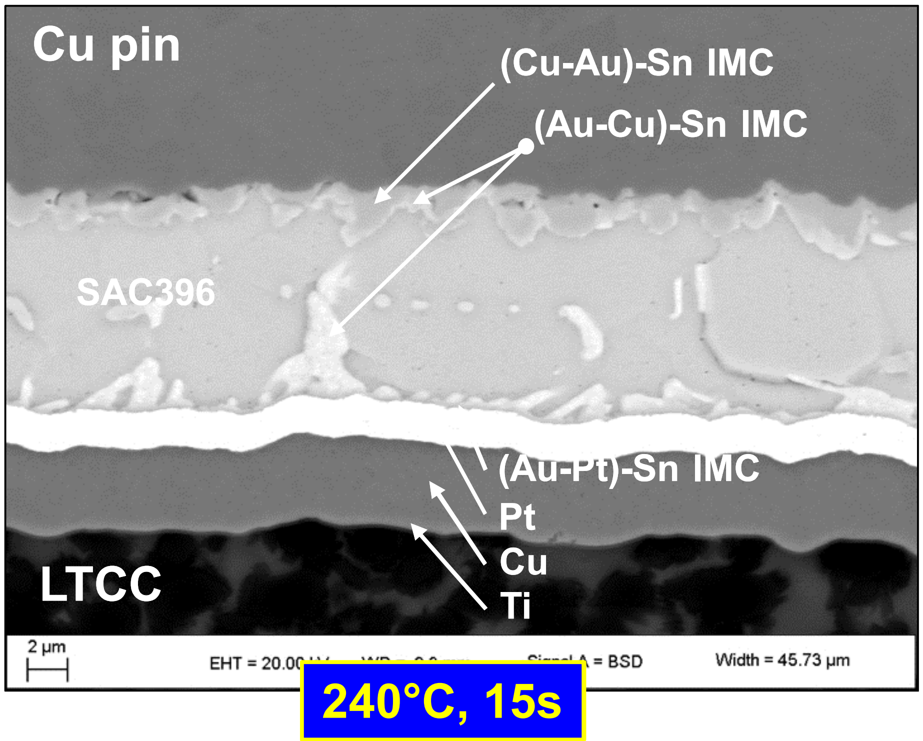


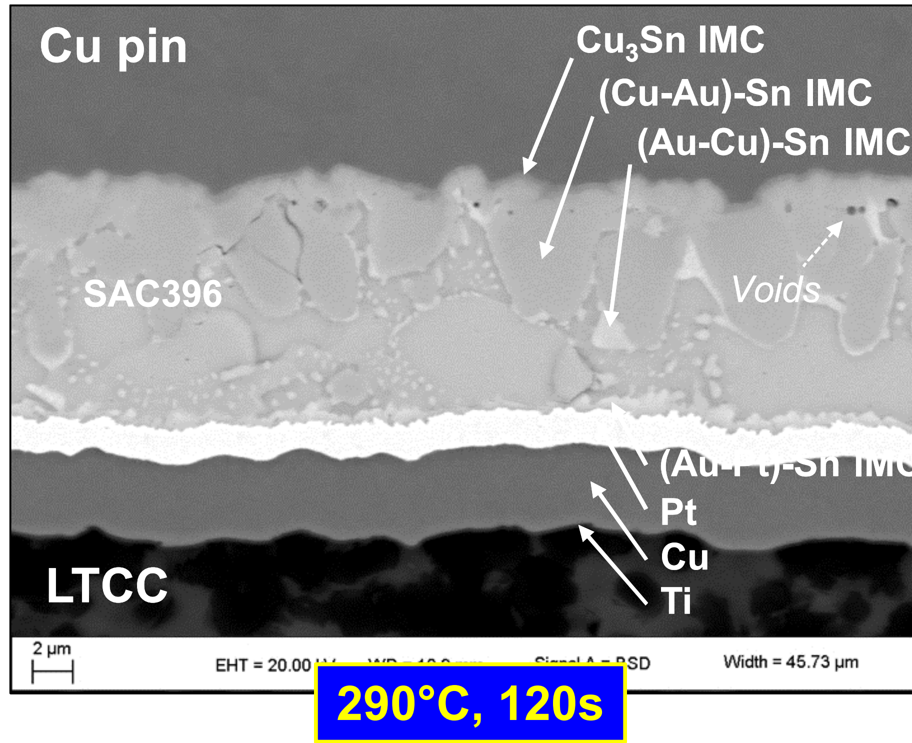
Fracture morphology

- **All joint strengths exceeded that of the bulk solder.**
- **The strength loss with soldering time and temperature was correlated to an increase of the solder failure mode.**
- **Increased solder failure mode was accompanied by an increased fracture path along the IMC at the solder/Cu pin interface.**
- **The increased presence of Au in the IMC layer decreased the intrinsic strength of the Cu/IMC interface with increased process "severity".**

Results – Soldering Process Parameters

- The SAC396 samples were examined versus the soldering process.

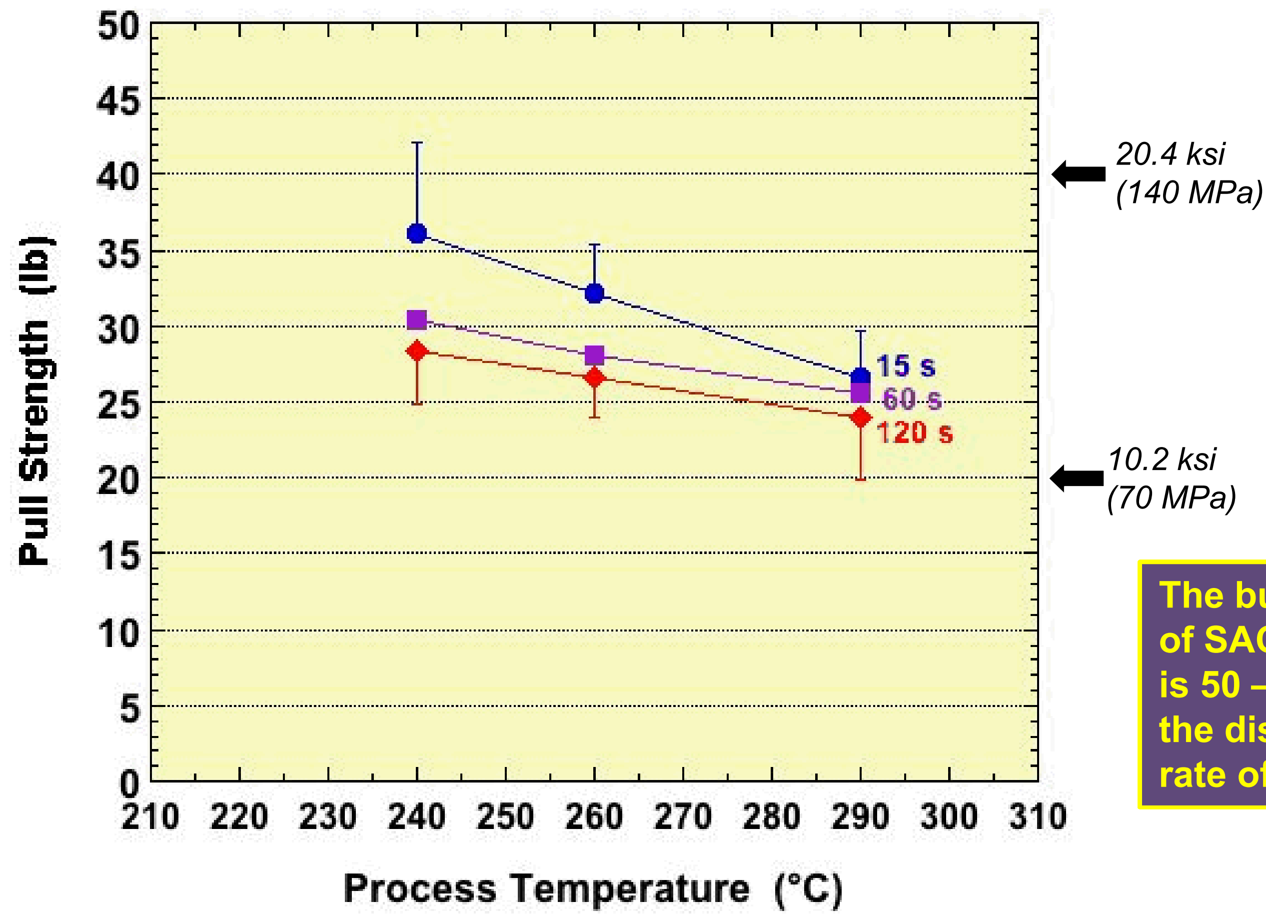




- The SAC396 joints had slightly different interface microstructures.
  - SAC396 retained Au more so in both interface IMC phases.
  - At 290°C, 120s, the SAC396 exhibited the Cu_3Sn phase at the solder / Cu pin interface.

Results – Soldering Process Parameters

- The **SAC396** solder joint strength is shown, below.



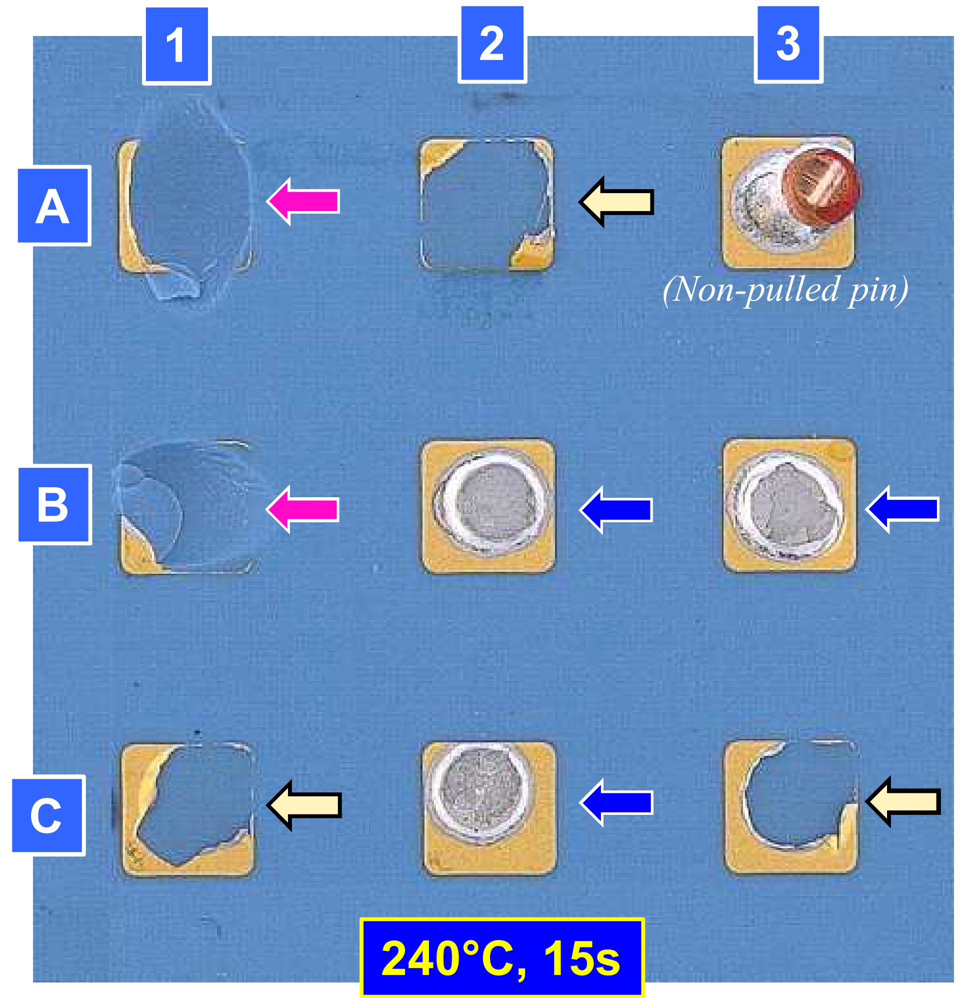
The bulk strength of SAC396 solder is 50 – 70 MPa at the displacement rate of 10 mm/min.

The strength magnitudes and trends replicated those of the Sn-Pb solder joints over the same temperature range.

Results – Soldering Process Parameters

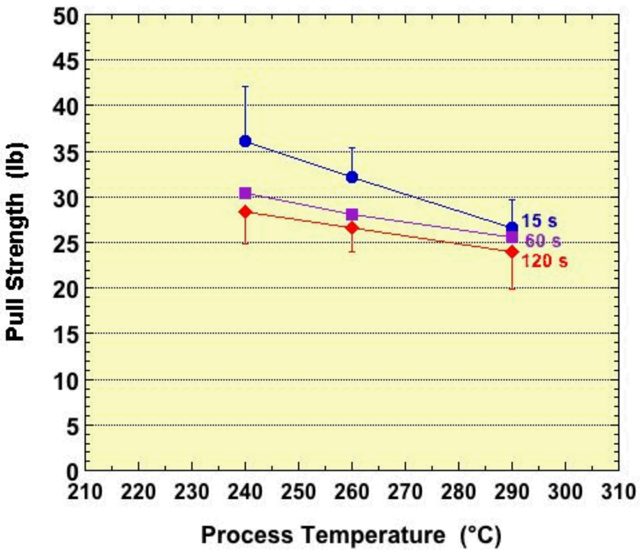
◆ The SAC396 solder joints exhibited the same failure modes as were observed with the Sn-Pb samples.

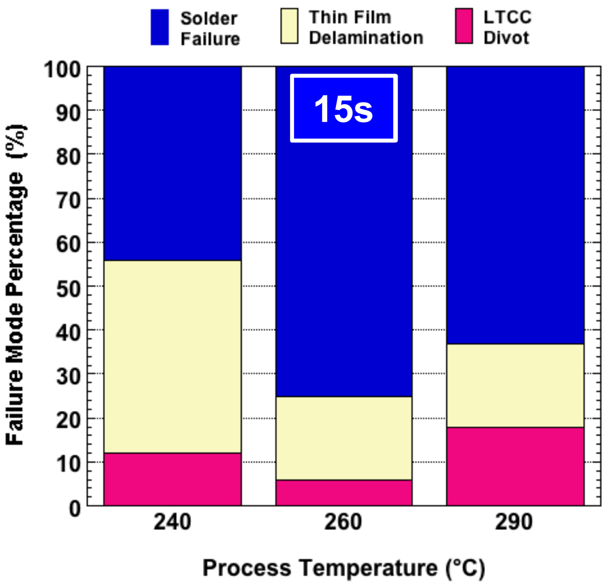
- Yellow arrows indicate thin film delamination.
- Blue arrows indicate solder failure.
- Magenta arrows indicate divot failure.

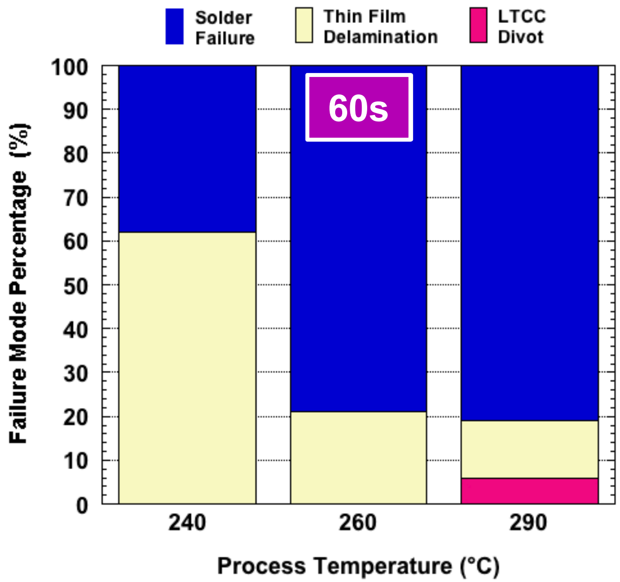


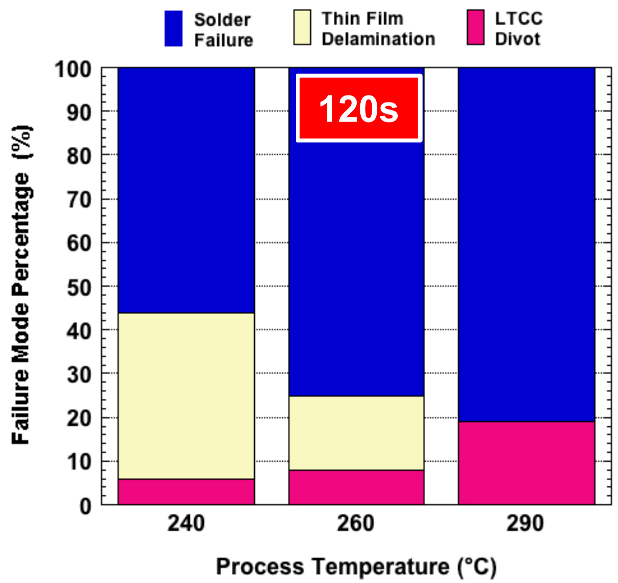
Results – Soldering Process Parameters

- The SAC396 solder failure mode data are shown for the three process times.
  - *240 – 290°C:* Increasing the process temperature caused delamination and divot failure modes to be replaced with solder failures.
  - There is a *persistent presence of the divot failure mode, particularly for 15s and 120s*



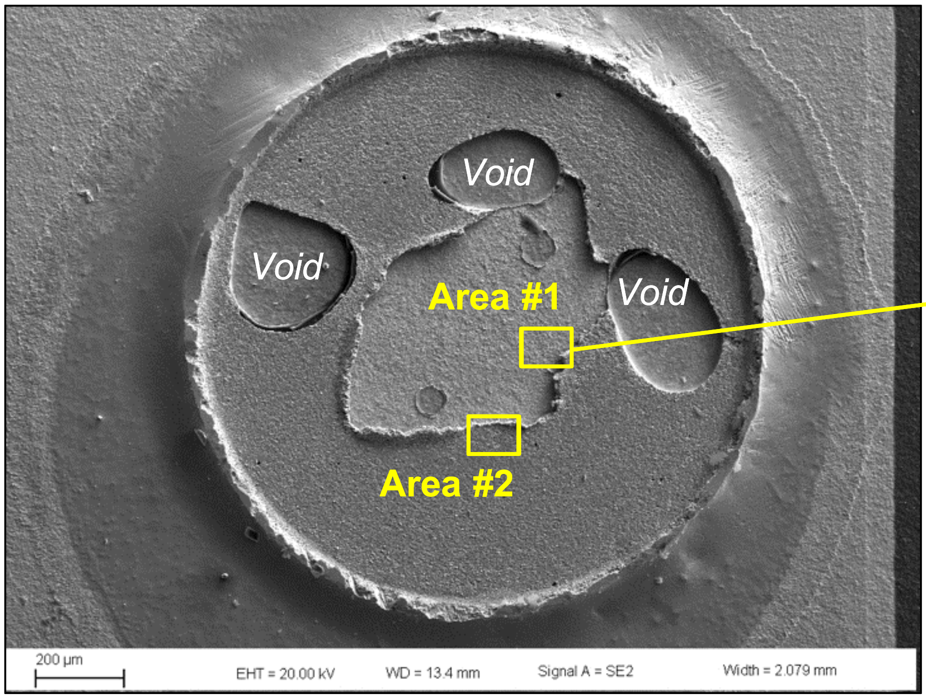


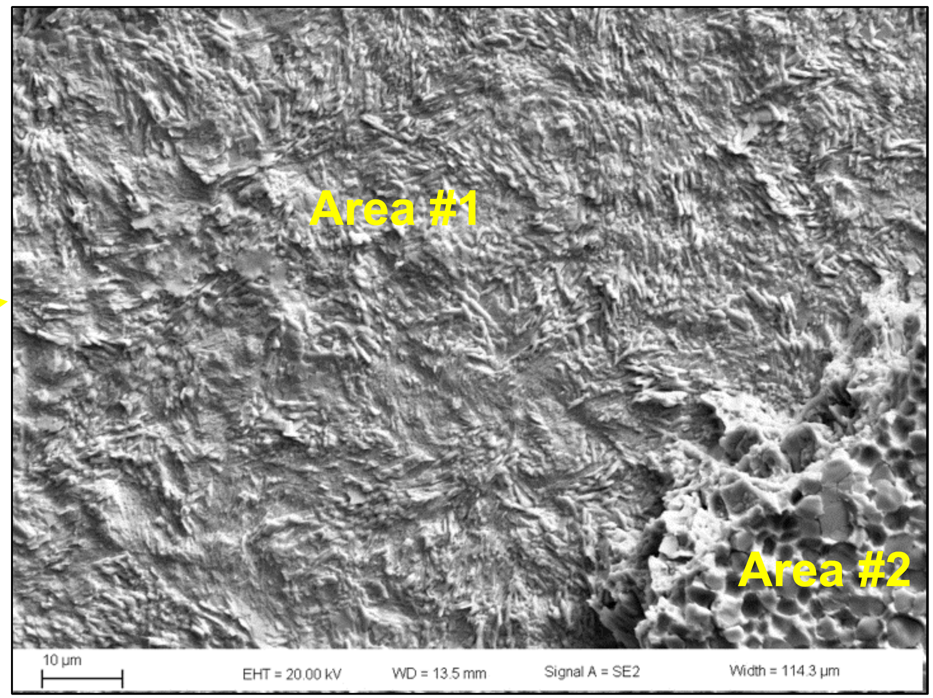




Results – Soldering Process Parameters

- The **thin film delamination** and **divot failure** mode morphologies were similar to those of the Sn-Pb solder.
- The SAC396 **solder failure mode** was examined more closely.
- The EDX analysis indicated **area #1** as the **Pt/Pt-Sn IMC interface**.

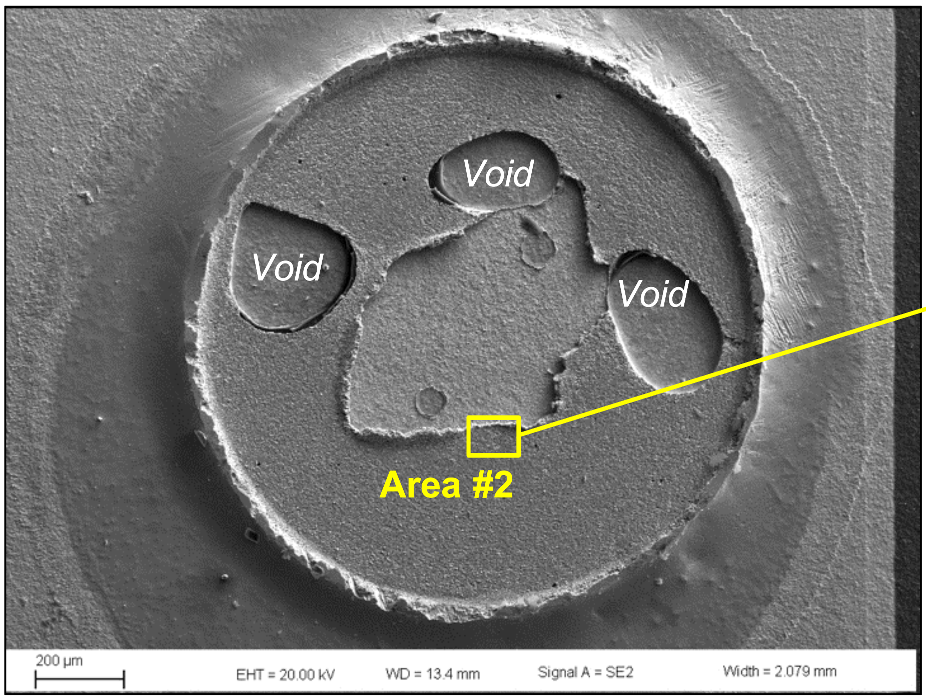


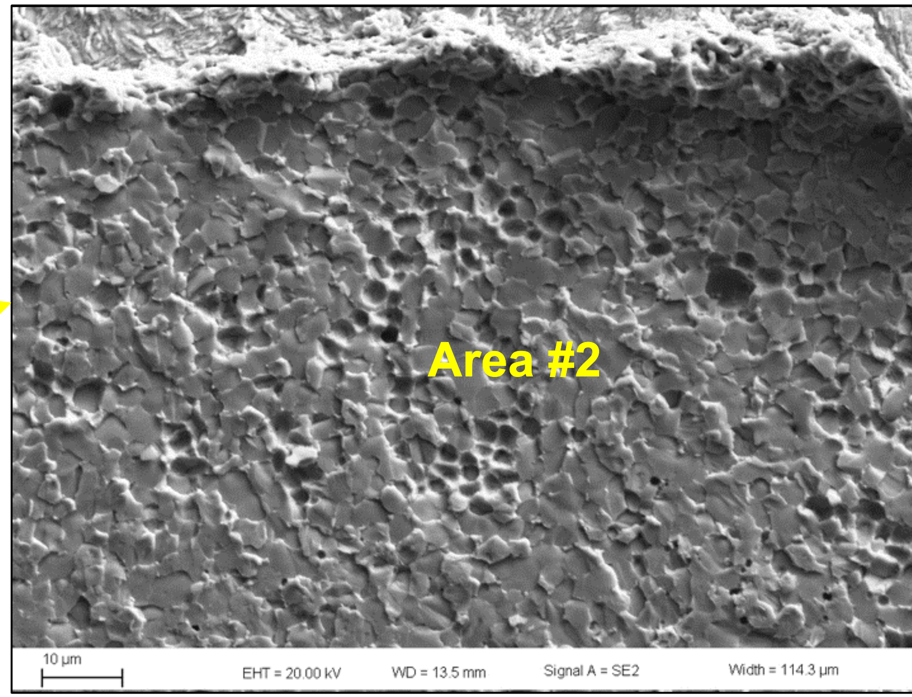


SAC396 solder; 240°C, 15s

Results – Soldering Process Parameters

- The **area #2** fracture surface had a brittle, intergranular morphology.
- The EDX analysis confirmed that the **area #2** crack path passed through the ***low-Au*, (Cu-Au)-Sn IMC layer**.

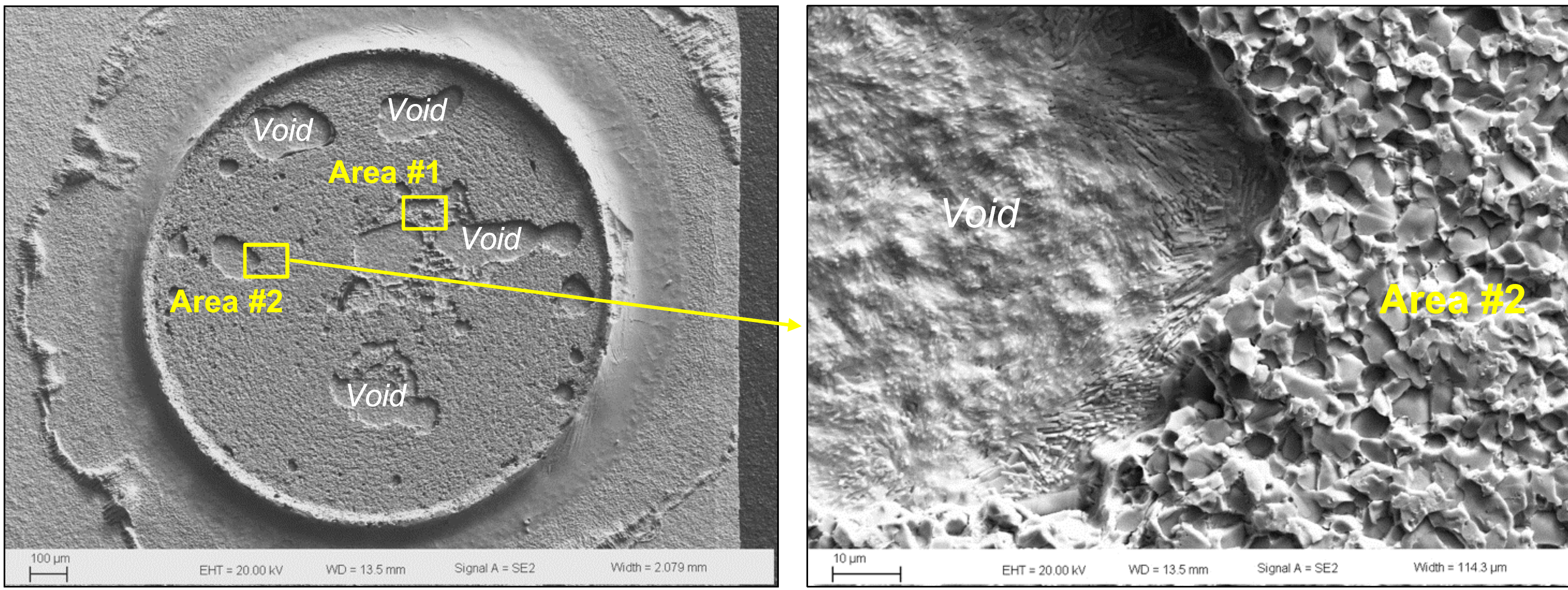




SAC396 solder; 240°C, 15s

Results – Soldering Process Parameters

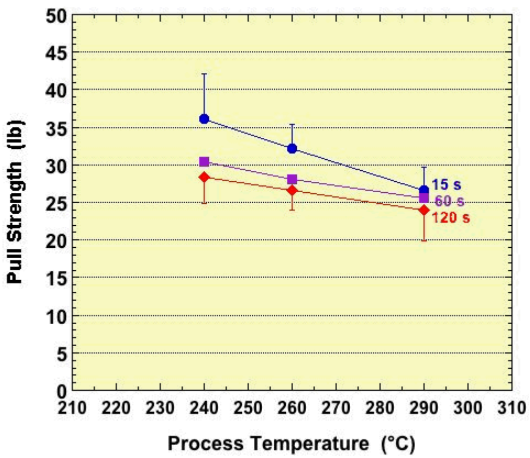
- The more severe process parameters caused an increase in the **area #2** fracture morphology, after taking the voids into account.
- Interestingly, EDX analysis indicated that the **area #2** crack path favored the ***low-Au, (Cu-Au)-Sn IMC layer***.



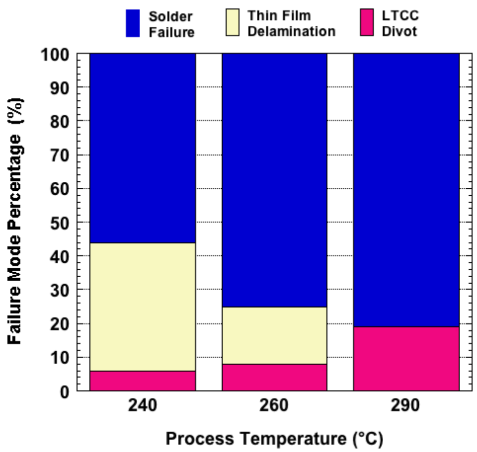
SAC396 solder; 290°C, 120s

Results – Soldering Process Parameters

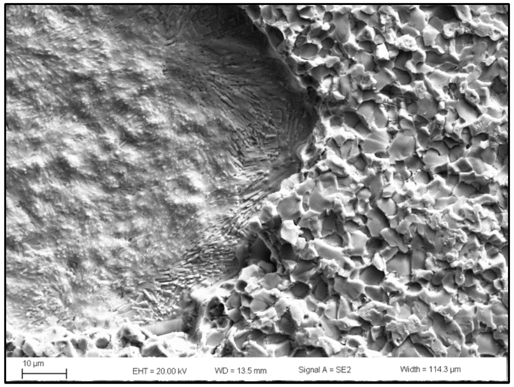
◆ **An analysis was made, based on all three data sources:**



Pull strength



Failure mode analysis

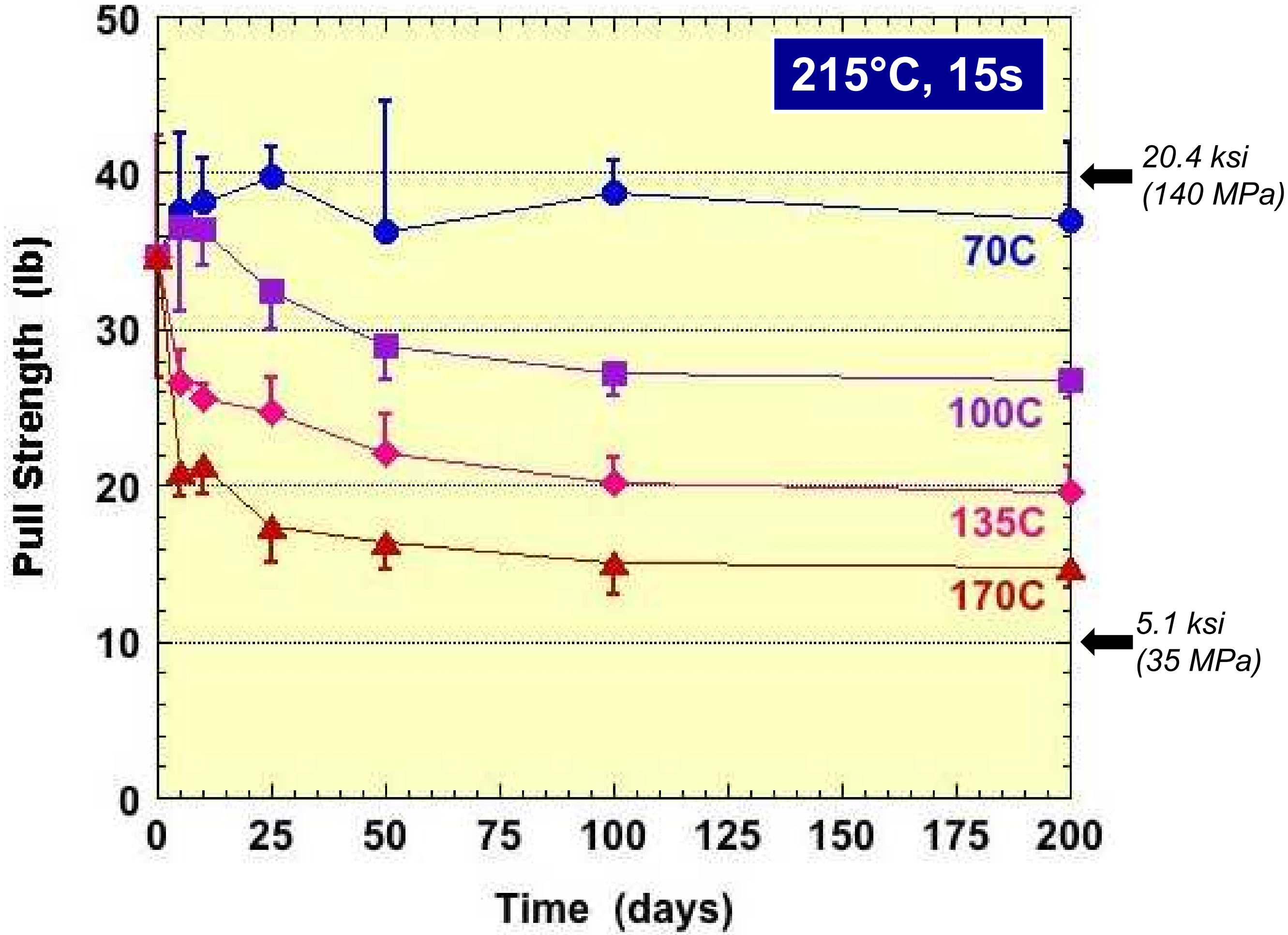


Fracture morphology

- **All joint strengths exceeded that of the bulk solder.**
- **The strength loss with soldering time and temperature was correlated to an increase of the solder failure mode.**
- **Increased solder failure mode was accompanied by an increased fracture path along the (Cu-Au)-Sn IMC at the solder/Cu pin interface.**
- **The divot failure mode maintained a presence, the cause of which were *higher CTE mismatch residual stresses generated in the LTCC bulk*.**

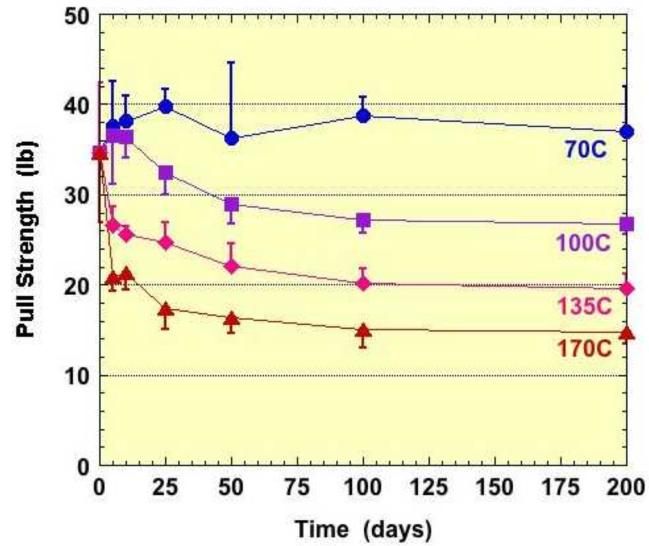
Results – Solid State Aging, Sn-Pb Solder Joints

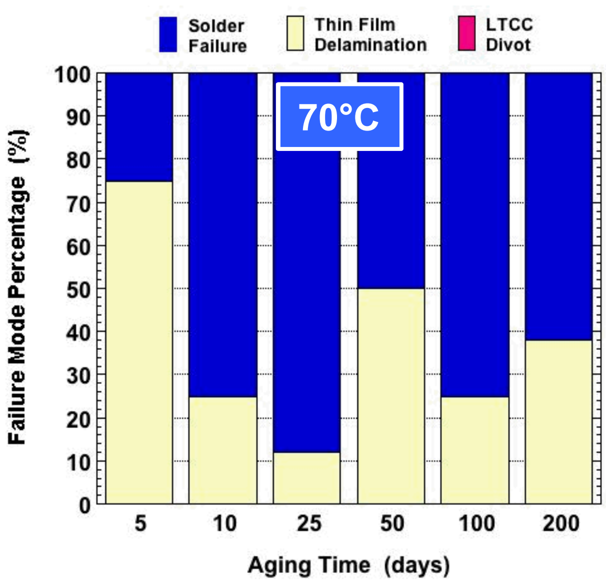
- The Sn-Pb solder joints processed at 215°C for 15s experienced a loss of pull strength with an increase of solid-state aging.

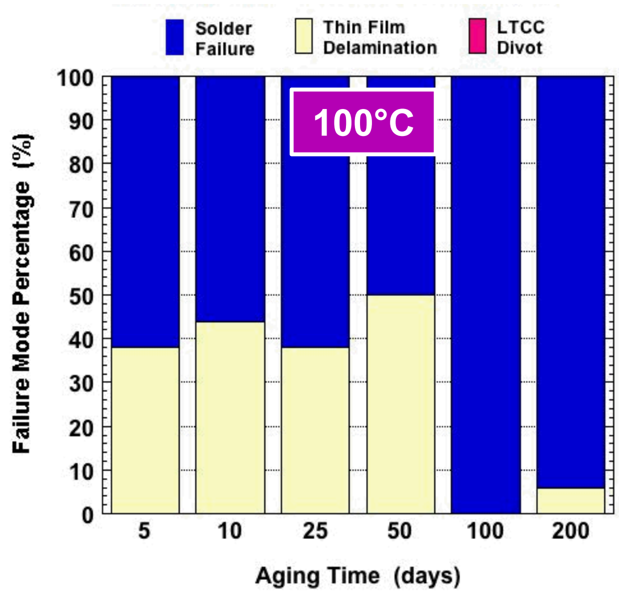


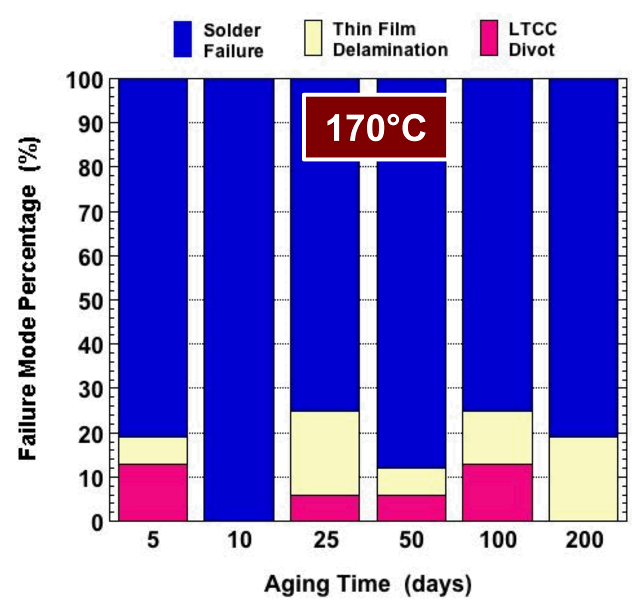
Results – Solid State Aging, Sn-Pb Solder Joints

- **The pull strength data were correlated to the failure modes:**
  - ***Solder failure*** **mode increased with the severity of aging at the expense of the delamination failure mode.**
  - ***Divot failure*** **mode appeared in the 135°C and 170°C data, albeit, at low percentages.**



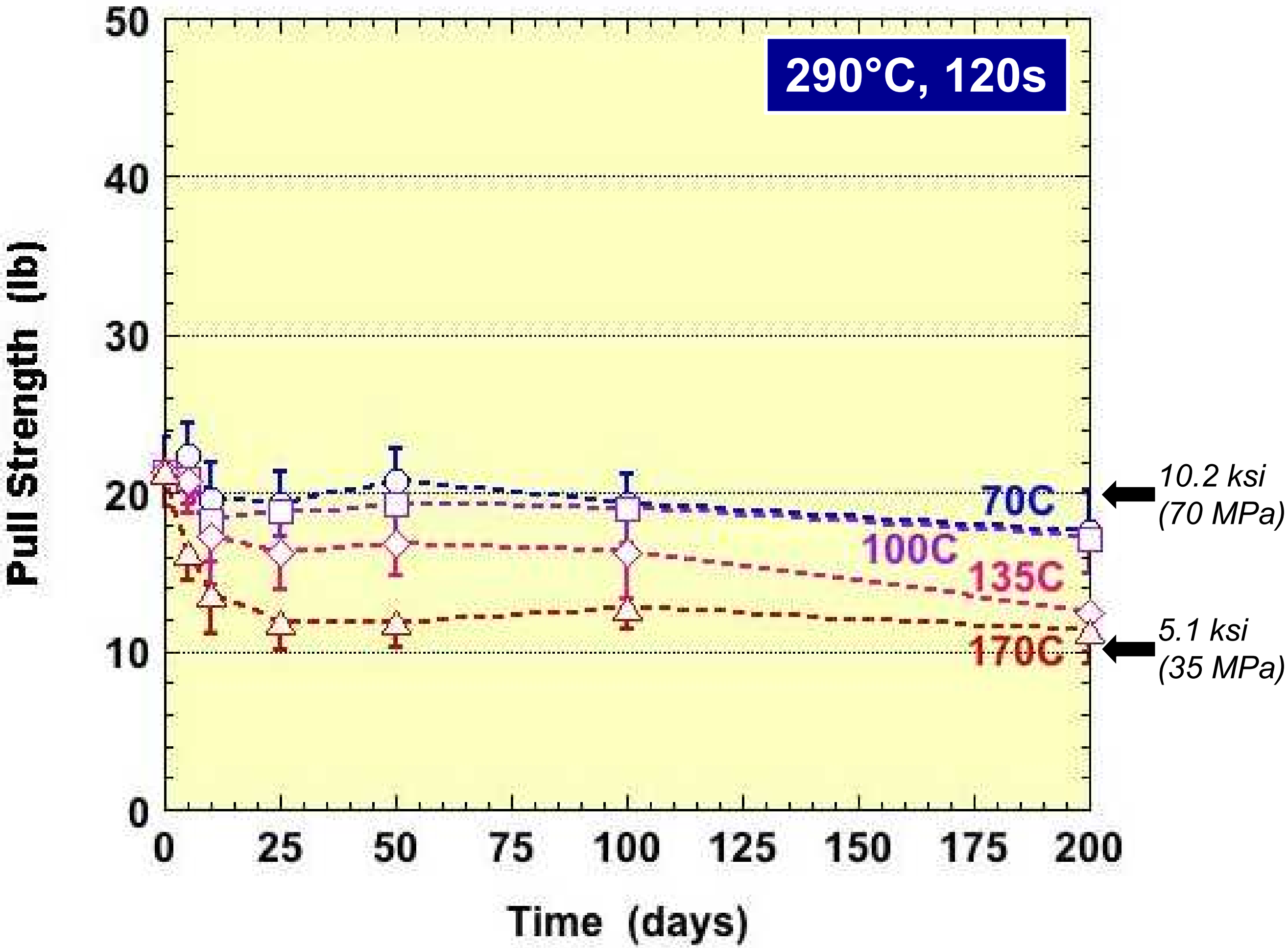






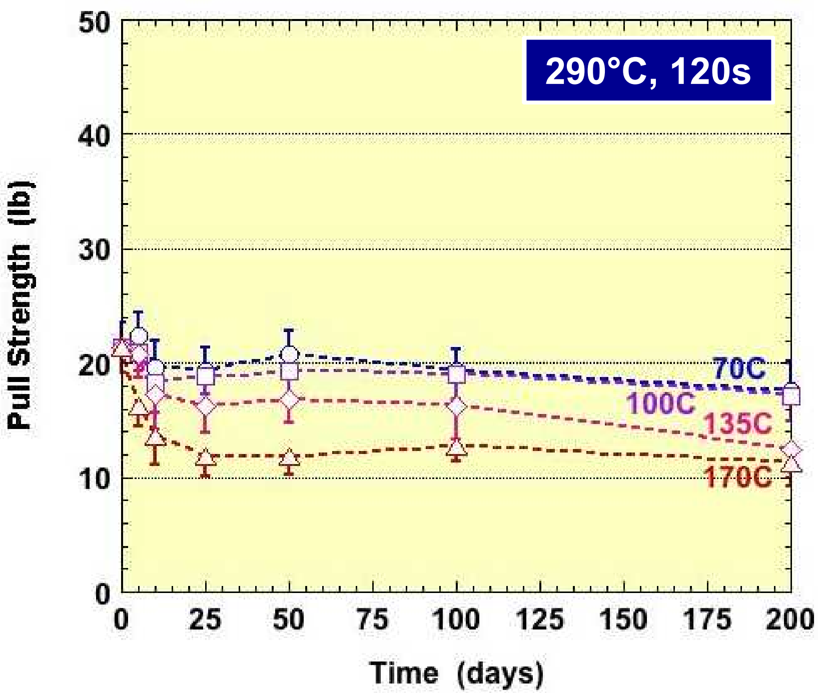
Results – Solid State Aging, Sn-Pb Solder Joints

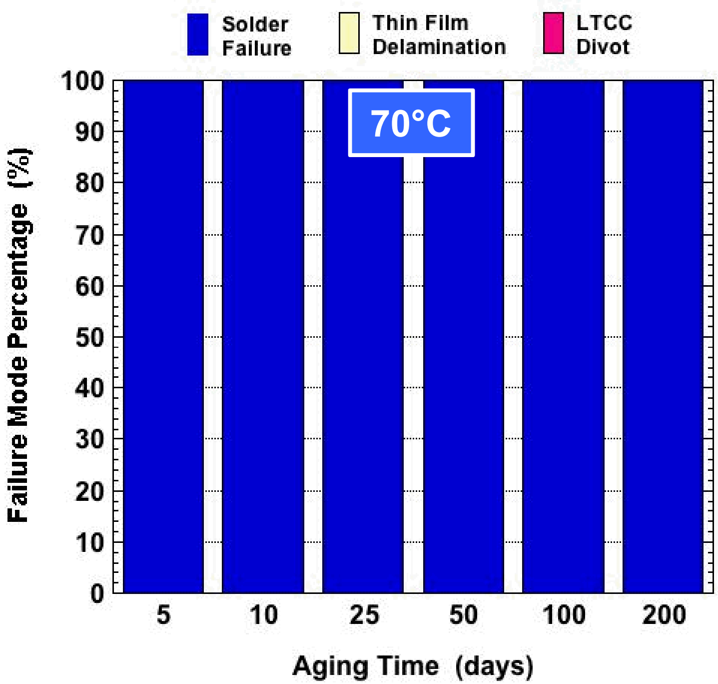
- The Sn-Pb solder joints processed at 290°C for 120s experienced a loss of pull strength with an increase of solid-state aging.



Results – Solid State Aging, Sn-Pb Solder Joints

- The fracture sites exhibited exclusively, or nearly so, the solder failure mode for *all* aging temperatures and time durations.





- The lower strength limit is similar between [215°C, 15s] and [290°C, 120s].
- The more severe process conditions "collapsed," more effectively, the pull strengths following solid-state aging.

Summary

- **A study was performed to evaluate the tensile strength of Sn-Pb and SAC396 solder joints made to 0.20Ti-4.0Cu-2.0Pt-0.25Au (μm) thin films on low-temperature, co-fired ceramic (LTCC) substrates.**
- **The strength performance was evaluated as a function of process (soldering) parameters for both Sn-Pb and SAC396 solder joints.**
- **The Sn-Pb joint strengths were also assessed as a function of solid-state aging (70 – 170° C; 5 – 200 days).**
- ***Both solders* exhibited similar pull strengths as well as the same strength loss with increased severity of the process parameters.**
    - **All strength magnitudes were more-than-adequate to meet the needs of engineering applications.**
    - **The strength loss was attributed in both cases to an increase in the solder failure mode – specifically, the *(Cu-Au)-Sn IMC layer*.**

Summary

- **The solid-state aging caused the Sn-Pb solder joints to exhibit a loss of pull strength with increased temperature and time.**
  - **However, the strength loss was sensitive to the process (soldering) parameters.**
  - ***It appeared that the harsher process parameters accelerated, rather than superimposed upon, the effects of solid-state aging.***

- **The explicit effect had by the Ti-Cu-Pt-Au thin film in the strength of the Sn-Pb and SAC396 solder joints included these factors:**
  - **The role of Au in the IMC formation.**
  - **The thin film delamination failure mode that predominated the high pull strengths.**
  - **Formation of the Pt-Sn IMC layer observed after solid-state aging …** ***stay tuned !!!***