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Thermal Testing and Quality Assurance of BGA, LCC, & QFN Electronic Packages

Graduate Project

The University of New Mexico
Department of Mechanical Engineering

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Introduction

The purpose of this project is to experimentally validate the thermal fatigue life of solder interconnects for a variety of surface mount electronic packages. Over the years, there has been a significant amount of research and analysis in the fracture of solder joints on printed circuit boards. Solder is important in the mechanical and electronic functionality of the component. It is important throughout the life of the product that the solder remains crack and fracture free. The specific type of solder used in this experiment is a 63Sn37Pb eutectic alloy. Each package was surrounded conformal coating or underfill material.

Conformal coating helps protect the board from environments such as electrostatic discharge and humidity. It is commonly used in broad types of engineering disciplines such as commercial, military, research and development, etc. Conformal coating can also pose a risk for the life of the board because of the difference it has in the thermal expansion coefficient. This can greatly decrease the life of the product if it regularly sees high temperature variations. This leads to a shorter fatigue life of the solder. The fatigue life is a common mechanical problem in the field of electronic devices. Adding underfill can help the fatigue life of the solder. However, applying underfill adds time to manufacturing and production. This ultimately increases the cost per unit. The study of conformal coated printed circuit boards with and without underfills was done to three different surface mount electronic packages.

The electronic packages studied were Leadless Ceramic Chips (LCC), Quad Flat No-Lead (QFN) packages, and Ball Grid Arrays (BGA). When the package was not underfilled, the coating was allowed to flow underneath. The assembly was analyzed and tested to obtain the best available combination of conformal coating, underfill, and potting to design the most robust and reliable circuit board. Different types of conformal coatings were tested with and without underfills for each chip. Six of each scenario was manufactured for the sake of individual defects and imperfections.

Finite Element Analysis (FEA) was performed by an engineer at Sandia Laboratories for both LCC and QFN packages. From the FEA results, an acceleration profile was derived and number of temperature cycles to fail the solder interconnects were found. Experimentation was done as a secondary measure to validate this data to show confidence in this analysis.

Accelerated testing functions as a quality check for the product. Accelerated testing is extremely useful in the research and development phase of engineering. It can save money from the potential of early life defects and the costs that come along with warranties. Accelerated testing makes a weaker design more robust and checks the reliability of a strong design in a shorter amount of time. It is extremely helpful in a world where deliverables are in high demand and scheduling is tight. There are many different types of acceleration tests. Accelerated testing helps the engineer gain an understanding of what needs to be improved and what works well.

Our circuit boards were accelerated inside closed a thermal chamber because of the high number of use cycles.

The ultimate goal of this experimentation is to help identify what will prevent any premature cracking or fracturing in the solder alloy. It is important to understand if underfilling each component is or is not needed. If the number of cycles to failure without underfill far exceeds the design life of the unit, then underfill is not necessary.

Materials

There can be many different materials that make up electronic package assemblies such as underfills and coatings. The package protects the semiconductor from a variety of different environments that the circuit board is exposed to during assembly, shipping and handling, and operations of the device. However a package can cause thermal mismatches due to the different materials that come into close contact with one another. For this project, different coatings were studied with and without underfill. Due to the difference in thermal properties, the life of the solder can be drastically reduced if no underfill is used.

Conformal coatings protect the electronic components on a circuit board from environmental and mechanical interactions such as moisture, humidity, particulates, corrosion, as well as electrostatic discharge and vibration. Coating can be fairly simple to apply onto a Printed Circuit Board (PCB). Before coating the board, the surface and all components should be clean and free from all particulates and foreign object debris (FOD). Coatings can be dipped, sprayed, or spread onto a board. Uvikote 7503 and Arathane 5750 were both chosen as the two types of coatings studied. Arathane is Military Specification (Mil spec) approved and will cure within 7 days at 20°C. It is translucent in appearance and is made up of a two part polyurethane compound [2]. Uvikote 7503 is also a translucent, Mil Spec approved coating , that is made up of two components [1]. When exposed to ultraviolet (UV) light, Uvikote is able to cure to the electronics assembly. At 23°C, Uvikote can be postcured in 14 days.

Every circuit board was experimentally tested in conformal coating. Half of these units were underfilled. Underfill serves a quality purpose for protecting the solder joints from shock, vibration and various thermal environments. If the product undergoes these various stresses, underfilling can increase the reliability, and extend the life of the electronic package. For underfill to be applied, it is usually dispensed along the edge of the package in a straight line. It then spreads under the rest of the chip. Underfill covers the top surface of the PCB and the bottom surface of the chip. Depending on the brand, it can take between 5 minutes and 1.5 hours to cure [27]. It makes the product more rigid, and is very effective in mitigating coefficient of thermal expansion (CTE) mismatching [31]. For the underfilled boards in these environmental tests, Almatis 20% was used. The mechanical properties of the underfill material can change as the temperature goes towards the glass transition temperature of 80°C. Table 1 shows the mechanical properties of Uvikote, Arathane, and Almatis 20%.

Material	Young's Modulus (MPa)	Poisson's Ratio	Thermal Expansion Coefficient $(1/^oC)$	Glass Transition Temperature (°C)
Arathane 5750 Conformal Coat	8.80	0.499267	190.0×10^{-6}	-70
Uvikote 7503 Conformal Coat	28.0	0.497667	222.0×10^{-6}	-55
Almatis 20% Fill Underfill	5,443	0.3684	40.60×10^{-6}	80

Table 1. Coating and Underfill Mechanical Properties [6]

Solder joints provide mechanical connection and electrical conduction by making contact from the electronic package to the substrate. It has a low melting point, it's affordable, and is favorable for contact onto metallic surfaces [12]. 63Sn37Pb was used in this research. There has been a considerable amount of research on the mechanical characterization of Tin-Lead solder. Thermal stress is one of the main reasons why solder fails. The amount of strain the solder interconnects experience varies on the location and geometry. It is treated as a very ductile material, and is assumed to be isotropic. The alloy's material properties vary significantly as the temperature ranges from -60 to 100°C. The mechanical properties of 63Sn37Pb at different temperatures are shown in Table 2.

Temperature (^oC)	-60.0	21.0	100.0
Young's Modulus (MPa)	48,276	43,255	36,860
Poisson's Ratio	0.38	0.39	0.40
Thermal Exp. Coef. $(1/^oC)$	25.0×10^{-6}		
Melting Temperature (°C)	183		

Table 2. 63Sn37Pb Solder Mechanical Properties [6]

It is important to note that there are different standards and specifications that are undergone when soldering. Sandia follows a requirement for soldering based off of space and medical applications based on the standard defined by IPC-JSTD-001F [34]. Soldering is based on class 3, high performance, and harsh environment electronic products. This class is more demanding than the other three, and states equipment will have little to no down time, and must function properly when required.

Polyimide was chosen for each PCB tested in these experiments. Along with FR-4, Polyimide is an extremely popular choice for the PCB material. The different Modulii, CTEs, and Poisson's ratios are showed in table 3. These material constants for underfill, coating, 63Sn37Pb solder, and polyimide were necessary in determining the FEA results that were performed.

Material	Arlon 85N
Young's Modulus XX, ZZ (MPa)	22,069
Young's Modulus YY (MPa)	5,517
Poisson's Ratio YX	0.0234
Poisson's Ratio ZX	0.150
Poisson's Ratio ZY	0.380
Shear Modulus XY (MPa)	5,545
Shear Modulus YZ (MPa)	5,545
Shear Modulus ZX (MPa)	9,593
Thermal Expansion Coefficient XX,ZZ (1/°C)	17.0×10^{-6}
Thermal Expansion Coefficient YY (1/°C)	55.0×10^{-6}

Table 3. Polyimide Mechanical Properties [6]

Surface Mount Technology

There are many different kinds of electronic packages that do not require the use of through holes in a circuit board. Surface Mount Technology (SMT) started to become widely used in the 1980's [30]. SMTs have many different forms. Examples are semiconductors, transistors, and capacitors. Quad Flat No Lead (QFN), Leadless Ceramic Chips (LCC) and Ball Grid Arrays (BGA) are all of the semiconductor family. All of these have their own advantages, disadvantages, and applications. Adding these components into the design of regular PCBs greatly reduces the manufacturing cost. Pick and place techniques help simplify the manufacturing process.

Quad Flat No Lead

The Quad Flat No Lead (QFN) chip carrier is a semiconductor package [15]. The solder connections are present underneath the perimeter of the housing. This can pose limitations for the overall design because the number of interconnects is limited. QFNs are soldered on the lands to make contact onto the PCB. They can be used in applications such as Bluetooth devices, and wireless headsets. These chip carriers are light in weight and typically carry a low profile. This can be advantageous for the placement of PCBs in thin assemblies. Figure 1 shows the testing specimen for these experiments.

Figure 1. [18]

Leadless Ceramic Chip

There are a few advantages to using a Leadless Ceramic Chip (LCC). They typically have a low number of joints, are rugged, have low inductance, and are affordable [10]. The performance of an LCC is adequate compared to its competitors. LCC's can be susceptible to potentially large temperature differences. The change in temperature can lead to cracks and even fractures in the joint. Figure 2 shows the LCC laid out over the board. The chip carrier package used in this experiment has 24 solder interconnects. Like the QFN, the LCC package has its solder contacts around the perimeter.

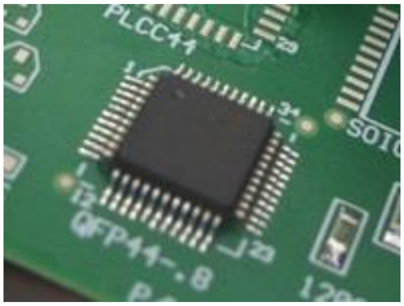

Figure 2. [23]

Ball Grid Arrays

An alternative to leadless packages are Ball Grid Arrays (BGA). BGAs are a common component in integrated circuit technology [3]. They are also referred to as a flip chip package, and are permanently attached to the integrated circuit. They are recognizable from the grid-like orientation that the solder balls are placed. Like the QFN and LCC, the number of solder points is usually contained in the name of the BGA, for example, BGA 437 has 437 solder points. Instead of having interconnects around the perimeter of the chip, BGAs are used on the bottom surface and occupy a smaller space. Figure 3 illustrates the BGA on the bottom of the chip carrier package.

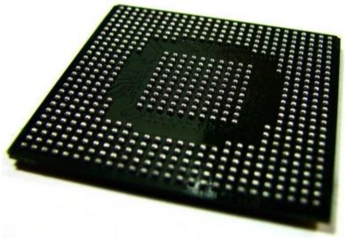

Figure 3. [4]

In addition to saving more space on the board, BGAs have improved thermal performance compared to QFNs and LCCs. They also provide a smaller thickness for the overall electronics assembly. This is essential in tight close fitting assemblies and can meet the requirements of a mechanical envelope easier than other packages. While BGAs offer several advantages, there are also disadvantages that are commonly encountered. The installation cost is typically more expensive because of the special alignment and mounting tools that are needed. BGAs are also more difficult to assemble due to the close spacing of the interconnects, which makes the assembly by hand almost impossible.   The solder balls on the package are first heated heated. The BGA is then flipped and is able to be aligned to the circuit board because of surface tension. The solder balls are cooled and the distance between each one remains consistent.

Manufacturing

The PCBs being tested were all fabricated and manufactured at Sandia. The boards were populated by Gary Patrizi. Each board had its own specific electronic package placed and soldered on top. The boards had 32 total spots for components to be placed in and came in a 5x6 grid with 2 extra pads near the top. It was decided that each row had a different combination of underfill and coating from one another. It is currently being discussed on what to do test on row 5. Each rows specification are shown in table 4.

Row	Conformal Coating	Almatis 20% Underfill
1	Uvikote	N
2	Uvikote	Y
3	Arathane	N
4	Arathane	Y
5	Uvikote or Arathane	?

Table 4. PCB Coating and Underfill Layout

Thermal Chamber

The thermal chamber is manufactured by Associated Environmental Systems. The model number is SD-308. The temperature ranges from -65 to 200°C. The internal volume is 5 cubic feet. This chamber was convenient because the test could be run over night and on weekends. The chamber uses a chiller as the cooling agent instead of liquid nitrogen which has to be continuously monitored. This chamber has simple usability and settings that allow the user to write a profile and allow it to cycle the temperature automatically. It is standard procedure to write the profile as a check list, to make it easy to visualize when initially writing the profile. This check list is listed in the Appendix.

Figure 4. Associated Electronics Environmental Chamber

Figures 5 & 6. Associated Environmental Systems Internal Chamber and DAQ.

The other chamber considered for experimentation was a standard Highly Accelerated Life Test (HALT) chamber. The temperature range is -100 to 200°C. The advantage of using a HALT chamber instead of a standard chamber is the fast temperature ramp up times to quickly go in between temperature extremes. The HALT chamber wasn't used due to schedule conflicts with other testing groups. This particular testing also wasn't used because the fast ramp times to temperature wouldn't be fully taken advantage of and weren't necessarily needed.

Thermal Cycling

Almost every engineering design is exposed to a set of temperature differences during its lifetime. These temperature changes can happen in thousands or even millions of cycles. During the high temperature phase the material can experience creep depending on the time of the cycle, temperature extreme and melting point of the material. Through the cycling process the combinations of materials can be stressed from thermal expansion and contraction which can lead to crack appearances leading to fractures as explained later.

For this project the Unit Under Test (UUT) will be exposed to a maximum and minimum temperature and will be held at 20 minute dwell times for each cycle. This leads to a compressive and tensile strain hold for the cold and hot temperatures respectively. An example of this can be shown in figure 4 [19].

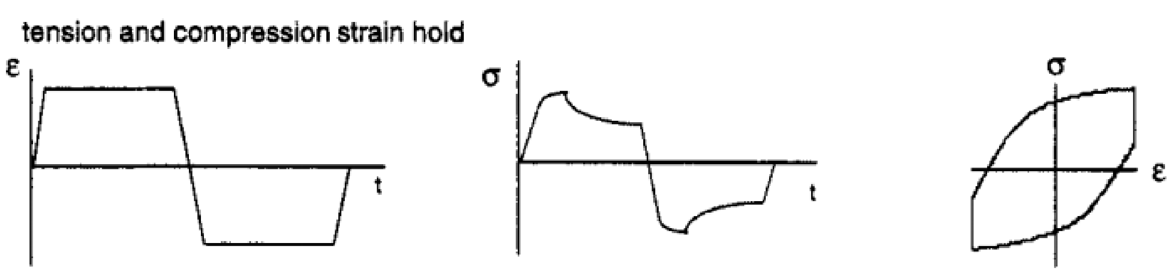

Figure 4. Strain Hold for Thermal Cycling (Remy, 1994)

The strain is held constant over a period of time for both cold and hot temperature cycles. The middle graph shows that as the strain is held to a constant value the stress is then relaxed. When stress is plotted as a function of strain the graph shows the constant strain as the vertical component of the graph.

Because of the difficult constraints and geometries of electronic packaging, FEA is usually performed to show the contour plots of stress and strain for thermal cycling [22]. Without explaining the theory in too much detail, the finite element method derives strain from the node deformation. The stress is in tern found from the strain. The equivalent strain and Von Mises stress have been used in the past to quantify the state of the solder [37] from the FEA. The Von Mises stress in terms of the principle stresses is defined as:

$$\sigma_{vm} = \left(\frac{1}{\sqrt{2}}\right) * \sqrt{(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2}$$

Von Mises stress is of course compared to the yield stress σ_y, in a conservative manner. The equivalent strain is defined in terms of the calculated principle strains as:

$$\epsilon_e = \left(\frac{\sqrt{2}}{3}\right) * \sqrt{(\epsilon_1 - \epsilon_2)^2 + (\epsilon_2 - \epsilon_3)^2 + (\epsilon_3 - \epsilon_1)^2}$$

For this testing, the thermal cycle consisted of temperature extremes of -20 and 70°C. The ramp rates were determined to be 3°C/min, and the dwell time for each temperature extreme was 20 minutes. Figure 7 shows a graphical representation of the thermal cycle profile starting at ambient.

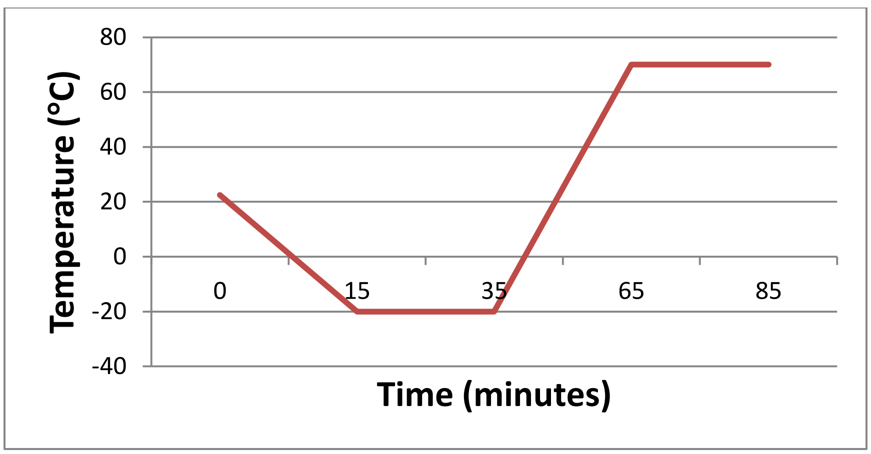

Figure 7. Thermal Cycle Profile

After a certain number of cycles were preformed, the UUTs were brought back down to ambient and held there until the user could safely remove them from the thermal chamber. The explanation of how this profile was derived is explained in the acceleration testing section.

Thermal Expansion

The change in temperature is critical to consider when designing PCBs. Depending on the materials in the assembly, the constraints, and the difference in temperature that the product experiences, there can be plastic deformation from thermal stresses alone. For there to not be any plastic deformation the temperature difference has to stay small enough to stay in the elastic range of the material. As the temperature increases, there is a positive change in length on the material leading to a positive normal strain. Conversely, as the temperature decreases, the length becomes smaller, and the material exhibits a negative normal strain. The Coefficient of Thermal Expansion (CTE) is a constant material property that describes how the material reacts to a temperature change. In many instances, engineers are unable to control the environment of their product. This is why it is important to select materials in an assembly that have as close of a coefficient of thermal expansion as possible. The change in length a material undergoes from a temperature difference is:

$$\Delta l = \alpha l_0 \Delta T$$

Where α is the linear coefficient of thermal expansion. It is defined as strain per unit temperature. For Isotropic materials, the change in area and volume expand or contract two and three times as much as the length does respectively. How a material expands or contracts depends on the bonds of the materials atoms. For example: silicon carbide and diamond have strong atomic bonds and have higher CTE values than common metals such as stainless steel. It is important to note that if the material being subjected to a change in temperature is free, there will be no induced stress. Thermal stresses can appear in a couple of ways. The first would be if the material is under constraint. It can also depend on how other interacting materials react to the heat. Other instances would be if the temperature distribution is non-uniform. Examples of this would be external heat, or if the temperature profile along the material is transient. In electronic packages, the thermal stress is caused by both of these factors.

Thermal expansion happens in all three directions. It also does not affect the shear strain components in the strain tensor. The normal strains can be defined as:

$$\epsilon_{11} = \left(\frac{1}{E}\right)[\sigma_{11} - \nu(\sigma_{22} + \sigma_{33})] + \epsilon_{11}^{p} + \alpha\Delta T$$
$$\epsilon_{22} = \left(\frac{1}{E}\right)[\sigma_{22} - \nu(\sigma_{11} + \sigma_{33})] + \epsilon_{22}^{p} + \alpha\Delta T$$

$$\epsilon_{33} = \left(\frac{1}{E}\right)[\sigma_{33} - \nu(\sigma_{11} + \sigma_{22})] + \epsilon_{33}^{p} + \alpha\Delta T$$

The plastic strain that has already taken place in the material is defined as ϵ_{ij}^{p}. This project focuses on the thermal cycling stress analysis and does not add any mechanical force or vibration into the testing environment.

Electronic Package Thermal Stress

When two or more objects meet at an interface, the change in temperature often cannot be neglected because of the differing CTE values. As already described, a non-uniform temperature profile, or constraint scenarios can cause thermal stress. Both of these cases are commonly seen in electronic packaging. Individual parts of the assembly will exhibit more strain than others when an assembly of materials have different CTE constants. Ways to maximize the life of the solder joint is to increase the height h, minimize the CTE mismatching and to keep the size of the electronic package as small as possible [36].

Shown in the previous tables, the CTE for Arathane and Uvikote are significantly greater than Almatis 20%, 63Sn37Pb, and Polyimide. The conformal coating is able to flow underneath the electronic packaging and is allowed to cure to test specimens where no underfill material is used. As the board is in operation the coating expands faster than the rest of the assembly as the heat flows from the package to the substrate. This poses a risk for the reliability of the solder joints. When the heat migrates from the package to the substrate, the coating expands at a much faster rate than the solder and with the added constraints; the solder is under a much more stressed state. In a cross section such as figure 8 [21], the solder takes up considerable less area than the coating does. The solder can typically be neglected when analyzing this layer of the composite. The amount of thermal stress resulting in the coating layer can cause the joints to fracture or crack. This poses many risks for the component such as reliability and life expectancy.

Horizontal displacements dominate the deformation in electronic packages. Electronic packages are often symmetric about an axis that is in the center of the chip. There is no resulting deformation from the differing CTE values along the axis of symmetry. As the distance away from the axis increases, the resulting stresses also increase. Figure 8 illustrates how the package responds to the CTE mismatch [21].

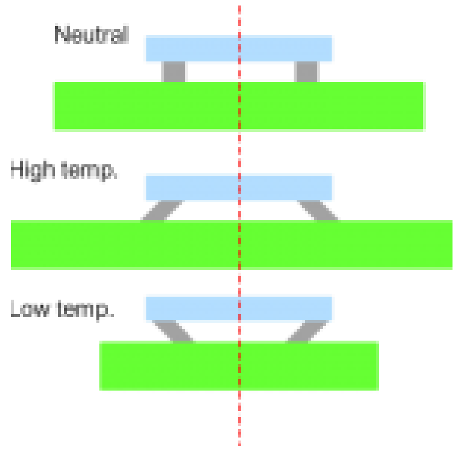

Figure 8. Solder Joint Strain from CTE Mismatch (Sharon, DFR Solutions)

When the temperature increases, the materials expand and the resulting force pulls the solder away from the symmetric axis. As the temperature decreases, the materials shrink at various amounts depending on their given CTE values, and a compressive like force pulls the solder toward the axis of symmetry. The distance from the symmetric axis to the solder joint is referred to as the Distance to the Neutral Point or (DNP). As this DNP increases, so does the stress that the solder joint experiences.

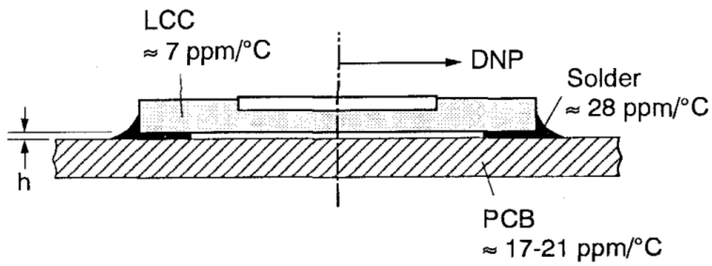

Figure 9. Thermal Expansion of an LCC Package (Han/Guo, 1996)

Figure 9 shows the approximate CTE values corresponding to each assembly material for an LCC [11]. This is also similar for a QFN. For electronic package assemblies, the maximum average shear strain of a solder joint $\gamma_{ave}^{max}$is:

$$\gamma_{ave}^{max} = DNP * (\alpha^{PCB} - \alpha^{LCC}) * \Delta T * \frac{1}{h}$$

h is equivalent to the solder joint thickness. The height can be characterized by the distance the LCC is away from the PCB.

Figure 10 shows the cross sectional layout of a common BGA component and how it is susceptible to thermal expansion. As already stated, the DNP is in the center and the strain becomes larger the further away.

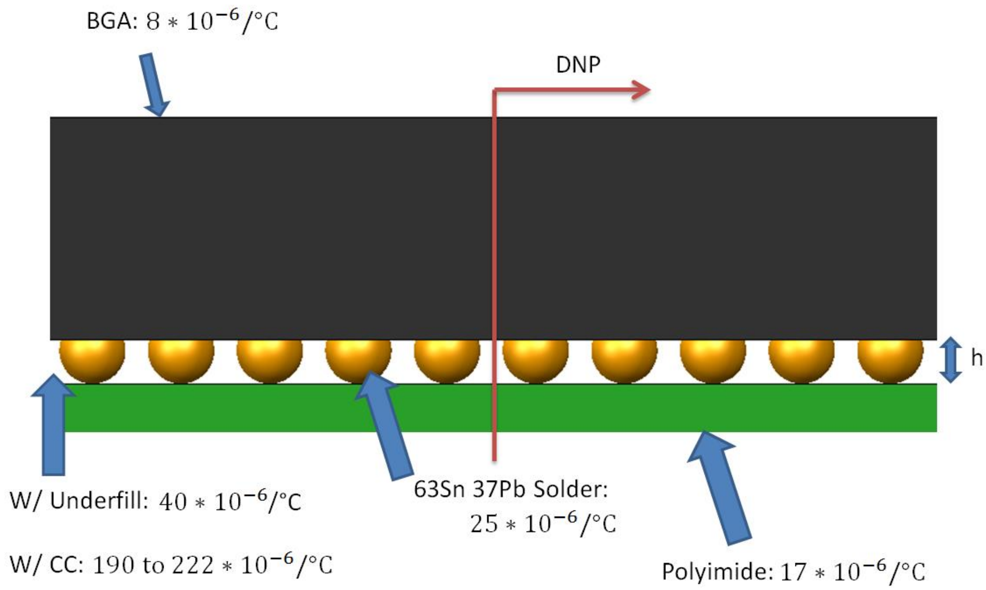

Figure 10. Thermal Expansion of a BGA Package

For void growth that leads to solder fractures, the equation below relates the stress as a function of temperature extremes [14].

$$\sigma_t = 3\Delta\alpha\Delta TK$$

Where *K* is the bulk modulus of the conductor. This assumes that the passivation film that covers the conductor, such as silicon nitride, remains rigid.

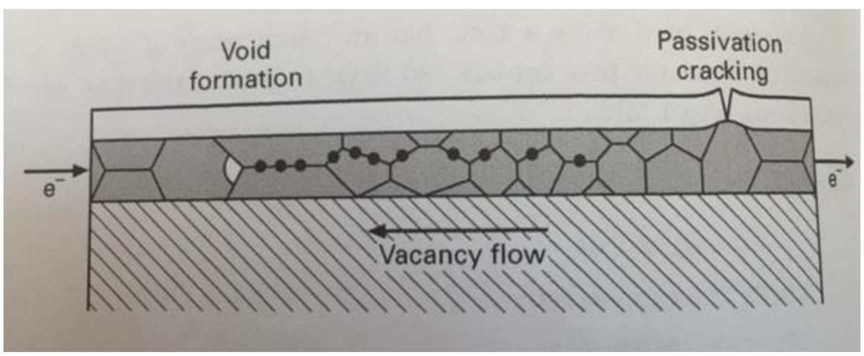

Figure 11. (Meyers, 2009)

Figure 11 portrays how the solder interconnect, (in this case made of aluminum) is covered by a passivation layer over a silicon board [14]. It can be seen that the vacancy flow is in the opposite direction of the electron flow. This also leads to the solder alloy fracturing.

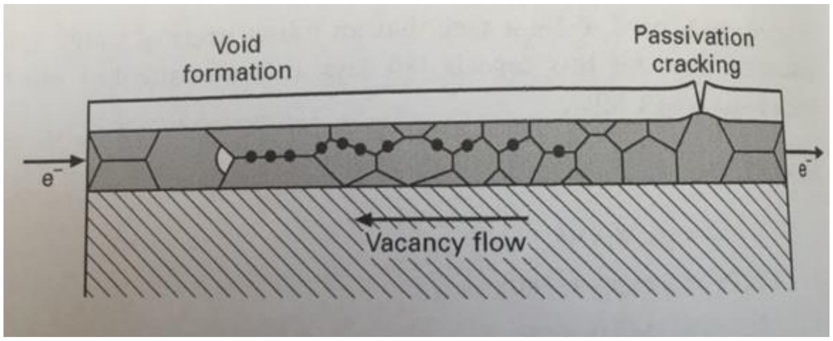

Figure 12. (Meyers, 2009)

Figure 12 also shows the vacancy flow in the opposite direction of the electrons, and how the passivation layer cracks due to the formation and buildup of voids that result from the thermal mismatch.

Creep

Creep is defined as material plastically deforming at a constant stress at a temperature a fraction of the melting point. For creep to take place, the temperature of the environment is typically in the range of 40% to 65% of the melting temperature [14]. The material undergoes both mechanical and chemical degradation during this environment. Mechanical degradation depicts how the material expands as time increases. Chemical degradation describes how the material reacts with its environment.

Creep can especially take place because of the low melting point of solder. Because the melting temperature of 63Sn-37Pb solder is 456K. Creep must be taken into consideration during the 20 minute dwell time at 393K. This can very well induce a fracture in the solder alloy. Cavities start to form in between grain boundaries after creep has taken place. Once this happens the cavities begin to grow and come closer to one another ultimately leading to a fracture. The cracks appear at the grain boundaries. There are equations that predict the time to failure.

$$\dot{\epsilon} t_r = k$$

The Monkman-Grant equation is described above [14]. It is dependent on the material's parameters. Where $\dot{\epsilon_s}$is the steady state creep rate, t_r is the time to rupture, and k is the material constant.

Glass Transition Temperature

Part of the process in choosing an appropriate thermal profile was to take into the glass transition temperature (T_g) of the underfill, coating, and solder alloys. If testing temperature falls below the T_g, the material can function as a glass, meaning that no specific order exists between the atoms [14]. This phenomenon takes place for metals, polymers, and ceramics. The packing between the atoms is less effective when they are in a glassy state. The atoms are packed in a random order and will occupy more space than a crystalline structure.

The higher extreme was bounded by the glass transition temperature of Almatis 20% as 80°C. Uvikote and Arathane were found to be -55°C [1] and -69°C [2] respectfully. To stay as close to this temperature as possible, it ensures that the underfill remains in a glass state. This will be similar to the real life scenario of the product.

Crack Propagation

If the SnPb eutectic solder does become damaged from the thermal cycling it is still possible for the unit to function electrically. It is simply not enough diligence to daisy chain the unit, and perform a continuity check. The cracked solder still qualifies as mechanical damage to the unit. The crack can easily transform into a fracture if stressed further over time. It is not until the lead is fully open where current will not be able to flow through the joint. This will in turn cause a hard failure in the device. There are different modes that describe how cracks are allowed to propagate. They are often referred to as opening, in-plane shear, and out-of-plane shear. The crack propagation modes are presented in figure 13 [16].

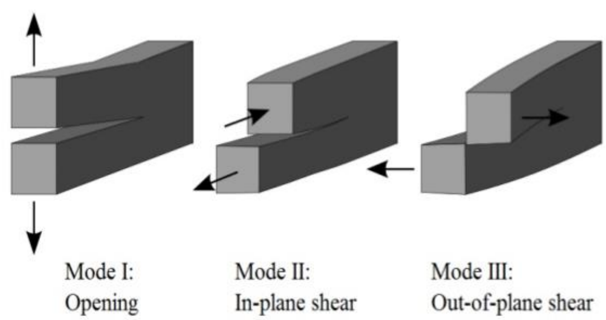

Figure 13. Modes of Failure (Patil, 2014)

Thermal cycling leads to the "open" case of crack propagation in solder joints. Assuming plane strain, the fracture toughness can be described in terms of stress [14]:

$$K_{IC} = Y\sigma\sqrt{\pi a}$$

Where a is the semi-length of the crack, Y is called the stress intensity factor and is geometry dependent. Once a crack is initiated it becomes a stress concentrator. The fracture toughness of the solder alloy is 8.36 $MPa\sqrt{m}$ [32]. This was determined from the "open" crack propagation case. According to the Griffith criterion, a crack will become larger if the elastic strain energy released is larger than the surface energy from the new crack surfaces. Under most cases the solder joint does not fail at the interface. It usually fractures just below [8]. Figure 14 illustrates a fractured joint under thermal fatigue.

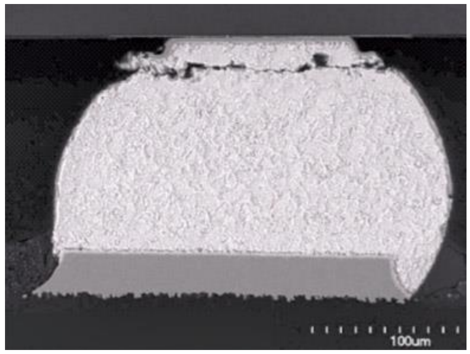

Figure 14. Common Solder Fracture (Edwards, 2012)

Through the FEA model it is possible to predict where the cracking will occur given the geometry. This will be analyzed more after testing with x-ray analysis.

FEA Study

The LCC and QFN electronic packages were modeled using the FEA software developed at Sandia called "CUBIT". These models were simplified due to geometry and to save computational processing time as explained above. There were many different types of modeling scenarios for LCC and QFN chips. Due to the difficulties to achieve some of these scenarios physically the experimentation was scaled down to conformal coating with and without underfill. For example, it would be difficult at the component level to ensure there was a void under an LCC while the PCB is coated. The temperature extremes that were simulated were -50 to 85°C. The dwell times were for 1.5 hours. As expected, the number of cycles to failure was higher if the package was not underfilled. Experimentation was not performed in the same manner as the modeling. The temperature range was narrower, and the dwell time was taken to be 20 minutes to perform a higher number of cycles. This adds a lower number of cycles to failure explained in the acceleration section below.

Environment Safety and Health (ES&H)

There were a couple of issues and concerns pertaining to ES&H while testing. While checking for functionality in between testing cycles, time had to be taken to bring the board up to a safe "usable" temperature. After the extreme cycles were complete, the board was brought up to ambient conditions and held at a constant temperature in the chamber for 20 minutes. The thermocouples were also monitored to verify the parts were at a safe temperature. The use of SnPb solder did not bring any ES&H concerns during testing and inspection. Strict Sandia safety procedures were practiced when soldering the chips into the board. The thermal chamber is secured with a stainless steel latch and when opened, the safety switch disengages and the thermal cycling stops. There is also a minimal amount of outgassing produced from the coating during the experiment [1& 2].

Acceleration Testing

Accelerating the mechanical environment is a useful practice that is rapidly gaining popularity. Perhaps the most useful aspect of accelerating the mechanical testing is to save time, and ultimately save money. The primary goal of acceleration testing is to gain an understanding of the performance and life of the product in a timely manner. Engineers can perform the test quickly and efficiently without the worry of extending deadlines and design phase changes. Acceleration Testing (AT) is part of the field known as quality and qualification engineering. This concept can save millions of dollars in qualifying the product in the design phase rather than spending time repairing each unit after it has already hit production. It is important to consider a few factors when accelerating thermal tests. One can increase the use rate of the product lifespan or the aging rate to accelerate the reliability. There are many different mathematical models that can be used to see how fast a product is accelerated. It is extremely important to determine the correct acceleration profile for the component. Choosing an incorrect profile can lead to different failure modes and will lead to useless information for the product. For this project the aging rate was increased by altering the use environments the product functions in.

The sole purpose of accelerated testing is to check for possible failure modes in the unit in the R&D phase rather than after it has already hit production.   This is done by making the test environments more extreme than the use environment. The temperature environment was made more severe by increasing the maximum and minimum temperature extremes, the temperature ramp rate, and the number of cycles performed. The temperature extremes, ramp up and down rate, dwell time, and number of cycles all have a number of effects on the acceleration test [33].

The higher change in temperature extremes causes the material to strain more [33]. Obviously it is important to consider the temperature range the tester is capable of as well as the glass transition temperature of the epoxies and fill materials. This was further explained in the glass transition temperature section. At the larger temperature extreme creep can take place if the testing temperature is greater than about .45 to 0.6 the melting temperature of the material.

The dwell times that the maximum and minimum temperatures are held also play a large role in accelerating the life of the part [33]. In general the longer the dwell time in each model, the longer the Acceleration Factor (AF). Dwell times are also used to ensure that the tested component has hit a steady state temperature. There also is a negative effect if the time of dwell is too long. This would limit the number of testing cycles and extend the life of the test which can be poor for the equipment.

The ramp rate is also an important factor when dealing with AT. This helps accelerate weaknesses in the product that are thermal rate dependent [33]. The strain rate increases as the ramp rate increases. Increasing the strain rate leads to the stress in the solder to rise. All of the acceleration models described in the next section do not take into account thermal change rate.

One of the most important factors in acceleration testing is the number of thermal cycles performed. For qualification and quality performing somewhere between 5 and 20 cycles can be adequate [5]. In some mathematical models, the number of cycles is not taken into account when calculating the acceleration factor. The primary focus in accelerated testing is to perform a large number of cycles in a short amount of time.

Acceleration Models

There are several different models that have been developed to determine the AF. Various AF models were researched and compared to gain a better understanding on how the normal environmental profile can be increased. Coffin Manson, Vasudevan, Miremadi, and Clech acceleration models were all used and compared to gage a better understanding of which thermal profile would be the most optimal.

Coffin Manson Equation

The Coffin-Manson equation was developed by L.F. Coffin in 1954 and S.S. Manson in 1953. The equation is used for low-cycle fatigue experiments and is commonly used for solder fatigue. The long expression for the number of cycles to failure [33] is:

$$N_f = A * f^{-a} * \Delta T^{-b} * \exp\left(\left(\frac{EA}{K}\right) * \left(\frac{1}{T_{max}}\right)\right)$$

- N_f = number of cycles to failure
- A =coefficient
- f = cycle frequency
- a = -1/3
- ΔT=Temperature range through 1 cycle
- $b = 1.9$
- EA = Activation energy taken to be 0.42
- K = Stefan Boltzmann constant $8.623*10^{-5}$ eV/K
- T_{max} = Maximum Temperature

For Sn-Pb solder the Coffin-Mason equation can relate the number of cycles to failure N_f, to the plastic shear strain range $\Delta\gamma_p$, or the equivalent plastic strain $\Delta EQPS$ [6].

$$N_f = \left(\frac{1.14}{\Delta\gamma_p}\right)^{\frac{1}{0.51}} = \left(\frac{1.31636}{\Delta EQPS}\right)^{1.96078}$$

This simplified form of Coffin-Manson is particularly useful in FEA studies for solder reliability. The number of cycles to failure is found from the equivalent plastic strain. The plastic strain is calculated from FEA results which are derived from temperature the UUT is exposed to. The strain is a function of the change in temperature and how the solder is constrained.

The Coffin Manson equation can also be expressed in terms of AF. This takes into account the dependent factors explained above such as temperature extremes, and number of cycles. It can also be defined as the ratio as number of cycles to failure for the experiment and use environments [33].

$$AF = \frac{N_L}{N_H} = \left(\frac{\Delta T_H}{\Delta TL}\right)^b * \left(\frac{f_L}{f_H}\right)^{-a} * \exp\left(\left(\frac{EA}{K}\right) * \left(\frac{1}{T_{KL}} - \frac{1}{T_{KH}}\right)\right)$$

- AF = Acceleration Factor
- N_L=Number of cycles to failure at the use condition
- N_H=Number of cycles to failure at the experimental condition
- ΔT= Temperature Range
- f = Cycles per day
- T_{KL}= Maximum use temperature in Kelvin
- T_{KH}= Maximum experimental temperature in Kelvin
- EA = Activation Energy
- K = Stefan Boltzman Constant $8.623 * 10^{-5}$eV/K

The subscript H and L are for the accelerated testing and use conditions respectfully. The other constants and variables are the same as the number of cycles. One note of concern is that Coffin Manson model does not depend on the dwell time and ramp rate of the conditions. They are not explicit as they are both expressed in the number of cycle's term of the equation. Coffin Manson is unable to distinguish thermal cycling compared to thermal shock. The difference between the two is generally described by the temperature ramp rate [33].

There were other AF equations that were researched to see how Coffin Manson differed compared to other acceleration factor models. It is important to note that each equation takes into account different test variables. The Vasudevan model takes into account cycles per day for use and test temperatures. Dauksher and Miremadi take into account the change in temperatures and dwell times with different constant variations. All of these models can be used for the purpose of solder joint fatigue. These are listed to show the differences between them, and how there are different methods and assumptions used in each. These models were compared in Matlab to gain an understanding of the differences between them and how varying the test parameters would affect the AF.

The Dauksher model [36] can be defined as:

$$AF = \frac{N_2}{N_1} = \left(\frac{\Delta T_1}{\Delta T_2}\right)^{1.75} \left(\frac{t_1^{HOT}}{t_2^{HOT}}\right)^{\frac{1}{4}} exp\left(1600\left(\frac{1}{T_{2,MAX}} - \frac{1}{T_{1,MAX}}\right)\right)$$

The Vasudevan model [36] is:

$$AF = \frac{N_1}{N_2} = \left(\frac{\Delta T_1}{\Delta T_2}\right)^{-1.9} \left(\frac{f_1}{f_2}\right)^{-.33} \exp\left(1414\left(\frac{1}{T_{1,max}} - \frac{1}{T_{2,max}}\right)\right)$$

The Miremadi model [36] is:

$$AF = \frac{N_o}{N_t} = \left(\frac{\Delta T_t}{\Delta T_0}\right)^{a} \left(\frac{t_t}{t_0}\right)^{b} \exp\left(c\left(\frac{1}{T_{max,0}} - \frac{1}{T_{max,t}}\right)\right)$$

The Coffin Manson method combined with using FEA software to calculate an equivalent number of cycles to failure is the primary method that Sandia uses to accelerate testing. There has been a considerable amount of research done to determine the acceleration profile for these materials. The accelerated profile analytically found was -50 to 85°C with a ramp rate of 2.666°C/min. The dwell time for each extreme was taken to be 1.5 hours. The predicted number of cycles to failure for QFN and LCC packages is viewed in table 5.

24 LCC Cycles to Failure		
	Profile 1	Profile 2
Arathane	22.2	8.7
Uvikote	10.4	5.5
Arathane w/ UF	692.9	328.6
Uvikote w/UF	321.9	163.4
QFN Cycles To Failure		
	Profile 1	Profile 2
Arathane	32.4	10.4
Uvikote	9.4	4.9
Arathane w/ UF	4800	2000
Uvikote w/UF	2300	1000

Table 5. Analytical Predicted Number of Cycles to Failure

The experimental acceleration profile is slightly different compared to the analytical profile. The temperature range will be -20 to 70°C. This range will keep all materials in between their glass transition temperatures and allow for over shoot in the chamber. The dwell time will be 20 minutes for each extreme instead of 90. This will allow for more cycles to be complete in one day. The ramp rate will be 3°C/min to reach the hot and cold cycles. Starting out, a goal of 40 cycles will need to be reached to verify the cases without underfill are valid. It will be difficult to achieve 4800 cycles as the FEA predicts for underfilled QFNs coated with Arathane. After 40 cycles are complete, testing will be continued to observe how the components do with Almatis 20% underfill. This approach makes sense because of the amount of time will vary depending on the scheduling and availability of the thermal chamber and amount of testing time.

Procedure

There were several steps taken to ensure that the testing was performed in the most optimal manner. It will take approximately 1.5 hours to complete a full thermal cycle. 5 cycles will be run throughout the day. We will able to complete 50 cycles in a two week period. After 5 cycles are complete, the units were removed from the chamber and are to be inspected. An electrical continuity check was performed that would indicate a positive connection between the electronic device and the circuit board. As an additional verification, an x-ray scan was also performed every 10 cycles. This was to ensure that even though there was continuity between the board and the device, there was no cracking in the solder that could still constitute a failure.

Electrical Continuity

One of the steps taken to verify that the solder is still making optimal contact is to see if there is still an electrical path from the device to the board. This can be done by either using a digital multimeter (DMM) or a continuity tester. A Fluke® DMM will be used for checking continuity for these tests. When an electrical path has been made the DMM will beep. If there is no continuity the DMM functions as an open switch and there is no beep from the device.

X-Ray Screening

In some cases it has been reported that there may still be continuity between the device and the circuit board even though the solder is cracked. An X-ray scan can be performed to verify that the 63Sn37Pb eutectic solder remains continuous throughout. This is a new technique and is an extra verification for the mechanical failure of the joint. Eric Bower and Paul Vianco will assist with their equipment in the X-ray cross section screening. The equipment used and process will be further explained next semester.

Work In Progress

All of the test units have been purchased and delivered, and the boards have already been fabricated. Our group is currently waiting for the PCBs to be populated and then be conformal coated and underfilled. Testing is projected to begin in early January. In addition to testing, I plan to further expand on this report with results of the experiments, discussion of what happened and why, and conclusions. I am also considering adding FEA on my own to add to this project to compare my results.

Additional Tests

As part of a subset to this project, I will also perform thermal cycling on Commercial Off the Shelf (COTS) ground pins to verify how well they dissipate electricity over time. The goal is to accelerate the regular use thermal cycle that the ground pins undergo in a similar fashion to the solder fatigue on the electronic packages. This is to ensure that the ground pins make sufficient contact to the aluminum base plate and effectively transfer the current to ground. There will be a variety of ground pins that are tested to gain an understanding on which one will be the most optimal to use. The different options are listed in table 6.

Pin Option	Feature
1	Press Fit (Original)
2	Weld
3	Press Fit (shorter and more robust)
4	Helicoil
5	Wire with conductive epoxy

Table 6. Pin Options

The press fit option is the default design and will be treated as the control for the other pins. Options 1 and 3 are pins that have a knurled diameter and are pressed into a drilled hole in the aluminum base plate. Press fitting is relatively easy and fast to assemble for production.

Figure 15. Pressfit Ground Pin (Mill-Max)

Option 2 is to have a pin laser welded into the aluminum. While welding does a decent job of interfacing two different parts, it is difficult to weld aluminum and the pins are also made out of a brass alloy which is a concern. The welding option is to simply be compare the press fit pins and are being analyzed as an alternative. Option 4 is to have a stainless steel insert helicoil and bolt as the grounding method. This is a secure connection and it's easy to assemble in the ground wire to the base plate. The last option that will be studied is using an annealed wire that will be connected to the aluminum with a conductive epoxy. This would also provide a viable alternative to the stainless steel insert and press fit pin. This particular type of wire is expensive and not easy to find.

Solder joint fatigue and ground pin connections are just a few examples of why accelerated testing is so important today. There are many different reasons why is should be performed and why it is widely used in industry. This project will help myself in my engineering career as I plan to do other accelerated testing projects in the future. There is much more to be understood in this field as accelerated testing is an up and coming practice.

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Appendix

Matlab

```
% Accelertion Factor Calculations
clear,clc

t1_max = input('What is the test max temperature? (K)')
t1_min = input('What is the test min temperature? (K)')
time1 = input('What is the dwell time of the test?')
f1 = input('How many cycles per day?')

t2_max = input('What is the use max temperature? (K)')
t2_min = input('What is the use min temperature? (K)')
time2 = input('What is the dwell time of use?')
f2 = input('How many cycles per day?')

% Change in temperatures
dt2 = t2_max-t2_min;
dt1 = t1_max-t1_min;

% Dauksher Acceleration Factor Model
Dauksher = ((dt1/dt2)^1.75)*((time1/time2)^.25)*exp(1600*((1/t2_max)-
(1/t1_max)));

% Vasudevan Acceleration Factor Model
Vasudevan = ((dt1/dt2)^1.9)*((f1/f2)^.33)*exp(1414*((1/t2_max)-(1/t1_max)));

% Miremadi AF Model
%For a plastic ball grid array:
a = 1.26;
b = .02;
c = 3503;

Miremadi = ((dt1/dt2)^a)*((time1/time2)^b)*exp(c*((1/t2_max)-(1/t1_max)));

% Clech Acceleration Model
c1 =4.5654;
Clech = ((dt1/dt2)^2)*(((1-(c1*(dt1^-1)*(((time1^-
.19275)*exp(705.5/t1_min))+((time1^-.19275)*exp(705.5/t1_max)))))...
    /(1-(c1*(dt2^-1)*(((time2^-.19275)*exp(705.5/t2_min))+((time2^-
.19275)*exp(705.5/t2_max)))))));

Z = (1-(c1*(dt2^-1)*(((time2^-.19275)*exp(705.5/t2_min))+((time2^-
.19275)*exp(705.5/t2_max)))));

% Coffin Manson
CM = (dt1/dt2)^.25;

N = f2^(1/3)
CM1 = (((t1_max-t1_min)/(t2_max-
t2_min))^1.9)*((90/20)^(1/3))*exp((.42/8.623*10-5)*(1/t2_max)*(1/t1_max))
```