Transmission Level High Temperature Superconducting Fault Current Limiter

Final Technical Report

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Project Objective

The primary objective of this project was to demonstrate the feasibility and reliability of utilizing high temperature superconducting (HTS) materials in a Transmission Level Superconducting Fault Current Limiter (SFCL) application. During the project, the type of high temperature superconducting material used evolved from 1st generation (1G) BSCCO-2212 melt cast bulk high temperature superconductors to 2nd generation (2G) YBCO based high temperature superconducting tape. The SFCL employed SuperPower's "Matrix" technology that offers modular features to enable scale up to transmission voltage levels. The SFCL consists of individual modules that contain elements and parallel inductors that assist in carrying the current during the fault. A number of these modules are arranged in an m x n array to form the current limiting matrix.

The following performance characteristics were used to determine the suitability of the HTS conductor for the SFCL operation:

- Fast quench response time in the order of few milliseconds
- Utilize the inherent properties of the superconducting materials, the bulk BSCCO2212 (able to be magnetically triggered) and then the YBCO, such as the high critical current density (1–2 MA/cm^2, high n-values in the range of 20 – 40)
- Demonstrate fast current transfer from the HTS element to a parallel shunt impedance, within a few milliseconds
- Demonstrate fast recovery of the HTS elements to superconducting state under repetitive breaker re-closing sequences, while potentially carrying normal load current [recovery under load (RUL)]
- Produce longer HTS elements to reduce the number and power losses of interconnections
- Test prototype SFCL modules at prospective transmission line fault currents
- Demonstrate the capability to handle transmission level voltages in the SFCL configurations while in the operating cryogenic environment.
- Evaluate the benefits of 2G FCL over that of BSCCO-2212, based on response time, energy capability, recovery and cost
- Use the data developed with-HTS conductor to design a HTS SFCL alpha prototype for operation at 138 kV with a normal load current of 400 – 1,200 A and fault levels of 30 – 63 kArms

Background

A fault condition may result in an electric power transmission system from events such as lightning striking a power line, or downed trees or utility poles shorting the power lines to ground. The fault creates a surge of current through the electric power system that can cause serious damage to grid equipment. Switchgear, such as circuit breakers, is deployed within transmission substations to protect substation equipment. When power delivery networks are upgraded or new generation is added, fault levels can increase beyond the capabilities of the existing equipment, with circuit breakers in an "over-duty" condition. This problem necessitates upgrades such as the modification of substations or replacement of multiple circuit breakers.

To avoid these expensive upgrades, a SFCL can be applied to reduce the available fault current to a lower, safer level (20%-50% reduction) where the existing switchgear can still protect the grid. Superconducting fault current limiters employing high temperature superconductors provide the necessary current limiting impedance during a fault condition, but have essentially zero impedance during normal grid operation. Therefore, SFCLs have no negative impact on overall system performance, contrary to other conventional current limiting devices, such as a current limiting reactor (CLR) that produces large voltage drops, circulating currents in transformers and substantial energy loss. The current limiting impedance is introduced into the system by taking advantage of the transition of the superconducting material from the superconducting state (resistance = 0) to a highly resistive ohmic normal state as the fault current exceeds the critical current capacity of the superconducting material. This switching is done passively and brings into the circuit any parallel shunting elements whose L/R characteristics can be designed to optimize the use of the superconductor properties and current sharing between elements.

A SFCL can provide a solution which is more economical than many conventional solutions to breaker over-duty problems. Numerous utilities have expressed the need for a device that can economically address breaker over-duty problems in an over-stressed network, particularly at transmission level voltages. The availability of a SFCL allows the utility to accommodate increasing fault currents due to added generation while preventing breaker failures and associated problems such as welded contacts, though fault stresses on aging infrastructure and the need for extensive bus bracing. In addition, the utility maintains flexibility to accommodate load growth while avoiding adverse side effects imposed by existing solutions (bus splitting, expensive breaker upgrades, etc.)

This execution of this program can be broken down into three distinct phases based on the technical progress and evolution of the HTS technology. These phases are:

Phase 1 Initial work based on BSCCO2212 melt cast processed bulk elements with Nexans as a partner and supplier of the HTS material. MFCL concept used in this phase. (Aug. 2003-Aug. 2005) Nexans exited the program after Aug. 2005.

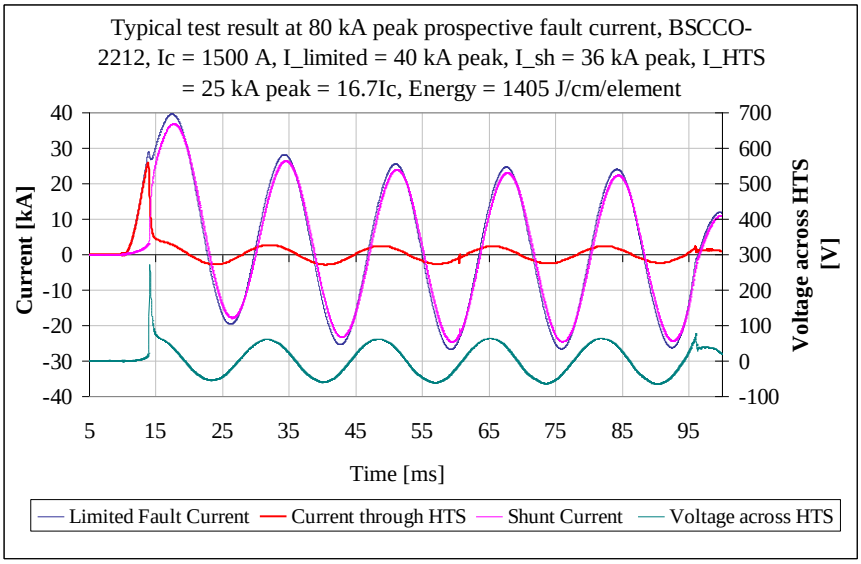
Phase 2 A "Reduced Effort Status" (RES) period in which deficiencies in the BSCCO 2212 MCP pushed the project toward using 2G YBCO based HTS tapes. During the RES period, a focused effort on evaluating the effectiveness of the 2G YBCO HTS tapes in the fault current limiting role was successfully conducted. The SFCL concept was developed in this phase and carried on throughout the project. (July 2005 – June 2006).

Phase 3 A return to the full program scope with the SFCL work based on YBCO based 2G HTS as the superconducting material. Sumitomo Electric was also added as a partner with high voltage expertise. (June 2006 – December 2010).

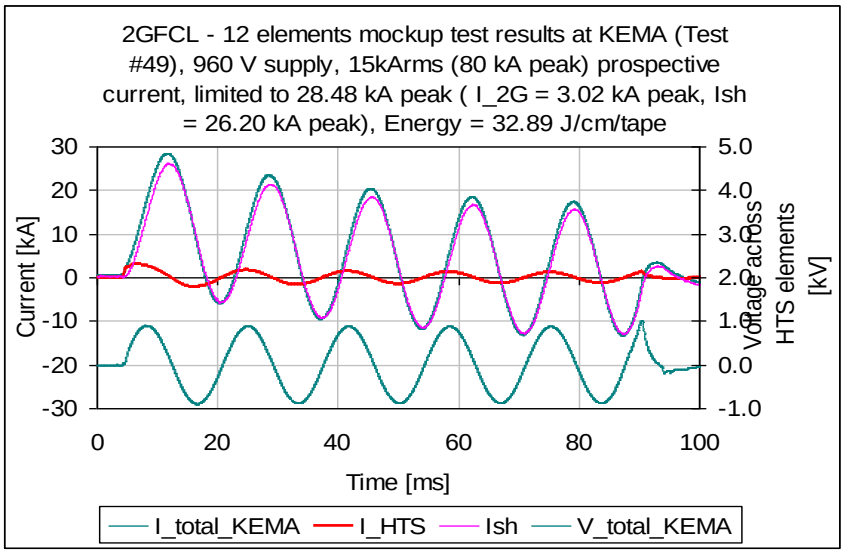
In all of these Phases we worked with American Electrip Power (AEP) as the host utility that provided guidance on the types of fault current which might be seen as well as many of the aspects needed to be resolved on integrating the SFCL into the grid and what acceptance tests would need to be performed.

To address the market pull for an economic transmission-level HTS FCL, SuperPower developed the Matrix Fault Current Limiter (MFCL) (US Patent 6,664,875) initially utilizing Melt-Cast Processed (MCP) BSCCO-2212 HTS elements. Successful testing of a single-phase 'Proof of Concept' prototype MFCL was completed in July 2004. This device was rated at 8.6 kV line to ground (15 kV L-L) and 800 A_{rms} continuous current. First peak prospective fault currents up to 25.6 kA were applied for testing. The ratio of limited fault current to prospective fault current was 84% at the first peak and 56% by the third cycle. However, during this testing a number of the MCP elements failed.

In 2005, some initial tests were carried out during the RES period using then current production 2G HTS tapes in a prototype module which demonstrated the viability of the 2G HTS to operate in a SFCL environment. Figure 1 is a comparison between the fault limiting performance of some MCP elements and some of the early 2G HTS tests. As can be seen in the results (Figure 1a), the MCP, while transitioning in the first peak, required a substantial current level before transitioning resulting in a transition time of several milliseconds before the bulk of the current was transitioned to the parallel shunt circuitry. The 80 kA prospective current (the fault current without the SFCL device) was reduced to 40 kA in the first peak. The development of a voltage spike across the MCP element is indicative of high power being deposited in the MCP element which often resulted in mechanical / thermal failures in the non-homogeneous MCP structure. In contrast, the 2G HTS elements provided a smooth, rapid transition (~ 1 millisecond) with no irregular voltage developed across the system. The 80 kA prospective current was reduced to 28.48 kA in the first peak. Clearly, the 2G HTS was shown as a viable alternative to the MCP elements in these early tests.



(a)



(b)

Figure 1: Comparison between the fault current limiting performance of (a) a melt cast (MCP) BSCCO-2212 element and (b) of an early 2G-HTS mockup with 12 tape elements. Tests performed at KEMA Powertest in Chalfont, PA.

These results laid the ground work for the redirection within this program to investigate and develop a robust and reliable 2G-HTS conductor alternative that is tailored to SFCL applications by optimizing the 2G-HTS structure and associated SFCL module components.

Program Elements and Results

The project contained 6 major technical tasks in addition to the program management function. These 8 tasks were:

1.0 SFCL Specification Development
2.0 HTS Development
3.0 SFCL Matrix Development
4.0 Pre-Prototype Matrix Assembly Design, Fabrication and Test
5.0 High Voltage Capability Development
6.0 Prototype Conceptual Design
7.0 Program Management

1.0 Specification Development

In this task, SuperPower worked with utilities to develop the range of specifications that would be required for utilization of an HTS based SFCL in a utility environment. These specifications encompassed the operating conditions that a SFCL would be expected to work under and the expected performance that the SFCL would have to provide in the system. Also included in these activities would be the development of acceptance criteria for the SFCL device.

There were several levels of utility input for the specification development task. The first level looked at specific needs within the American Electric Power (AEP) grid that drove the SFCL requirements. Working with AEP, we identified a site with broad general application to the utility market space to guide the specification development. The TIDD substation on the AEP was selected and has the following operating characteristics.

- Operating current: 1200 Arms,
- Operating voltage: 138 kV
- Prospective fault current: 13.8 kArms (~37 kA peak)

Figure 2 shows the proposed SFCL installation site in the TIDD substation. Much of the work under this project included these specifications in our design envelope as they impacted such functions as recovery under load, number of parallel tapes required to handle the current levels, the length of tapes required to handle the voltage drop across the device, the parallel shunt impedance levels required impacting the complexity of design, etc.

In addition, we used the "typical" AEP reclosure sequence (Figure 3) during our design and testing activities within the program to simulate the timing of faults and recovery times available to the SFCL system. Most of the testing focused on the first three 5 cycle faults as it was expected that the SFCL system would fully recover to the superconducting state in the 135 seconds between the third and fourth 5 cycle faults and the 160 seconds between the fourth and fifth cycle faults. This reclosure sequence defined the recovery times that the SFCL would need to meet.

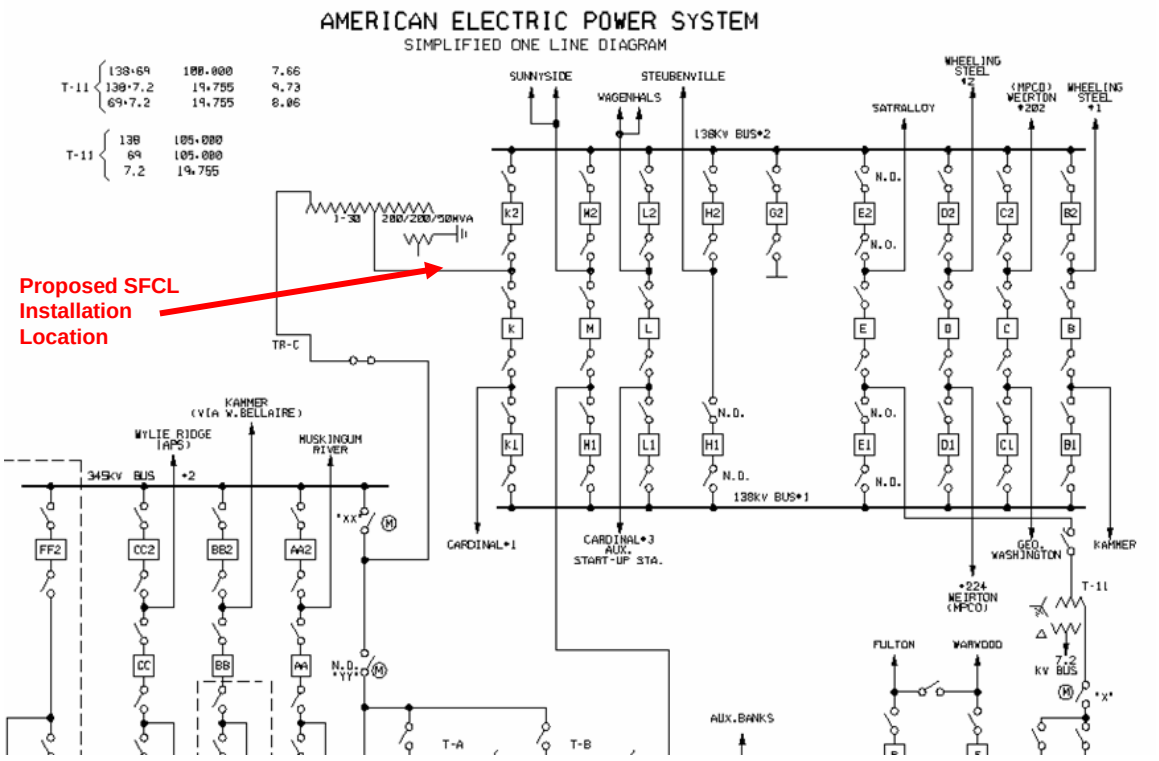


Figure 2: Simplified One Line Diagram of the AEP TIDD substation indicating the proposed SFCL installation site.

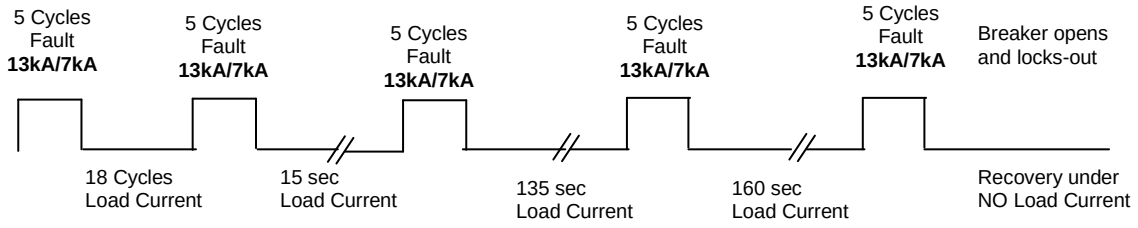


Figure 3: Typical AEP reclosure sequence during a fault event.

Secondly, SuperPower worked with AEP and the National Electrical Energy Testing, Research and Applications Center (NEETRAC) to develop acceptance testing specifications for the SFCL device. Periodic reviews with utilities with an interest in the project, coordinated through NEETRAC included: Florida Power and Light, Exelon, Southern Company, Baltimore Gas and Electric, Entergy and Con Edison.

The resultant acceptance specification (Table 1) draws upon the following industry acceptance standards.

- Circuit Breakers – ANSI C37.06 and C37.09
- Transformers – IEEE C57.12.00 and C57.12.90
- Series Reactors – IEEE C57.16

Table 1: Proposed Acceptance Standards for a Commercial 138 kV 2G HTS SFCL Device

Acceptance Test	Based On	Test Sequence / Values
60 Hz Withstand with PD Measurements	ANSI Breaker Spec C37.06 Table 4 ANSI Transformer Spec C57.12.00 Table 6	125 kV / 5 min 145 kV / 2 min 125 kV / 60 min 310 kV / 1 min
BIL Lightning Impulse	ANSI Reactor Spec C57.16 Table 5	1.2×50μs,650kV, (-)polarity
Chopped Wave	ANSI Transformer Spec C57.12.00 Table 6	3μs chop,715kV, (-)polarity
Switching Impulse	ANSI Transformer Spec C57.12.00 Table 6	250×2500μs,540kV, (+) and (-)polarity

Thirdly, Superpower's overall SFCL development activities utilized a Technical Advisory Board (TAB) to evaluate and guide the SFCL projects in conjunction with DOE Readiness Review program and included the following members:

- Utility members: AEP, New York Power Authority, Southern California Edison, Con Edison, Entergy
- Academia: Rensselaer Polytechnic Institute (RPI)
- Funding sponsors: DOE and EPRI

2.0 HTS Development

In this task, the team members investigated in Phase 1 the design and development requirements for the BSCCO2212 MCP HTS elements that would be used in the device. In Phases 2 and 3, the team members evaluated several different approaches to improve the SFCL performance characteristics based on the properties of the then available 2G HTS tape. There are several considerations as to what drives the BSCCO2212 MCP elements and the 2G HTS tape design operating in an SFCL environment. These include:

System Considerations:

- Operating current – This drives the number of BSCCO2212 MCP elements or 2G HTS tapes in parallel that are required in the SFCL device and take into account the critical current of the HTS elements under the target temperature and magnetic field operating windows as well as operating margins.

- Operating voltage – This drives the total length of either the BSCCO2212 MCP elements or 2G HTS tape required in order to withstand the voltage drop across the HTS sections which is typically described as an allowable V/cm that the HTS constructions can withstand without failure.

- Fault levels – The fault level determines the level of impedance that must be introduced by the SFCL and the resultant energy deposition that is seen in the SFCL elements (BSCCO2212 MCP elements/2G HTS tape assemblies, shunts, etc.).

- Parallel shunt – The properties of the parallel shunt circuitry (i.e. L/R) drives the current sharing between the elements and resultant energy deposition in each of the system components.

The first three of these system considerations directly drive the HTS elements performance requirements. In addition, the HTS elements themselves must address the following:

Direct HTS Considerations:

- Energy to failure (statistics) – In order to operate reliably over the long term, the HTS elements must withstand the energy deposited in them during a fault and the development of statistical data is required.

- Temperature rise and tolerance during fault transient - During the fault transient, there is significant energy deposited in the HTS elements leading to significant temperature rise. The architecture of the BSCCO2212 MCP elements and later 2G HTS tape were modified to both limit and be more tolerant of the temperature rise.

- Recovery under load (RUL) – Many of the tests conducted on samples and assemblies prepared in this program looked at the properties of the HTS material under recovery under load (RUL) conditions. RUL can arise if there are multiple feeds onto a bus that is protected by the FCL. If the fault is on only one of the feeds, the remaining feeds continue to provide current that must still flow through the FCL while it is recovering from the heating of the fault level. The HTS elements ability to carry current and transfer heat to its surroundings to enable a net cooling is a challenging design problem and can limit the operational window of the FCL system.

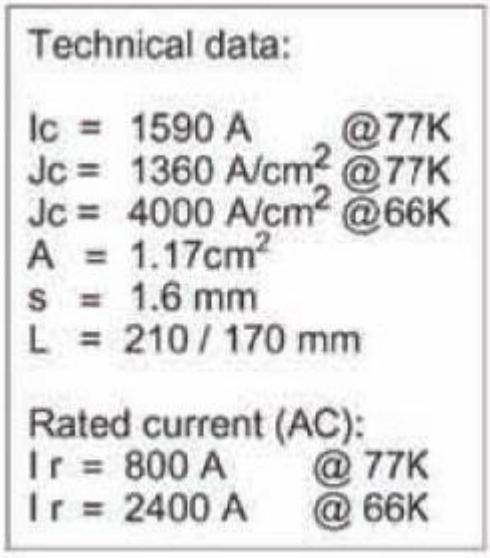
- Heat transfer – The ability of the HTS elements to recover (recool) after a fault transient requires significant heat transfer into the surrounding coolant bath, typically under boiling heat transfer conditions. Modifications of the HTS to enhance the heat transfer mechanisms are critical to a successful SFCL device. Enhanced heat transfer can also be accomplished by modifying the conditions of the cryogenic cooling bath through sub-cooling or other techniques.

2.1 BSCCO2212 MCP Development

In Phase 1, BSCCO2212 MCP HTS elements were provided by Nexans to the program. These elements were prepared by a centrifugal melt casting technique which resulted in a tubular structure of the HTS material. The grains of the BSCCO2212 were aligned such that the c-axis of the grains was in the radial direction of the tube. Post casting reoxygenation of the HTS material was also carried out. Silver contacts for current transfer into the BSCCO2212 elements were also provided. Typical performance characteristics of the BSCCO2212 MCP elements are listed in Table 2 below.

Figure 4: Examples of some of the BSCCO2212 MCP elements used in the Phase 1 work. The black part is the BSCCO2212 HTS material with silver end caps.

Table 2: Typical performance characteristics of theBSCCO2212 MCP elements used in Phase 1 work. A is the cross-sectional area of the leads, s is the wall thickness, L is overall length.



During the testing of the BSCCO2212 MCP elements in Phase 1, local hot spots developed in the material that led to local d=performance degradation and eventual failure of the cast tubes under repeated thermal and fault current cycling. This was traced to in homogeneities in the cast structure that while improved upon over the course of the programs were not fully resolved. Many of these degradation regions were centered around the end silver connections. Several different Ag end cap configurations were evaluated in the program that did show some improvement. After multiple test runs of these elements (Section 3), it was determined that the BSCCO2212 MCP elements had not achieved sufficient reliability to proceed with further development of the SFCL based on this material.

2.2 YBCO Based 2G HTS Tape Development

With the problems encountered with the BSCCO2212 MCP elements, alternative forms of HTS materials were evaluated first in Phase 2 and further developed in Phase 3. It was determined that the 2G HTS tapes based on YBCO being developed by SuperPower were a better alternative HTS material for use in the SFCL systems.

The architecture of SuperPower's 2G HTS tape (Figure 5) consists of a base Hastelloy C276 substrate that forms the "backbone" of the conductor. The substrate is electropolished and then 5 buffer layers are deposited (total thickness ~ 165 nm) to provide several functions including diffusion barrier, lattice matching and most importantly the preferentially textured surface for growing the 2G HTS epitaxial film. This texture is necessary to develop the structure in the 2G HTS film that is capable of carrying extremely high currents exceeding 1 MA/cm^2. The HTS film is then capped by a silver layer that acts both as a protective layer above the 2G HTS film and as a low

resistance contact path for current flowing into the HTS film. In many applications, an additional surround copper stabilizer layer is added. For SFCL use, the copper stabilizer is usually not utilized as it lowers the normal state resistance of the 2G HTS tape to low levels such that the 2G HTS tape cannot develop the required impedance during a fault transient.

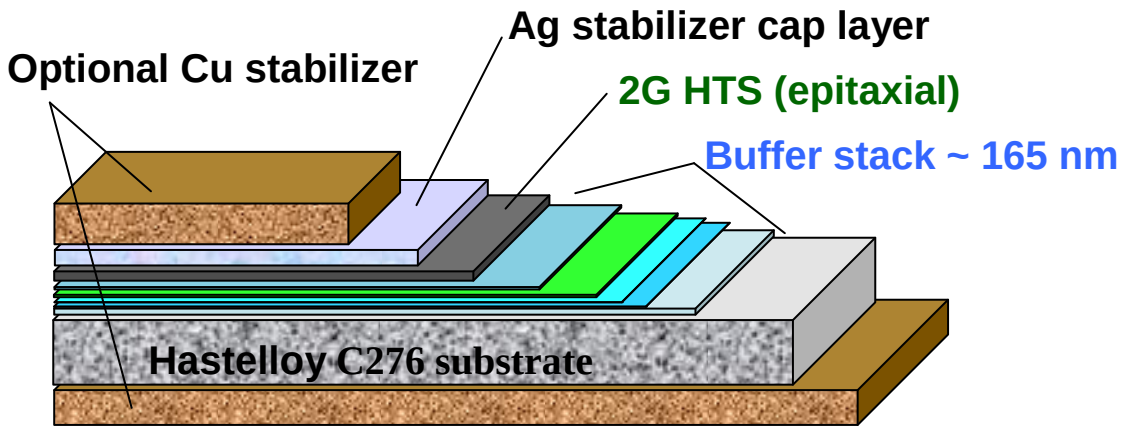


Figure 5: Architecture of the SuperPower 2G HTS tape.

During the project (particularly in Phase 3), several modifications to the 2G HTS tape were evaluated to understand their impact on the 2G HTS tape performance in the SFCL function.These tasks are described in the following sections

2.2.1 – Modification of metal content in the conductor

In this task the impact of the metal content and composition of both the Ag stabilizer and substrate materials were evaluated. All of these tests were conducted in an open LN_2 bath. The three areas investigated were:

a) Ag stabilizer thickness

Ag stabilizer thickness is adjusted during its deposition by cylindrical magnetron sputtering and can range from sub-micron up to 5 microns in thickness with a "standard" thickness of nom. 2 microns. The deposited Ag is of high purity and low resistance and has a significant impact on the normal state resistivity of the composite 2G HTS structure. Simulation and well correlated test results were obtained on conductor samples with variable Ag stabilizer thickness. It was found that varying the silver stabilizer thickness mainly affects the life expectancy of the 2G tapes related to energy, current, resistance and temperature rise. For the same system parameters, as the Ag stabilizer thickness increases the dynamic resistance of the conductor decreases with little change in the mass of the conductor. Thus the amount of current through and the energy deposited into the conductor during a fault increases resulting in a higher temperature rise. However, varying the stabilizer thickness has minimal impact on the overall current limiting performance of the device itself. Figure 6 shows simulated results for a given

operating condition (5 cycle fault - 4 tapes in parallel, 100 micron thick substrate, parallel shunt impedance of 7 mΩ) with pure Ag thicknesses ranging from 1.0 to 4.0 microns. As can be seen in the plot, the current, energy and temperature rise increase with added silver thickness while the sustained V/cm does not change.

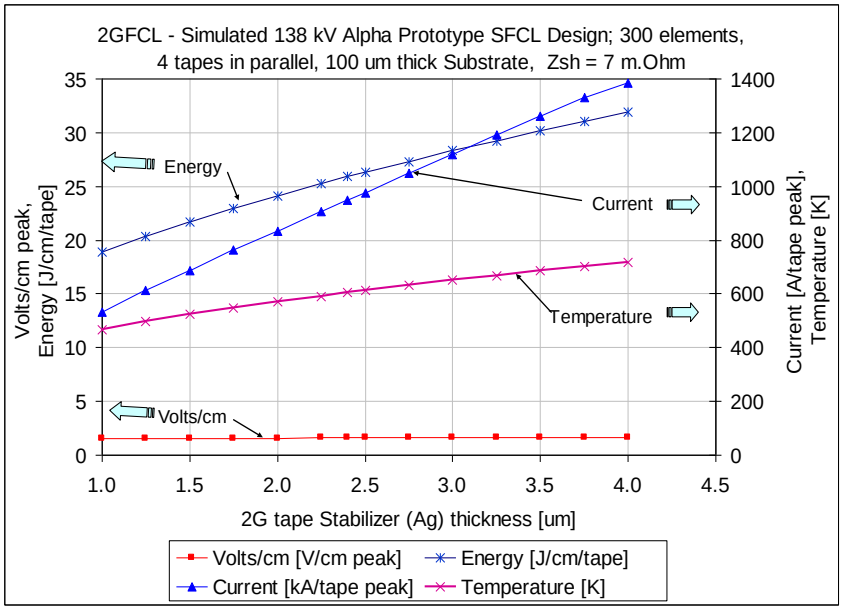


Figure 6: Impact of silver thickness on current, energy and temperature rise during a 5 cycle fault for 4 parallel tapes (100 micron substrate) and parallel 7 mΩ shunt.

While a thinner Ag minimizes the temperature rise in the tape during a fault, too thin of a Ag layer did not always result in uniform coverage of the HTS layer. Balancing these factors, a 2.0 – 2.5 micron Ag thickness was settled on as the most advantageous thickness for most operating conditions with a parallel shunt in the 5 – 10 mΩ range. For lower parallel shunt impedances, a thinner Ag thickness could be used.

b) Ag stabilizer composition

Simulations indicated that the use of alternative stabilizer materials other than pure silver can improve the 2G HTS tape performance. Alternate stabilizer materials with a higher resistance than pure Ag limit the current sharing in the 2G HTS with a parallel shunt, lowering the energy deposition and temperature rise of the tape. In addition to the higher resistance, the choice of alternative substrate materials was limited to alloys which would have materials that were compatible with the 2G HTS processing and would not detrimentally react with the HTS layer. Ag-Au alloys were selected for evaluation since they provided the lower resistance required (see Figure 7) and they had been successfully used in conjunction with 1G superconductors in current lead applications, indicating a

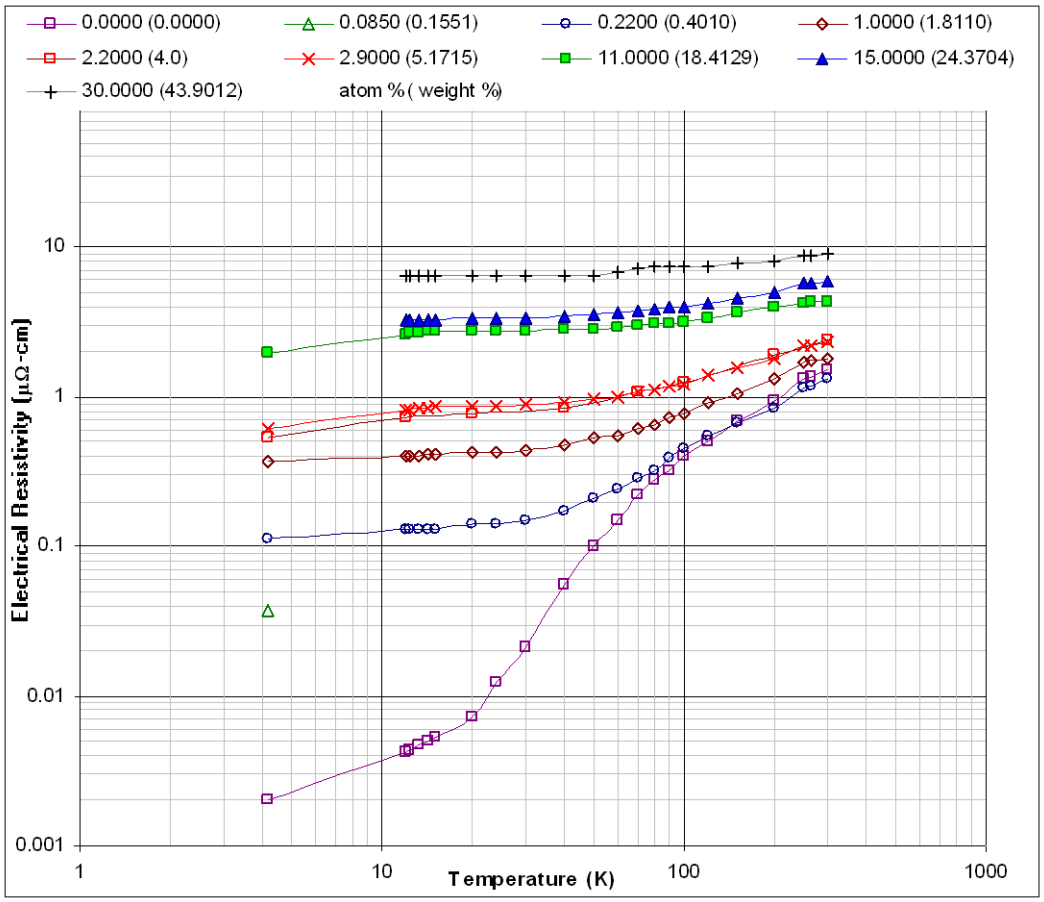


Figure 7: Electrical resistivity of Ag-Au alloys versus temperature. Alloys modeled were focused on the 2.9 and 11 atomic percent Au in Ag

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level of compatibility with copper oxide based superconductors. Alloys of 2.9 and 11 atomic percent Au in Ag were modeled and compared with both pure Ag and pure Cu results. As can be seen in Figure 8, the final temperature after a 5 cycle fault for the pure Ag and pure Cu were the same (~600K) since they both have similar resistivity vs. temperature properties. For 2.9 atomic percent Au, the final temperature after a 5 cycle fault decreased to ~ 550K. For 11 atomic percent Au, the final temperature drops even further to ~ 425K. Sputtering targets were obtained containing 2.2 atomic percent (4.0 weight percent) Au in Ag and 2G HTS tape samples prepared.

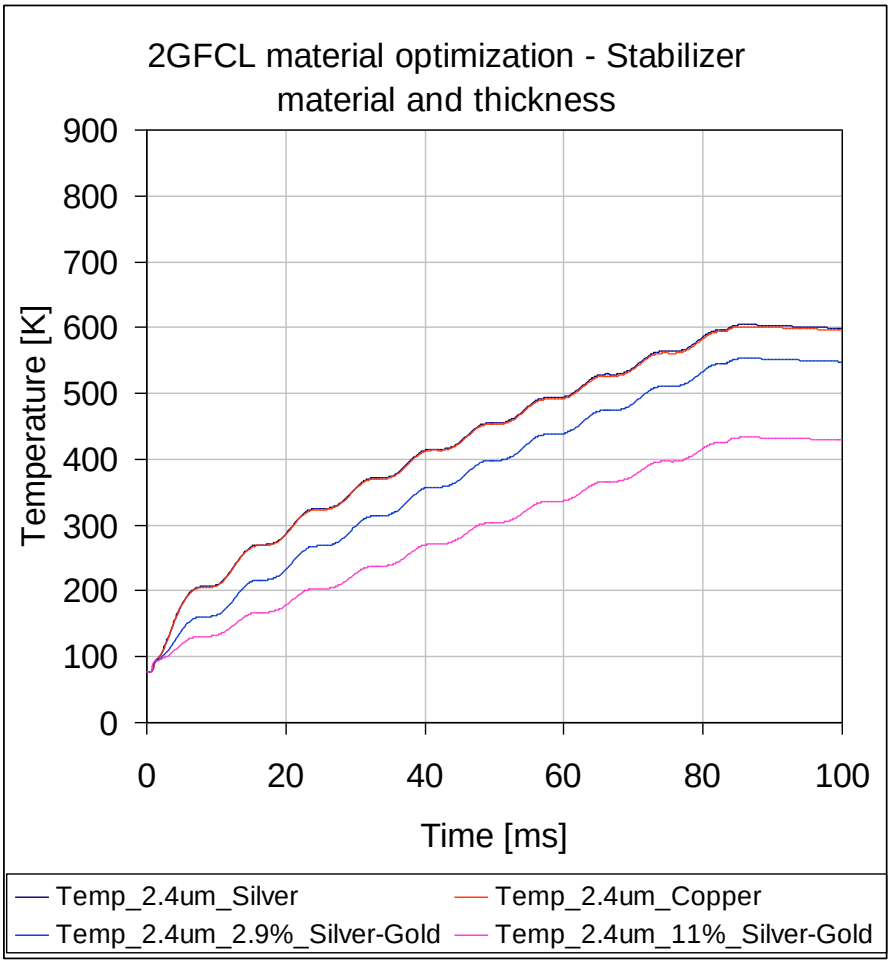


Figure 8: Simulated results for the temperature rise in samples with 2.4 micron thick stabilizer composed of pure Ag, pure Cu, 2.9 atomic percent Au in Ag and 11 atomic percent Au in Ag for a 5 cycle fault.

One negative effect of the higher resistance of the 2.2 atomic percent Au in Ag at low temperature is a resultant transient over-voltage (Figure 9) seen during the first half cycle indicating a delay in the transition to current sharing with the shunt. This over-voltage can result in overheating in the 2G HTS tape. It was determined that in order to use the Ag alloyed materials, the full system needed to be optimized (i.e. the parallel shunt voltage) in order to manage the transient overvoltage.

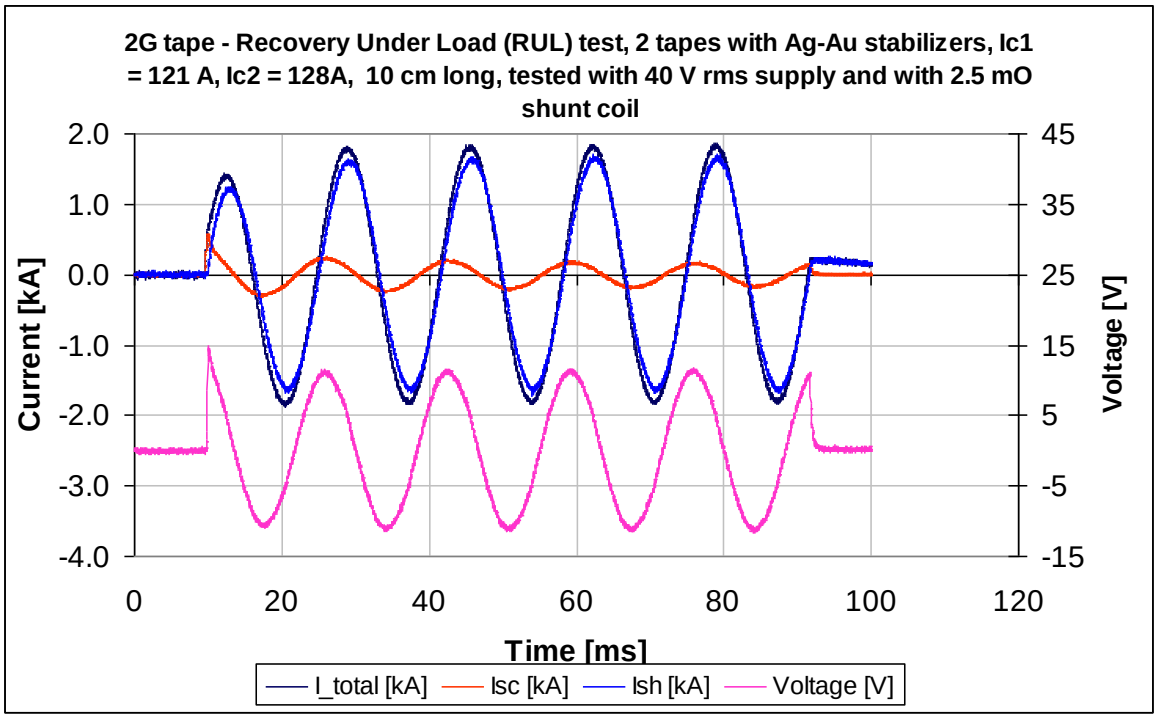


Figure 9: Five cycle simulated fault response for 2 parallel Ag-2.2 atomic percent Au tapes (4 mm wide, 77K Ic = 121 and 128 A) with parallel 2.5 mΩ impedance shunt coil. Note resultant over-voltage during the first cycle indicating a delayed transition to current sharing with the shunt coil.

c) Substrate thickness

The impact of substrate thickness was also studied. 2G HTS production material uses either 50 or 100 micron Hastelloy C276 substrate. The results for varying substrate thickness were similar to those for the pure Ag stabilizer material. As the substrate thickness increases, the resistance decreases and hence the current and energy deposited in the conductor increases during a fault (Figure 10). One difference with the substrate is the relative thermal mass that is added with additional thickness. Being a very resistive material, the Hastelloy® thickness can be doubled with marginal decrease of the overall composite resistivity. As with the stabilizer thickness, varying the substrate thickness has minimal impact on the overall current limiting performance (V/cm) of the device. In addition to standard production 50 and 100 micron thick substrates, samples were also prepared using 75 and 200 micron substrate materials. Limited testing on these samples indicated that the performance matched the simulations.

Based on the tests on samples with varied substrate thickness, a 100 micron Hastelloy C276 substrate was selected as the optimum thickness for the 2G HTS conductor under the broadest range of operating conditions. Substrates of 50 micron thickness tended to have a higher failure rate while substrate of 200 micron thickness would require substantial modification to the production line for minimal advantage.

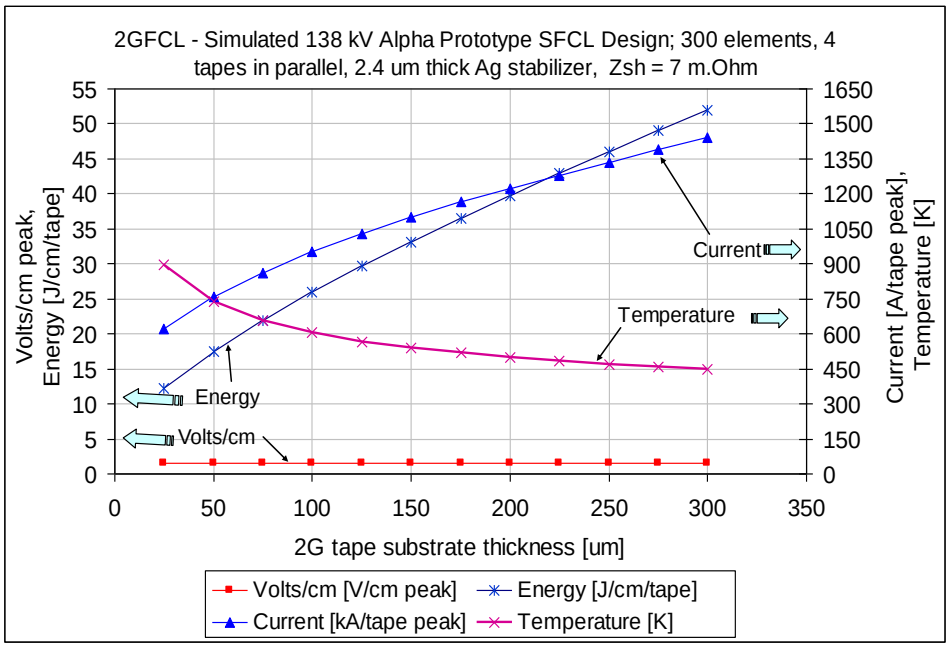


Figure 10: Modeled impact of Hastelloy® C276 substrate thickness on current, energy and temperature rise during a 5 cycle fault for 4 parallel tapes (~2 micron Ag) and parallel 7 mΩ shunt.

2.2.2 – Addition of high resistance heat sink

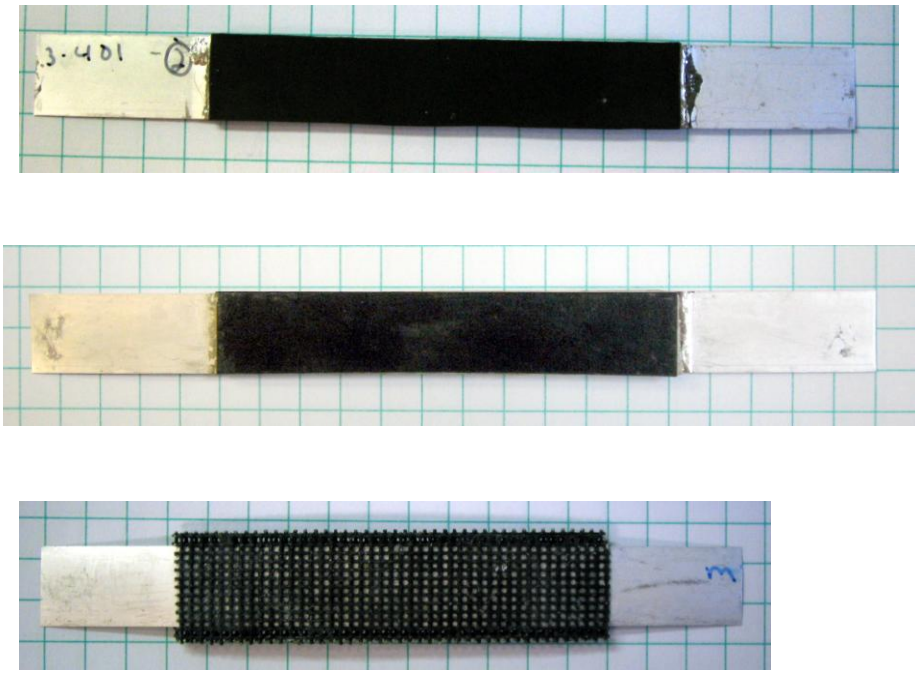
During the fault transient, the 2G HTS superconductor undergoes rapid heating due to the significant levels of energy deposited in the 2G HTS composite. Since the duration of the fault (5 cycles) is short, the quenching and subsequent heating of the tape can be conservatively treated adiabatically with no effective cooling from the surrounding bath. Following the heating of the 2G HTS tape, the heat transfer to the LN_2 bath or other heat sink begins the recovery process for cooling the superconductor back to low enough temperatures so that it recovers its superconducting properties.

In this subtask, we evaluated the impact of adding a parallel high resistance heat sink to the 2G HTS tape to understand how the temperature rise might be mitigated during the fault transient and recovery by adding significant mass to the structure to absorb the energy deposition and reduce the overall composite temperature rise. The heat sink needed to be of high resistance (or insulating) in order to keep the dynamic resistance of the 2G HTS composite high. Two materials were evaluated as potential high resistance heat sinks that could be incorporated with the 2G HTS structure.

- ~ 1 mm thick carbon (graphite)
- SiC mesh

The carbon plates were attached to the 12 mm wide 2G HTS plates using either low melting point indium solder or a Ag filled epoxy. The SiC was attached using Ag filled epoxy. Photos of the various samples are shown in Figure 11. The critical currents of the

samples show no degradation compared to control samples of the 2G HTS without carbon or SiC additions.



(a)

(b)

(c)

Figure 11: Samples of 12 mm wide 2G HTS tape with a) carbon strip attached to both sides of the tape with indium solder, b) carbon strip attached to both side of the tape with Ag filled epoxy, and d) SiC mesh attached to both sides of the tape with Ag filled epoxy.

The sample with the soldered carbon sheets had a lower resistance than the control sample and the other samples with glued attachments due to the electrical conductivity of the carbon as well as the indium solder. During transient over-current testing, the sample failed at 570A (compared to an Ic of ~ 235A). Failure was located at the contact pads on the end of the tape. The sample with glued carbon sheets burned after a second pulse sequence at 1340 A tape current and the bottom carbon plate fell off. The glued SiC sample was able to sustain the target load test current of 1860 A without damage. All samples tested in parallel with a 2.5 mΩ shunt.

Figure 11 below shows recovery under load current and voltage traces for the SiC mesh sample. M3-138 is an internal run number for the underlying 2G HTS tape used in this assembly. The load current on the tape is +/- 150 A_{peak} and is then subjected to a 1860 A fault current. The resultant current and voltage traces can be broken up into 5 areas:

1) initial no load readings
2) initial pre-fault reading at 150 A load
3) fault transient (5 cycles) with peak fault of 1860 A
4) RUL zone where current through the superconductor rises and voltage drops
5) final recovery of the superconductor back to 150 A load.

During the fault transient and recovery, the current is being shared with the parallel 2.5 mΩ shunt.

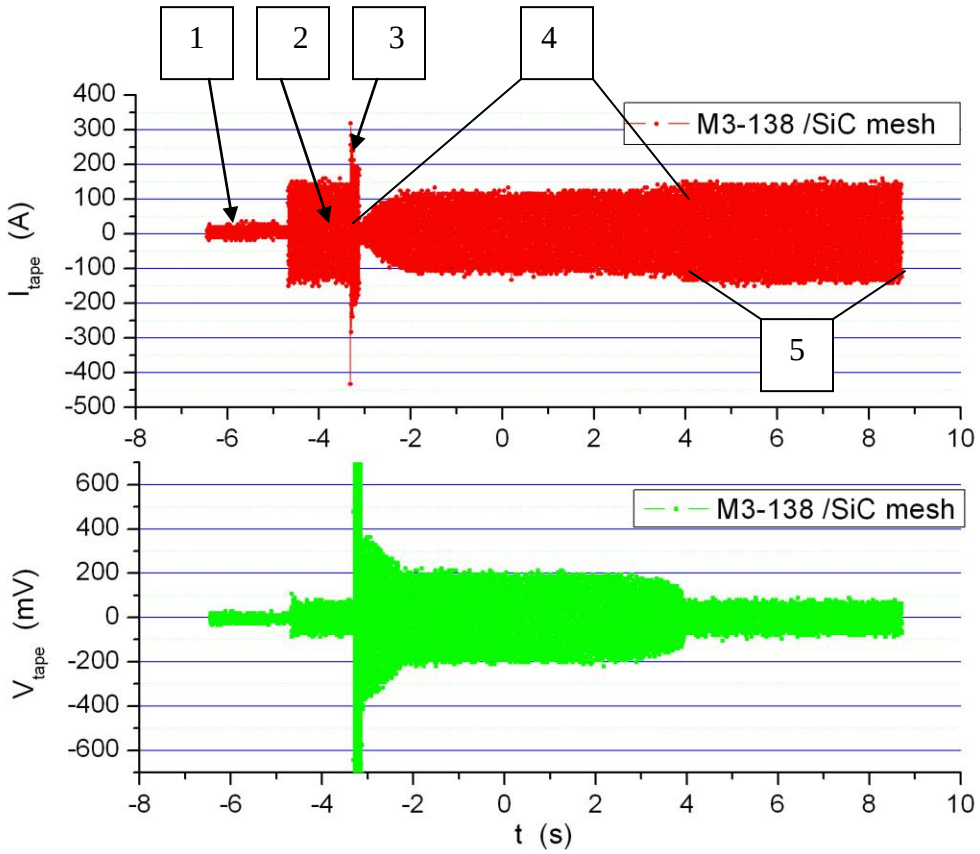


Figure 12: Current (top – red) and voltage (bottom – green) traces during a RUL test on the SiC mesh / M3-138 assembly in open bath LN_2. The 5 distinct zones described in the text are denoted.

The addition of a high resistance heat sink to the 2G HTS tape did not result in improved performance and recovery of the sample after a fault transient. While the SiC mesh demonstrated a RUL capability, it was no better than what was achieved with the M3-138 sample without SiC mesh. Also, with the solid carbon plates, heat transfer into and through the plates was insufficient to mitigate the temperature rise of the 2G HTS composite. Any potential benefit from the addition of the heat sinks was over powered by the loss of cooling by blockage of the tape surface to full contact with the LN_2 cooling bath.

2.2.3 – Modification of 2G HTS conductor surface to enhance heat transfer

During the recovery process, heat transfer to the cooling bath is of prime importance for the 2G HTS to recover to the superconducting state. During the fault transient, once the superconductor quenches (typically at 2-3 times the critical current), the current flow within the 2G HTS structure transfers to the Ag stabilizer and the Hastelloy C276 substrate. The resistance of these parallel components and the impedance of the parallel shunt elements determine the current sharing between the HTS components and the shunt. Within the 2G HTS composite structure itself, the relative resistances of the Ag

and Hastelloy C276 determine the current sharing between these two components of the structure. The very high normal state resistance of the HTS layer, combined with its thin geometry precludes any appreciable amount of current flow in the HTS layer in the normal state. The resultant I^2R heating within the composite HTS structure is then generated during both the fault transient and recovery phases. In order to remove the heat from the 2G HTS composite structure, the heat needs to move from within the structure to the surface of the tape and then transfer to the LN_2 cooling bath. Two heat transfer mechanisms are at work here, the conduction of heat within the structure itself to the surface and the heat transfer from the surface of the tape into the bath. An analysis was conducted to determine the rate limiting step in this heat transfer process. The Biot number was evaluated for the 2G HTS composite structure under a range of operating conditions. It was found that the heat transfer within the 2G HTS composite structure in almost all cases was faster than the heat transfer from the surface of the 2G HTS tape to the LN_2 bath.

Due to the high temperatures generated within the HTS tape during the fault transient, heat transfer to the LN2 bath is governed by the LN2 boiling curve (Figure 13). The horizontal axis is the temperature difference (ΔT) between the tape surface (T_{wall}) and the cooling bath (T_{sat}) while the vertical axis indicates the heat flux from the tape into the bath. Four distinct zones exist on the boiling heat transfer curve. At low ΔT (below ~ 2K), there is convective heat transfer from the surface to the LN2. With ΔT between ~2K and ~15K, there is nucleate boiling heat transfer between the surface and the LN2 bath with discrete bubble formation and rapid replenishment of liquid to the interface. From ΔT of ~ 15K to ~ 30K, there is a transition zone between nucleate boiling and film boiling. With film boiling, a continuous layer (film) of evaporated gas is set up on the surface of the tape. This film limits the heat transfer from the tape to the bath since the thermal diffusion across this vapor layer is much lower than into and through a liquid. With the rapid rise in temperature of the 2G HTS tape to several hundred Kelvin in the 5 cycle fault, the heat transfer immediately moves to the film boiling regime once sufficient energy is deposited into the LN2 bath to set up the vapor film. During cooling, the heat flux into the bath decreases with the film boiling (the minimum denoted as the Ledenfrost point) and becomes the determinant point behind recovery back to the superconducting state.

In general, the boiling heat transfer curve can be shifted based on the surface condition of the heat source. Two approaches were evaluated to modify the heat transfer conditions from the surface of the 2G-HTS tape. The first of these was to develop striations (filaments) in the surface of the tape using processing first developed for low AC loss conductors. As seen in Figure 14, these striations are cut into the top layers of the tape down through the buffer stack to the substrate layer. This patterning disrupts the formation of the film during boiling and extends the temperature range of the nucleate boiling regime, slightly broadening it and shifting it to the right. Fault current tests were conducted on these samples and demonstrated improvement in the recovery when compared to unstriated tapes of similar performance (see Figure 15).

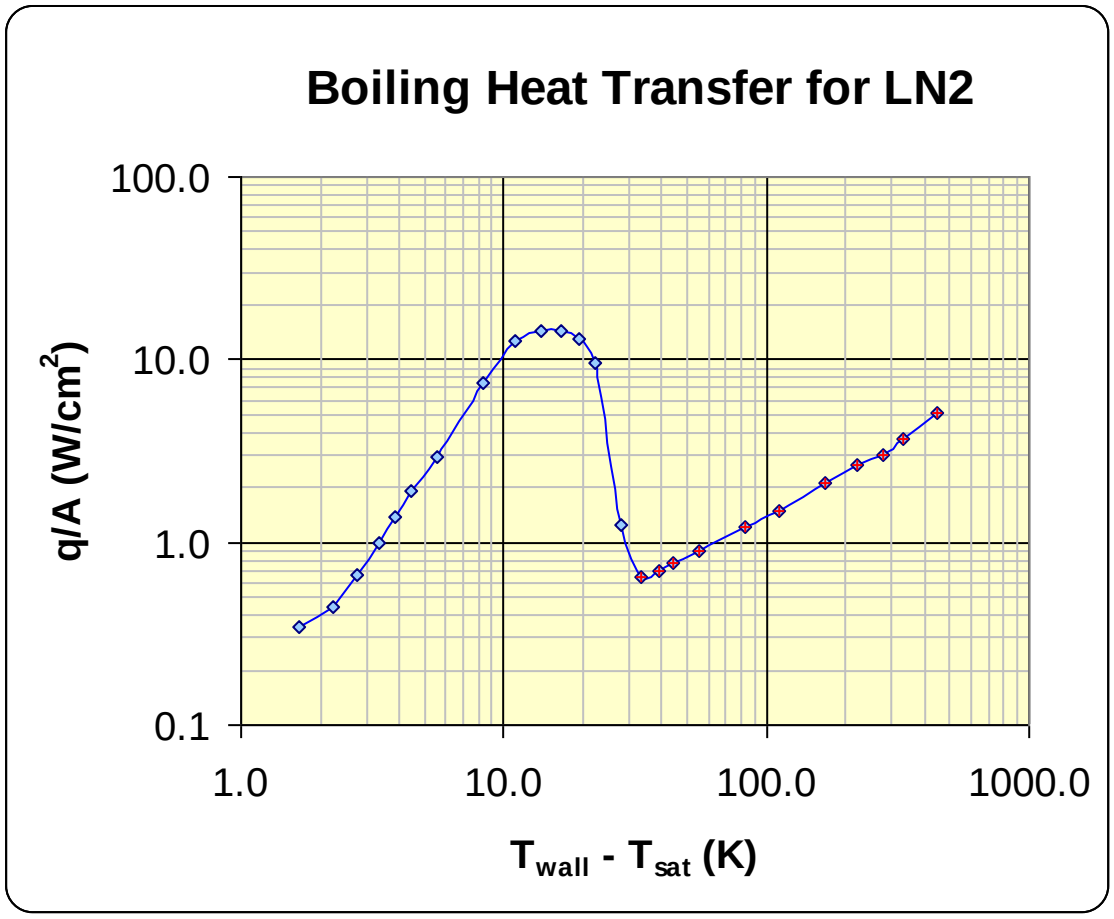


Figure 13: Typical boiling heat transfer curve for LN2 under atmospheric conditions. The film boiling regime is highlighted with red symbols.

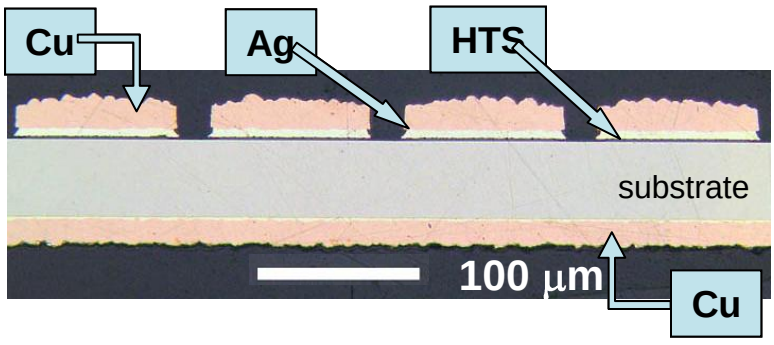
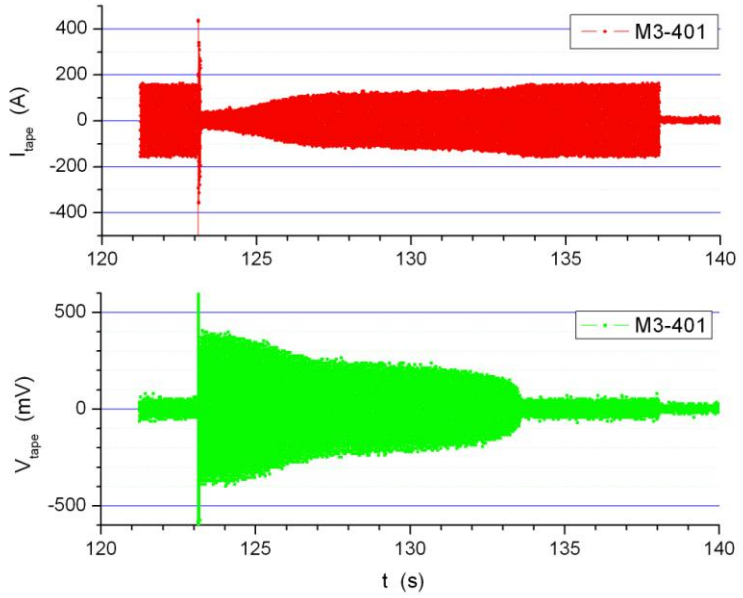
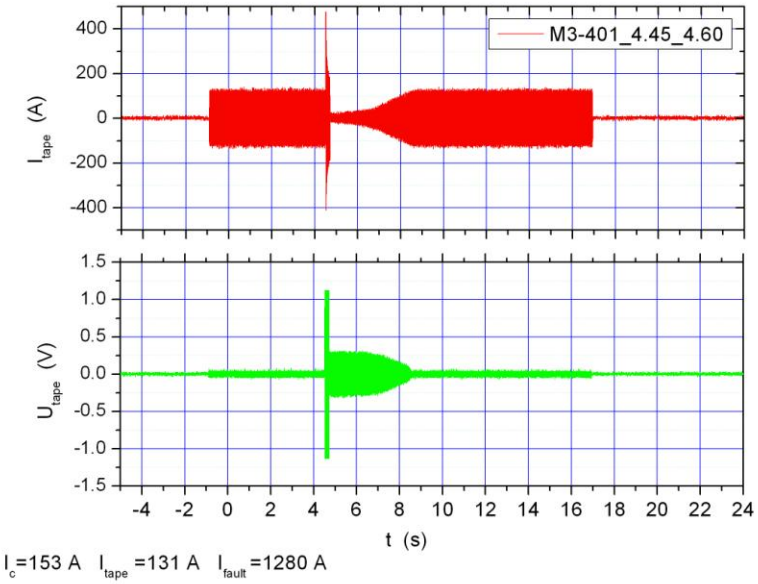


Figure 14: Cross-section of 2G-HTS tape showing striations cut into the surface of the tape .



I_c = 252 A I_{tape} = 172 A I_{fault} = 1600 A



I_c=153 A I_{tape} =131 A I_{fault} =1280 A

Figure 15: Fault recovery traces for unstriated (top) and striated (bottom) 2G-HTS samples (run M3-401). Recovery for unstriated tapes is ~ 10 seconds while for striated samples it is ~ 4 seconds. Fault current for striated samples (1280 A) adjusted to 80% of unstriated samples (1600 A) to account for 20% of material removed from the tape.

The samples used for the tests in Figure 15 consisted of 12 mm wide tape from production run M3-401. The striated samples had about 20% of the material removed from the tape surface compared with unstriated material. The fault current levels for the two samples were adjusted from 1600 A (unstriated) to 1280 A (striated) to reflect the 20% removal of conducting material from the tape surface. A significant reduction in the recovery time was noted from ~ 10 seconds (unstriated) to ~ 4 seconds (striated). It should be noted that the Ic of the striated tapes was reduced to ~ 60% of the unstriated tapes. Since this is well below the expected 20% value, it is indicative of additional damage to the YBCO layer during the striation process.

The second surface modification technique evaluated looked at adding "dots" of solder to the tape surface (Figure 16). Indium was chosen for the dots due to its low melting point and ease of bonding to the silver surface. After the fault and during recovery, a superconducting current path develops along the tape following the evolution of the local temperature profile. The idea behind this concept is to facilitate the formation of a continuous superconducting path along the tape by locally modulating its heat capacity and heat transfer to the coolant and thus creating a temperature distribution favorable for the recovery process. The placement of the additional surface material (indium "dots") at regular intervals along the tape can achieve this beneficial result. In this way, the "randomness" of the normal domain distribution is removed and formation of large hot spots is suppressed along the tape. Normal state regions are broken down to small islands that can more quickly recover back to the superconducting state. This process is illustrated in Figure 17.

Figure 16 Indium "dots" test sample – 12 mm wide with 5 indium dots placed along tape. Current and voltage tap connections are also located on each end.

As can be seen in Figure 18, the recovery time for samples with indium dots compares favorably to samples with unmodified surfaces. In these Recovery Under Load (RUL) tests, the current refers to current flowing in the tape after quench is initiated. With the indium dots, there is an approximate 2 second recovery time advantage for RUL currents of 40 – 70 A (as compared to Ic's in the tape of ~ 250 A). Measurements were conducted in a liquid nitrogen bath at atmospheric pressure (77K).

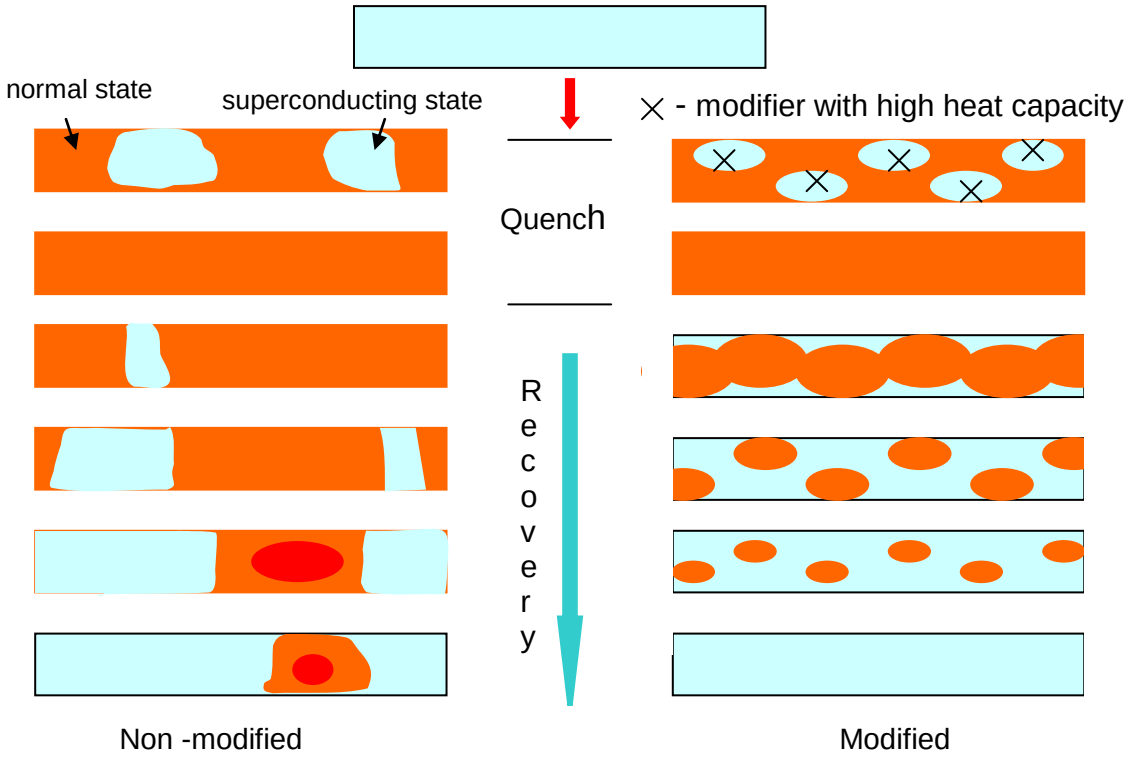


Figure 17: Illustration of the enhanced recovery process with the presence of a sample modified with indium dots (right column) as compared with an unmodified sample (left column). The presence of the indium dots promotes recovery at regular intervals due to the higher local heat capacity and enhanced heat transfer to the coolant bath, mitigating against hot spot formation.

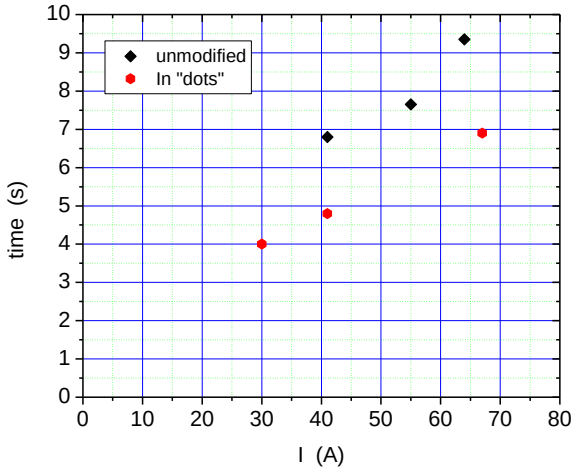


Figure 18: Plot of recovery time versus Recovery Under Load currents for unmodified samples and samples modified with indium "dots". Base 12 mm wide tape Ic is ~ 250 A (77K, self field). There is a ~2 second recovery time improvement with the modified tapes. Cooling done in 77K LN2 bath at atmospheric pressure.

For both the striated samples and samples modified with indium dots, there is clear evidence for enhanced cooling and recovery with the samples. To implement these approaches in long length production tapes will require substantial manufacturing development activities that need to be warranted commercially.

2.2.4 – High current conductor
In this task we evaluated

i) the impact of higher critical current tapes on the quench, fault current and recovery behavior of the system; and

ii) the impact on performance with a mix of tapes of different critical currents.

The impact of higher critical current tapes affects the number of parallel tapes required to carry the current under standard operating conditions. For example, if 1200 A of Ic is required for the design, this can be provided by either 6 x 200 A Ic tapes or 4 x 300 A Ic tapes. Time to quench (typically the time to reach 2-3 times Ic) would be unaffected between the two cases, assuming similar Ic's in parallel tapes (the case with mixed Ic's is discussed below). The main impacts of using fewer tapes with higher critical currents are twofold. First, since fewer tapes are used in parallel, the effective normal state resistance of the tape set is higher resulting in a higher V/cm being generated across the tapes for a given current. Secondly, with fewer tapes, the mass of the tape set is reduced leading to faster temperature rise as energy is deposited into the tapes after the quench. As a result of these consequences, if a higher Ic tape is used, the architecture of the tape may have to be altered (additional mass to offset the temperature rise) and/or the system parameters such as the parallel shunt impedance may have to be optimized so that the current sharing between the HTS tapes and parallel shunt falls within acceptable operating limits.

The effect of varying critical current with parallel tapes was tested by placing 2 tapes with large differences in Ic (roughly a factor of 2X) in parallel and then subjecting them to fault current. The results of these tests are illustrated in Figure 19. The disparity in Ic between the 2 samples leads to the lower Ic tapes switching faster than higher Ic tapes. This is due to the difference in time it takes for the fault current to reach the higher quench current (~ 2 to 3 times Ic).associated with the higher Ic tapes. This is borne out in the test results, with the low Ic tape quenching ~ 0.5 ms faster than the high Ic tapes. Once both tapes have quenched, there in no difference in the normal state resistivity of the tapes and the fault current limiting function performs as designed. The main concern is current sharing between the two tapes during the fault transient. If the current did not adequately share and switch between tapes, voltage transients and/or hot spots could develop and result in damage to the tape. We did not see the development of overvoltages and did not experience any damage to the tape. While we did not see any detrimental effects from mixed tapes with different Ic's, we would not recommend this as common practice without extensive testing, particularly if a large number of parallel tapes are used.

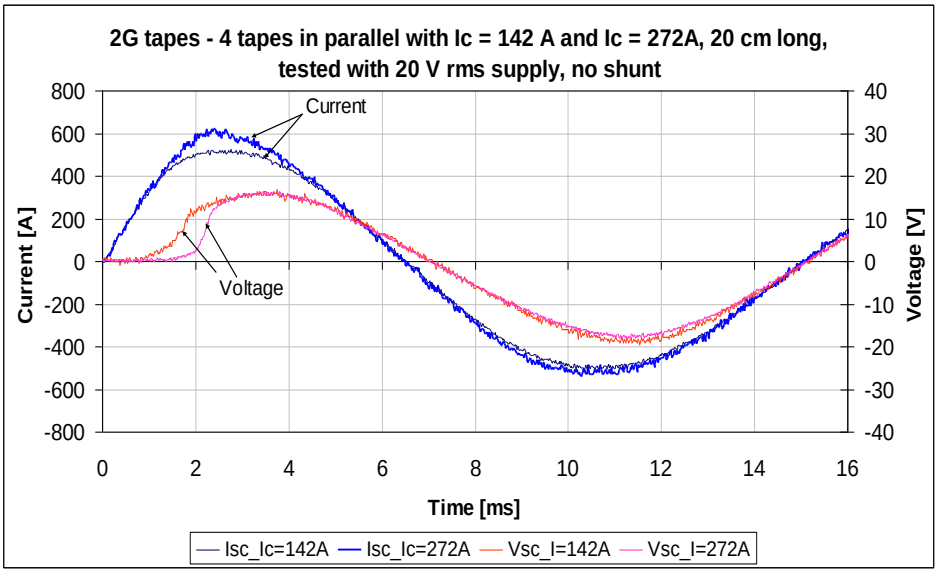


Figure 19 Plot of voltage and current traces for two parallel tapes with a wide variation (142 A vs. 272 A) in conductor Ic. Other tape parameters the same. As expected, the lower Ic tape transitions before the higher Ic tape. No overvoltage or hot spot damage was experienced in these tests.

2.2.5 Long length integrated conductor

In this subtask we evaluated the impact of the various conductor modifications on the long length production of the 2G HTS tapes. Variations in Ag thickness and composition are readily incorporated into the production process. Hastelloy substrates up to 100 microns thick can readily be used, although twice the length of 50 micron substrate material can be processed on a given set of spools due to the reduced thickness. As noted before, surface modifications such as striations or added surface structures such as indium dots would require extensive production tooling development which would require commercial justification to implement. The development of higher current 2G HTS tapes is an ongoing process that fell outside the scope of this project. In addition, continuing cost reduction in the 2G HTS process is required to bring the price / performance of the tape to levels that are commercially feasible for widespread introduction into the marketplace.

3.0 HTS Matrix Development

The Superconducting Fault Current Limiter (SFCL) Matrix is based upon parallel superconducting elements and shunt elements as indicated in Figure 20 below. Under standard operating conditions, the current in the SFCL flows through the superconducting elements since the impedance of the superconducting elements is essentially zero. In parallel with the superconducting elements are shunt coil elements, typically consisting of wound copper coils with high X/R ratios. Since these shunt elements have high impedance as compared to the superconducting elements, during standard operation there is essentially no current flow through them.

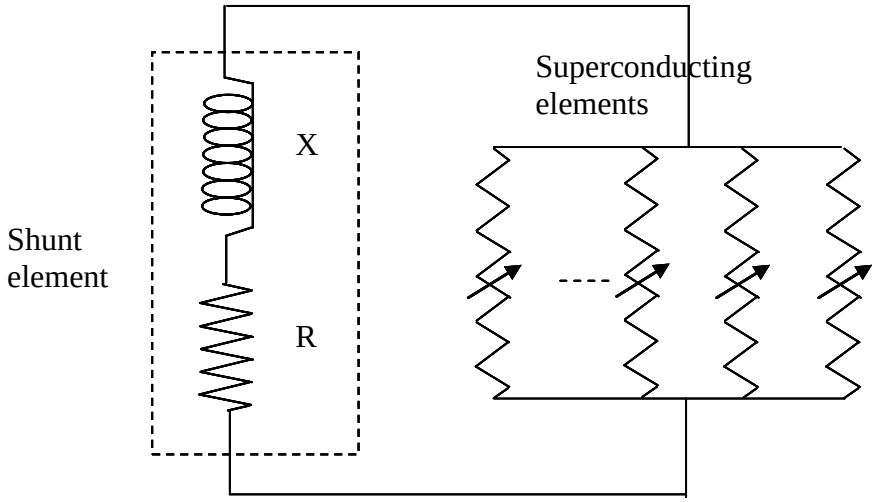


Figure 20: Schematic of a SFCL Matrix. consisting of a number of parallel superconducting elements in parallel with a shunt element.

During a fault transient, the superconducting elements rapidly transition ("quench") to the normal, non-superconducting state. Due to the high dynamic resistance in the quenched state of the superconducting elements, a substantial portion of the current switches into the shunt element, introducing a large impedance into the grid, reducing the fault current to levels that can be tolerated further down the line.

The number of superconducting elements required in parallel is driven by the operating current of the system. The number is derived by taking the peak current of the system and dividing it by the critical current of the individual elements. The peak current is adjusted by a factor to reduce the operating index losses. Typically, the operating current is set at a level of ~80% of the critical current. For example, for a system operating at 1000 Arms, the peak current is 1414 A. With the 80% factor, this value is raised to 1414 A/0.8 = 1768 A. For BSCCO2212 MCP elements, this would require 1 element operating under subcooled LN2 conditions. For parallel 2G HTS tapes, assuming ~ 300 A critical current per tape, the number of tapes required is 1768 A / 300 A = 6 tapes.

The length of each superconducting element required is driven by the voltage of the system. Based on the operating parameters of the system, the HTS elements are able to

sustain a given V/cm across its length without degradation. For the BSCCO2212MCP elements, this value was found to be ~ 6V/cm. For elements made out of parallel HTS tapes, the value was typically, in the range of 1.0 -2.0 V/cm. For example, for a phase voltage of 80 kV, using BSCCO2212 MCP elements with a V/cm limit of 6V/cm, the total length of elements in series would be 80,000V/6 V/cm = 13334 cm = 133 m. With a typical length of 20 cm per BSCCO2212 MCP element would require 667 elements per phase assuming 1 element is sufficient to carry the current load. With 2G HTS tapes with a V/cm limit of 1.6 V/cm, the length of each tape required is 80,000 V / 1.6 V/cm = 50000 cm, = 500m. Using the prior calculated current requirement requiring 6 parallel tapes, the total tape length requirement for the phase is 6 x 500 m = 3000m.

3.1 MFCL Matrix Development (Phase 1)

In Phase 1 of the project, the functionality of the BSCCO222 MCP elements were tested using the MFCL concept in a pre-prototype proof of concept demonstration. The MFCL concept is depicted in Figure 21 where the number of parallel current limiting matrix elements is determined by the current requirement of the system and the number of the sereial current limitin modules is determined by the voltage of the system. Within the current limiting matrix elements you have the BSCCO2212 MCP element in parallel with an inductive winding of copper. During normal superconducting operation, the zero resistance of the superconducting element drives all of the current flow through the BSCCO2212 MCP element. During a fault transient when the critical current of the BSCCO2212 MCP element is exceeded, it becomes a highly resistive element (comparable to stainless steel) and most of the current flow is then shunted through the parallel inductive element of resistive copper. The combined resistive and inductive elements put a impedance into the line thus limiting the fault current. The beauty of the MFCL concept also lies in the placement of the parallel inductive winding in relation to the BSCCO2212 MCP element. In practice, the BSCCO2212 MCP element is placed in the clear bore of the inductive winding so that when the current is transferred to the inductive winding during the fault transient, a magnetic field is generated by the inductive winding and projected onto the BSCCO2212 MCP element aiding in a uniform quench of the HTS element to mitigate the formation of hot spots. This is enabled by the BSCCO2212's critical current vs. magnetic field quench performance in the LN2 environment. This is referred to as the triggering mechanism which by aiding in the simultaneous quench triggering of all of the HTS elements ensures the voltage is evenly distributed across the superconducting components.

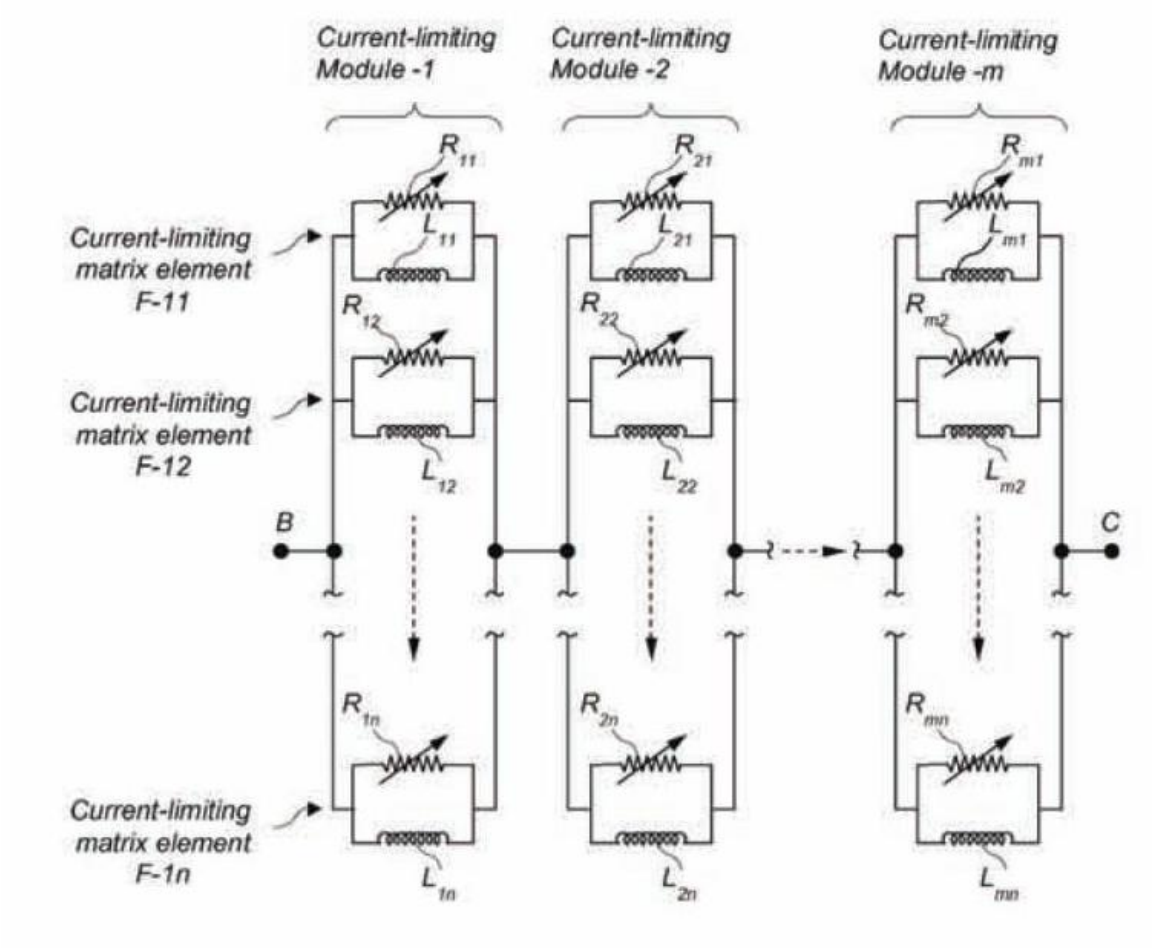


Figure 21 – Schematic of the MFCL current limiting matrix concept

3.2 SFCL Matrix Development (Phases 2, 3)

During Phases 2 and 3, the HTS material in the matrix was changed to 2G HTS YBCO based tapes. During this time, a parametric modeling tool was developed to evaluate the operational parameter space for the SFCL. Critical input parameters such as operating current and voltage, the critical current(s) and dynamic resistance of the 2G HTS tapes, the reclosure sequence of the grid and the available cooling are input into the model. A typical view of the model is given in Figure 22. Outputs include plots of the voltage and currents in the superconductor and shunts, temperature rise and fault current reduction.

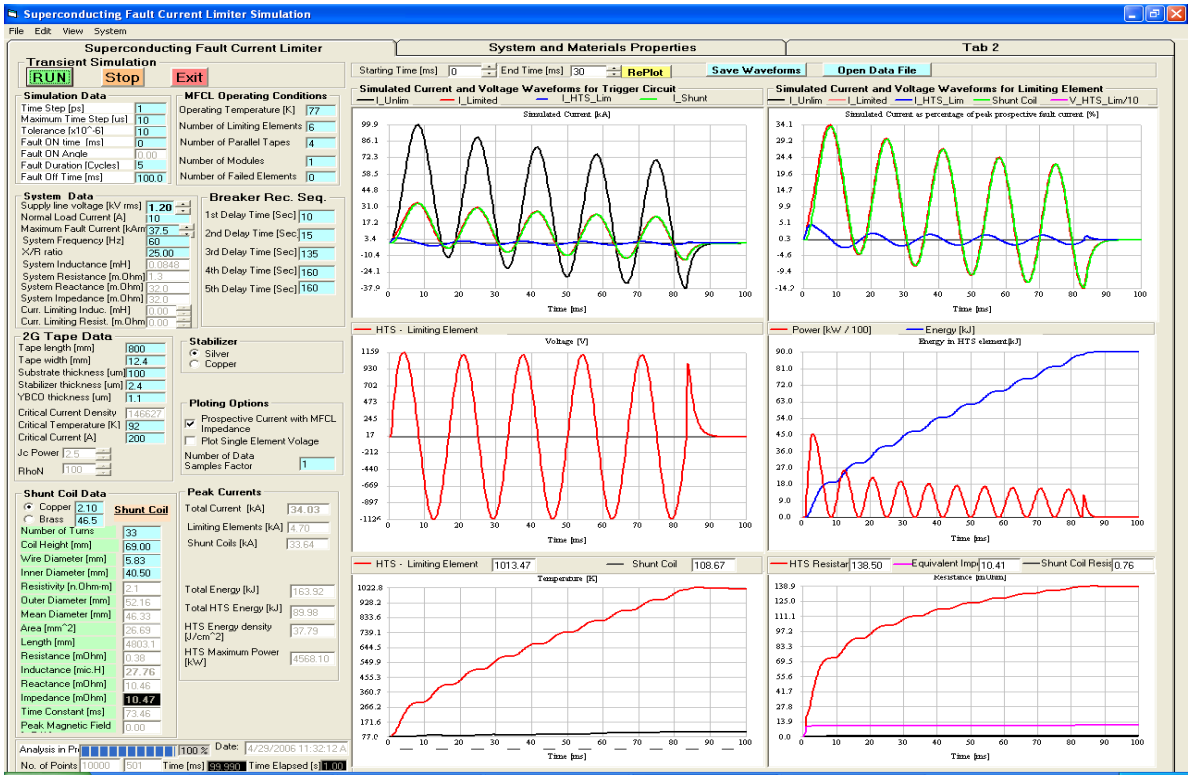


Figure 22 Example of the parametric modeling tool developed for evaluating the SFCL under a range of operating parameters. Output includes plots of the voltage and current traces for the superconductor elements and shunt coils, temperature rise and fault current reduction.

In addition to the overall system modeling, studies were conducted on critical elements of the SFCL matrix including:

a) thermal aspects of the cooling during recovery, including recovery under load
b) mechanical aspects of the shunt coils under high pulse loading
c) design optimization of the current connections to the 2G HTS tapes

a) Thermal modeling

ANSYS and other models were developed to predict the final temperature of the 2G HTS tape when subjected to given fault conditions and durations. Since the heating takes place almost instantaneously during the fault transient, the bulk of the calculations were based on adiabatic conditions. Fault energies of up to 25 J/cm were used for most of the calculations as the upper limit for safe operations. Two superconducting element designs were evaluated. The first of these were a basic straight element design, consisting of parallel straight lengths of 2G HTS tapes with terminations at each end. The second element design is a meander path where the 2G HTS tapes are wrapped in a continuous path around "pullies", minimizing the number of end terminations and the associated losses. Examples of the models are shown in Figures 23 and 24.

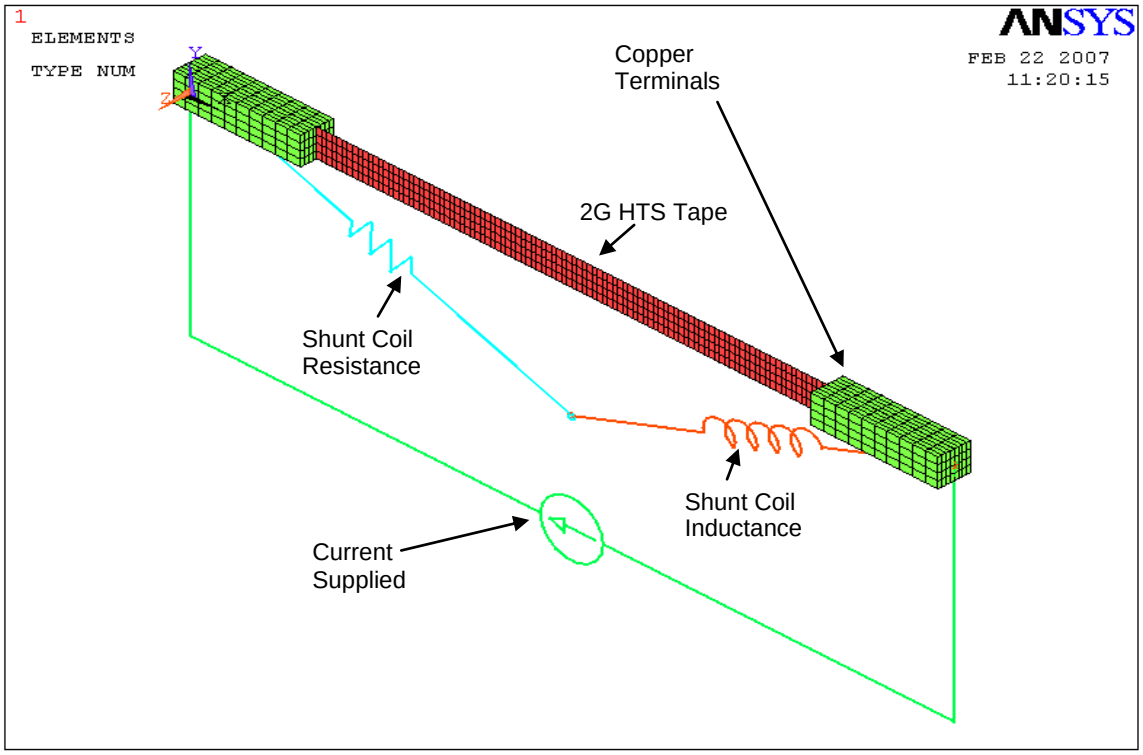


Figure 23: ANSYS model schematic of a straight 2G HTS element. Multiple parallel tapes can be included. Parallel shunt elements can also be included.

The heat transfer from the 2G HTS and shunt elements to the LN2 coolant bath was also modeled. During the fault transient the 2G HTS tape heats several hundred Kelvin into the film boiling regime. Cooling from the film boiling regime was modeled under both atmospheric and other conditions such as subcooled and/or pressurized LN2 bath (see Figure 25). Observations of the results of the modeling include that most of the time during recovery is spent in the film boiling regime and that the minimum film boiling value (the Ledenfrost point) is a critical parameter with respect to the ability of the material to recover. The copper terminals act as heat sinks and impact the cooling of the tape near the terminals. In addition, the critical current of the tape was shown to have an influence on the recovery, mainly associated with the reduced mass that had to be chilled.

Transient cooling effects were evaluated to see if any additional benefit was available. Transient cooling takes into account the amount of energy required to diffuse into the LN2 to set up the film boiling. The calculations indicated that at best, only a few percent of the fault energy generated is mitigated by the transient cooling, leaving the adiabatic model as sufficiently accurate to conservatively describe the cooling process.

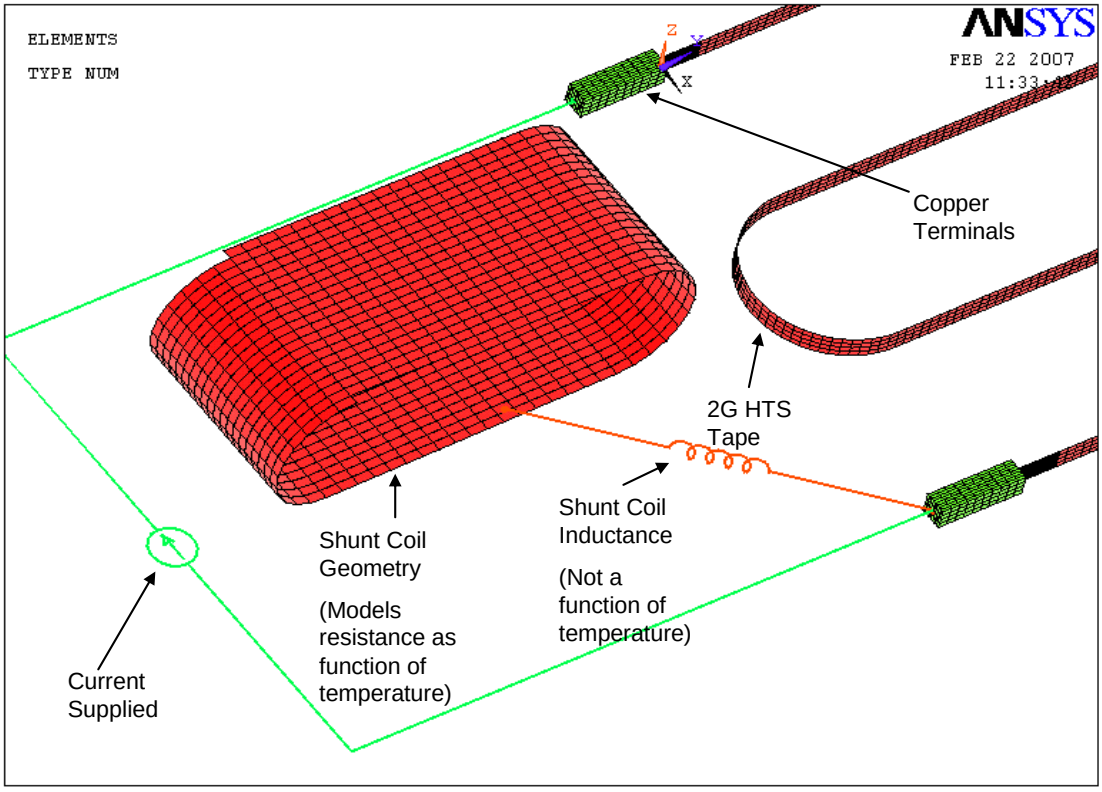


Figure 24: ANSYS model schematic of a meander path 2G HTS element , including shunt coil.

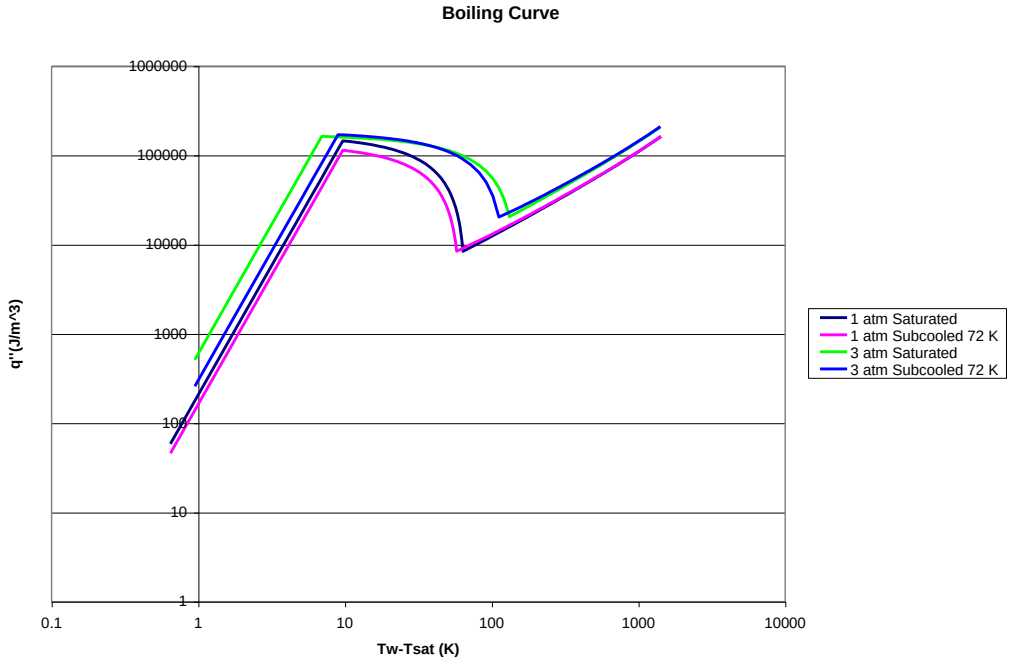


Figure 25: Modeled LN2 cooling curve for different operating conditions.

The modeling of the cooldown and recovery,, including recovery under load, was conducted for a multitude of operating conditions. Some of these modeling results are shown in Figure 26 which plots the voltage across the superconducting elements under a variety of operating conditions. As the voltage returns to zero, the superconducting elements have sufficiently recooled and the elements have recovered to their prefault state.

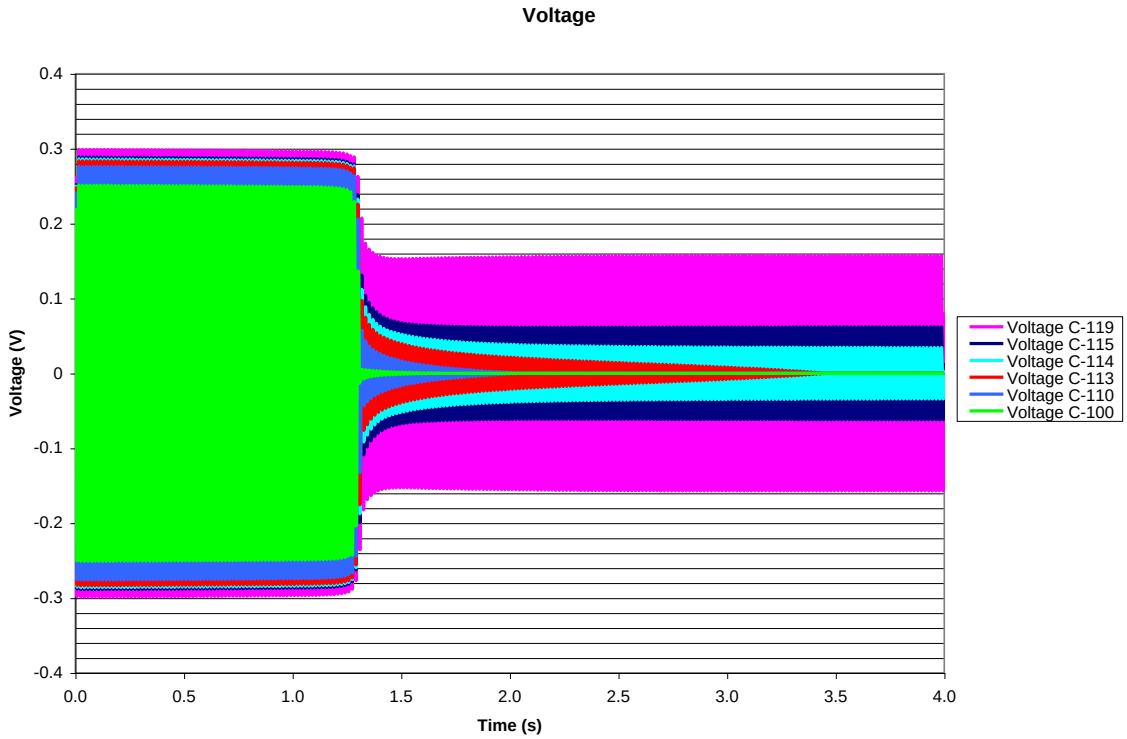


Figure 26: Voltage vs. time plots for a variety of operational conditions (C-100 to C119). Some plots show recovery ranging from ~ 1.3 seconds to 3.5 seconds. Three conditions do not recover within 4 seconds.

b) Mechanical aspects of the shunt coil design

During the fault transient, once the superconducting elements quench, the bulk of the fault currents rapidly switch into the parallel shunt coils. These high currents subject the shunt coils very high hoop stresses that can lead to failure of the shunt coils. Figure 27 shows an early shunt coil design that failed due to the high magnetic stresses in the coil. In addition to the magnetic loading, the coil is also subject to thermal heating during the fault transient. After a number of these early failures, a more systematic design study was implemented.

The design study had three main objectives:

- to design the shunt coil to withstand the electromagnetic forces during the fault transient
- to design the shunt coil to withstand the thermal loading during the fault transient

- to design the shunt coil for minimal normal losses during cooling to aid in the recovery process
- to design robust shunt coil connections

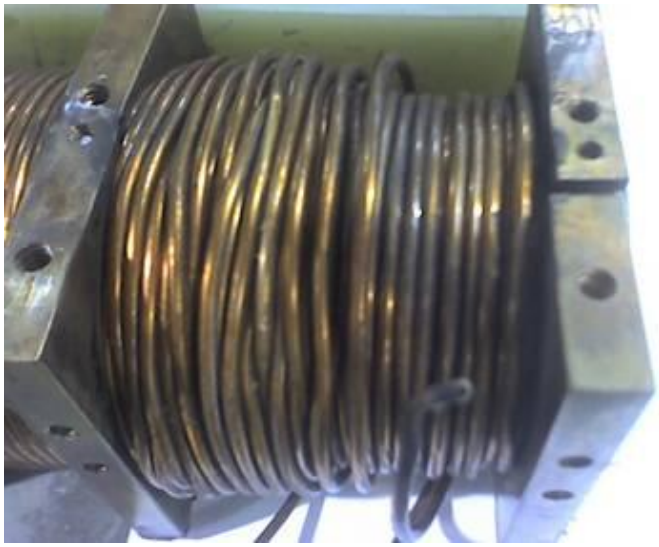


Figure 27: Photo of an early shunt coil that failed during a fault transient test. The coil was subjected to very high hoop stresses and thermal loading during the test, resulting in a failure of the copper windings.

Two shunt coil configurations were initially evaluated, a solenoid coil design and a racetrack coil design. Earlier shunt coil designs were modified to change the copper conductor from round to an insulated rectangular conductor for improved packing factor and mechanical support. In addition, stainless steel overbanding was added to contain the high hoop stresses on the outer diameter windings. FEA model results for these two configurations are shown in Figure 28. The results indicate that there is no advantage with the rectangular racetrack coils. The later designs were then focused on the circular solenoid designs. For typical system parameters under consideration, it was determined that the target operating current in the shunt coil during the fault was ~ 27 kA. Six circular coils (4 with overbanding, 2 without, Figure 29) were fabricated and tested at KEMA Powertest in Chalfont, PA. The test currents included loadings that followed the American Electric Power reclosure sequence. For example, for a 40 kA test, the shunt coil would be subjected to 4 shots at 40kA and 3 shots @ 40kA series (5 cycle fault, 18 cycles off, 5 cycle fault).

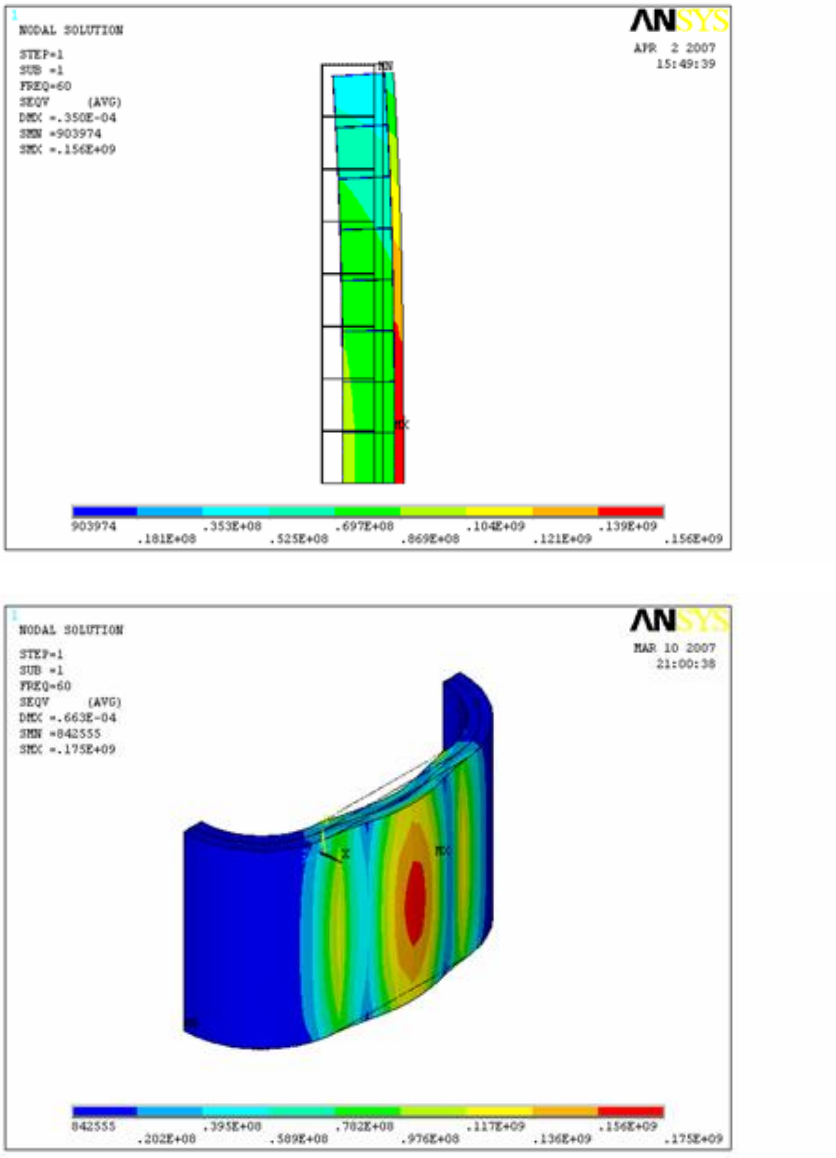


Figure 28: ANSYS stress results on 2 different shunt coil designs – circular coils (top) and racetrack coils (bottom). Analysis showed no benefit for the racetrack configuration and future work focused on the circular designs.

The tests at KEMA showed that for coils without overbanding, breakdown of the Formvar type insulation occurred at hoop stresses of resulting from fast pulsed current loading of 30-35 kA. This result is shown in Figure 30. Overbanded coils L1 and L2 were tested up to 40 kA without any signs of damage as shown in Figure 31. To find the limit on the overbanded design, coil S1 was taken up to 55 kA without damage with catastrophic failure at 65 kA.

Figure 29: Six demonstration shunt coils, 4 with stainless steel overbanding (rear) and two without overbanding (front).

Figure 30: Shunt coil without overbanding with indications of insulation damage after pulsed current loading of ~ 35 kA. Coil has just been removed from LN2 bath.

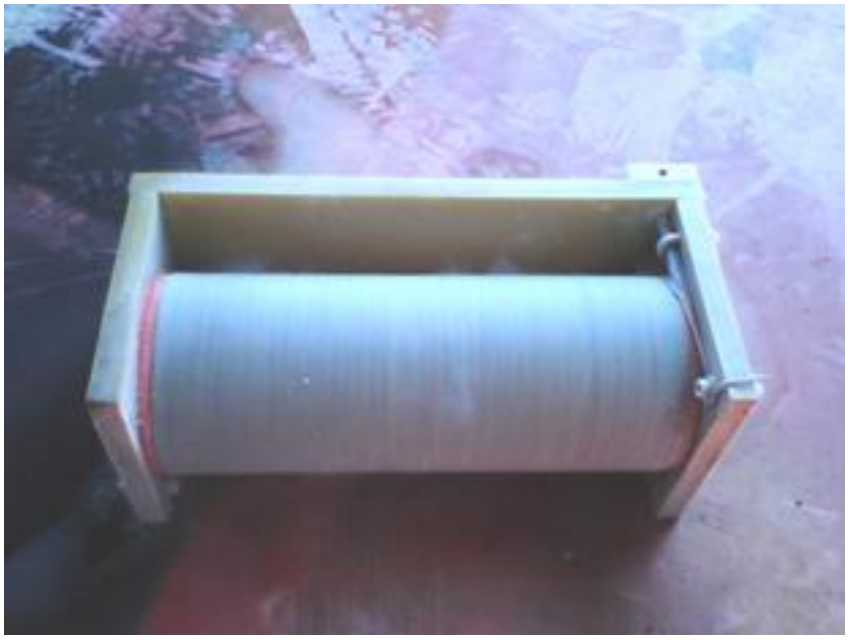


Figure 31: Shunt coil with stainless steel overbanding after being subjected to a 40 kA set of tests of 4 shots at 40kA and 3 shots @ 40kA series (5 cycle fault, 18 cycles off, 5 cycle fault) with no indication of damage.

Subsequent to these tests a design methodology was in place that ensured the shunts coils would mechanically sustain the stresses they would be subjected to during the fault transient. Shunt coils fabricated after this point in the program did not suffer from degradation in any of the fault current tests conducted. In addition to the stresses encountered during a fault, the shunt coils were modeled to evaluate the X/R ratio shift they would undergo during the heating the coils would experience during the fault. The reactance of the coils were unchanged, but the resistance of the coils could increase by a factor of up to 10 or more due to the change in copper resistivity (typically CDA110) with temperature rise (~77K to up to 400K).

c) Current transfer into the tapes

Current transfer and distribution into the 2G HTS tapes is critical to the operation of the SFCL. In this task, the current transfer into the 2G HTS tape from the end contacts was modeled and verifying experiments conducted. Early in the program, mechanical versus soldered joints were evaluated. These tests showed that mechanical joints offered superior reliability versus soldered joints, particularly when thin Ag was used as the stabilizer on the 2G HTS tapes.. The pressure required to give reliable joints was determined early on using a test rig that measured contact resistance versus applied pressure. When the 2G HTS tape is superconducting, the current readily transfers through the outer Ag layer into the zero resistance HTS layer. During the fault transient, the current in the 2G HTS that does not transfer to the parallel shunt, redistributes and is carried in both the Ag and Hastelloy C276 layer. One result of the modeling was that the current flow into the tape is a function of the temperature of the tape and contact (tied to

the normal state resistivity of the various components versus temperature). Examples of the contact modeling are shown below in Figure 32, showing how the current transfer changes based on the whether the 2G HTS is superconducting or in the quenched "normal" state.

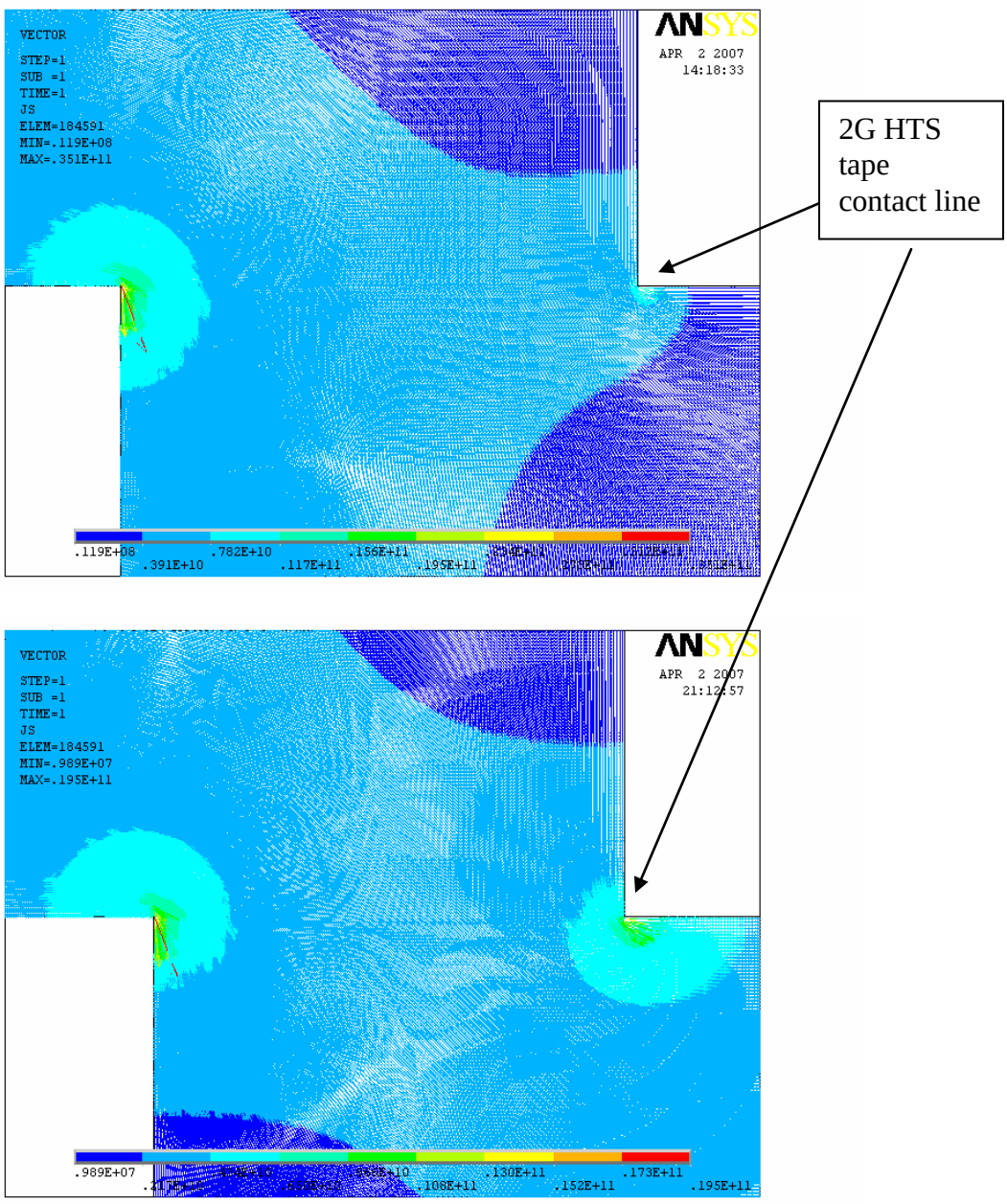


Figure 32: Current distribution vs. location in a mechanical contact with the superconducting tape located as indicated between the top and bottom blocks. Top plot is for when the 2G HTS tape is in the superconducting state. Bottom plot is after the 2G HTS tape has quenched.

4.0 Matrix Module Design, Assembly and Test

4.1 MFCL Matrix Module Design, Assembly and Test

In Phase 1, the design requirements for the MFCL pre-prototype are summarized in Table 3 below. The matrix of the BSCCO2212 MCP elementsand parallel connected inductors are contained in the matrix assembly immersed in the liquid nitrogen bath in the system cryostat consisting of an inner pressure vessel and outer vacuum vessel. The pre-prototype MFCL contained 36 elements connected in series, each consisting of a BSCCO2212 MCP tube connected in parallel with an inductive winding surrounding the tube. Heat is removed from the bath with two Cryomech AL-300 Gifford McMahon cryocoolers. The external connectionis made to the matrix through a set of lead assemblies that penetrate the vacuum vessel, travels through the vacuum space, penetrates the pressure vessel and the connects to the matrix in the liquid nitrogen bath.
The MFCL was tested in two stages. A scaled mock-up of the matrix device was tested in an open LN2 bath in late 2003 at the Center for Advanced Power Systems (CAPS) at Florida State University. This testing at CAPS demonstrated the BSCCO2212 MCP performance and consistently achieved the 6 V/cm electric field strength on the material. The test results also validated the desired dynamic concepts of the matrix concept including equal current sharing, no interference from the magnetic fields from adjacent elements and rapid dynamic resistance development and current transfer to the current limiting impedance.

Table 3: MFCL Pre-Prototype design requirements.

Property	Magnitude
Line-to-line voltage	15 kV
Phase-to-ground voltage	8.66 kV
Load Current	800 Arms
Overcurrent allowance	20 %
Prospective Fault Current (Symmetrical)	10 kA
Limited Fault Current (Symmetrical)	8 kA
Prospective Fault Current (Asymmetrical)	25 kA
Fault duration	3 cycles
Cryostat Operating Temp. Range	74K to 77K

The single phase cryostat is approximately 1.5 m in diameter and 2.75 m tall. An additional 0.25 m in height is added for the bushings. The overall weight of the assembly is ~3 tons when filled with LN2. Other than the voltage design, the basic approach (shown in Figure 33) is scalable to the larger full system design.

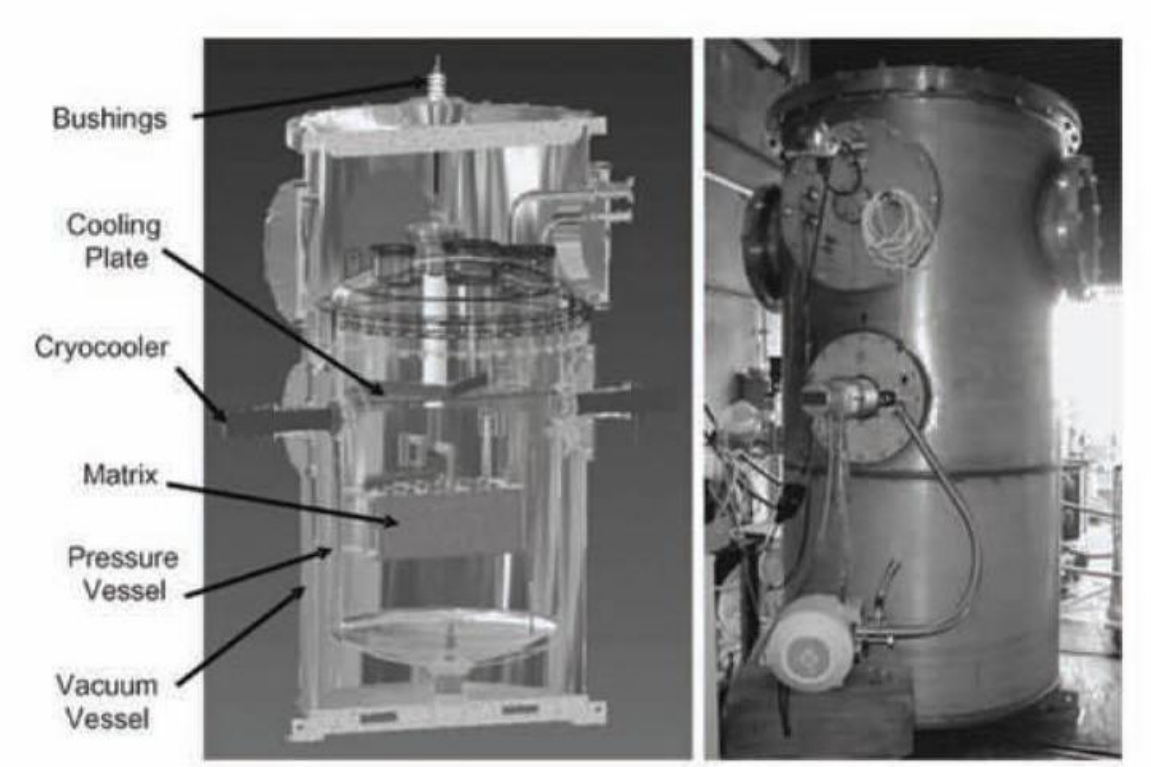


Figure 33: (left) Schematic of the pre-prototype proof-of-concept demonstration unit with major components identified and, (right) photo of the actual unit undergoing test.

After the CAPS test, the single phase prototype was constructed and testing of the MFCL was conducted at KEMA PowerTest outside of Philadelphia, PA. Figure 34 shows the the schematics of the test circuit wosed for testing the pre-prototype MFCL at KEMA. The test system consists of the short circuit power source capable of providing a prospective symmetrical rms current of 10 kA (asymmetrical peak fault current of around 25 kA), at voltages of up to 8660 Vrms. The supply has the capability to vary both voltage and system source impedance to control the voltage and short circuit current fo the MFCL assembly.

Pre-qualification tests of the matrix assembly were conducted at 480 Vrms and 2400 Vrms. The first set of tests at 480 Vrms was conducted with a partially populated matrix of assembly of 6 out of the possible 36 elements. Twenty two faults were applied with fault durations ranging from 0.5 to 3 cycles and prospective currents ranging from 20 – 27 kA asymmetrical first peak. This was followed by a series of tests with a fully populated matrix of 36 elements at the conditions shown in Table 4. Figures 35 and 36 show example waveforms from the tests. This shows the current limiting before the first peak of the prospective surrent and shows significant current limiting in effect by the third cycle. Table 5 summarizes the current limiting performance achieved in the Phase 1 test program.

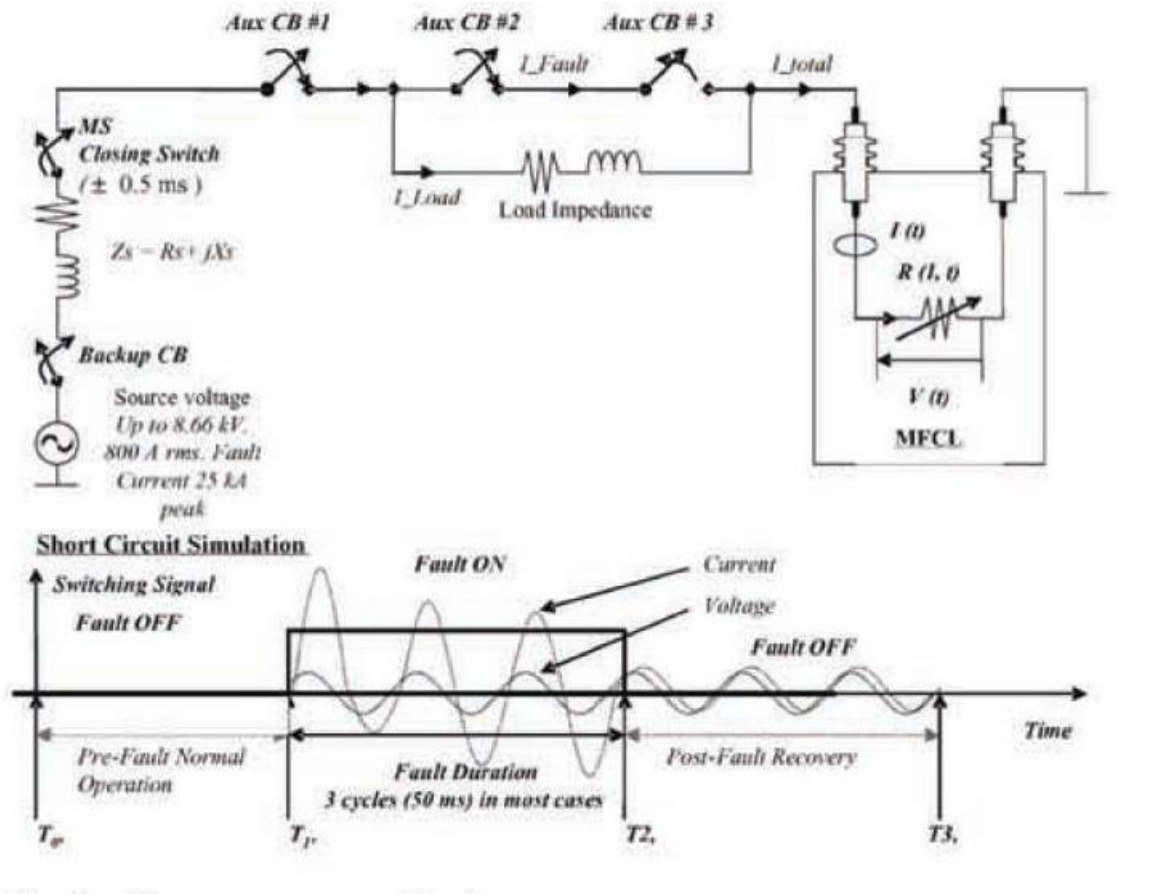


Figure 34 MFCL Pre-prototype test circuit used in the KEMA testing.

Table 4: Summary of applied faults used in MFCL testing

Input Voltage (Vrms)	Fault Duration (Cycles)	Asymmetric First Peak (kA)	Cryostat Temp	Faults Applied
2400	.5 to 3	17 to 27	77K Open Bath	9
4160	.5 to 3	19 to 23	77K	6
4160	3	17 to 25	74K	3
8660	.5 to 3	19 to 23	77K	5
8660	3	17 to 25	74K	3

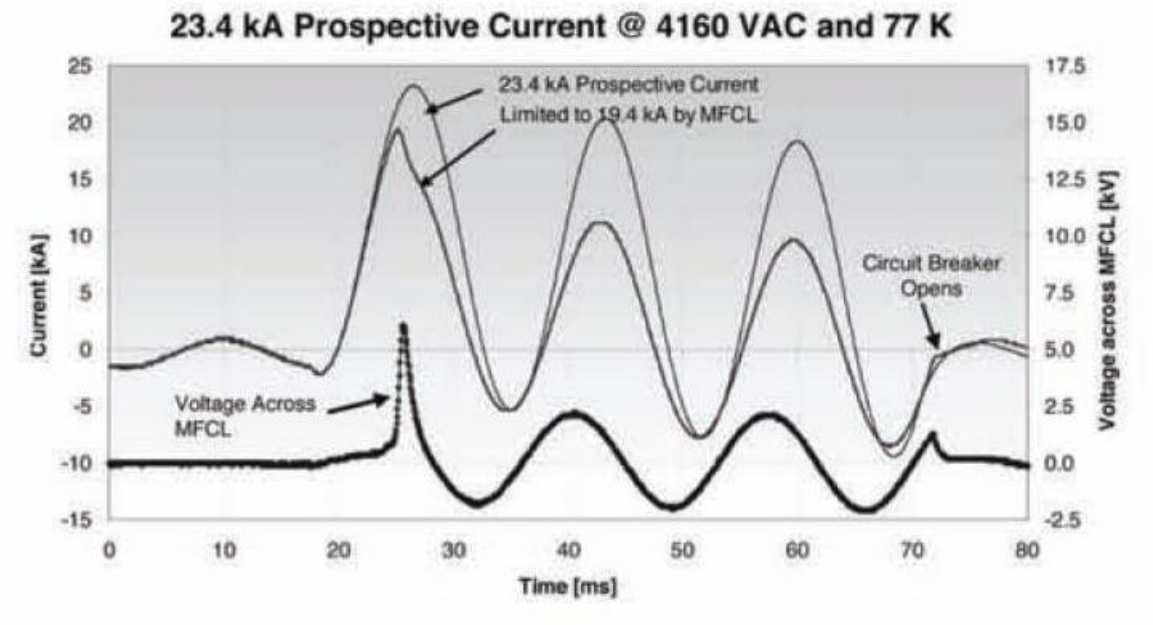


Figure 35: MFCL achieves first peak limiting at 4160 Vrms.

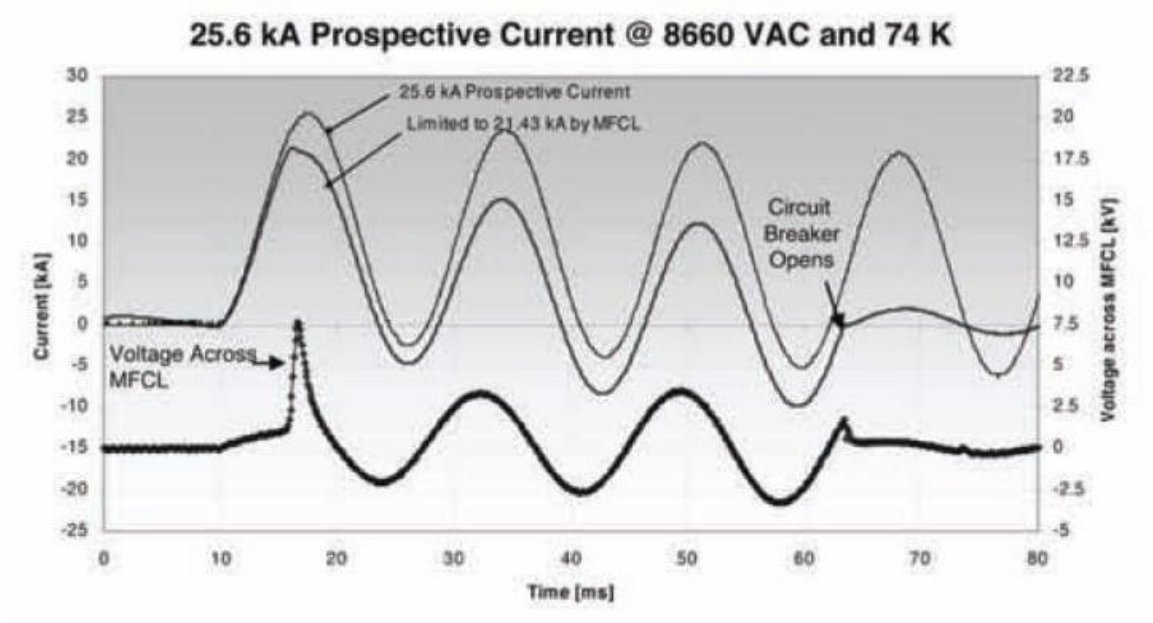


Figure 36: MFCL achieves 84% first peak limiting at 8660 Vrms.

Table 5: Summary of current limiting performance during the MFCL testing

Input Voltage	First Peak Current (kA)	Avg. First Peak Limiting	Limiting at 3rd Cycle
2400	23.6	73.4%	44.4 %
2400	27.2	68.6%	39.2%
4160	23.4	82.6%	52.3%
8660	25.6	83.7%	55.9%

4.2 SFCL Matrix Module Design, Assembly and Test

After the move away from BSCCO2212 MCP elements to 2G HTS based elements beginning in Phase 2, new SFCL design concepts were developed. One major difference was the elimination of the magnetic triggering. This was driven by the fact that the YBCO based 2G HTS tapes were much less sensitive to magnetic quenching than the BSCCO2212 MCP elements. Also, the uniformity of the 2G HTS tapes was superior to the BSCCO2212 MCP elements and being of much lower thermal mass would thermally quench more uniformly. In phas s 2 and 3,, physical samples of matrix modules were designed, fabricated and assembled and then tested. As data was gleaned form each test sequence, it was fed back into the designs and improved versions developed. The first baseline design that evolved, shown in Figure 37, consisted of 12 straight elements of 4 parallel 2G HTS tapes. These elements were connected at the ends through copper contacts. Shunt coils were attached between each pair of adjacent elements. Test data on this structure was shown in Figure 1b.

The next design stage looked at reducing the number of intermediate connectors and replacing them with support pullies. The resultant meander path design (Figure 38) was modeled and several prototypes with intermediate improvements built and tested. The improvements implemented in subsequent designs included improved shunt coils, improved terminations, improved mechanical support around the pullies and improvements in the voltage design (Figure 39). Later designs extended the length of the module and focused on the cooling aspects of the system (Figure 40). The final matrix module design evolved into an enclosed structure that had the advantage of voltage isolation and enhanced LN2 cooling (Figure 41).

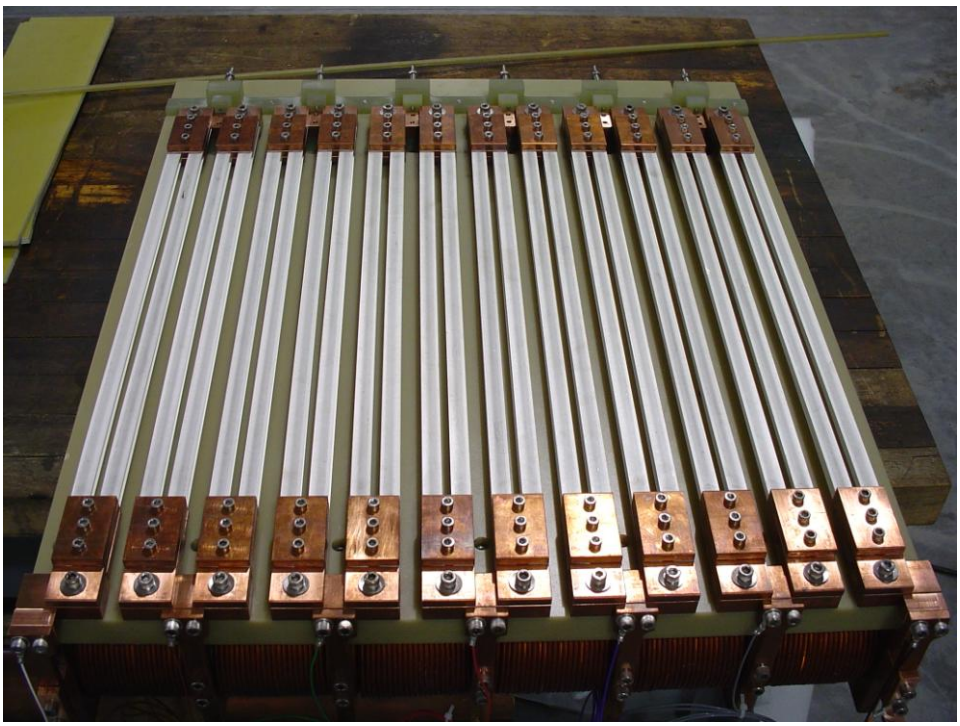


Figure 37: Baseline SFCL matrix module consisting of 12 lengths of 4 parallel 2G HTS tapes with end block connectors. Six shunt coils can be seen at the bottom of the photo under the structure.

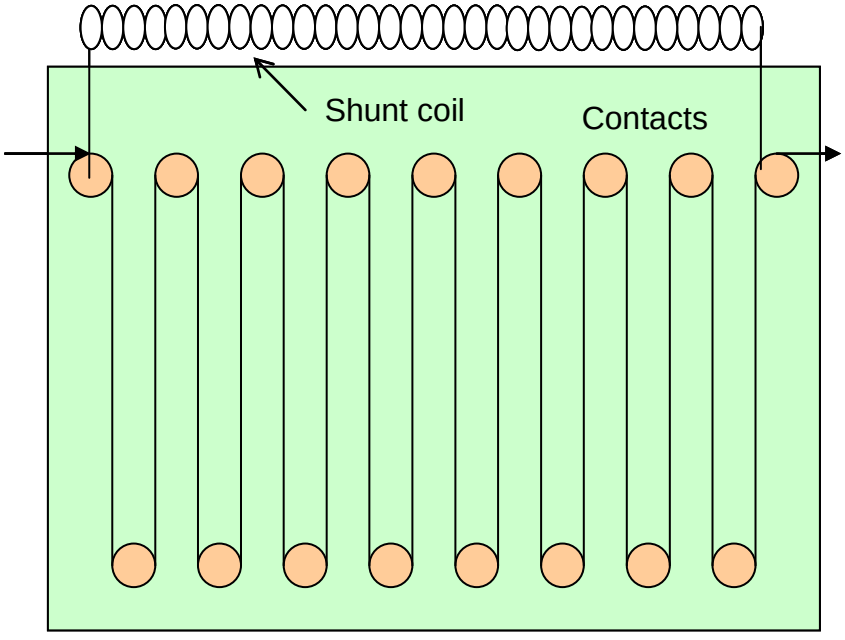


Figure 38: Schematic of meander path concept, significantly reducing the number of contacts.

Figure 39: Intermediate meander path module construction with voltage rings (top and bottom). Shunt coils are present between the meander path and voltage rings.

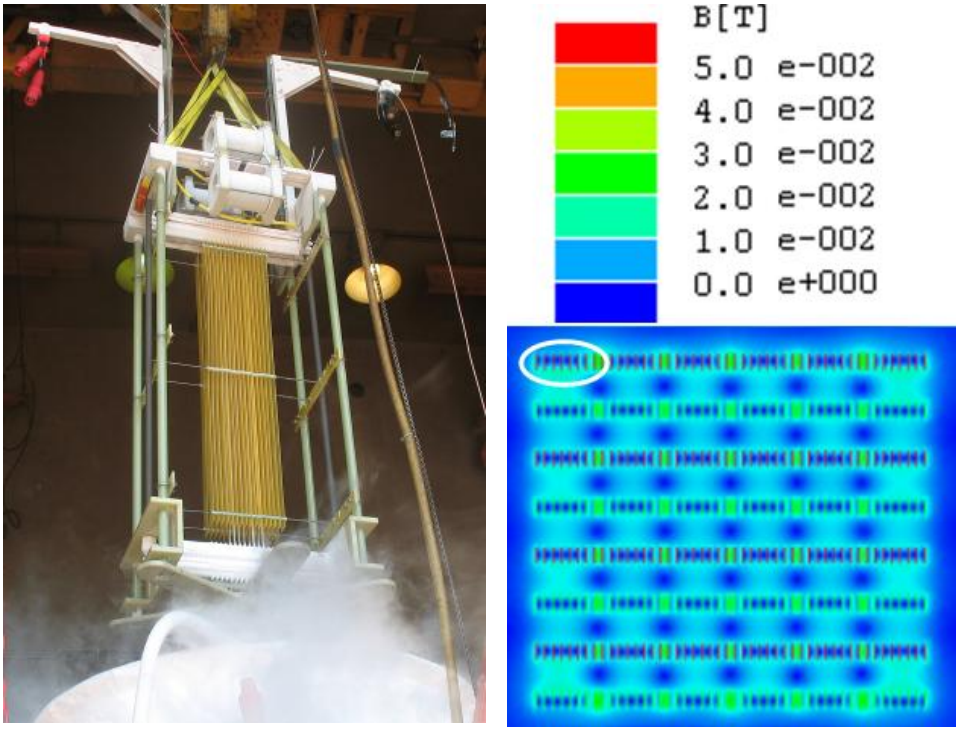


Figure 40: (left) Long length open structure SFCL module after removal from LN2 bath during test at KEMA Powertest in Chalfont, PA. 2G HTS tapes are in a meander path located between the vertical fiberglass epoxy strips. Shunt coils are located at the top of the structure (right) magnetic field plot of the SFCL matrix assembly.

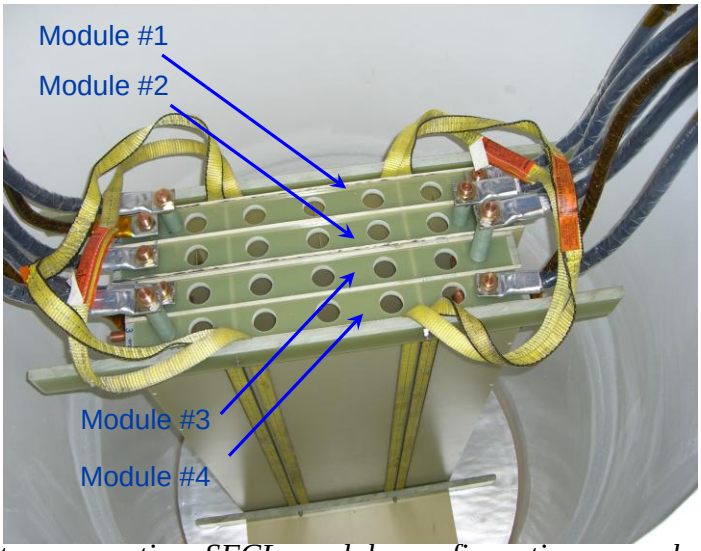


Figure 41: Later generation SFCL module configuration – enclosed meander path elements with voltage isolation between modules and directed coolant flow. Module sets are ~ 1 meter long and are shown within a LN2 test cryostat prior to LN2 being added.

Module tests were conducted at either KEMA Powertest in Chalfont PA. or at the Center for Advanced Power Systems (CAPS) at Florida State University in Tallahassee, FL. Each of these facilities was able to provide the controlled power and voltage to simulate the fault conditions that the SCFL modules would see in the field during operation. KEMA has higher power capability, but CAPS has more flexibility to rapidly simulate a wide range of operating conditions. CAPS uses a Power Hardware in the Loop (PHIL) system simulations to mimic inputs to the SFCL from the grid (Figure 42).

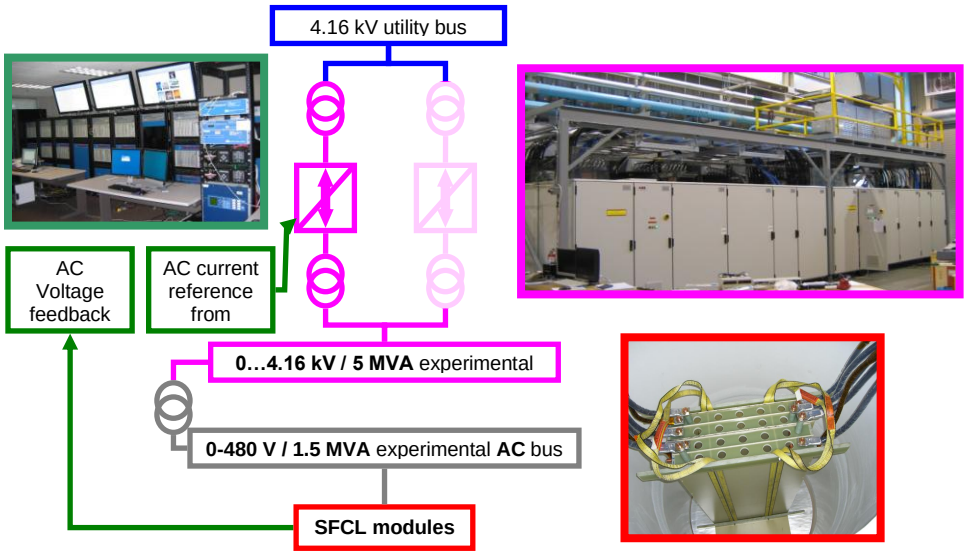


Figure 42: System setup at CAPS for the last set of module tests in 2009. The PHIL system allowed the testing of a wide range of operational parameters with minimal time and cost for setup changes.

The flexibility of the PHIL system permitted evaluation of multiple test environments without incurring costly and time consuming setup changes. In addition, PHIL allows one to easily replicate several system conditions that are often difficult to reproduce, i.e. reclosing.

Typical testing conditions at KEMA were driven by the AEP reclosure sequence as shown in Figures 43 and 44. Test results taken at KEMA on the module shown in Figure 37 are shown in Figures 45 and 46. These conditions include recovery under load which is a difficult proposition depending on the source and magnitudes of the different faults. For some conditions, the HTS elements are unable to recover – the remaining load in the line is too high and generates too much heat in the system that the superconducting elements are unable to be sufficiently cooled for full recovery. Much modeling and testing was conducted to find the limits of the design space in which RUL was possible. A schematic indicating some of the design constraints with respect to RUL is shown in Figure 47. Figure 48 shows the results of modeling under different operating conditions resulting in successful RUL.

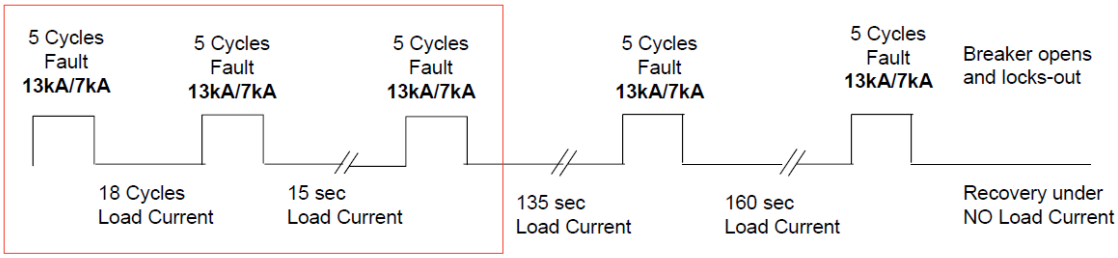


Figure 43: Typical AEP reclosure sequence that was utilized in a typical test at KEMA.

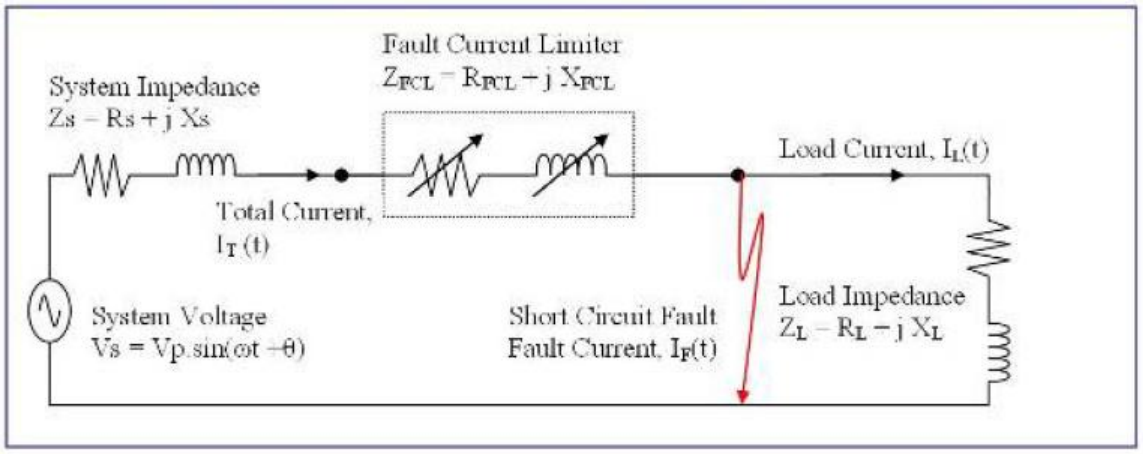


Figure 44: Test schematic of KEMA test system.

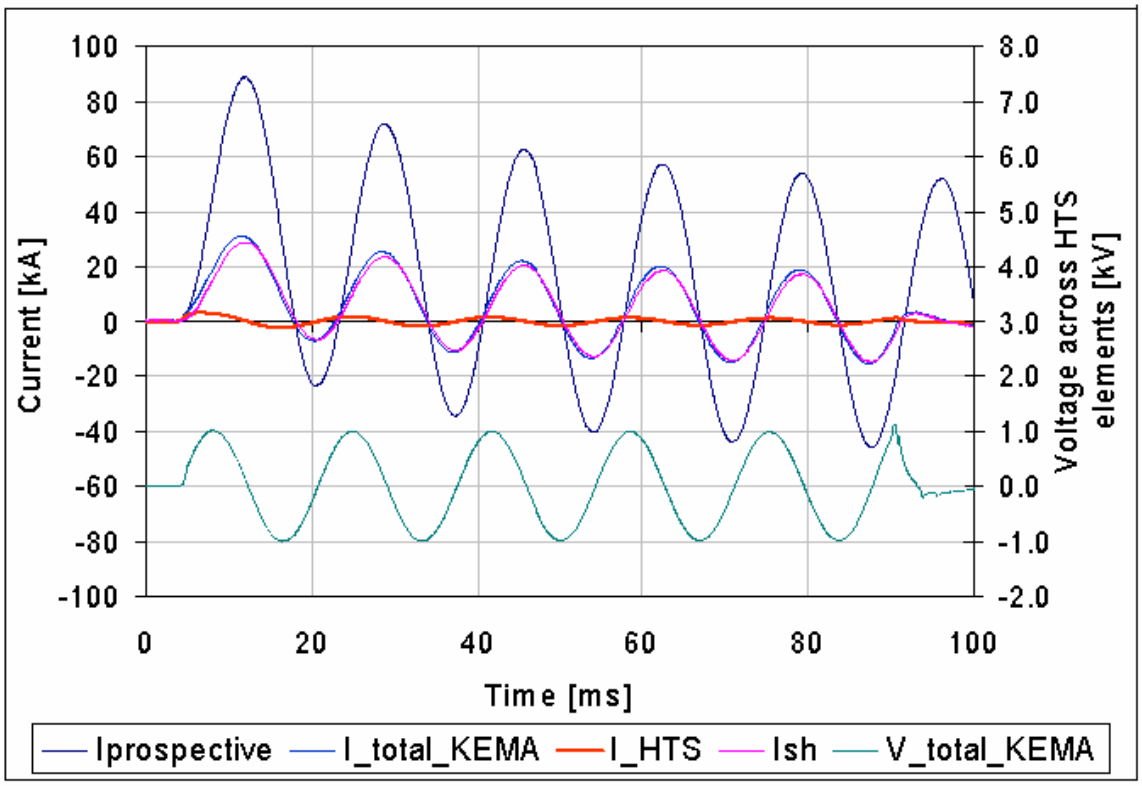


Figure 45: Test result at 1080 V supplied voltage with prospective asymmetric fault current of 33.75 kArms (90 kApeak). Iprospective is the prospective fault current, I_total KEMA, I_HTS and I_shunt are the currents flowing through the full assembly, the 2G HTS elements and the shunt coils, respectively. V_total is the voltage across all the 2G HTS elements connected in series.

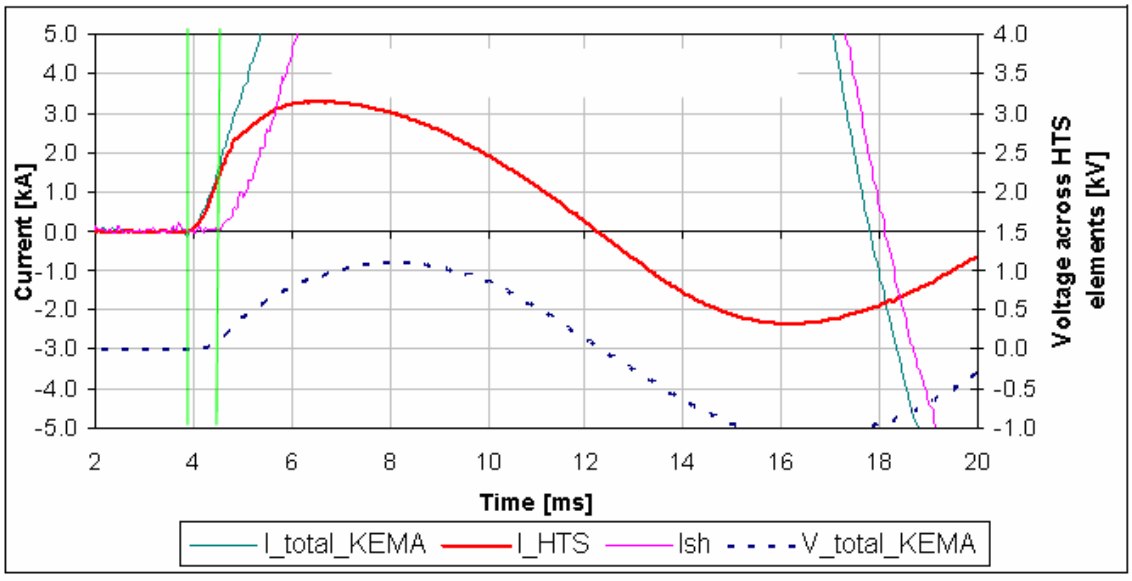


Figure 46: Closeup of the first peak transition showing the initiation of quench of the HTS elements and beginning of current flow within the parallel shunts within < 1msec.

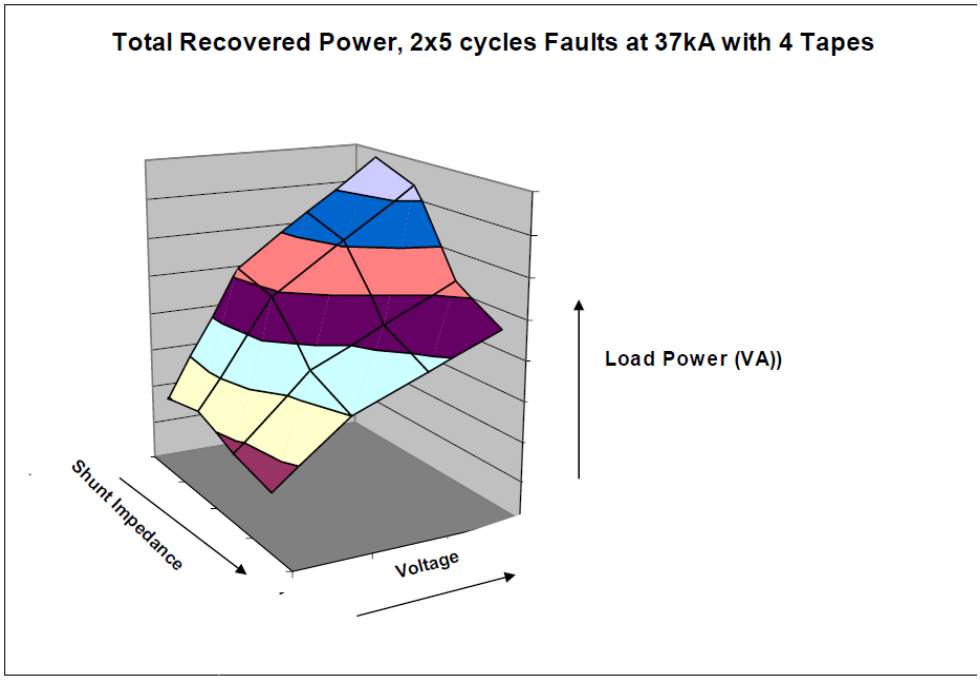


Figure 47: Design constraints driving the ability to recover under load (RUL) in a SFCL system

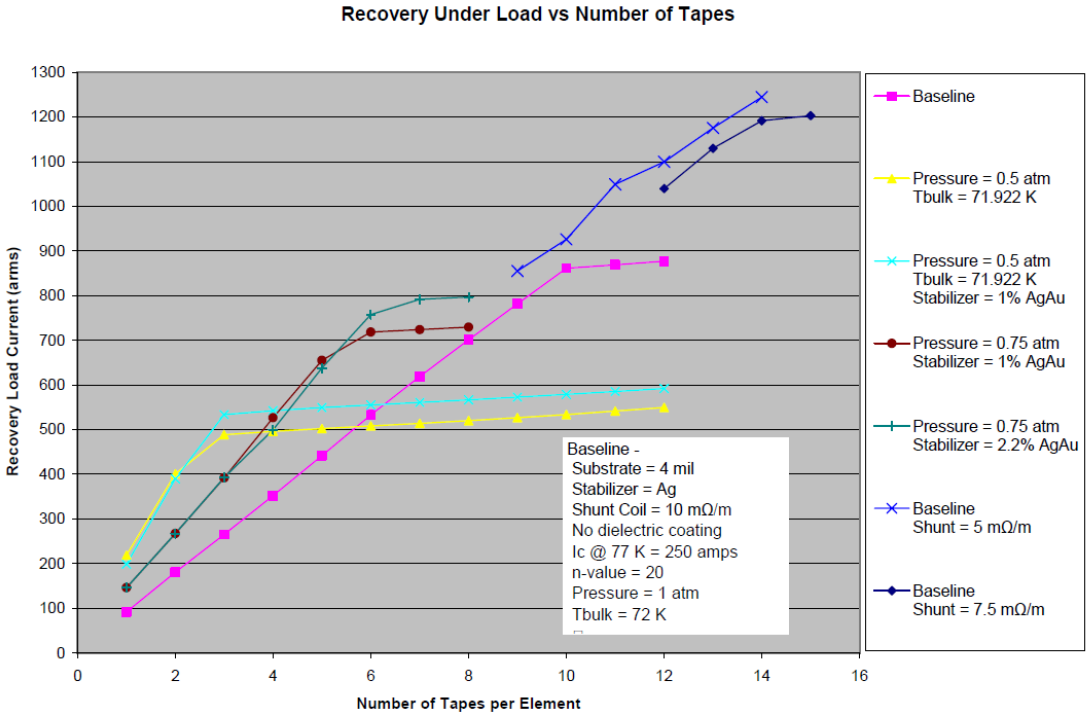


Figure 48: Model design space for RUL

5.0 High Voltage Modeling, Experimentation and Hardware Development

During the project, modeling, experimentation and hardware development to handle the high voltage environment in the cryogenic environment was extensively conducted with our partners Oak Ridge National Laboratory (ORNL) and Sumitomo Electric. While high voltage in the electric utililty industry is well understood and design protocols are in place, the addition of the cryogenic environment is a new regime. In particular, in the fault current limiter application with the HTS elements immersed in liquid nitrogen, you are faced with the issues of solid / liquid / gaseous interactions, particularly during a fault transient. Much analysis and experimentation was conducted, particularly at ORNL to understand the limitations of operating high voltage equipment in this new environment. Particular attention was paid to the impact of bubble formation during a fault transient on the dielectric strength of the LN2 bath. Even under the best of circumstances, it is not possible to suppress bubble formation during a fault transient…there is simply too much energy being deposited into the HTS elements that are in contact with the LN2 coolant. Bubbles will form...but you can mitigate their effects and collapse the bubbles under certain conditions. Different test configurations were used to look at the effects of bubble formation and distribution on the breakdown strength across a gap filled with LN2 consistent to what would be seen in an SFCL matrix structure. A schematic of this work is shown in Figure 49. It is known that the electric field inside of a gas bubble is enhanced over the surrounding bulk liquid due to differences in the dielectric constant between the two phases. This enhancement facto "f" can be as high as 11% for a spherical bubble (as depicted in Figure 50) and is independent of bubble size. It has also been shownthat there is a spatial variation of the electric field in the vertical ("z") direction as depicted in Figure 51. The collective data comparing breakdown strength in LN2 with and without bubbles is shown in Figure 52 and includes the Cumulative Probability of Failure for the two cases.

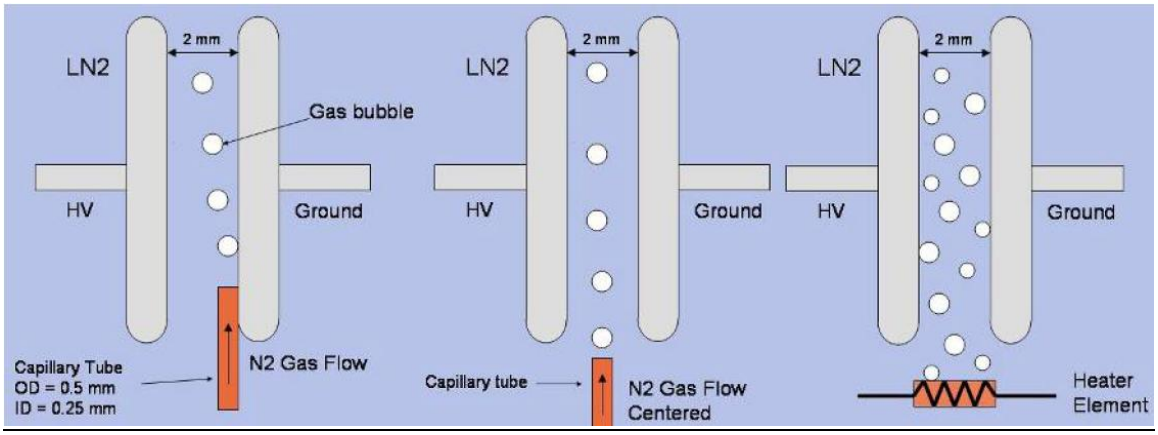


Figure 49: Some of the configurations evaluated across a 2 mm gap filled with LN2 subjected to different bubble placement and sources.

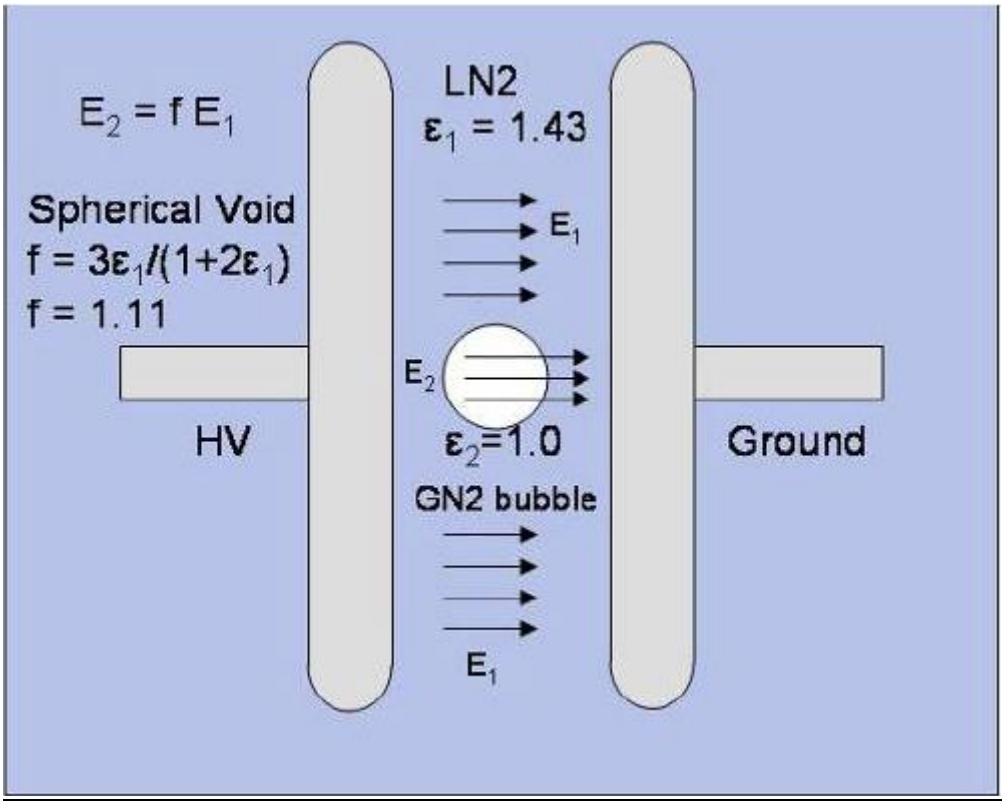


Figure 50: Model depicting field enhancement in a spherical bubble within a fixed gap.

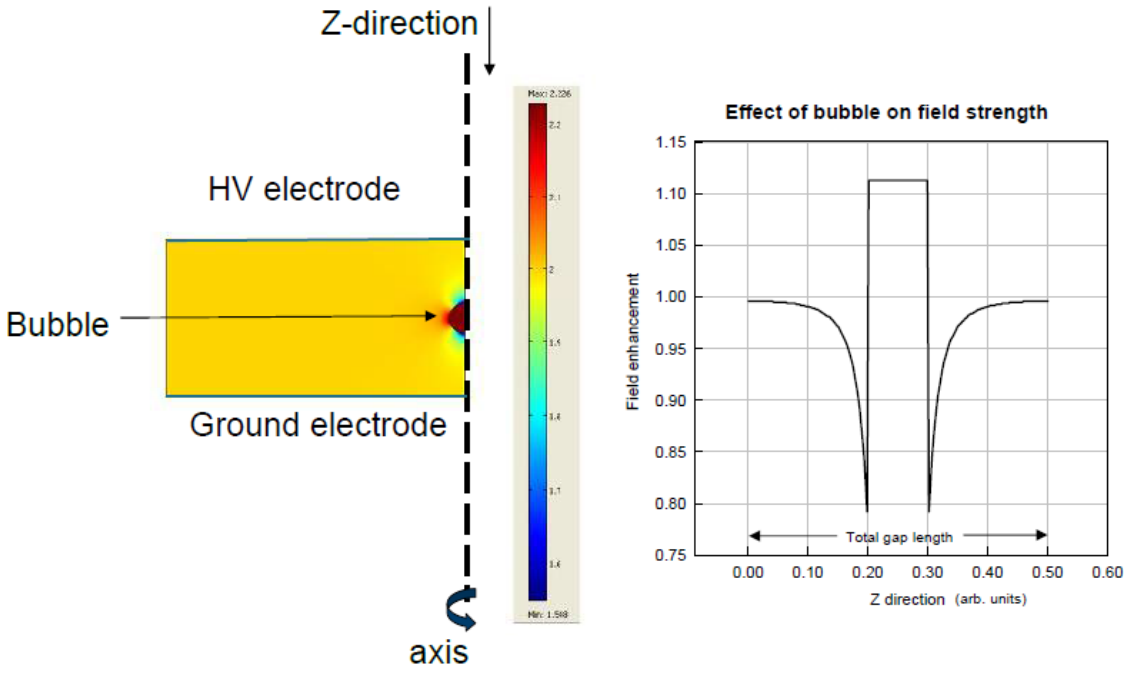


Figure 51: Spatial variation of the electric field in the vertical "z" direction.

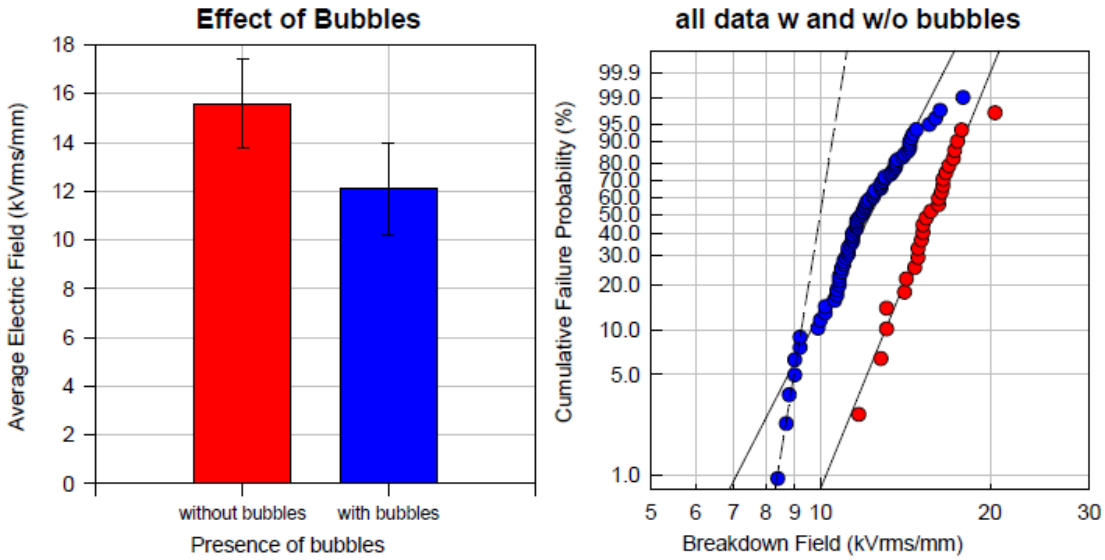


Figure 52: Impact of the presence of bubbles in LN@ on breakdown strength and probability of failure.

Additional data was taken to understand the impact of gap length. It was shown (Figure 53) that while the peak voltage during impulse was relatively constant at ~ 40-45 kV/mm, the breakdown voltage dropped with gap length. These results had a strong impact on the resultant HV design of the SFCL units and the need to precisely understand the voltage distribution within a unit and gap distances.

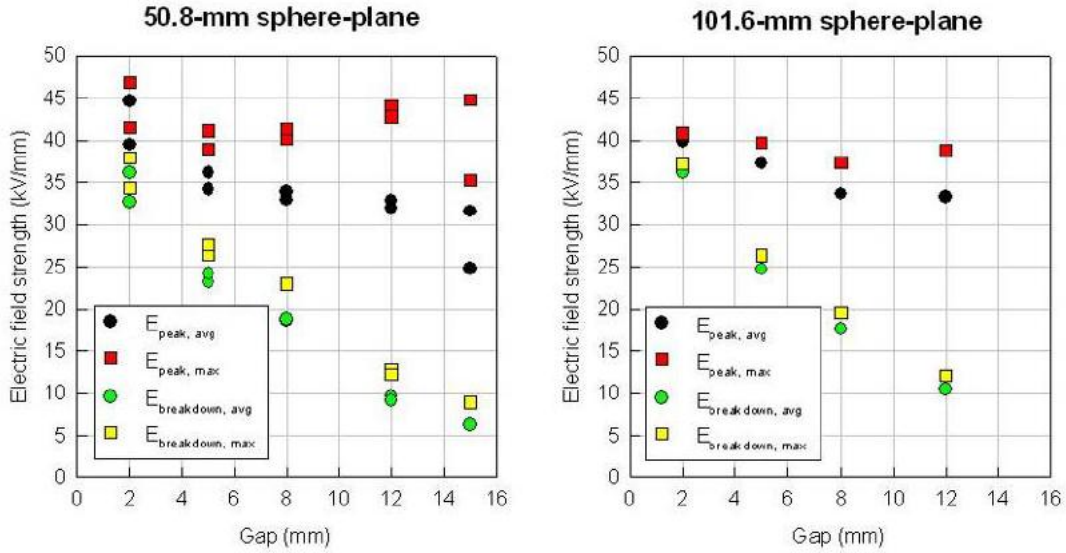


Figure 53: Impact of gap distance on peak voltage and breakdown voltage.

6.0 2G HTS SFCL Module Prototype Conceptual Design

In this effort, we conducted preliminary conceptual designs for a i) single phase Alpha device; ii) a three phase Beta device; and iii) a three phase pre-commercial SFCL device. The operational windows for these devices were based on specifications developed earlier in the program (see Section 1.0) and knowledge gained during the performance of the project.

The single phase Alpha device conceptual design (Figure 54) was based on the following design specifications and design parameters:

- 138 kV Class (80 kV Phase)
- 1200 A rms load current
- 14 kA rms sym. (37 kA peak) fault current limited by 50%
- 1 meter long elements, 12 tapes per element (300 elements total)
- 25 J/cm/tape energy capability
- Test condition, 3 atm (abs) LN2, subcooled to 70K
- Full recovery to superconducting state within 15 sec.
- AEP reclosure sequence
- RUL – 100 Arms RUL load current per tape
- Connector loss of ~ 150 to 300 W

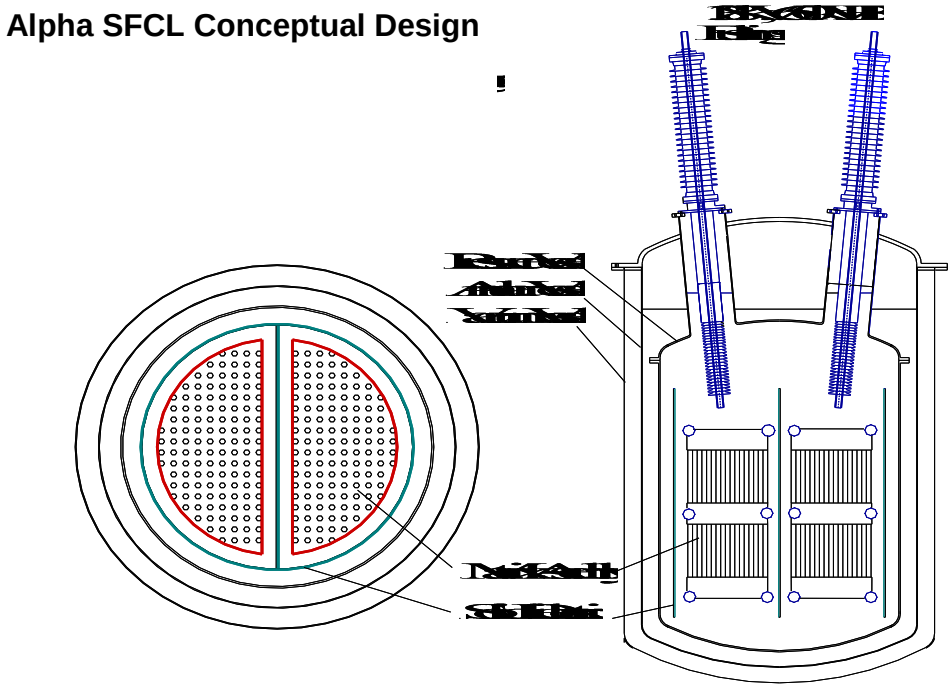


Figure 54: Initial Alpha SFCL conceptual design showing major components: 2G HTS matrix assembly, HV bushings, vacuum vessel and cryogenic containment, dielectric components.

The conceptual design phase for the Alpha device included the development of 3D CAD models for the major components to ensure sufficient spacing and fitup. Examples of these modeling efforts are shown below in Figures 55 and 56.

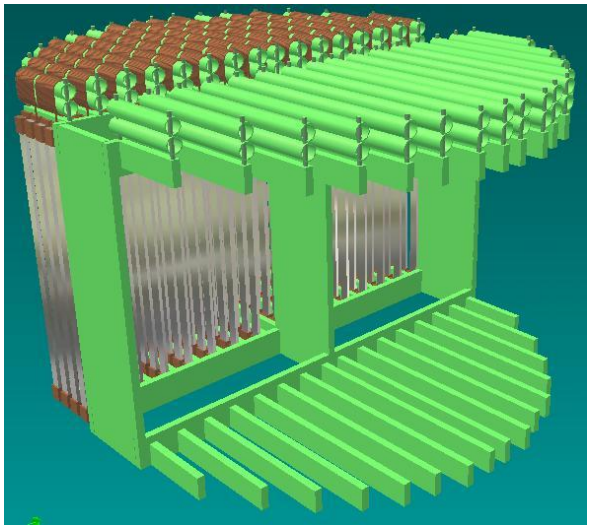


Figure 55 3D CAD model (Inventor) of the Alpha conceptual design Module Support Structure with simple common component features that can be easily expanded. The open structure permits LN2 cooling of the meander path 2G HTS tape elements (seen in rear).

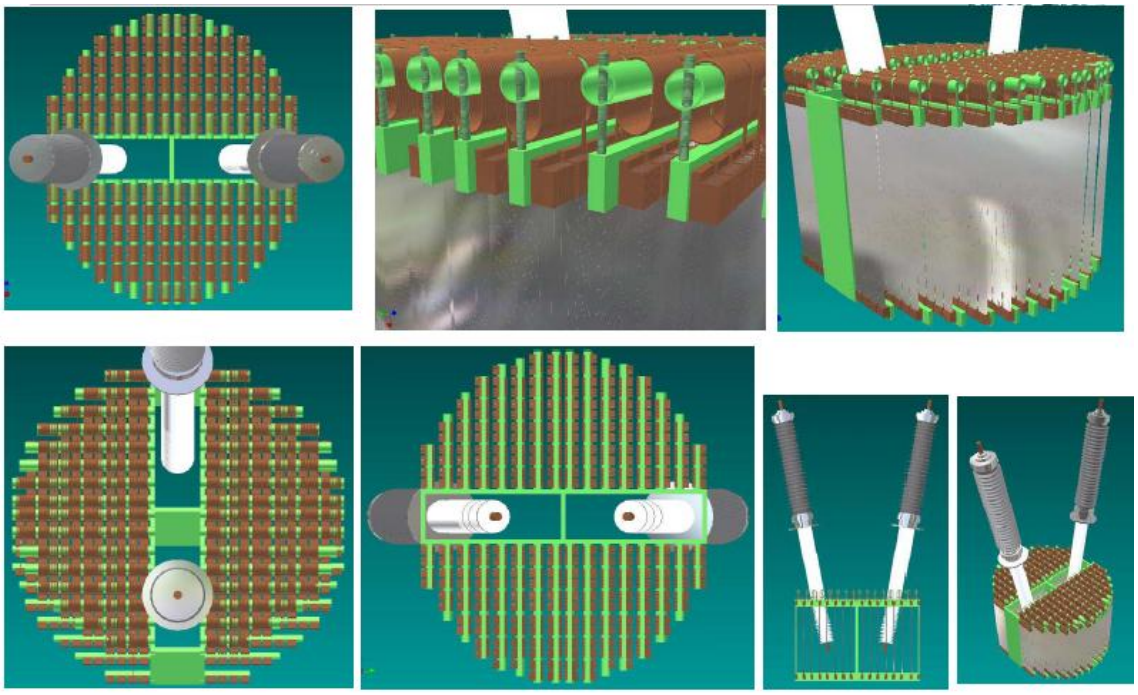


Figure 56: Montage of Alpha device components, including HV bushing placement.

The three phase Beta device is viewed as either simply three independent Alpha devices appropriately interconnected or a system with three Alpha device 2G HTS module structures with shared cryogenics. Shared cryogenics has some advantages from the standpoint of a potentially more efficient cryogenic and vacuum system. A drawback of using shared cryogenics is the potential for more complex dielectric interactions between the three phases all contained within the same structure with a shared cryogenic liquid (breakdown / flashover path?) between the phases. Which is the best approach to adopt is still undetermined. The decision on which design approach to take will require construction and testing of the Alpha device in order to validate certain dielectric design rules.

A three phase pre-commercial device would take the results of the Alpha device and Beta device testing and address any performance shortfalls in the revised design. In addition, cost reduction strategies would be implemented to bring the price of the units into a more favorable commercial position.

Summary / Conclusion.

The use of 2G HTS in a superconducting fault current limiter module has been validated and techniques to improve the performance of the 2G HTS tape have been explored. Several of the methodologies developed to improve the performance and recovery of the tape can be readily implemented as needed in the production of the 2G HTS tape. Other methodologies are more difficult to implement into production and a benefits analysis will need to be conducted to understand the impact of the improvement on the commercial viability of the process versus the improved performance that can be achieved.

SFCL modules have evolved through the time covered by this program into compact standalone modules with discrete current and voltage capabilities. Current modules (i.e. as shown in Figure 34) have a current capability of 1-2 kA and a voltage capability of ~3200 V. These modules can be stacked to reach the performance levels required for the full system.

System level conceptual designs have been developed and will continue to be improved as performance data for various components continues to be collected. Preliminary acceptance criteria for the SFCL system has been developed with various utility groups and forms a basis for developing a more formal specification for future commercial SFCL devices.