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A First-Principles Approach to

Total-Dose Hardness Assurance

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A First-Principles Approach to Total-Dose Hardness Assurance

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1. INTRODUCTION

When I first began doing radiation tests in 1984, the subthreshold (midgap) test method of Winokur and McWhorter [1,2] had just been developed, and I wasn't sure exactly what sort of response to expect from the MOS transistors I was trying to test. Still, I was fairly sure that the drastic changes in threshold-voltage shifts due to interface- and oxide-trap trap charge (ΔV_{it} and

ΔV_{ot}) that occur in Fig. 1 between the first and second (30 and 60 krad(SiO$_2$)) radiation levels was not the radiation-induced charge trapping that I was trying to measure. What went wrong? One can see from the current-voltage (I-V) traces of Fig. 2 that the gate oxides were not destroyed. However, from the large "stretchout" (likely due to interface traps) and shifts (likely due to oxide traps) in the curves [1,2], it was clear that a lot more damage had been done to the device between the end of the first exposure and the end of the second exposure than during any of the other irradiation intervals.

Figure 1: Inferred threshold voltage shifts due to interface- and oxide-trap charge for nMOS transistors with 45-nm gate oxides irradiated with Co-60 gamma rays at a dose rate of ~ 400 rad(SiO$_2$)/s at +10 V bias.

Figure 2: I-V curves for the devices and exposures of Fig. 1.

Figures 1 and 2 turned out to be a simple and dramatic illustration of the point that, if one follows a poorly thought-out test plan, one often gets a meaningless result. I was originally shown "how" to do total-dose exposures by someone who did not realize a basic point about device testing. That is, if one simply clicks a switch to turn on some types of non-current-limiting power supplies while MOS gates and drains sit unprotected, one can get transient spikes that can damage the device for reasons (high-field or high-current stress induced damage) that have nothing to do with the device's fundamental radiation response. I quickly learned not to do this! The example of Fig. 1 is extreme, but it serves to illustrate the important point that blindly following a test plan is not enough. *One must have an idea of the likely impact of test conditions on the test results, and on how the test results relate to device response in the use environment.* This will be a recurring theme of our discussion below.

2. DESIGN MARGIN AND SAFETY FACTORS

The groundwork for a cost-effective hardness assurance program is laid at the system design level. If radiation hardness constraints are not adequately considered at this point, hardness assurance testing can be difficult or impossible. If a 3-krad(SiO$_2$)-hard commercial device is selected as the cornerstone of a 200-krad(SiO$_2$) system, without hefty shielding, no amount of cleverness (or expense) in hardness assurance will salvage a poor design. On the other hand, if parts are selected on the basis of characterization tests that have demonstrated the part can survive radiation levels well in excess of system requirements, hardness assurance testing difficulty, time, and expense can be kept to a minimum. For discussions of conservative design practices and safety factors in the design/hardness-assurance cycle, the reader is referred to the short course segment and related articles by Pease and co-workers [3-5], the recent review by Holmes-Seidle [6], as well as military handbooks [7,8] and other publications [9-14]. Because these issues have been discussed so thoroughly in Refs. [3-14], we will not repeat the discussions here, but we cannot overemphasize their importance to a successful hardness assurance program.

As just one practical example of how design margin can be used to reduce hardness assurance costs and difficulty, the Qualified Manufacturers List (QML) test methodology permits reduced

sampling in lot acceptance tests for components certified to meet radiation levels 2-10 times more severe than system requirements. Further, routine lot acceptance tests may be waived if the parts are certified to levels more than 10-times greater than the intended application [5,15-19]. Thus, judicious use of design margin and safety factors can reduce lot acceptance costs without significantly increasing system risk.

3. FOCUS

Keeping in mind the importance of design margin and safety factors, our remaining discussion will focus on how to perform cost-effective, conservative total-dose tests in several common applications. These test methods are based on a first-principles approach to estimating (or bounding) device response in the use environment, and can be used in support of the device characterization phase of system design as well as in the ultimate lot acceptance testing. So, for example, if one wishes to establish a well-defined safety factor for a particular use environment, one should base this factor on tests performed with a similar use environment in mind. Else one may be unpleasantly surprised to find that parts thought to be hard enough for the intended application on the basis of testing under one set of conditions may actually fail in the environment of interest, as we will discuss in detail below.

The discussion will focus primarily on small-signal MOS device and circuit response, though bipolar response will also be discussed briefly. Special issues associated with power electronics [20,21] are not treated, though many of the test methods discussed here can also be applied to evaluate their response [22,23]. We will also not discuss total-dose testing issues for GaAs or other III-V semiconductor technologies, because (lacking gate insulators) they usually are not nearly as sensitive to ionizing radiation effects as MOS or bipolar devices. The reader is referred to treatments of the displacement effects due to high-energy protons and electrons that impact their response in a space environment [24-30]. Further, special total-dose testing issues associated with CCD's [31-34], photonic components [35-40], specialized sensors (e. g., HgCdTe [41-43]), etc. will not be addressed here, though they can be critical to system survivability. Both ionization and displacement effects can be important to the response of many optoelectronic components in a space environment [31-44].

The primary environment considered below is the near-earth space environment, which has been described in detail in previous short courses and recent reviews [45-51], and which will not be described here. Of course, conclusions reached for a low-dose-rate space environment also apply to equivalent low-dose-rate environments, such as electronics in high-energy particle accelerators or nuclear reactors. We will also briefly discuss testing issues associated with generic tactical and high-dose-rate weapon environments. Finally, we will concentrate on the response of electronics at ordinary ambient temperature (~ 25°C). The special challenges associated with cryogenic or high temperature operation [52-56] will not be addressed.

4. SOURCES AND ENVIRONMENTS

Sources employed in typical total-dose radiation effects studies are grouped schematically by dose rate in Fig. 3. For high-dose-rate exposures, which are representative of a generic high-dose-rate weapon environment, a good choice is a linear accelerator (LINAC), though LINAC's are more commonly used for dose-rate-induced photocurrent testing. For the experiments described in detail below, the White Sands Missile Range (WSMR) LINAC was used. The beam consisted of 20-MeV electrons, and was tuned to provide ~ 8 μs pulses at a dose rate of ~ 6 x 10^9 rad(SiO_2)/s. Thus, the dose per pulse was ~ 48 krad(SiO_2). For higher total-dose irradiations, multiple pulses were generated at a rate of 10 Hz. For the parts considered here, these conditions allowed repeatable operation of the LINAC, reliable dosimetry, and avoidance of space charge effects--all important considerations when using a LINAC for high-rate total-dose testing [45,57-59].

Figure 3: Sources suitable for simulating high-dose-rate weapon and low-dose-rate space environments, as well as laboratory (intermediate dose rate) sources more appropriate for simulating some types of tactical military applications and for hardness assurance testing.

Typical laboratory sources were also used. An AECL Gammacell 220, with a dose rate of ~ 278 rad(SiO_2)/s, and an ARACOR Model 4100 Semiconductor X-ray Irradiator [60], with dose rates from ~ 50 to ~ 5000 rad(SiO_2)/s, were chosen as common laboratory sources that are often used in lot acceptance and/or QML-based hardness assurance programs [16,17,59,61,62]. These sources are also excellent simulations of many types of "tactical" military environments.

Finally, to approach a "space-like" environment, devices were also exposed in a Shepherd Cs-137 gamma source at dose rates ranging from 0.002 to 0.2 rad(SiO_2)/s. Dosimetry can be a challenge in many of the sources, and (while important) is beyond the scope of this course. The reader is referred to Refs. [59,63,64] for discussions of appropriate dosimetry practices in these different radiation sources. With some care, however, one can achieve inter-source calibrations accurate to better than ± 10-15% [59], which is just outside typical part-to-part variations in radiation response for MOS threshold voltages on a well controlled line [61].

To make contact with possible use environments, one must know not only the relative dose rates of the irradiation sources and the environments of interest, but also the typical irradiation type and energies. In a weapon environment, one can have a wide range of x-ray and gamma-ray energies, which can make simulation fidelity a very difficult challenge. These issues are beyond the scope of the present short course, and indeed are typically not addressed in the open literature [65]. In a typical satellite environment, the dose is deposited by energetic protons and electrons, whose relative densities and energies will depend on many factors. The most notable of these are the orbit of the satellite and the status of the solar cycle (i. e., whether there have been recent flares) [45-51]. Because satellite electronics are typically shielded at least modestly [49], it is generally presumed that the lowest energy electrons and protons do not reach the electronics, and that Co-60 irradiations provide a reasonable simulation of the ionization effects in a space environment. (Note that Co-60 irradiation does not provide a good simulation of displacement damage effects, without correcting at minimum for differences in nonionizing energy loss in the particle versus photon environments [24,29].) However, some adjustments may be required to com-

pensate for the potentially large differences in Co-60 and proton charge yield [45,66]. For the purposes of this course, we assume that corrections for the effects of shielding and proton charge yield have been applied to arrive at the total ionizing dose and dose rate specifications for a given system. The remaining issue to confront is that of the widely different dose rates of the laboratory irradiation source and the use environment. Finally, we should mention that, with corrections for dose enhancement and/or charge yield [17,59,61,67], 10-keV x-ray irradiations can also be useful in a hardness assurance program, as we discuss later.

5. MOS TESTING ISSUES

Because of their low power requirements, and increasing dominance in the digital IC world, MOS electronics are very important components of virtually all military and space systems. For that reason, and because of their sometimes complex and somewhat bewildering response, we will give an especially thorough treatment of MOS total-dose testing issues. And, because of the attention being given to the space environment at present, most of the discussions will center around total-dose qualification of parts for space and other low-dose-rate environments. In particular, a detailed discussion of the technical basis for US MIL-STD 883D, Test Method 1019.4 [68] will be provided.

5.1 Defects in MOS

MOS total-dose response is governed almost exclusively by ionization effects in critical insulating layers in the devices, and by defect buildup at or near the critical interface between the Si channel layer and the SiO_2 gate oxide [45,57,69]. A schematic illustration of the most important defects in modern MOS gate oxides [70] is shown in Fig. 4. Defect location is shown in Fig. 4(a), and their impact on electrical response is indicated in Fig. 4(b). Historically [69], defects in the MOS system have been grouped into "oxide traps" and "interface traps." Oxide-trap charge shifts the threshold voltage of MOS transistors. For thermal oxides in a radiation environment, the dominant oxide-trap charge is positive and due primarily to radiation-induced trapped holes [45,57,69]. These shift the threshold voltage of a MOS transistor negatively. Interface traps will shift the threshold voltage of an n-channel MOS transistor positively, and that of a p-channel transistor negatively [45,57,69]. Interface traps also lead to mobility degradation [71,72]. Recently, it has become increasingly clear that is can be difficult with standard characterization techniques to distinguish between the effects of interface traps and near-interfacial oxide traps (i. e., "border traps") on MOS transistor I-V characteristics [70,73-85], like those of Fig. 2. Although this can be an important distinction in studies of the physics of MOS charge trapping, it is not critical to the discussions of MOS hardness assurance here. Moreover, for the hardened transistors for which most of the charge separation measurements have been performed in this study, interface-trap effects usually are more important than border-trap effects [79,82]. So, for the remainder of this course we will adopt the historical convention of assuming that most of the defects that do not exchange charge with the Si during the measurements ("fixed states" in Fig. 4(b)) are oxide traps, and most of the defects that exchange charge with the Si ("switching states" in Fig. 4(b)) are interface traps.

Figure 4: Physical location (a) and electrical response (b) associated with defects in MOS gate oxides. (After Ref. [70].)

Properties of interface traps and oxide traps and methods to estimate their densities in irradiated MOS devices have been reviewed in detail many times [45,57,69], and the nature of border traps is an emerging topic of great interest [70,73-85]. However, here we will concentrate on the significance of these defects in radiation hardness assurance testing, and will not discuss the basic mechanisms that underlie this response in significant detail. For a review of the basic mechanisms of radiation response and hardening techniques, the reader is especially urged to read last year's short course segment by Jim Schwank [45], as well as many other reviews in the literature [57,69]. Of course, it is not only important to understand the radiation response of MOS gate oxides, but (as discussed later) the response of parasitic isolation oxides (e. g., field oxides) can also be quite important to MOS radiation response [45,57,69].

5.2 Dose-Rate Effects

The principal difficulty associated with defining a simple total-dose test method for MOS electronics is illustrated clearly in Fig. 5, which shows threshold voltage shifts for an early version of a radiation-hardened CMOS process developed at Sandia National Laboratories [86]. Irradiations at dose rates typical of conventional laboratory sources (20-200 rad(SiO_2)/s) showed relatively large negative threshold voltage shifts at a dose of about 1 Mrad(SiO_2). A negative threshold voltage shift in an nMOS transistor can cause failures due to excess leakage current in MOS IC's. Unfortunately, testing at lower dose rates, closer to space environments, showed large positive threshold voltage shifts at even lower doses! Positive threshold voltage shifts (often called "rebound" or "super-recovery," in which the value of the threshold voltage not only "turns around" with increasing total dose but also exceeds its preirradiation value [87,88]), can lead to circuit and system failures due to reductions in noise margin, speed, and timing problems [86,89]. So, testing MOS devices at rates of 20-200 rad(SiO_2)/s gave *both the wrong failure dose and the wrong failure mode for a space application.* Conversely, if one were using low-rate irradiation to attempt to qualify a MOS device for use in a higher-rate application (e. g., some high-dose-rate weapon applications [58,59]), again the wrong failure doses and failure mechanism would be observed. The origin of the response in Fig. 5 is the combination of the annealing of oxide charge with increasing time or decreasing dose rate, and the continued increase in interface traps with time, as we will discuss in detail below.

Figure 5: Threshold voltage shifts versus dose and dose rate for Co-60 (2 - 200 rad(SiO_2)/s) and Cs-137 (0.1 rad(SiO_2)/s) irradiations of MOS transistors with 45-nm oxides from Sandia's old baseline technology. The "failure levels" indicated on the figure at ± 1 V are for illustration purposes only. Real failure doses in MOS IC's may be at higher or lower levels. (After Ref. [86]).

A similar type of effect is illustrated in a different way in Fig. 6, based on experiments and modeling performed by Allan Johnston on a Z80A NMOS microprocessor [87]. Here the dose required to produce a given positive or negative threshold voltage shift (± 0.45 V) on an input transistor is plotted as a function of dose rate. Again, at higher rates, the failure is due to oxide-

trap charge which causes negative threshold voltage shifts. At intermediate rates, the level of oxide-trap charge has decreased somewhat and the amount of interface-trap charge increased, leading to a near cancellation of the two effects at ~ 1 $rad(SiO_2)/s$. How this cancellation may naturally occur in some types of process development, in which the criteria for process step selection is minimizing the net n-channel threshold voltage shift of nMOS transistors, has been discussed by Winokur et al. [90]. At lower rates, interface traps lead to rebound effects and device failure due to positive threshold voltage shifts at lower doses again. While the dramatic peak observed in Fig. 6 at intermediate dose rates may not exist for all MOS IC's, this kind of behavior certainly is a concern for establishing MOS total-dose test standards. By testing at a single dose rate, as was allowed in versions 1019.1 - 1019.3 of the US military total dose test standard [86,91], one could never be sure whether one could accurately assess the correct failure dose or failure mode for MOS devices and IC's with responses like those of Figs. 5 and 6. The examples we have provided here are for simple transistor parameters; similar effects for a wide range of IC parameters are observed in Refs. [58,88,89,92-101].

Figure 6: Dependence of nMOS circuit failure level for Z80A microprocessors on the dose rate of the irradiation. (After A. H. Johnston, Ref. [87]).

5.3 Technical Basis for MIL-STD 883D, Test Method 1019.4

The above discussion of Figs. 5 and 6 shows why a new test method was required for space applications of MOS devices and IC's. In this section and those that immediately follow, we illustrate the technical basis of the present US Military Standard 883D, Test Method 1019.4, which is the first standard test that checks specifically for rebound failures in space. Unless otherwise stated, discussions apply equally to bulk, epitaxial, or silicon-on-insulator (SOI) MOS devices. An exception is that some issues associated with parasitic field oxides in bulk or epitaxial MOS devices must be discussed in the context of sidewall and/or buried insulators on SOI materials [102].

5.3.1. Time Dependent Effects. To lay the groundwork for the new test method, a series of experiments was performed to determine the equivalence between higher-dose-rate exposures and subsequent annealing and low-dose-rate testing [59]. Figure 7 shows threshold voltage shifts as a function of postirradiation anneal time for nMOS transistors with 60-nm gate oxides. "Zero" on the time axis is taken to be the beginning of each of the respective irradiation periods. Data are shown for LINAC, x-ray, and Cs-137 irradiations to a total dose of 100 krad (SiO_2) at 6 V bias, followed by room-temperature anneal at the same bias. Dose rates range from 6 x 10^9 to 0.05 $rad(SiO_2)/s$. Trends in the data are qualitatively consistent with those illustrated by Figs. 5 and 6 above. That is, at high rates, the threshold shifts are fairly large and negative, dominated by oxide-trap charge. At lower rates, the shifts are positive, indicating an excess of interface traps. Threshold-voltage shifts following high-rate irradiation plus room-temperature anneal at the same bias are, to within the experimental uncertainty, equal to low-dose-rate exposures at equivalent times [59]. This common response is reinforced by Fig. 8, where I-V curves are overlain from 10-keV x-ray exposures followed by a 1-week anneal, and from a 1-week Cs-137 exposure to the same dose. Clearly, there is no difference in response.

Figure 7: Threshold voltage shifts for nMOS transistors with 60-nm gate oxides built in a variation of Sandia's old baseline technology versus postirradiation anneal time for varying dose rate exposures to a dose of 100 krad(SiO_2). The irradiation and anneal bias was 6 V. (After Ref. [59].)

Figure 8: I-V curves for the devices of Fig. 7 following a 7-day exposure to Cs-137 irradiation to 100 krad(SiO_2) at 0.165 rad(SiO_2)/s, and a 10-keV x-ray exposure to the same dose followed by room temperature anneal for 7 days. The irradiation and anneal bias was 6 V. (After Ref. [59].)

Figures 9 and 10 show the values of ΔV_{ot} and ΔV_{it}, respectively, inferred via the subthreshold technique of Winokur and McWhorter [1,2] for the data of Figs. 7 and 8. Values of ΔV_{ot} in Fig. 9 show an approximately linear-with-log-time decrease, and lie on a common "transient-annealing curve," which has been observed by many authors to govern the trapped-hole neutralization rate in MOS oxides [59,86,103-107]. (This behavior is apparently independent of whether the dominant oxide-trap charge neutralization mechanism is true annealing or compensation by electron capture at border traps [83,88,108], or whether the hole neutralization process is dominated by tunneling or thermally activated processes [109].) In contrast, the interface-trap buildup in Fig. 10 increases with increasing time, at least up until times greater than ~ 10^5 s for these devices. At long times and fixed total dose, the value of ΔV_{it} is approximately constant with increasing irradiation time or annealing time. The mechanisms responsible for this type of interface-trap buildup have been discussed extensively [45,57,69,85], and are beyond the scope of this course. No "latent" buildup, corresponding to a further increase in interface-trap density after an apparent saturation, is observed for these devices [110,111]. It is the different time-dependencies of oxide-trap charge neutralization (Fig. 9) and interface-trap buildup (Fig. 10), as well as their different effects on MOS threshold voltage, that lead to the changing magnitude and sign of the threshold voltage shift (Fig. 7). Despite these dependencies, it is reassuring that the response of MOS devices under these irradiation and anneal conditions fall on universal defect growth and annealing curves over an extremely wide range of dose rates [59]. Thus, fundamentally different processes are not occurring during irradiation at different dose rates; differences are just due to differences in time dependent oxide-trap charge neutralization and interface-trap buildup. It is important to note that the equivalence of high-rate irradiation and annealing to low-rate response occurs only when electric fields and temperature are constant throughout the irradiation and annealing sequences [59]. This does not present a practical problem for MOS devices under typical worst-case radiation response conditions, but causes difficulties in defining hardness assurance tests for bipolar devices [112], as we will discuss later.

Figure 9: ΔV_{ot} versus irradiation and anneal time for the devices and irradiation conditions of Fig. 7. (After Ref. [59].)

Figure 10: ΔV_{it} versus irradiation and anneal time for the devices and irradiation conditions of Fig. 7. (After Ref. [59].)

5.3.2. Constraints on Low-Dose-Rate Hardness Assurance. The results of Figs. 7-10 show that MOS device response in a low-dose-rate application (e. g., space or high-energy particle accelerator) should be no different than after a higher-rate irradiation and equivalent annealing period. While this is extremely useful information, very-low-dose-rate exposures and very-long-term anneals are often expensive and impractical for hardness assurance tests. To shorten the irradiation and/or annealing period, it must be recognized that *one cannot perform a cost-effective standard test that fully simulates the response of a MOS device at the end of its life in a space environment.* This is because, with higher-rate irradiations and/or anneals, one cannot simultaneously reproduce the amount of oxide- and interface-trap charge that will exist in an irradiated MOS oxide after years of exposure in space. Instead, one can only define a test sequence that will ensure that a device will perform within consistent, bounded limits during its lifetime [104,113,114].

There have been several approaches to attempt to explicitly address MOS hardness assurance for low-dose-rate applications. These have included part categorization methods [117,125], attempts to model and predict device long-term response [18,22,23,91,103,106,115,118-122,124], and methods to conservatively bound the response of MOS devices and IC's at low dose rates [17,58,59,88,93,100,104,113,114,116,123]. Some of these techniques require extensive characterization tests, test structure data, and/or test-structure-to-IC-correlations which are often not possible to obtain given system cost and part availability constraints. Therefore, the most common general approach used in the past, and that employed in US MIL-STD 883D, Test Method 1019.4 (TM 1019.4) [68], is that of bounding part response in the space environment. TM 1019.4 was developed subject to the following constraints [104,113,114]:

1. **The test must screen out both interface- and oxide-charge related failures.**
2. **The test must work for both hardened and commercial IC's.**
3. **The test must be *conservative* (that is, good product is allowed to be excluded on the basis of the test method, but bad product is not allowed to be accepted).**
4. **The test must be relatively inexpensive, and easy to perform and interpret.**
5. **The test must *not* depend on the availability of test structures. Indeed, the method should be useful even in absence of knowledge of the IC's radiation response.**

Because of these constraints on a *standard* test method, *optimized* tests can be developed for a well-characterized technology that improves on standard tests, for example by being less conservative, as illustrated below. We now discuss in detail the technical basis that underlies the main sequence of MIL-STD 883D, Test Method 1019.4, as applied to MOS IC's. Throughout this discussion, we will cite examples that primarily deal with well-characterized Sandia processes; however, qualitatively similar effects (at least with respect to their relevance to a discussion of test methods for low-dose-rate applications) have been reported on many other technologies in the literature [20,22,23,56,58,87,91-99,117,123]. Thus, it should not be presumed that these recommendations are relevant to only one type of technology. In general, the tests outlined below are *conservative* (and perhaps too much so for some) for all MOS technologies of which we are aware.

5.3.3. "Rebound" Testing. The idea behind MIL-STD 883D, Test Method 1019.4 (TM 1019.4) is very straightforward. Because the two dominant defect types in MOS oxides shift the threshold voltage differently, and because their time dependencies are so strikingly different (compare Figs. 9 and 10), it is recognized that *a single device or circuit test performed immediately after any single irradiation cannot provide a conservative estimate of CMOS response in space.* Because oxide traps shift the threshold voltage negatively, and interface traps shift the threshold voltage of an nMOS transistor positively, *at least two independent tests are required to bound the separate contributions of each type of defect to the device response* [104,113,114]. How one accomplishes this task can be debated; indeed, there are a number of plausible methods one might envision to do this. What cannot be disputed, though (unless either oxide trap or interface trap effects can be rigorously demonstrated to be negligible in a technology of interest), is that at least a two-step test must be performed to assess the suitability of MOS devices or IC's in a low-dose-rate environment in a practical, cost-effective manner.

Bounding oxide-trap charge effects in space is relatively straightforward. As illustrated in Fig. 9, oxide-trap charge decreases monotonically with decreasing dose rate or annealing time [103-109]. Thus, *(1) as long as the dose rate of any laboratory exposure is greater than the expected dose rate in space, there will be more oxide-trap charge after the laboratory irradiation than in space.* Further, because interface-trap charge tends to increase with increasing irradiation and/or annealing time, *(2) there will be less interface-trap charge after a laboratory exposure than in space.* Taken together, these two points ensure that gate (or field) oxide transistor threshold voltage shifts will be more negative after a laboratory exposure than in space (see Fig. 7), so a laboratory test is already conservative with respect to oxide-trap charge effects [104,113,114]. That the test may be *overly* conservative for many device types is an important issue that is discussed below.

Bounding interface trap effects in space is a more difficult matter. With room temperature irradiation and/or room-temperature annealing, one can *never* be confident that one has performed a fully conservative test for positive threshold voltage shifts and mobility degradation effects associated with interface traps. This is because, as discussed in the previous point, there will simply always be more oxide-trap charge and fewer interface traps following such a sequence than in space. See Fig. 7, for example. With increasing irradiation and/or anneal time, the nMOS threshold voltage shift is becoming more and more positive. Thus MOS IC's built with processes like that of Fig. 7 will always have a more positive threshold voltage shift in space than in a corresponding laboratory test, unless the test sequence is modified to get around this difficulty. Thus, attempts to "simulate" MOS response in space simply by performing a low-dose-rate irradiation (at a rate that does not approximate the actual rate experienced in the application) are inherently nonconservative, unless characterization tests have been performed to show that no further interface-trap growth or oxide-trap charge annealing will occur in the devices of interest on time scales longer than that of the exposure. This is an important point that is often not appreciated in discussions of testing MOS devices for space applications.

To provide a conservative test for interface-trap effects in space, one must ensure that the *second part of the test sequence leads to a more positive nMOS threshold voltage shift following the laboratory test than will occur in space* [104,113,114]. (The reader should note that other

conditions are sometimes placed explicitly or implicitly on "rebound" testing in the literature that are stronger than this requirement [88,100], e. g., that the method must anneal out all the oxide charge while leaving the interface traps, but the stated condition is sufficient for the test to be *conservative* with respect to interface trap effects.) Figures 11-13 build on the early work of Schwank et al. [88] to show how one can design a "rebound" test to accomplish this goal.

Figure 11: Threshold voltage shift due to oxide-trap charge for nMOS transistors with 32-nm oxides built in Sandia's old baseline process, irradiated to 300 krad(SiO$_2$) with Co-60 or Cs-137 gamma rays. Gates were biased at 6 V during irradiation and annealing. Anneal temperatures were 25°C or 100°C. (After Ref. [113].)

Figure 12: Threshold voltage shifts due to interface-trap charge for the devices of Fig. 11. (After Ref. [113].)

Figure 13: Net threshold voltage shifts for the devices of Figs. 11 and 12. (After Ref. [113].)

First note in Figs. 11-13 that, as for the case of Figs. 7-10, Co-60 irradiation to 300 krad(SiO$_2$) at a dose rate of ~ 400 rad(SiO$_2$)/s followed by ~ 10^6 s of room-temperature annealing at the same bias (6 V) is equivalent to a 0.165 rad(SiO$_2$)/s Cs-137 exposure [59,113]. In Fig. 11 ΔV_{ot} recovery is accelerated by raising the temperature during annealing to 100°C [88], and in Fig. 12 the interface-trap buildup rate *increases* with 100°C annealing. This combination is ideal for providing a conservative test of interface traps at long times or low dose rates; the oxide trap charge is minimized, and the interface-trap charge is maximized. Thus, both components act to make the threshold shift more positive during annealing, as shown in Fig. 13. More importantly, the value of the threshold voltage shift in Fig. 13 is significantly more positive after the annealing sequence shown than it would be after a much longer period at 25°C, given any kind of reasonable extrapolation of the threshold-voltage shift during the next 1-2 decades of time in the 25°C data of Fig. 13. The comparison between interface trap effects at 25°C and 100°C is made more explicit in Fig. 14 for these devices, where times corresponding to 1 wk, 1 yr, and 10 yr are indicated for the interface-trap data. Indeed, it appears that the room-temperature curve is approaching a limit defined by the high-temperature data in this case.

Figure 14: Extrapolation of the data of Fig. 12 to space-like time scales. (After Ref. [59].)

Figures 11-14, as well as other studies on MOS devices [59,88,92-97,100,104,113,114], suggest that a "rebound test" at 100°C might be a suitable accelerated aging test for interface-trap effects at low dose rates. Why one should not try to further accelerate rebound effects is illustrated in Fig. 15, where it is shown that one runs the risks of *reducing* the value of ΔV_{it} if still higher temperatures are used [56]. For lower temperatures, ΔV_{it} increases or is constant with anneal time. Above a given temperature, though, interface traps begin to anneal. This temperature appears to be lower for increased damage, ranging from a low of 100°C for the baseline devices irradiated to 1.0 Mrad(SiO$_2$) to a high of ~ 175°C for Mod B devices irradiated to 1 Mrad(SiO$_2$).

A similar range of results was observed for other technologies in later work by Lelis et al. [126]. Hence, "rebound testing" can provide an effective way to test for interface-trap related failures in space, but care must be exercised that interface-trap annealing does not occur at the temperature chosen for the rebound test.

Figure 15: Postirradiation interface-trap buildup and annealing as a function of increasing anneal temperature over a period of up to 20 days. All irradiation and annealing was at 10 V bias. Devices were built either in Sandia's old baseline (circles and squares) or improved "Mod B" process. The annealing sequence consisted of 3 days at 25°C, 1 day each at 75, 100°C, etc., as shown by the dual x-axis. At the end of the sequence, the baseline devices were held at 250°C for 3 days, and the Mod B devices were held at 250°C for 10 days. (After Ref. [56].)

That one usually cannot use a single test after a high-temperature annealing sequence to *simulate* (as opposed to assist in bounding) the low-dose-rate response of MOS devices is confirmed in Fig. 16. Here we show leakage current as a function of irradiation and anneal time for devices built in a commercial process by Oki Semiconductor [86,89,114]. At higher dose rates and shorter anneal times, the leakage is a primarily a result of parasitic field oxide inversion due to radiation-induced-hole trapping; at low dose rates and/or very long annealing times, the leakage is primarily due to hole trapping in the gate oxide (because of the more effective recovery of the parasitic field oxide leakage current at long times or low dose rates [86,89,114]). In Fig. 16 it can be seen that Co-60 irradiation at any of the dose rates shown provides a conservative estimate of the leakage at long times, because the leakage current decreases with decreasing dose rate or increasing anneal time. However, even if the device is irradiated to *5-times* the dose level of interest (here ~ 6 krad(SiO_2)), i. e., to 30 krad(SiO_2), the leakage current at the end of a subsequent one-week, 100°C anneal is less than that after room-temperature anneal or low-dose-rate irradiation to an equivalent or longer time. Thus, as expected from the above discussion, one *cannot* ordinarily design a single-point test to conservatively estimate both interface- and oxide-trap charge effects in a space environment [114].

Figure 16: Leakage current at 0-V gate bias as a function of total dose, dose rate, and annealing time and temperature for Oki transistors. The open symbols are for room temperature annealing; the solid symbols are for 100°C anneals. (After Ref. [114].)

5.4 TM 1019.4

5.4.1. Main Flow. Figure 17 conceptually illustrates how rebound testing can be employed to "transform" laboratory irradiations into an assessment of interface-trap effects at low dose rates in a space, accelerator, or other low-dose-rate irradiation environment. This is translated into a detailed flow chart of the main sequence of TM 1019.4 in Fig. 18 [68,93,113,114]. The initial irradiation to 50-300 rad(Si)/s is specified to be performed in a Co-60 gamma source at a temperature of 24 ± 6°C. A (1.5 mm Pb)/(0.7 mm Al) container for the devices is required to minimize potential dose enhancement effects [64], unless these effects have been characterized and shown to be negligible for the sources being used.

Figure 17: Schematic illustration of typical dose rates associated with weapon, laboratory, and space and accelerator radiation sources/environments.

Figure 18: Main sequence of the US military-standard ionizing radiation effects test method (MIL-STD 883D, Test Method 1019.4). (After Refs. [68,93,113,114].)

The range of dose rates and the timing requirements specified in the document are intended to assist in standardizing test results [16,86], and to make contact with some types of tactical radiation environments. If all dose rate and timing specifications in the main flow of TM 1019.4 are satisfied, a part that passes the testing sequence of TM 1019.4 is qualified for use in either a tactical or space application. For parts that are intended for use only in a low-dose-rate space application, the text of TM 1019.4 permits testing at lower dose rates, as discussed below. Below we will also discuss some details of the test flow at length, as there has been some confusion and controversy about these points. It is hoped that this discussion will at least make the original intent of the test method clearer, and facilitate decision making about its "proper" use in a total-dose hardness assurance program. Before discussing these points, though, it is also necessary to briefly consider how TM 1019.4 compares with its European standard test counterpart, ESA/SCC Basic Specification (BS) No. 22900 [16,127].

5.4.2. Comparison to BS 22900.

TM 1019.4 shares many similarities with BS 22900, but also contains some differences in test philosophy and test details. These similarities and differences have been discussed in detail in a recent review article by Winokur et al. [16]. Some important differences between the methods are summarized in Table 1.

Table 1: Summary of some important differences between the US military total-dose testing standard, TM 1019.4, and its European counterpart for space, BS 22900. (After Ref. [16].)

Parameter	TM 1019.4	BS 22900
Environments Covered	Tactical and Space	Space
Radiation Source	Co-60 Gamma	Co-60, Electron Accelerator
Dose	± 10% of specification; additional 50% overstress required before rebound test	± 10% of specification; no overstress required before rebound test
Dose Rate	50-300 rad(Si)/s; lower rates permitted for space applications	Exposure time ≤ 96 h; Window 1: 1-10 rad(Si)/s; Window 2: 0.01-0.1 rad(Si)/s
Anneals	No room temperature anneal; 1-wk, 100°C rebound test	24 h room temperature anneal; 1-wk, 100°C rebound test

The lower dose rates specified in BS 22900 are a consequence of its focus purely on space and other low-dose-rate radiation environments. TM 1019.4, which also covers tactical military environments in its main test flow, specifies higher dose rates unless it is known that the parts

will only be used in a space or similar low-rate application [68]. The lower rates and the 24-h room-temperature anneal in BS 22900 will be less conservative for oxide-trap charge related effects (but still sufficiently conservative that the test remains effective) than will be the main sequence of TM 1019.4, for reasons discussed in section 5.8 below. Using an electron accelerator instead of a Co-60 source allows one to increase the amount of displacement damage for a given level of ionizing radiation damage [24,25], which may be beneficial for simulating the space environment for some types of analog bipolar circuits, CCD's, and other components that are more sensitive to displacement effects than are typical MOS devices [24-34]. The lack of a 50% overstress in BS 22900 could be significant, for reasons discussed in the next section, if characterization testing is not sufficient to ensure that worst-case bias conditions are used in the irradiation and anneal portions of the test. Nevertheless, in general, the two tests are quite similar in spirit and in most details, and discussions of one overlap significantly with the other [16]. This is convenient for discussions of hardness assurance for low-dose-rate applications that overlap both communities.

5.5 Overstress Requirement in TM 1019.4

Data like that of Figs. 11-15 led to the recommendation of performing a one-week, 100°C biased anneal after irradiation as a standard rebound test to serve as a conservative screen for interface-trap related failures in space [59,88,104,113,114]. However, several issues other than just nMOS postirradiation response under static irradiation/anneal bias conditions were also considered before arriving at a final recommendation for the TM 1019.4 main test sequence [104,113]. We consider several of these points in the next section, which discusses the addition of ~ 50% margin in the rebound test described in TM 1019.4 [68].

5.5.1. Switched-Bias Effects. MOS IC's in real system applications are not usually held in one bias condition for the duration of a mission. Therefore, it is important to consider the effects of changing the MOS gate bias during irradiation. For example, in Fig. 19 it is shown that switching the bias during irradiation or between irradiation and annealing can sometimes lead to more positive nMOS transistor threshold voltage shifts than steady-state bias conditions [102,122,128-132]. For Fig. 19, devices irradiated with 0 V on the gate and annealed at 6 V (the "0/6" case) show nearly a ~ 40% more positive n-channel threshold voltage shift than devices irradiated and annealed at static bias (the "6/6" case) [129]. This trend has also been observed after 100°C annealing [129]. The increase in nMOS threshold voltage shift is due both to a decrease in the amount of net positive oxide-trap charge in the 0/6 case than the 6/6 case, and to an increase in the number of interface traps [115,122,129].

Figure 19: Threshold voltage shifts as functions of irradiation and annealing time for nMOS transistors with 32-nm oxides irradiated to 1.0 Mrad(SiO_2) in a Co-60 gamma source at a dose rate of ~ 278 rad(SiO_2)/s. Devices were irradiated either at 6 V or 0 V bias, and then annealed at room temperature either at the same or at switched bias conditions. Devices are labeled by (irradiation/annealing) bias; for example, (0/6) = (0 V rad/6 V anneal), etc. (After Ref. [129].)

A significantly more positive value of nMOS threshold voltage shift has also been observed for AC-bias stressed devices than for DC-bias, for example in Fig. 20. This is associated with radiation-induced charge neutralization effects during the AC-bias irradiations, as discussed in detail in Refs. [115,122,133]. Moreover, these effects have been observed for many different types of devices with significant interface-trap densities [102,115,122,128-133]; that is, devices for which rebound effects are most important to assess correctly! Thus, some margin is required in a standard test method to guard against underpredicting the interface-trap density in a device operated under switched-bias conditions. A second irradiation to a level ~ 50% above that of the specification is one way to achieve this margin, and has been incorporated into the main testing sequence of TM 1019.4 [68,104,113].

Figure 20: Threshold voltage shifts versus dose for 10-V, 0-V, and 50-kHz (10/0 V) square-wave irradiations of nMOS transistors built in Sandia's old baseline process. The dashed curves are fits to the steady state data. The solid curve is the AC response predicted by a semi-empirical model discussed in Ref. [122]. The triangles are the measured AC-bias data. (After Ref. [122].)

5.5.2. pMOS Transistors. Up until now, we have been discussing nMOS response almost exclusively, because of its importance to nMOS and CMOS circuits, and because the nMOS transistor is the more challenging case to account for in hardness assurance testing. We should not neglect the point that pMOS transistors in CMOS circuits will recover somewhat during the 100°C anneal associated with the rebound test in TM 1019.4. Figure 21 shows threshold voltage shifts and components due to oxide- and interface-trap charge for a pMOS transistor irradiated to 200 krad(SiO_2) and annealed at 100°C [113]. The change in pMOS threshold voltage during annealing will not be as great as the change in the nMOS threshold voltage because ΔV_{ot} and ΔV_{it} are both negative for pMOS transistors [45,57,69], and the ΔV_{it} component's growth can compensate partially for the ΔV_{ot} component's annealing, as in Fig. 21. Still, a 1-week, 100°C anneal may not be simultaneously conservative for n and pMOS response, because the pMOS threshold voltage shift in space may be more negative than that following the anneal. However, because the interface-trap growth at long times in pMOS transistors is nearly always less than the trapped-positive-charge neutralization (see Fig. 21), *the initial Co-60 exposure and subsequent test should be conservative for pMOS threshold-voltage shifts.* The 50% overstress in TM 1019.4, however, will increase the pMOS threshold shift after the anneal. This may assist in the detection of potential speed and timing problems in circuits with degraded nMOS and pMOS characteristics [113].

Figure 21: Threshold voltage shifts as a function of irradiation and anneal time for pMOS transistors with 32-nm oxides irradiated to 200 krad(SiO_2) in a Co-60 gamma source at a dose rate of ~ 278 rad(SiO_2)/s at 0 V bias, then annealed at 0 V. (After Ref. [113].)

5.5.3. Interface-Trap Annealing. In Fig. 15 it was shown that, for some device types, interface-trap annealing can be a significant problem in rebound testing if the anneal temperature was significantly higher than 100°C. Even at 100°C, though, some (apparent) annealing of interface traps has been reported in the literature [22,23,97,129], although it cannot be ruled out that some

of this apparent interface-trap annealing may be due to border-trap effects [73,74]. One case is shown in Fig. 22, where nMOS transistors are irradiated and annealed at 6 V and 0 V [129]. In two cases, the bias is constant between irradiation and anneal; in the other two, the bias is switched. Independent of other factors in Fig. 22, devices annealed at 0 V show small, but significant, interface-trap annealing. Devices annealed at 6 V show no reduction in the inferred interface-trap density during the annealing period. This raises the possibility that devices which are biased in the "off" condition during rebound testing may recover somewhat, though this becomes less important if one has already built in the 50% margin via overstress testing in TM 1019.4.

Figure 22: Threshold voltage shifts due to interface-trap charge versus irradiation and anneal time for n-channel transistors with 32-nm oxides from Sandia's old baseline process, irradiated to 200 krad(SiO_2) and annealed at 100°C. Irradiation and anneal labeling is the same as for Fig. 19. (After Ref. [129].)

5.5.4. Latent Interface Traps.
Although interface trap buildup ordinarily is observed to saturate at long annealing times, as shown in Figs. 12 and 14 for example, long-term increases have been observed after an initial saturation period in some technologies [110,111]. Mechanisms causing this "latent" buildup are not well understood at this time, nor is it known what fraction of technologies will show latent buildup. In all cases observed to date [110,111], latent interface trap buildup is significantly accelerated at 100°C over the buildup rate at room temperature. However, in some technologies it is not clear that a 1-wk rebound test fully factors in the possible contribution of latent interface trap buildup for MOS low-dose-rate response [110]. The additional 50% overstress provides some extra margin against this type of response, though checking for additional interface-trap buildup at long times during elevated-temperature anneal tests during device characterization would seem prudent.

We conclude that, though the text of TM 1019.4 permits one to omit the 50% overstress on the basis of characterization testing, one should be careful first to perform a series of characterization tests that checks for (1) switched-bias effects, (2) pMOS response, (3) interface-trap annealing, and (4) latent interface-trap effects before waiving the 50% overstress [113]. For complex MOS IC's, it may not be straightforward from conventional parametric tests to assure that these areas are not of concern for a given process/technology. This is an example where detailed characterization studies and/or test structure irradiations, like the transistor testing illustrated here, may give a better feeling for these effects.

5.6 IC Data.

Although TM 1019.4 was developed on the basis of a first-principles approach to hardness assurance, it is always worthwhile to check to see whether it really works for circuits! One barrier to acquiring data of this type is that irradiation and annealing data taken per the conditions of TM1019.4 must be compared to low-dose-rate IC data. These sorts of comparisons are in relatively short supply in the literature, though there is no shortage of data supporting large rebound effects in some types of MOS IC's [58,86-89,92-100]. One example in which an explicit comparison of TM1019.4 and low-dose-rate data was performed is shown in Fig. 23 [58]. For

CMOS SRAM's, read access time is particularly sensitive to rebound effects in nMOS transistors. Here, it is plotted as a function of dose for relatively low-rate (solid symbols) and TM1019.4 testing, including the 50% overstress discussed above. Clearly, as intended, the rebound overtest in TM1019.4 leads to enhanced read-access-time degradation over that observed in the low-rate exposures. While this is by no means a definitive check of the assumptions underlying TM1019.4, which was mostly developed on the basis of test structure (transistor) data, it is always reassuring to see that the circuit response follows that of the test structures. We will discuss the comparison of IC and test structure radiation response further below, in connection with the QML approach to radiation hardness assurance.

Figure 23: Read access time as a function of different test conditions and total doses for 16k SRAM's irradiated either at a dose rate of 0.2 rad(SiO_2)/s, or according to TM1019.4 (including a 50% overstress at a given dose before rebound testing). (After Ref. [58].)

5.7 Relaxing Rebound Test Requirements

Rebound testing is an absolute necessary for many part types, and is a small price to pay to avoid possible catastrophic system failure due to improper part selection. Nevertheless, it is certainly more expensive to do rebound testing than it would be to omit it, if "safe" to do so. For this reason, TM 1019.4 contains many possible ways to avoid having to do rebound testing as part of a *routine* lot acceptance program [68].

One way to determine whether a rebound test is required during lot acceptance for a device of interest is to perform full characterization tests on devices made in the same process technology. If it can be demonstrated that rebound failures are not a problem for the devices and irradiation conditions of interest, TM 1019.4 allows the rebound test to be omitted during lot acceptance [68]. We emphasize that this action should not be taken lightly, and certainly not without evidence that the devices are being manufactured on a process line for which key variables that affect radiation-induced interface-trap buildup, like postoxidation temperatures and annealing ambients [17,45,57,69,90,134-138], are under careful control. Evidence of sufficient control could be demonstrated, for example, with lot sample tests using a 10-keV x-ray source to irradiate test structures that accompany the product wafers [17,18,61], as discussed further below. If, and only if, (1) interface-trap densities of the test structures remain under statistical process control, and (2) the control level is below trap densities for which it has been demonstrated that product circuits will pass testing for the given application per the full TM1019.4, including rebound testing, then it is reasonable for the parties to the test to agree to waive rebound testing during routine lot acceptance of product from that line to avoid unnecessary expense [68,104].

Unfortunately, not all product required for low-dose space systems can be procured from vendors who can (or will) demonstrate sufficient control of interface-trap densities to allow a waiver on rebound testing. Certainly, this would almost never be the case for a commercial line in which radiation hardness is neither a requirement nor a consideration during the product cycle [69,139,140]. And, for a commercial line, a successful "spot test" on one product run cannot be used to "bless" future (or past!) product runs, without evidence of control of variables impacting

radiation hardness [18] (which is virtually impossible to obtain from a purely commercial line). However, for low-dose systems, it may be possible to waive rebound testing on the basis of a *first-principles* estimate of the maximum number of interface traps that can be generated in a MOS transistor with a gate oxide of a given (known) thickness. In Fig. 24 we plot the maximum positive threshold voltage shift that interface traps may induce in MOS devices with 20-nm, 50-nm, and 100-nm oxides. These curves are derived from a simple calculation performed in the same spirit as a previous estimate of maximum hole trapping in MOS devices by McGarrity [141]. Specifically, it is assumed that interface-trap buildup can be described with the equation [104,141,142]:

$$\Delta V_{it} \approx (q/\varepsilon_{ox}) \, \kappa_g \, f_y \, f_{it} \, (t_{ox})^2 \, D \,, \tag{1}$$

where -q is the electronic charge, ε_{ox} is the oxide dielectric constant, κ_g (the charge generation efficiency) is the number of electron-hole (e-h) pairs generated in SiO_2, f_y is the probability that a given e-h pair does not recombine, f_{it} is the interface-trap generation efficiency (i. e., the total number of interface traps created per e-h pair), t_{ox} is the thickness of the SiO_2 gate oxide, and D is the dose. The values of Fig. 5 were calculated assuming a charge generation efficiency of ~ 8 x 10^{12} $cm^{-3}rad^{-1}(SiO_2)$ [143], and a charge yield of ~ 80% [143,144], both of which are reasonable for biased MOS devices in space. A value of f_{it} of ~ 20% was selected as typical of, or greater than, literature values of f_{it} for MOS devices that exhibit very large interface-trap buildup [20,90,104,136,142,145]. Shifts in Fig. 24 assume no offsetting contribution to threshold voltage due to oxide-trap charge, even though this will be non-zero in space, and thus are intended to provide a conservative upper bound on the maximum device rebound for a given gate oxide thickness [104]. (Interface traps in field oxide regions of MOS devices do not adversely affect device response, because they shift the field oxide threshold voltage away from depletion, so only interface traps in the gate oxide need be considered in this estimate.)

Figure 24: Maximum positive threshold voltage shift as a function of dose for nMOS transistors, calculated under the conditions of Eq. 1. (After Refs. [104,141].)

Except for circuits with delicate timing requirements or low noise margin [87], or devices like power MOSFETs where it may not be possible to tolerate even small reductions in output drive current [20-23], circuits and devices with gate oxides thinner than ~ 100 nm can often function with the small positive threshold-voltage shifts observed below 5 krad (dashed line) in Fig. 24. For thinner oxides, this point of acceptability moves to higher doses. For example, Eq. (1) suggests that a 10-nm oxide should have less than +0.06 V rebound at 100 krad(SiO_2)! Thus, for thin enough gate oxides and low enough total dose requirements, it should be possible to waive rebound testing in many cases [104]. As technologies continue to evolve, MOS gate oxide thickness continues to shrink. State-of-the-art commercial oxides are now about ~ 9-12 nm, so rebound should become less of a concern in the future, at least for systems with modest total dose requirements. This is good news! Of course, in absence of knowledge about device processing or circuit response, even for these types of devices, a limited amount of characterization testing that includes elevated-temperature annealing to screen for possible interface-trap effects certainly would be prudent for sensitive devices and IC's. Still, oxides in older technologies are thicker,

so MOS IC's with oxides much thicker than 10-20 nm are routinely used in space systems. Thus, rebound testing cannot be dismissed without appropriate characterization testing and process control. Especially for advanced ICs in low-dose space applications, however, it is hoped that some reduction in testing expense can be realized via first-principles analysis per Eq. (1) [104].

5.8 *Less Conservative Oxide-Charge Tests*

The above discussions have centered on using TM 1019.4 as a conservative test for MOS hardness in space. However, there is also evidence that many devices that fail the initial "oxide-charge" portion of TM 1019.4, when it is performed at a dose rate of 50-300 rad(SiO_2)/s, may actually be hard enough to function in space because of oxide-trap charge neutralization [86,93,103,104,116,121]. Although it is better to throw out a good device than to fly a bad one, it is useful to consider alternate approaches to the first part of TM 1019.4 (i. e, the initial irradiation-to-specification and test) that are less conservative with respect to oxide-trap charge. Such a test is especially useful for low-dose space systems (e. g., 5-20 krad(SiO_2)), for which some commercial non-radiation-hardened devices might fill system needs. We present this example in quite a bit of detail, because of its practical significance, and because it illustrates the type of analysis one must do during the device characterization phase of a project to relax some of the requirements of TM 1019.4.

Figure 25 illustrates how the "failure dose" of three commercial devices depends on the dose rate of the exposure. The Oki 81C55 is a device with a rapidly-recovering field oxide that causes failure during Co-60 irradiation at 50-300 rad(SiO_2)/s, but not at dose rates (< 0.1 rad(SiO_2)/s) typical of space applications [89]. At low rates, failure is caused by oxide charge trapping in the MOS gate oxide [86]. The SGS 4007 and the Harris HM6504 are commercial devices that recover very slowly after Co-60 irradiation at 50-300 rad(SiO_2)/s, and exhibit failure doses at low dose rates that are similar to those observed at high rates [104,114]. Thus, the Oki device is typical of devices that will function at much higher doses in space than during Co-60 exposure at 50-300 rad(SiO_2)/s, and the HM6504 and the SGS 4007 are typical of slow-annealing devices that will fail in space at doses only slightly higher than during Co-60 exposure at 50-300 rad(SiO_2)/s.

Figure 25: Failure dose versus dose rate for three types of commercial MOS devices. Irradiations at dose rates greater than 1 rad(Si)/s were performed with Shepherd or AECL gamma sources. Irradiations at lower rates were performed with Shepherd Cs-137 sources. For these sources, dose (Si) $\approx$ dose (SiO_2). (After Ref. [104].)

The wide range of variation in annealing rates among commercial devices is further illustrated with the vintage data of Fig. 26, in which n-channel transistor threshold voltage (not shifts, here) is plotted versus irradiation and anneal time for 4007-series inverters made by five different manufacturers [106]. The Fairchild inverter shows rapid hole annealing, as well as some interface-trap buildup. In fact, the primary issue raised by the Fairchild data of Fig. 2 is whether there is so much oxide-charge annealing and interface-trap buildup that the devices might fail in space due to positive threshold-voltage shifts (i. e., rebound). At the other extreme in annealing rate,

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the Solid State Scientific (SSS) devices show almost no recovery for the times measured. The National, RCA, and Motorola devices show intermediate recovery rates. Thus, Figs. 25 and 26 illustrate the wide range of device recovery rates that a test must cover to maximize acceptance of good parts while rejecting all bad parts. Moreover, both gate- and field-oxide recovery due to oxide-charge annealing must be accounted for, as in modern commercial technologies the isolation oxides are likely to be of more concern than the gate oxides [139,140] (though the same annealing principles apply [104]).

Figure 26: nMOS transistor threshold voltage versus dose for 50 rad(SiO$_2$)/s Co-60 irradiations of 4007-series inverters. The gate bias was high during all exposures. (After Ref. [106].)

One (very) obvious candidate for a less conservative test for oxide-trap charge failure in space is simply to irradiate at lower dose rates. This is illustrated by the Oki data of Fig. 25. Clearly, lower-dose-rate irradiation leads to a higher dose-to-failure than Co-60 irradiation at 50-300 rad(SiO$_2$)/s, but still provides a conservative test for oxide charge effects at the still lower dose rates (<< 0.01 rad(SiO$_2$)/s) typical of many space systems. One could therefore replace the Co-60 irradiation at 50-300 rad(SiO$_2$)/s in TM 1019.4 with lower-dose-rate irradiation and still obtain a conservative estimate of oxide charge effects in space, as is done in BS 22900 [16,127]. Indeed, the body of TM 1019.4 allows one to do so, if it is known that the application of the devices being tested is exclusively a low-dose-rate radiation environment [68]. Such an option is not allowed for higher-rate applications (e. g., some weapon applications), where a low-rate test would be inherently non-conservative for oxide-charge effects, as discussed further below.

There are a few practical difficulties with this approach. Low-dose-rate exposures are often expensive, difficult, and time consuming. There are also special challenges associated with dosimetry at very low dose rates [59]. Moreover, for devices like the HM6504 and the SGS 4007 in Fig. 25, one could perform very-long-term exposures and still find that the device is unsuitable for system application. These potential difficulties do not rule out low-dose-rate irradiation as a less conservative test of oxide-trap-charge related effects in space, especially for systems with modest total dose requirements that allow low-rate exposures to be performed on manageable time scales. Still, it is worth considering an alternative approach based on Co-60 irradiation at 50-300 rad(SiO$_2$)/s and room temperature annealing, as has been proposed recently [93,104,116].

To illustrate the technical basis of the tests outlined in Refs. [93,104], for example, consider Fig. 27. Here we have simulated the response of non-radiation-hardened oxides following Co-60 irradiation and 25°C anneal via linear response theory [104,106]. The approach taken to derive these results is very general, and has been validated for many types of MOS circuits and devices [103-107]. The specific modeling is described in Ref. [104]; however, the general conclusions drawn do not depend on the exact details of the analysis. In Fig. 27 we compare the response of MOS devices following Co-60 irradiation and room-temperature anneal to their projected response after low-dose-rate irradiation to the same dose. (Interface trap effects are neglected in this discussion, and would have to be assessed separately via rebound testing at the conclusion of the room temperature anneal [93,104,113,114].) The results of Fig. 27 are derived from measured (commercial, 45 nm thick) gate-oxide response to 40-krad(SiO$_2$) Co-60 irradiation at a dose

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rate of ~ 240 rad(SiO$_2$)/s, followed by a 1-week room-temperature anneal (curve B). In previous work, this Co-60 irradiation and annealing response has been shown to match low-dose-rate response over more than 4 decades of annealing time [104,114], justifying the approach illustrated here. In Fig. 27, this response is extrapolated an additional 2 decades to ~ 10^9 rad(SiO$_2$)/s via linear response analysis, per the method of Refs. [104,106], and plotted as curve B, which illustrates a 10% per decade annealing rate. To generalize the discussion to higher and lower annealing rates, projected irradiation and anneal curves are plotted in Fig. 27 for otherwise identical devices having annealing rates of 5 and 15% per decade of annealing time (Curves A and C, respectively).

Figure 27: Projected values of nMOS gate-oxide or parasitic field oxide threshold voltage for non-radiation-hardened MOS transistors. Data points are derived from linear response analysis predictions, which are variations on a set of experimental annealing data, as described in Ref. [104]. The starting value of the threshold voltage is taken to be 1 V for the gate oxide and 15 V for the field oxide. No significant changes occurs for times less than 10^7 s for the low-rate response curves.

As a convenient criterion for the discussion of Fig. 27, we can define failure to be the point at which the nMOS gate- or field-oxide threshold voltage becomes less than 0 V; that is, the point at which the gate or parasitic field oxide transistor goes into depletion mode [86]. At or near this point, increased leakage in the device can lead directly to circuit functional failure, or to system failure because of excessive power dissipation [86,89]. Figure 27 shows that devices with gate or field oxides that trap large amounts of oxide charge and anneal very slowly (Curve A) fail after Co-60 irradiation (V_{th} < 0 V), and also fail in space for the same reason. Faster annealing devices (Curves B and C) also fail after Co-60 irradiation (V_{th} < 0 V), but function acceptably at low dose rates (for the solid curves, V_{th} > 0 V).

In Fig. 27, the devices of Curve C recover (V_{th} > 0 V) approximately one day after irradiation, and the devices of Curve B recover after about 11 days (~ 10^6 s). However, for any reasonable annealing time, even up to 1 year (~ 3 x 10^7 s), the threshold voltage is more negative following Co-60 irradiation and room-temperature annealing than at the end of the low-dose-rate exposure. Thus, Fig. 27 confirms that Co-60 irradiation and room-temperature annealing can provide a conservative response of oxide-charge related failure in space, but the estimate is less conservative than that provided by TM 1019.4 [93,104,116].

Continuing with our analysis of the model results of Fig. 27, in Fig. 28 we compare the response at four points along the annealing curves of Fig. 27 to the responses projected at the end of the low-dose-rate irradiation, again as a function of the trapped-hole annealing rate. As expected from the discussions above, the amount of net positive oxide-trap charge remaining after Co-60 irradiation followed by short annealing periods at room temperature is greater than that present during low-dose-rate exposure, for all cases except (obviously) for zero annealing rate, where the quantities are equal. For an annealing rate of 10% per decade in Fig. 28, for example, Co-60 irradiation plus 1-*minute* anneal overpredicts the net oxide-trap charge in space by 129%, while Co-60 irradiation plus 1-*week* anneal overpredicts the oxide-trap charge in space by only 52%. In fact, increasing the anneal time from ~ 1 minute to ~ 1 week reduces the amount by

which oxide-trap charge effects are overpredicted in space by about 2.5-times at all annealing rates. Because leakage currents (especially near the point at which devices go into depletion mode) can scale exponentially with gate- or field-oxide trap charge density [61,146], such a reduction in oxide-trap charge can lead to huge changes in measured leakage currents.

Figure 28: Ratio of net oxide-trap charge following Co-60 exposure plus varying anneal times at room temperature to that observed at the end of a 30-year low-dose-rate exposure, as a function of trapped-hole annealing rate, for the data of Fig. 27. Linear response analysis was used to simulate these results. (After Ref. [104].)

On the basis of the results of Figs. 27 and 28, one conceivably could extend the annealing period as long as patience and practicality allows, to obtain progressively more realistic estimates of oxide-trap charge effects in space. However, one must ensure that the total annealing time at room temperature, t_A, does not exceed the following limit, $t_{A,max}$, where

$$t_{A,max} = D_T/R_M .$$ (2)

Here D_T is the system total-dose specification and R_M is the maximum dose rate at which any significant dose is deposited [104]. The limitation on t_A is necessary for systems in which a significant fraction of the dose can be deposited during a relatively short portion of the mission, e. g., during a solar flare or an excursion into the radiation belts [45-51]. Equation (2) is also potentially an important constraint to military space environments, where a satellite must not only survive the natural radiation encountered in space, but also must survive higher-rate weapon-related radiation environments. Keeping $t_A < t_{A,max}$ prevents devices that could fail during the brief period of exposure at higher dose rates from being accepted on the basis of their longer-time recovery. Obviously, for systems in which nearly all of the total dose is deposited at approximately the same rate, Eq. (2) provides no practical limitation on the allowed annealing times. And, for mixed-rate systems, as long as the above limit on anneal time is observed, Co-60 irradiation plus room-temperature annealing can provide an estimate of the effects of oxide-trap charge on MOS response in space that is less conservative than TM 1019.4's main test sequence (Fig. 18.) [104].

One possible way to incorporate a room-temperature anneal into a hardness assurance test plan based on TM 1019.4 is illustrated in Fig. 29. The dose and oxide thickness conditions at the outset of the test refer to the need to perform rebound testing [113], as discussed in the previous section, and do not apply to the oxide-trap charge related portion of the test (the initial Co-60 irradiation). The oxide-trap portion of the test (i. e., irradiation to the specified dose) must, of course always be done (though not necessarily at the dose rate specified in Fig. 29, for low-dose-rate applications). If devices pass the initial Co-60 test, one then can proceed directly to the rebound test in TM 1019.4. If one fails the Co-60 test, the text flow in Fig. 29 allows one to repeat the test after room-temperature annealing, subject to the time constraint of Eq. (2). If the devices pass after the room-temperature annealing, *rebound testing must still be done to check for interface-trap related effects* [104,113].

Figure 29: Example of a less conservative test for oxide-charge effects in space based on TM 1019.4. This test flow is *not* part of TM 1019.4, though testing at reduced rates is allowed by TM 1019.4 for space parts. (After Refs. [93,104].)

A complicating factor in applying the test method of Fig. 29 to IC's, or similar test flows discussed recently in the literature [93,104,116], has been pointed out by Sexton et al. [93]. That is, if the leakage current induced by the initial radiation exposure becomes so large that it heats the devices significantly, the test can become non-conservative due to thermally-assisted "over-annealing" of the oxide-trap charge. Hence, it is important that the IC remains truly at room temperature during the annealing portion of the test, and does not self-heat [93]. This is an issue for both TM 1019.4 and BS 22900. Of course, each method also specifies control of the device temperature during irradiation for the same reason [68,127], so such parts that have this problem ideally should be identified at the irradiation-testing phase.

5.9 Weapon Applications

5.9.1. Issues. The above discussions of TM 1019.4 have centered on adapting Co-60 irradiations and elevated temperature anneals to provide conservative estimates of MOS response in space, or for a similar low-dose-rate application. As discussed above, the initial Co-60 irradiation at a dose rate of 50-300 rad(SiO_2)/s in TM 1019.4 (but not the lower-rate irradiations in BS 22900) can also provide a reasonable simulation of many types of "tactical" weapon applications [86]. For tactical and high-dose-rate weapon applications in which the dose rate of exposure greatly exceeds 300 rad(SiO_2)/s, though, the main test flow of TM 1019.4 often does not provide a conservative estimate of MOS response [58,59]. One example of this is shown in Fig. 30. Here the quiescent leakage current, I_{DD}, is plotted as a function of dose for three different dose rates: 10^6, 1833, and 100 rad(SiO_2)/s. At the higher rates, there is a large increase in leakage current at 100-200 krad(SiO_2) due to the turn-on of a parasitic edge transistor associated with the field oxide in these devices [58,140]. At the lowest rate, no such increase is observed. These differences in response are due to the decrease in oxide-trap charge and increase in interface-trap charge in the edge region with decreasing dose rate (or increasing anneal time) that prevents the parasitic device from turning on and increasing I_{DD} at the lowest rate. Thus, *oxide-charge related failures in high-dose-rate radiation environments are not always identified in testing via TM 1019.4.* For these environments, one must either test under conditions that simulate the environment of interest, e. g., by exposing the devices at a LINAC or flash x-ray source [58], or an equivalent derivative test method must be employed.

Figure 30: Quiescent leakage current versus dose for IC's fabricated in Sandia's CMOS IIIA process irradiation at dose rates of 100, 1833, and 10^6 rad(SiO_2)/s. The 100 rad/s exposures were in a Co-60 source, the 1833 rad/s exposures were with 10-keV x rays, and the 10^6 rad/s tests were with 230-MeV protons at the TRIUMF cyclotron at the University of British Columbia in Vancouver, Canada. (After Ref. [58].)

5.9.2. 10-keV X-ray Irradiation. 10-keV x-ray tests are often performed to (1) characterize the basic radiation response of MOS structures, (2) track the hardness of a given technology via test

structure irradiations, and (3) to provide quick feedback about the hardness of a lot before submitting it to the further expense of packaging the devices and performing Co-60-based lot acceptance testing [60,61,67,146]. The data of Fig. 30 suggest that, because of the higher dose rates associated with typical 10-keV x-ray exposures [146], such irradiations might also be useful in a hardness assurance test plan for MOS electronics intended for use in some types of weapon applications. And this is true. However, a few issues must be addressed before one can use 10-keV x-ray irradiation to qualify parts for high-rate radiation environments. The first issue is that of the x-ray penetration depth. 10-keV x rays do not have enough energy to penetrate IC packaging material, so testing must either be performed at the wafer level or on unlidded parts [60,67,147]. On the other hand, 10-keV x rays penetrate nearly unattenuated the first 2 μm of common semiconductor materials [147], so one need not worry about attenuation effects (even for the thickest SOI materials) in chip-level x-ray exposures.

Two issues that have received a lot of attention in comparisons of 10-keV x-ray and Co-60 response are charge yield and dose enhancement [57,67]. Charge yield refers to the number of electron-hole pairs that escape initial recombination processes, and is very sensitive to electric field and ionizing radiation energy. At a given electric field, 1-MeV Co-60 gamma rays will have enhanced charge yield over lower-energy x rays. Differences are most pronounced at low electric fields. Dose enhancement occurs when low-energy x rays pass through an interface of materials with significantly dissimilar atomic numbers [57,67]. Because of the strong dependence of x-ray interaction (typically via the photoelectric effect) on atomic number, Z, "extra" dose is initially deposited in higher-Z material than the lower-Z material. Some of the secondary electrons generated by the x rays leave the higher-Z material and increase the dose in the lower-Z material above the equilibrium level that would have been deposited in absence of the nearby high-Z material [57,67]. Dose enhancement can also be observed during Co-60 irradiations if very-high-Z materials (e. g., Au or W) are nearby [63,64]. However, as long as Pb/Al filter boxes are employed during Co-60 exposures [64,68], dose enhancement is not usually an issue for typical semiconductor materials because the primary interaction of Co-60 gamma rays with Si and other low-Z materials is via the Compton effect, which has a much weaker Z-dependence [45,57,67].

Dose enhancement effects have been discussed in detail previously, and (despite some initial controversy) are generally well understood for x-ray irradiations [67,143,144,147-152]. Nevertheless, one must take into account differences in amounts of dose enhancement in use and test environments when attempting to use low-energy x-ray sources for high-dose-rate hardness assurance. Monte Carlo and discrete ordinates codes have been developed to do this [148,153-155], though results can depend strongly on the precise system environment and device geometry. Consequently, a standard treatment of dose enhancement effects is difficult to offer, though the problem is treatable on a system-by-system basis. This is an important issue to consider when establishing radiation and test requirements for systems in which MOS electronics may be exposed to high-dose-rate x-ray environments, especially if the devices or their immediate surroundings contain high-Z metallization layers [153-156], but is beyond the scope of the present discussion.

Charge yield (except perhaps for low-temperature applications with large dose enhancement [156]) can be addressed in a more general manner. A breakthrough in the understanding of x-ray charge yield was the ionization current measurements of Benedetto and Boesch [143], which showed that x-ray charge yield was significantly lower than had been expected based on earlier studies [147,157-159]. Their measurements are compared to others in the literature [143,144,149,158,160,161] in Fig. 31. Charge yield for Co-60 irradiations as estimated by Srour and Chiu [162], and later independently confirmed by Shaneyfelt et al. using an entirely different method [144], are shown in Fig. 32.

Figure 31: Charge yield as a function of oxide electric field for 10-keV x-ray irradiations of Si-gate MOS devices. The Benedetto and Boesch data are from Ref. [143]; the Dozier and Brown data are from Ref. [160]; the 47.5 and 60 nm oxide data are from Ref. [158]; the 350 nm oxide data are from Ref. [161]; and the 105 nm oxide data are from Ref. [144]. (After Refs. [143,144,149].)

Figure 32: Charge yield as a function of oxide electric field for Co-60 irradiations of MOS devices. The Srour and Chiu data are from Ref. [162]. (After Ref. [144].)

A comparison of these data illustrates some of the issues involved in using low-energy x-ray sources. For gate oxides, the electric field under worst-case bias is usually 0.5 - 2.0 MV/cm (though fields are increasing in modern devices with thin oxides). At ~ 1 MV/cm, Fig. 31 shows that the charge yield for x-ray irradiation is ~ 0.5. Figure 32 shows that the charge yield for Co-60 irradiation is ~ 0.7, which is ~ 40% higher. However, the presence of dose enhancement in the x-ray test almost perfectly counter-balances charge yield differences for MOS gate oxides. In Fig. 33, the relative amount of net positive oxide-trap charge for x-ray and Co-60 irradiations is plotted as a function of oxide electric field for Si-gate devices with 105-nm and 350-nm oxides [144]. A dose enhancement factor (DEF) of ~ 1.4 is assumed for the 105-nm oxide, and of 1.0 for the 350-nm oxide [144]. To within ~ 20%, these values agree with model predictions of dose enhancement in these devices [148]. Charge yields are estimated from Figs. 31 and 32 to arrive at the predicted response (solid lines), which is in excellent agreement with the experimental data (open and solid circles), suggesting that the dose enhancement and relative charge yield factors have been accounted for accurately in these x-ray and Co-60 irradiations. Thinner oxides show response similar to the 105-nm oxide in Fig. 33, though the dose enhancement factor is slightly higher [144,148]. For the 105-nm oxides, the device response is similar for x-ray and Co-60 ir-radiations at ~ 1 MV/cm due to the aforementioned near-cancellation between charge yield and dose enhancement effects [143,144,148]. At higher fields, the x-ray response is enhanced; at lower fields, the Co-60 response is enhanced, in agreement the general rule that *charge yield issues in 10-keV x-ray irradiations are more significant at low electric fields than at high fields.* For the thicker oxide, the x-ray irradiation shows an under-response for all field conditions. At 0.1 MV/cm, typical of the electric field across a MOS parasitic field oxide, the amount of under-response is nearly a factor of 2 [143,146,161].

Figure 33: Ratio of x-ray to Co-60 radiation-induced ΔV_{ot} as a function of oxide thickness and electric field during irradiation. The curves are predicted responses using the charge yield data of Figs. 31 and 32 and dose enhancement factors of 1.4 and 1.0. (After Ref. [144].)

X-ray charge yield can be an especially important concern for SOI devices. A cross-section of a mesa-isolated SOI device is shown in Fig. 34 [102,163]. For this type of device, the gate oxide, sidewall passivation, and buried oxide each typically have different thicknesses. The buried oxide frequently has no applied back-gate bias (a negative back-gate bias can mitigate total dose problems with the buried oxide [102,163,164]) to simplify system and circuit power supply issues [165-168]. Thus, fringing fields from the drain and the built-in work function potentials are often the dominant sources of the electric field across the buried oxide, which can be very low [102].

Figure 34: Cross-section of a mesa-isolated SOI transistor, highlighting different insulating layers. (After Refs. [102,163].)

The effects of the low fields across the buried oxides for comparisons of x-ray and Co-60 response are shown in Figs. 35 and 36 for SIMOX (Separation by Implanted Oxygen) and ZMR (Zone Melting and Recrystallization) materials, respectively. The SIMOX buried oxide is ~ 400 nm, and the ZMR buried oxide is ~ 2 μm thick [102,163]. All irradiations were performed with 0 V back gate bias at an equilibrium dose rate of ~ 278 rad(SiO_2)/s. For the SIMOX oxide in Fig. 35, the dose at which the back-gate threshold voltage crosses zero (and the parasitic back-gate transistor goes into depletion mode) is ~ 60% higher for the x-ray exposure than for the Co-60 irradiation. The amount by which the Co-60 response exceeds the x-ray response is even larger (nearly a factor of 3) for the thicker ZMR buried oxide in Fig. 36. For other SOI (and SOS) technologies, these factors can vary with buried oxide thickness--as well as back-gate, top-gate, source, drain, and body bias [102,165-168]--so this is an important parameter to quantify during characterization testing.

Figure 35: Back-gate threshold-voltage shifts (V) as a function of equilibrium x-ray and Co-60 dose for SIMOX devices with 0.4 μm buried oxides. (After Ref. [102].)

Figure 36: Back-gate threshold voltage shifts (V) as a function of equilibrium x-ray and Co-60 dose for ZMR devices with 2.0 μm buried oxides. (After Ref. [102].)

Based on the above discussions, similar differences in charge yield for x-ray and Co-60 irradiations are to be expected for any type of electronics technology in which low electric fields are experienced in thick insulating layers under operating conditions critical to device response. So, for example, large differences in charge yield are expected for some types of bipolar devices with thick isolation oxides [62,169-171]. Whether the lower x-ray or higher Co-60 charge yield factors are more appropriate for an environment of interest will of course depend on the dominant type of radiation anticipated under device use conditions. For example, soft x rays will have a charge yield comparable to a 10-keV x-ray source, and high-energy electrons will have a charge yield comparable to, or greater than, the Co-60 gamma rays [141]. Protons show an especially wide variation of charge yield with energy due to their greater mass [66]. Because of the uncertainties inherent in anticipating radiation types and energies for most systems, some margin in x-

ray testing to allow for reduced charge yield seems appropriate, if x-ray tests are to be used for part qualification for high-dose-rate weapon applications. For further discussions of technical issues associated with the use of a 10-keV x-ray source, please see Ref. [67].

5.9.3. Possible Test Methods. Figure 30 above illustrates the point that any testing based on Co-60 or 10-keV x-ray exposures will be fundamentally non-conservative due to oxide-trap charge neutralization effects. That is, a significant fraction of the positive oxide-trap charge that can significantly affect MOS device response at very short times (e. g., on the μs - ms time scales associated with some high-dose-rate weapon applications) can (1) anneal out, (2) be compensated via electron capture in border traps associated with the trapped positive charge [83,108,109], or (3) be offset by the time-dependent growth of interface-trap charge on the time scales of lower-dose-rate irradiations [86-89].

Short of using high-rate sources for lot acceptance testing, which is often expensive and impractical, one can only circumvent this problem via characterization testing and the use of margin and safety factors in hardness assurance testing [58,59]. These safety factors are above and beyond those employed as part of the system design phase (e.g., Section 2 above). An example is shown in Fig. 37, where the threshold voltage of an MOS transistor exposed to 50 krad(SiO_2) at a LINAC at a dose rate of 6 x 10^9 rad(SiO_2)/s is compared to a 10-keV x-ray exposure at 5550 rad(SiO_2)/s to 100 krad(SiO_2) [59]. A negative shift at 10 s following the x-ray exposure that is equal to the shift at ~ 10 ms following the LINAC exposure is observed, thus illustrating that additional dose in a laboratory test can sometimes (but not always) make-up for the increased annealing time. However, the dose rate still must be kept as high as possible in the laboratory exposure for devices which tend to have large interface-trap densities in gate *or field oxide* regions, as otherwise the positive shifts due to interface traps can prevent one from reaching the negative threshold voltage levels one can see at very short times following high-rate exposure [58,59]. Still, Fig. 37 highlights that, with characterization testing, often one can define practical 10-keV x-ray tests based on overtesting and margin that can be useful for hardness assurance testing for high-dose-rate weapon environments [58,59]. The amount of margin required will depend on the neutralization rate of the oxide trap charge in the gate and field oxides, the relative of amount of interface traps in these two regions and their buildup rates, and the system performance requirements (that is, the amount of leakage current associated with negative threshold voltage shifts that can be tolerated at short times).

Figure 37: Comparison of high-dose-rate LINAC and intermediate-rate 10-keV x-ray exposures of MOS transistors with 45-nm oxides from Sandia's old baseline technology. (After Ref. [59].)

5.10 *Synopsis of MOS Test Methods*

Defining optimized tests for high-dose-rate environments requires an understanding of system requirements and device time-dependent response that probably never can be captured in a simple test standard the way TM 1019.4 and BS 22900 allow low-rate response to be estimated. Still, we can offer the following test matrix for epi/bulk and SOI/SOS technologies as a starting point for characterization testing. The split between these two groups is necessary because of the

dramatic impact charge yield in the buried insulator can have on SOI/SOS device response. The matrix also presumes it is not already known from characterization testing that a particular failure mode can be neglected for a given technology. For example, SOI devices with intrinsically hardened buried oxides at high dose rates could be qualified the same as epi/bulk devices, as the charge yield issues in the buried oxide would not be significant if the buried oxide is not impacting device response. *We emphasize, however, that the absence of one failure mechanism (especially field or buried oxide leakage) in laboratory testing does not ensure its absence in a high-rate environment.* Look at Fig. 30 carefully again! For radiation environments in which a significant portion of the total dose is deposited at rates above the maximum rate achievable in laboratory sources ($\sim$ 1000-3000 rad(SiO$_2$)/s in an ARACOR Model 4100 X-ray Irradiator), characterization testing at a LINAC or equivalent high-rate source is necessary to avoid risk from possible non-conservatism of the test with respect to oxide-trap charge. The matrix presented in Table 2 should therefore only be used as a general guideline, and should not be presumed to be a serious attempt at a rigorous standard.

Table 2: Matrix of possible sources/tests useful for characterization testing and for developing hardness assurance plans for MOS devices used in weapon or space environments. For purposes of illustration, the breakpoint between high and low doses in this table is $\sim$ 5 krad(SiO$_2$), unless modified by arguments on maximum interface-trap buildup such as those in Section 5.7 above.

Environment	Epi/Bulk MOS	SOI/SOS MOS
Low Dose Space	Either x-ray or Co-60 testing	Co-60 preferred
High Dose Space	Co-60 exposure per 1019.4 or BS 22900, plus rebound testing	Co-60 exposure per 1019.4 or BS 22900, plus rebound testing
Low Dose Weapon (Tactical)	Co-60 per TM 1019.4 preferred, or x-ray with 2x margin	Co-60 per TM 1019.4
High Dose Weapon (Strategic)	X-ray preferred, with 2-3x margin	Both x-ray testing and Co-60 testing per TM 1019.4 with 2-3x margin
Military Space	Both x-ray testing with 2-3x margin, and Co-60 plus rebound testing required.	Both x-ray testing with 2-3x margin, and Co-60 plus rebound testing required.

Several points must be noted about Table. 2. For all applications involving possible high-dose-rate exposure, the tests below should be supplemented with high-rate characterization testing (e. g., with a LINAC). The break-point between a high- and low-dose environments is $\sim$ 5 krad(SiO$_2$) here, though this is for purposes of illustration only, and should not be taken as absolute guidance. Analysis like that in Section 5.7 above is required to modify this boundary, which is set by the requirement to check for significant interface-trap effects at low dose rates. Rebound testing is only required when stated explicitly. For example, in the "low-dose" space environment, rebound testing is not required (unless gate oxides are thicker than $\sim$ 100 nm or de-

vices or ICs are exceptionally vulnerable to small interface-trap densities [104]). If one cannot eliminate the need for rebound testing by means of characterization testing or analysis along the lines of Section 5.7 above, the "high dose" conditions apply. The "military space environment" is a combination of "high-dose-space" and "high-dose-weapon" environments. X-ray testing presumes using a 10-keV x-ray irradiator at a rate of > 1000 rad(SiO$_2$)/s and performing testing immediately after the end of the exposure. When both x-ray and Co-60 testing are suggested, of course separate lot samples are used for each type of exposure. For example, x-ray testing could be performed at the wafer level, and Co-60 testing (and rebound tests, if required) would be performed on a separate group of packaged parts. So, Table 2 is a useful starting point in hardness assurance test definition for MOS devices in weapon, space, or mixed environments.

5.11 *Effects of Burn-in*

A complication in the traditional MOS lot acceptance flow is recent work showing that reliability screens normally given devices before product is shipped can sometimes significantly affect their radiation response [169]. Because burn-in is performed at a much lower temperature than the device has already experienced during processing, it had previously been presumed that the radiation response of burned-in and non-burned-in devices would be similar, so lot samples for radiation testing could (to save time and expense) be pulled without receiving a burn-in. Figure 38 illustrates the danger of testing devices for a weapon application without burn-in. These commercial octal buffer/line drivers have a problem with excess leakage current in high-dose-rate applications. In. Fig. 38, devices which received a burn-in show much higher leakage current response following Co-60 irradiation to 150 krad(SiO$_2$) than do parts which did not receive a burn-in. Distressingly, the non-burned-in parts easily pass the parametric test limits for these devices, while burned-in parts (more representative of shipped-product response) fail the test. At higher dose rates typical of some weapon environments, these parts could cause system failure due to their high leakage currents.

Figure 38: Static power supply leakage current as a function of dose for commercial octal buffer/line drivers with or without a pre-irradiation 150°C burn-in, irradiated with Co-60 gamma rays at 90 rad(SiO$_2$)/s. The dashed line represents a parametric failure level of 1 mA. (After Ref. [169].)

Enhanced leakage currents associated with burn-in have also been observed in the hardened SRAMs of Fig. 30 [169]. An initial characterization study of gate and field oxide transistors suggests that burn-in may remove some interface-trap precursors in these technologies [169]. Without compensating interface traps, gate-, field-, or edge-transistor leakage can be unacceptably high in a high-dose-rate application [86,89,140]. If devices are to be burned-in before being used in such systems, the results of Ref. [169] show clearly that one must perform radiation testing on burned-in parts (unless the devices have been shown not to exhibit changes in radiation response due to burn-in, or unless the response of burned-in devices can be correlated accurately to that of non-burned-in devices). This effect must also be considered in interpreting the results of wafer level irradiations on non-burned-in devices for technologies that show this effect [169]. Finally, we should mention that this is most likely not a problem that is unique to MOS

technologies, as bipolar and BiCMOS devices which are prone to show parasitic leakage in recessed or trench field oxides (discussed below) may also be susceptible to the burn-in effect.

5.12 If Parts Fail.

The final topic to be covered in this section is what to do if parts fail a radiation test, like TM 1019.4 or BS 22900, during the hardness assurance phase of a project. The glib (and sometimes correct) answer is to throw away the bad parts and buy or build better ones! However, there are some steps to go through before making this decision. First, one should check to see that the parts were biased and tested correctly. Doing something as simple as putting a part into a socket or applying bias incorrectly can destroy a part quite independently of its radiation response (see Figs. 1 and 2, for example). Second, review the cause of the failure. Does it make sense with what you know about the part? For example, if failure analysis shows a blown input protection device, that's probably not a radiation-induced failure. On the other hand, if it's a commercial MOS IC that fails functionally and/or shows high leakage at a few krad, you may be stuck, because that's fairly normal behavior.

About the only options for dealing with real radiation-induced IC failure are to (1) for oxide charge related failures, use the less conservative tests in Section 5.8 above, if the application is a low-rate environment, and if permitted by the contracting authority, (2) for interface-trap charge related failures, consider a detailed characterization of the part over a wide range of dose rates and/or annealing times to try to accurately extrapolate device response in space, as was done for oxide charge in Fig. 27 (this can be a very difficult task, and is not recommended for the non-expert), (3) re-evaluate the radiation requirements for the system to see if the requirements on the part of interest can be relaxed without jeopardizing the system (and/or consider spot shielding the device), (4) try to get a more radiation-tolerant part (or a harder version of the present part), or (5) fly the bad part and accept the risk of reduced system lifetime. It is presumed that option (5) would not be chosen lightly.

6. Testing Issues for Bipolar Devices

Bipolar devices can fail in radiation environments due to parasitic leakage effects similar to those in MOS IC's [170-172], or due to gain degradation, where the device physics can be entirely different from that of MOS devices [173-176]. Figure 39 illustrates a typical parasitic leakage path for a bipolar IC [172]. As in a MOS parasitic field oxide, trapped positive charge in the oxide overlying the p-region between the two buried layers can cause the surface to invert, forming a parasitic leakage path. For this or other types of parasitic leakage-related failure modes associated with trapped-positive charge buildup in insulators, either in weapon or space environments, test methods for bipolar devices are similar to those for MOS devices [114]. Moreover, for gain degradation in high-dose-rate (e. g., strategic weapon) environments, similar tests can also be employed to those discussed above, though more attention must be paid to displacement effects associated with high-energy electrons and protons for bipolar devices (sensitive to minority carrier lifetime) than to MOS devices (sensitive to majority carrier lifetime). Where testing issues become more difficult for bipolar devices than for MOS devices is for IC's in which gain degradation is the primary failure mode, for space or other low-dose-rate

applications. We now discuss why this is the case, and provide some preliminary testing recommendations.

Figure 39: Cross-section of parasitic MOSFET that can invert during ionizing radiation exposure, causing buried-layer to buried-layer leakage in some bipolar technologies. (After Refs. [67,172].)

A cross-section of a modern bipolar junction transistor (BJT) similar to those used in Analog Devices Inc.'s (ADI's) XFCB BiCMOS process is shown in Fig. 40 [177]. The screen oxide which overlies the emitter-base junction is the primary problem in a radiation environment for many types of modern bipolar/BiCMOS technologies [112,173,174,178]. The buildup of positive oxide-trap charge in the screen oxide can greatly enhance the surface recombination rate in the p- base region of NPN transistors. (Analogous effects also apparently can occur in p-emitter regions of lateral or substrate PNP transistors with similar screen oxides [179-181].) The excess base current responsible for the gain degradation in these devices scales as $\sim \exp (N_{ox}^2)$, where N_{ox} is the net positive trapped charge density in the screen oxide. Thus, the devices are extremely sensitive to the oxide charge [173,174]. Moreover, the oxide electric field in the screen oxide ordinarily is small, and due primarily to base-emitter fringing fields (in the absence of accidental overlapping metallization). Finally, the screen oxides are typically of much poorer quality than MOS gate oxides, due to processing constraints associated with the need for a high base surface doping density and the high-temperature emitter drive-in anneal [112]. The combination of poor oxide, low electric fields, and extreme sensitivity of the excess base current can lead to dramatically different radiation response with respect to dose-rate and annealing effects for some bipolar devices than for the MOS devices considered in Section 5 above.

Figure 40: Cross-section of bipolar devices built in a BiCMOS process. The oxide above the emitter-base junction is ~ 545 nm thick for this process. (After Ref. [177].)

Two examples of these differences in response are shown in Figs. 41 and 42 [182,183]. These are representative of a lot of recent data in the literature that show similar effects [181-188]. Figure 41 is the original data of Enlow et al. in which the differences in bipolar and MOS post-irradiation response were first noticed [182]. For these devices, irradiation at a rate of 1.1 rad(SiO_2)/s caused much worse gain degradation than does irradiation at 300 rad(SiO_2)/s and/or performing a subsequent high-temperature anneal. Before this report, it had been considered likely that both MOS and bipolar devices would show gain degradation in space that were dominated by interface-trap effects [175,176], and that rebound tests might be an effective way to simulate bipolar gain degradation in space [114]. Figure 41 showed this was simply not the case. Figure 42 is a follow-on study by Nowlin et al. which reinforces the inability of room-temperature or elevated temperature anneals to increase the amount of gain degradation to levels observed at low dose rates [183].

Figure 41: Comparison of low-dose-rate and high-rate plus high-temperature annealing data for a development version of ADI's RBCMOS process. Devices were irradiated to 200 krad(SiO_2) at 1.1 or 300 rad(SiO_2)/s. The high-rate irradiations were followed by the 100°C anneals shown. The band of low-

rate response after irradiation to the same total dose is indicated by the region between the dashed lines. (After Ref. [182].)

Figure 42: Room-temperature and isochronal annealing data for ADI XFCB transistors. All measurements were taken after the devices were irradiated to 500 krad(SiO_2) with Co-60 gamma rays at a rate of ~ 240 rad(SiO_2)/s. Annealing points during the isochronal anneal correspond to 30 minutes of annealing at (A) 60°C, (B) 100°C, (C) 150°C, (D) 200°C, and (E) 250°C. The room temperature parts were characterized at the same times as the isochronally annealed parts. (After Ref. [183].)

Recent capacitance-voltage (C-V) and thermally stimulated current (TSC) tests on MOS capacitors processed similarly to bipolar screen oxides have strongly suggested that differences in the amount and distribution of oxide-trap charge following high- and low-rate irradiation may be responsible for the enhanced gain degradation of bipolar devices at low dose rates [112]. In particular, for 0-V irradiation of capacitors simulating bipolar screen oxides at ~ 25°C, the net trapped-positive charge density (N_{ox}) inferred from midgap C-V shifts is ~ 25-40% greater for low-dose-rate (< 10 rad(SiO_2)/s) than for high-dose-rate (> 100 rad(SiO_2)/s) exposure [112]. Device modeling shows that such a difference in screen-oxide N_{ox} is enough to account for the enhanced low-rate gain degradation often observed in bipolar devices, due to the ~ exp(N_{ox}^2) dependence of the excess base current [174,178]. At the higher rates, TSC measurements revealed a ~ 10% decrease in trapped-hole density over low rates. Also, at high rates, up to ~ 2.5-times as many trapped holes are compensated by electrons in border traps than at low rates for ADI devices under the irradiation conditions of Ref. [112]. Both the reduction in trapped-hole density and increased charge compensation reduce the high-rate midgap shift.

A physical model has been developed which suggests that both effects are caused by time-dependent space charge in the bulk of these soft oxides associated with slowly transporting and/or metastably trapped holes (e. g., in E_δ' centers) [112]. Figure 43 is annealing data from electron-spin-resonance experiments which supports the assertion that metastably trapped holes in E_δ' centers anneal more rapidly than more deeply trapped holes in E_γ' centers [189]. The space charge associated with these slowly transporting or metastably trapped holes was argued to both reduce the charge yield in the bulk of the screen oxides during high-rate irradiations more than during low-rate irradiations, and to force holes to be trapped somewhat nearer to the Si/SiO_2 interface during the high-rate irradiations than during the low-rate irradiations. Holes trapped nearer to the interface can be more easily annihilated or compensated by tunneling electrons, consistent with the TSC data. For additional details, please see Ref. [112].

Figure 43: Normalized densities of holes in metastable (E_δ') or deep (E_γ') hole traps, as measured via electron paramagnetic resonance. (After Ref. [189].)

On the basis of the model outlined in Ref. [112], it was predicted that bipolar transistors with enhanced gain degradation at low dose rates might show comparable behavior after higher-rate exposure, if irradiated at a temperature that was high enough to enhance the annealing of holes in metastable traps (and/or slowly transporting holes) at high dose rates, but low enough that holes

in deeper traps are not significantly affected [112]. Figure 44 verifies that prediction for XFCB devices [112]. The triangles represent the normalized excess base current (responsible for the enhanced gain degradation) as a function of dose rate for XFCB transistors irradiated with 10-keV x rays at 25°C. The squares are 60°C irradiations of the same devices. At 200 rad(SiO_2)/s, the 60°C data match the low-rate 25°C data exactly. At 20 (SiO_2)/s, the 60°C show greater degradation than at low dose rates. However, some annealing apparently occurs at 60°C at the lowest rate shown here, $\sim$ 1.7 rad(SiO_2)/s. The results of Fig. 44 strongly reinforce the ideas behind the model of enhanced gain degradation at low dose rates outlined above, as do preliminary results on RBCMOS devices [112]. Moreover, Johnston et al. also have irradiated LM324 operational amplifiers, with sensitive substrate PNP's, that show similar dose rate effects [181]. Their results are shown in Fig. 45. Here the parts irradiated at elevated temperature clearly show a response that is degraded from that at 25°C, but the low-rate response is worse still. Thus, more work is required to determined whether elevated-temperature *irradiations* might fill the same role as do elevated-temperature *anneals* in rebound testing of MOS devices [112,180,181].

Figure 44: Excess base current (normalized to preirradiation values) as a function of x-ray dose rate and irradiation temperature for ADI XFCB devices irradiated to 100 krad(SiO_2) at 0 V bias. (After Ref. [112].)

Figure 45: Change in input bias current as a function of dose, dose rate, and irradiation temperature for LM324 operational amplifiers. (After Ref. [181].)

Kosier et al. [184] have reported that the amount of gain degradation possible in bipolar structures like that depicted in Fig. 40 is ultimately limited by geometric factors that are independent of device bias or radiation dose rate. Thus, if a given bipolar device or circuit can still operate successfully after receiving the large amount of radiation (typically more than 1.0 Mrad(SiO_2)) required to reach this level of saturation, the difficult testing issues posed above can be avoided [184]. For many types of devices, however, failure occurs at lower levels, and test-to-saturation is not an option. At the present, it seems that one should perform detailed characterization testing of bipolar devices and circuits that are intended for use in a low-dose-rate environment. Once the basic response is characterized, then some combination of low-rate tests (e.g., at a rate below 10 rad(SiO_2)/s), elevated temperature irradiation, and/or use of safety factors must be combined to provide a conservative test of bipolar/BiCMOS devices prone to failures due to gain degradation in low-dose-rate radiation environments [112,180,187]. Clearly, defining improved standard hardness assurance tests for bipolar and BiCMOS devices is an important area for future work.

7. QML

Many of the test methods described in Section 5 above, though based on a first-principles understanding of total-dose radiation effects, were designed to be applied without special knowledge about the radiation response of the devices being tested. A clear example is TM 1019.4, in which the main test flow can be applied to conservatively test MOS devices for tactical or space applications even without the requirement for characterization testing to understand the response of the particular devices being tested. While this has advantages from the standpoints of stan-

dardization and simplicity, it also may lead to increased qualification costs for some types of devices. For example, if a given technology has been processed so that an insignificant number of interface traps can be created at the dose levels of interest, why go to the time and expense of rebound testing? This issue was explored in Section 5.7 above for devices which "happened" to have been processed acceptably to meet these conditions. Recently, there has been a lot of interest in applying some of the time and expense heretofore spent on lot acceptance testing to improve the underlying radiation response of a particular process, and then *use the knowledge developed in improving the process to reduce hardness assurance costs.* That is, apply resources to "build in" the quality, not try to shake it out during testing. This is the cornerstone of the Qualified Manufacturers List (QML) approach to radiation hardness assurance [15-19]. The QML methodology will be described in more detail by Nick van Vonno in the next section of the course [52], but we feel it appropriate to introduce the topic briefly here in the context of qualifying MOS devices for use in space applications.

The basic principle that underlies the QML approach to radiation hardness assurance is illustrated in Fig. 46 [18]. On the y-axis are savings, represented by reduced hardness assurance costs. On the x-axis is knowledge, which is obtained from studies of the fundamental radiation response of a given process, and from implementing that knowledge via improved processes. With very little knowledge about the response of a process, one must resort to simple, conservative tests--like TM 1019.4 for space environments, or like LINAC testing for high-dose-rate weapon environments. If one increases one's knowledge about a process, and finds that a few basic parameters control the radiation response (for example, nMOS transistor interface-trap buildup or field-oxide threshold-voltage shifts), one can shift the lot acceptance problem from a circuit-assessment task to a test-structure assessment task [16-19,61]. And test structures are much easier and less expensive to test than IC's. Finally, if one can isolate the critical areas of a process that determine the hardness of a given technology, radiation hardness assurance for that technology ultimately could be accomplished via process control verification [18]. For example, in-line statistical process control of initial threshold voltages, gate- and field-oxide thicknesses, and post-oxidation annealing temperatures may satisfy the needs of some low-dose (e. g., less than 5 krad(SiO_2)) tactical weapon applications [16,141]. Unfortunately, Figure 46 is easier to think about schematically than to apply in a verifiable way to actual IC technologies. However, the spirit of this process can certainly be useful in minimizing testing costs, as we discussed briefly in Section 5 above, and as we further illustrate in the discussions that follow.

Figure 46: Key correlations required to increase one's knowledge about a process technology to realize cost savings in hardness assurance testing. (After Ref. [18].)

A key element of a cost-effective QML program is wafer-level irradiation of test structures using a 10-keV x-ray irradiator, or an equivalent technique (if available), to ensure that appropriate process control is maintained [16-18,61]. As one example of a historical record of such data, consider Fig. 47. This is a chart of threshold-voltage shifts due to oxide-trap charge and interface-trap charge for Sandia's 3-μm radiation-hardened "Mod-B" process. Taking this one step further, Fig. 48 shows a ΔV_{it} control chart based on the same data, with deviations from statistical process control (SPC) marked with solid symbols. The reader is directed to Ref. [18] for

a discussion of what it means to be under SPC, and how deviations from SPC can be identified and corrective measures taken.

Figure 47: "X-bar, moving R" plot of threshold voltage shift due to interface and oxide trap charge for nMOS transistors with 45-nm oxides built in Sandia's Mod B process. (After Ref. [18].)

Figure 48: SPC of interface-trap charge for the data of Fig. 47. Average values (X-bar) and upper and lower control limits (UCL and LCL) are indicated. SPC violations are denoted by solid symbols. (After Ref. [18].)

Although one can see several "glitches" through the years that the process was monitored, some attributable to identifiable changes (mostly unintended) in the processing and some not traceable to a clear origin, it can be seen that the process was generally centered around well-defined mean values for interface- and oxide-trap charge densities. These were manageably small for applications requiring total-dose hardness of ~ 500 krad(SiO$_2$) or less. This is a very reasonable hardness "capability" level for a radiation-hardened technology with ~ 45-nm oxide thickness. Just as importantly, the deviations were manageable, and it was verified over the course of running the process that IC's whose test structures remained under control always passed lot acceptance tests [16-18]. Conversely, a lot that showed poor test structure data occasionally had trouble in meeting specifications. After a while, the only reason we kept doing the IC tests at Sandia on a regular basis on the parts that came from the lots processed during periods when the line was under demonstrated process control was because contracts forced us to do so! The idea behind QML is to allow such "wasted" lot acceptance tests to be waived if sufficient control of the process is demonstrated.

As one example of how the QML test methodology can be applied to streamline lot acceptance testing, consider Fig. 49. Here, the change in read access time is plotted for a 2k static RAM as a function of the threshold voltage shift due to interface-trap charge measured at the wafer level immediately after processing [18]. An obvious correlation is present, suggesting that one could use these test structure data as a measure of the circuit response. That is, as long as interface-trap charge levels during wafer level testing remain below those at which the IC still functions acceptably, the process is verified to be under sufficient control that lot acceptance testing with respect to this parameter is not required. Of course, tests to ensure control of oxide-trap charge in the gate and field oxide would also normally be required.

Figure 49: Change in read access time as a function of nMOS transistor ΔV_{it} for static RAMs and test transistors from Sandia's Mod B technology. The RAMs were irradiated in a Cs-137 source at 0.2 rad(SiO$_2$)/s, and the transistors were irradiated with 10-keV x rays at 16.7 krad(SiO$_2$)/s. The doses corresponding to the data points (left to right along the line) are 84, 280, 420, 840, and 1120 krad(SiO$_2$), respectively. (After Ref. [18].)

The QML approach to radiation hardness is still undergoing growing pains, being relatively new in philosophy compared to more traditional approaches based on simple lot acceptance

testing of IC's. Time will be required for vendors and users to agree on what must be measured to ensure that proper control of a process is being maintained, so that the full cost-saving capabilities of QML can be realized [15-19,52]. However, there is no doubt that some elements of QML (i. e., knowledge-based reduction in lot acceptable tests) are very useful, indeed essential, to defining cost-effective radiation hardness assurance test plans in the future.

8. Non-destructive Testing

Until now we have been discussing test methods that involve either irradiating a lot sample of the devices of interest (e. g., TM 1019.4), or a test structure that serves as a hardness verification surrogate. There has been a lot of interest in the past on trying to find electrical tests that can be used to predict, before irradiation, the hardness of an individual IC or device. An extensive report on early activities was generated by Ron Pease in 1978 [190]. Basically, his conclusion was a lot of things made sense to try, but nothing really worked convincingly.

This general rule remains true for integrated circuits have more than a few transistors. It has been shown recently that, for discrete MOS transistors or perhaps small-scale circuits in which individual transistor response can be isolated, the preirradiation $1/f$ noise of the transistor can predict the postirradiation oxide-trap charge [142,191-194]. This correlation is illustrated in Fig. 50, for five different wafers processed with different gate oxidation and annealing treatments from the same lot, but with all other process steps being identical [112,191-193]. The preirradiation noise power scales exactly with the postirradiation ΔV_{ot} for these devices. This correlation evidently occurs because both the preirradiation noise and postirradiation ΔV_{ot} are proportional to the density of oxygen vacancies/vacancy complexes in the oxide [195]. A correlation similar to that in Fig. 50 was noted for these devices between the preirradiation channel resistance and the postirradiation ΔV_{it}, but this is more difficult to exploit for a hardness assurance test, for reasons discussed in Ref. [192,196].

Figure 50: Postirradiation ΔV_{ot} versus preirradiation noise magnitude for MOS transistors with five different gate oxide processes. Wafers D and E received an 1100°C N_2 anneal to additionally soften the oxide; wafers A-C did not receive this anneal. (After Refs. [112,191-193].)

Unfortunately, it is difficult to extend these correlations to integrated circuit tests, which have more interest and impact on hardness assurance testing. Moreover, preirradiation tests for field oxide isolation (other than measurements of the initial field oxide threshold voltage) are not possible in an integrated circuit, since the parasitic field oxide transistor characteristics are only accessible after the device is irradiated. Some promise has been demonstrated for using $1/f$ noise as a screen for power MOSFETs [197]; however, more work is needed to determine the utility of the method. We conclude that non-destructive tests of radiation hardness using $1/f$ noise can be performed (at most) on discrete transistors and small-scale circuits, but it is unlikely that such a method can be developed with general applicability to large-scale IC's.

9. Conclusions and Future Trends

A first-principles approach to radiation hardness assurance was described that provides the technical background to the present US and European total-dose radiation hardness assurance test methods for MOS technologies, TM 1019.4 and BS 22900. These test methods could not have been developed otherwise, as their existence depends not an a wealth of empirical comparisons of IC data from ground and space testing, but on a fundamental understanding of MOS defect growth and annealing processes [16,113]. Because defect growth and annealing, and their effects on device response, can differ strongly in MOS and bipolar devices, it is not possible to apply the same rebound tests to bipolar devices that have been successfully applied to MOS devices in space applications [182-187]. Work continues to develop an optimized test for bipolar devices in space applications [180].

Rebound testing should become less of a problem for advanced MOS small-signal electronics technologies for systems with total dose requirements below 50-100 krad(SiO_2) because of trends toward much thinner gate oxides [104]. For older technologies with thicker gate oxides and for power devices, rebound testing is unavoidable without detailed characterization studies to assess the impact of interface traps on devices response in space [22,23,104].

The QML approach is promising for future hardened technologies. A sufficient understanding of process effects on radiation hardness has been developed that we should be able to reduce testing costs in the future for hardened parts. Of course, this point may be moot if the present trend continues toward the increasing use of commercial parts in space systems [52,139]. On a commercial line, one cannot derive benefits from knowledge gained during part development and characterization, because factors controlling radiation hardness are not identified and controlled. In the future, it seem prudent for hardness assurance standards to allow more relief to manufacturers who attempt to build in the quality via QML, and not just assess the innate hardness of an as-built commercial part.

Finally, it is hoped that the above discussions have demonstrated that the foundation for cost-effective hardness assurance tests is laid with studies of the basic mechanisms of radiation effects. Without a diligent assessment of new radiation effects mechanisms in future technologies, we cannot be assured as a community that the present generation of radiation test standards will continue to apply. If the past tells us anything, it is that there will always be surprises to deal with. I would rather deal with surprises up front during the device characterization or hardness assurance phase of a project that in assessment of a field failure. It is hoped that there will be budget enough in the future to do so.

10. Acknowledgments

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Increase in Trapped Charge Due to Oxide Damage
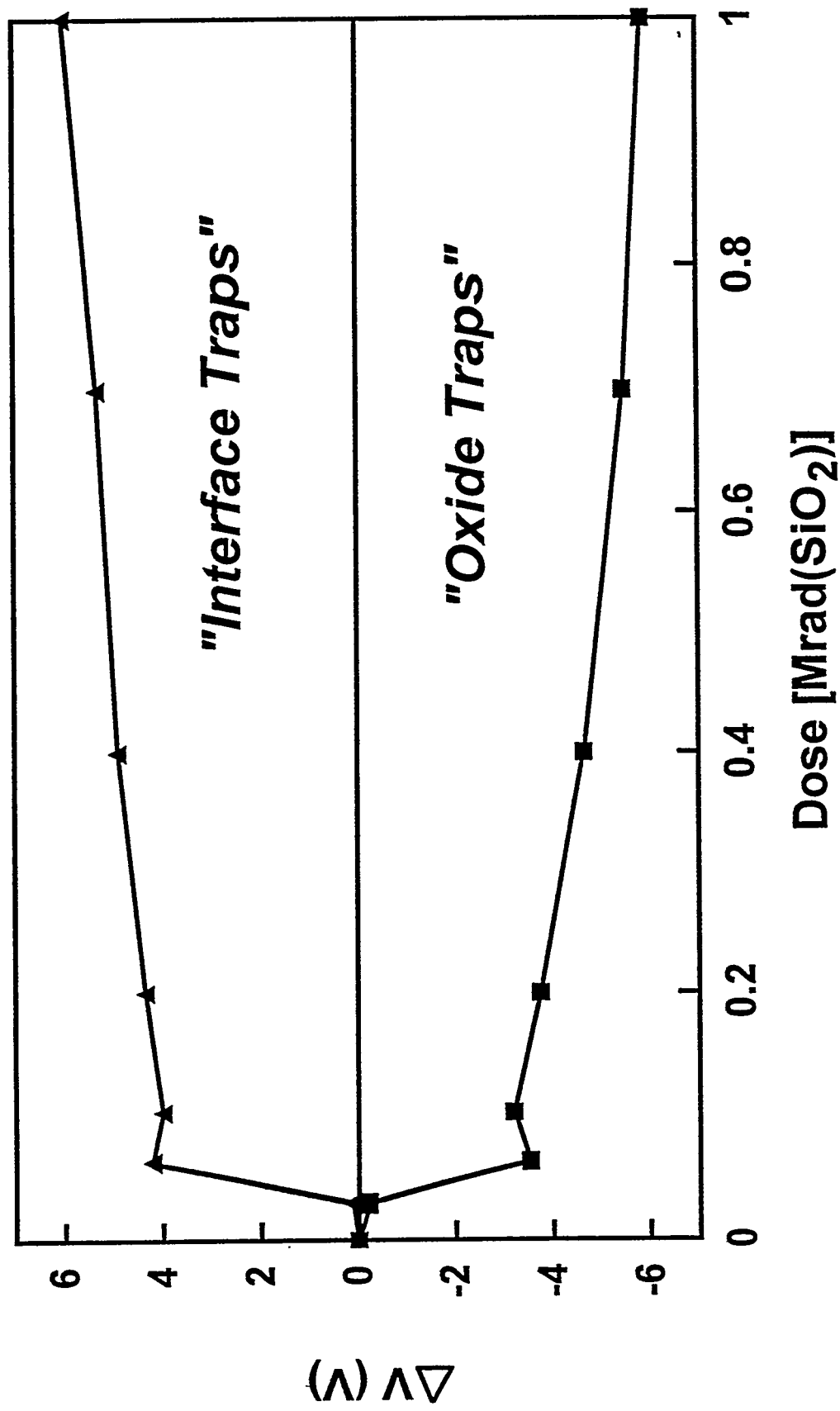
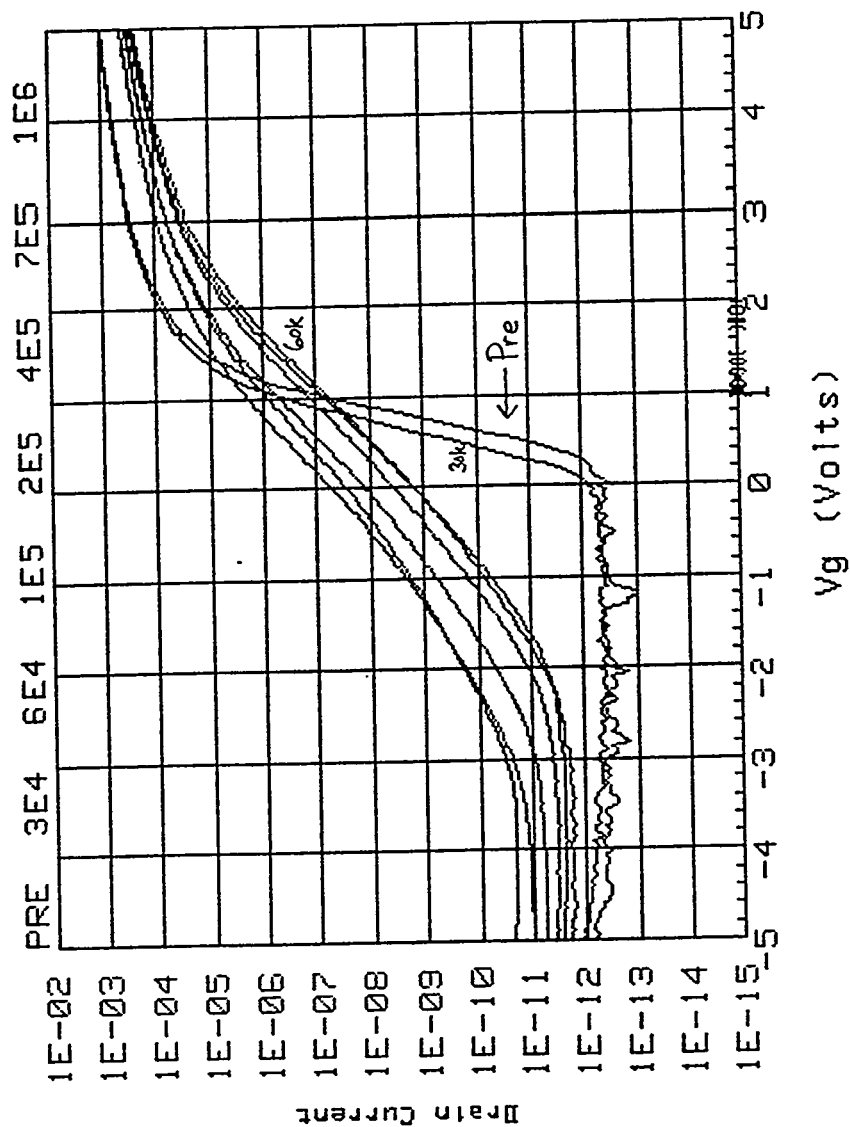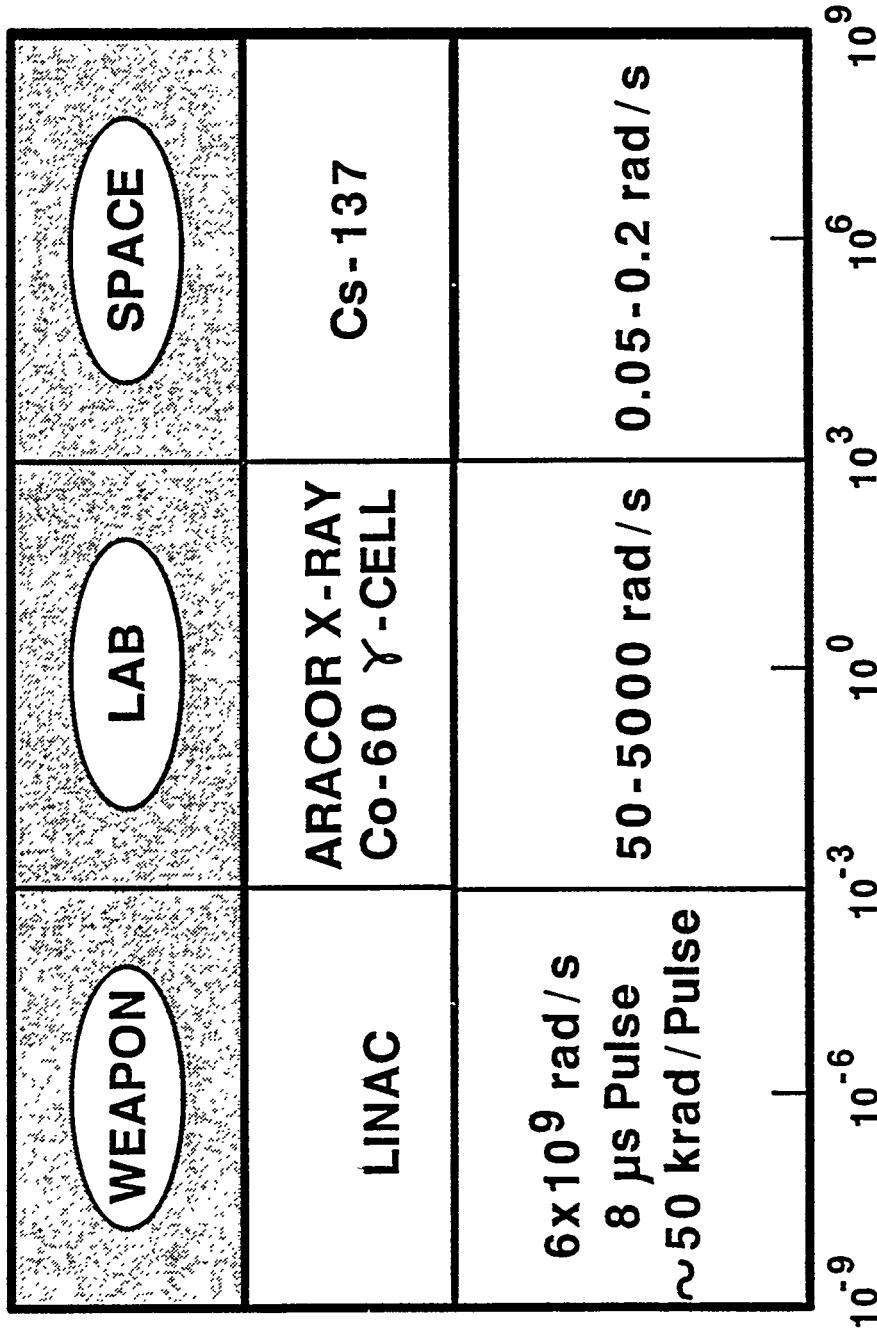## Attempted Co-60 Irradiation

Fig. 1

Nth 1038

PRE 3E4 6E4 1E5 2E5 4E5 7E5 1E6

60k

3k

←Pre

Vg (Volts)

Drain Current

PRE
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
1E-11
1E-12
1E-13
1E-14
1E-15

-5 -4 -3 -2 -1 0 1 2 3 4 5

Fig. 2

SOURCES

WEAPON	LAB	SPACE
LINAC	ARACOR X-RAY Co-60 γ-CELL	Cs-137
6×10^9 rad/s 8 μs Pulse ~50 krad/Pulse	50-5000 rad/s	0.05-0.2 rad/s

| 10^{-9} | 10^{-6} | 10^{-3} | 10^0 | 10^3 | 10^6 | 10^9 |

TYPICAL EXPOSURE TIMES (sec)

Fig. 3
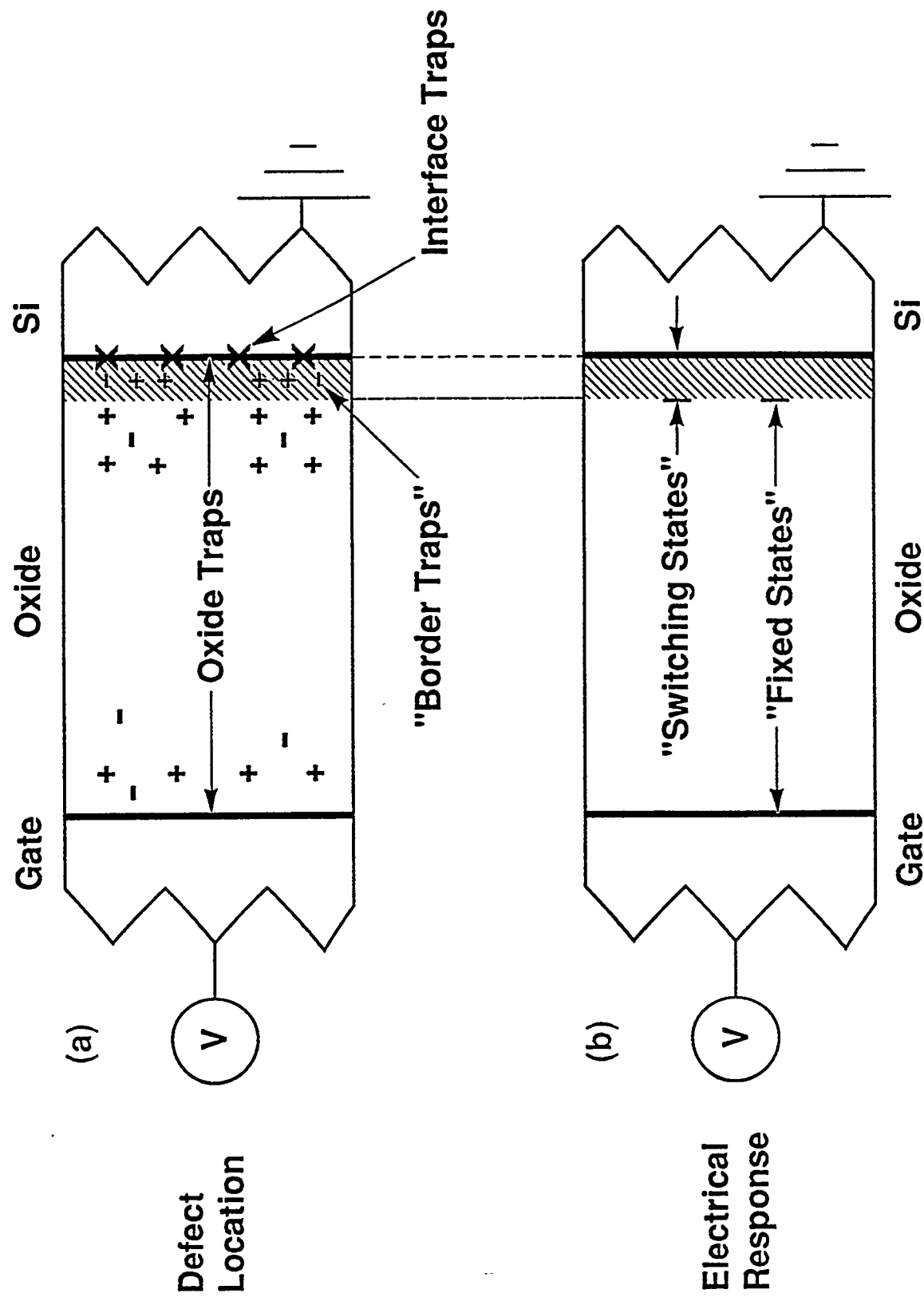
Fig. 4

THRESHOLD-VOLTAGE SHIFT VERSUS DOSE
AT VARYING DOSE RATES
(WINOKUR, ET. AL., 1986 IEEE NSREC)

THRESHOLD-
VOLTAGE
SHIFT

ΔV_{th} (V)

2.0

1.0

0.0

-1.0

TIMING "FAILURE"

0.10 rad (SI)/s

2

20

200

LEAKAGE "FAILURE"

DOSE (rad (SI))

10^4

3 5 10^5 3 5 10^6

86TP2000.30
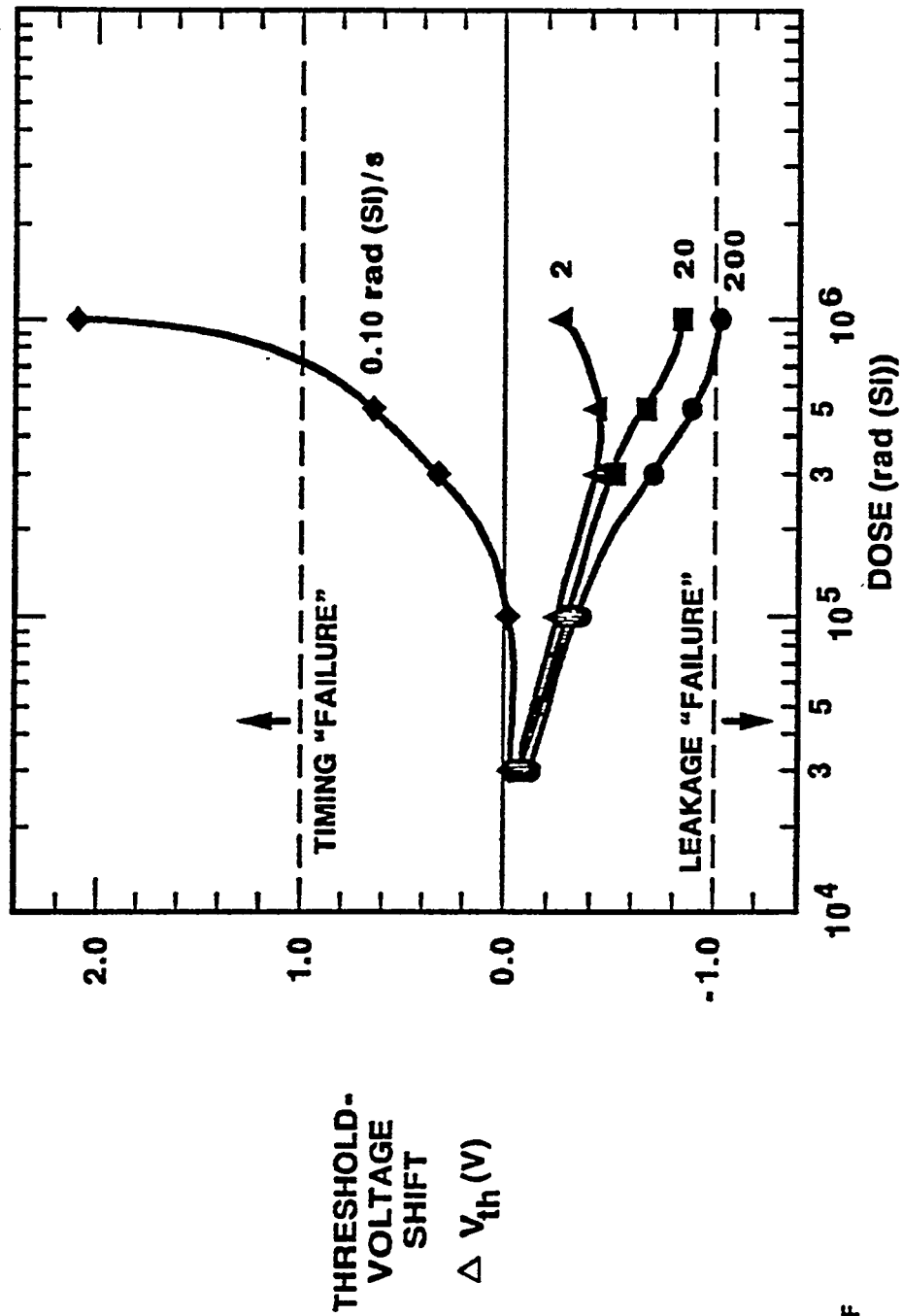
PSW/DMF
12/86

Fig. 5

IC FAILURE LEVEL DEPENDS ON DOSE RATE *

FAILURE LEVEL (krad (Si))

DOSE RATE (rad (Si)/s)

MODEL CALCULATION ●   MEASURED FAILURE LEVELS ■

FAILURE CRITERIA: $\Delta V_{th} = \pm 0.45V$

FAILURE DUE TO POSITIVE THRESHOLD SHIFT

FAILURE DUE TO NEGATIVE THRESHOLD SHIFT
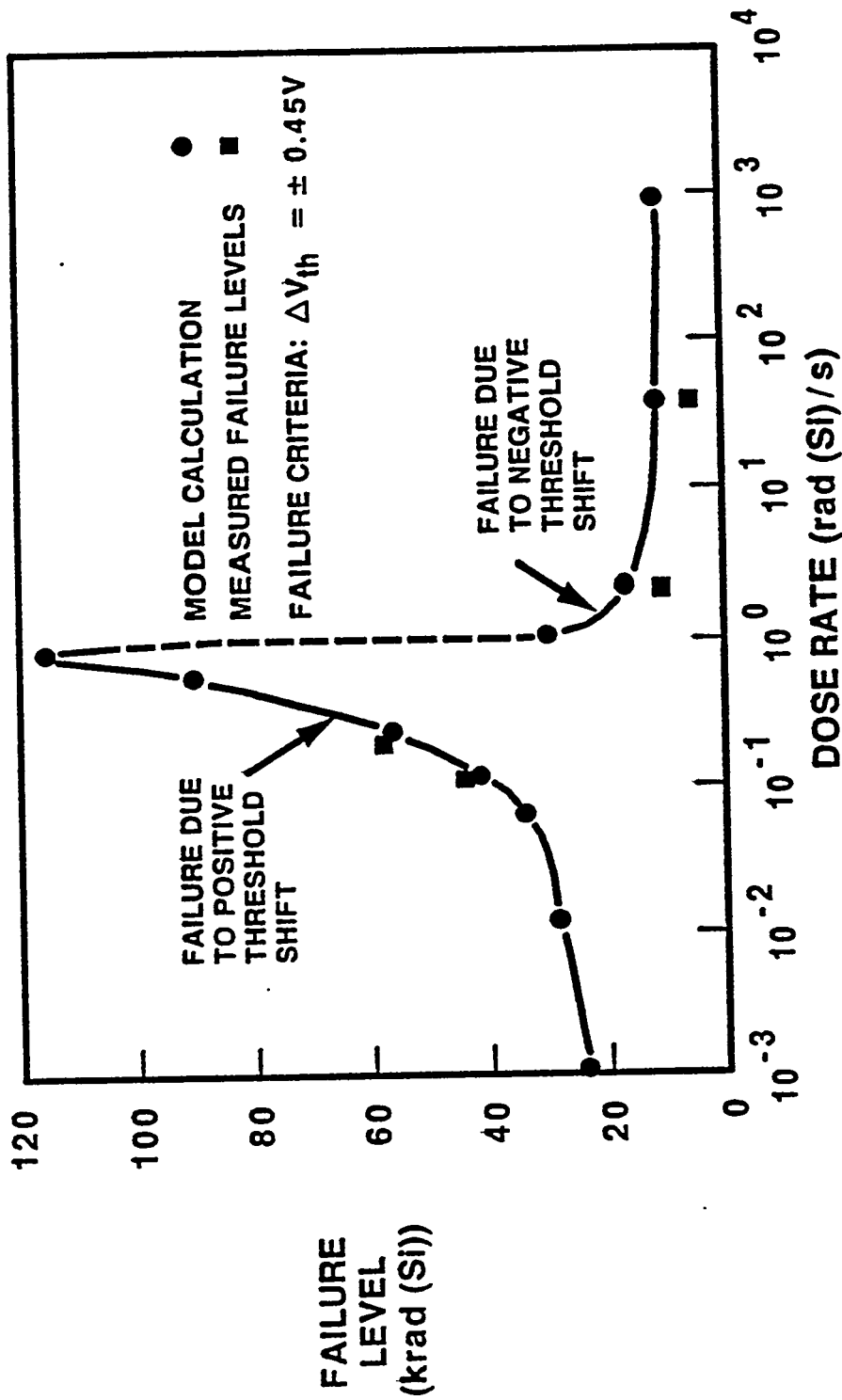
Fig. 6

* AFTER JOHNSTON, IEEE TRANS. NUCL. SCI. NS-31, 1427 (1984)-

86TJ2000.09

PSW 7/86

△Vth vs. POSTIRRADIATION ANNEALING TIME
FOR VARYING DOSE-RATE EXPOSURES

100 krad   N-ch (6V) t_{ox} = 600Å

X-ray, 50-5000 rad (SiO_2)/s

Cs-137 0.16 rad/s

Cs-137 0.05 rad/s

LINAC, 6×10^9 rad/s

△Vth (V)

0.8   0.4   0   -0.4   -0.8   -1.2   -1.6

TIME (sec)

10^{-1} 10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7
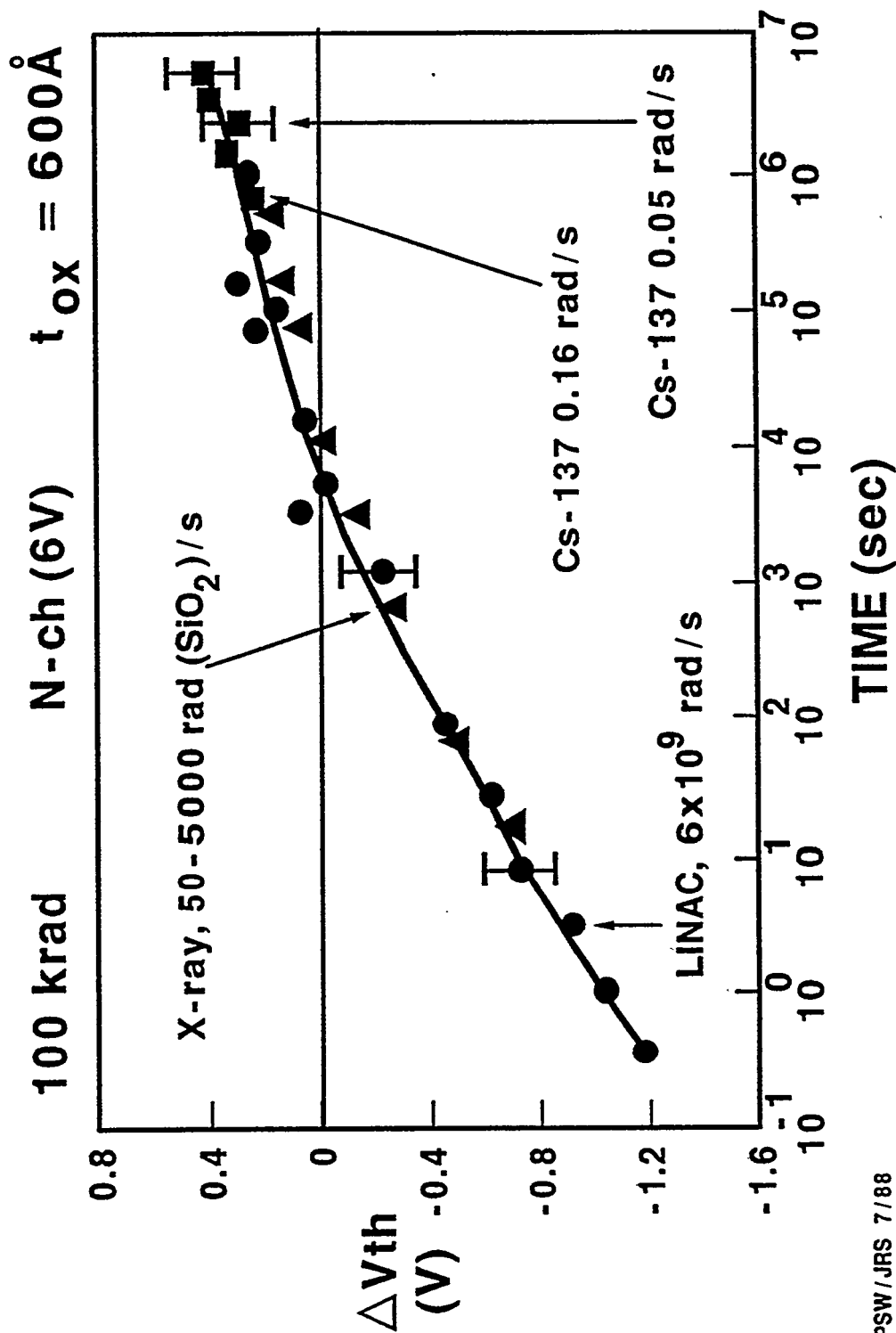
Fig. 7

CURRENT-VOLTAGE TRACES FOR X-ray + ANNEAL AND LOW-DOSE-RATE EXPOSURES AT t = 7 DAYS N-ch (6V) $T_{ox} = 600$ Å
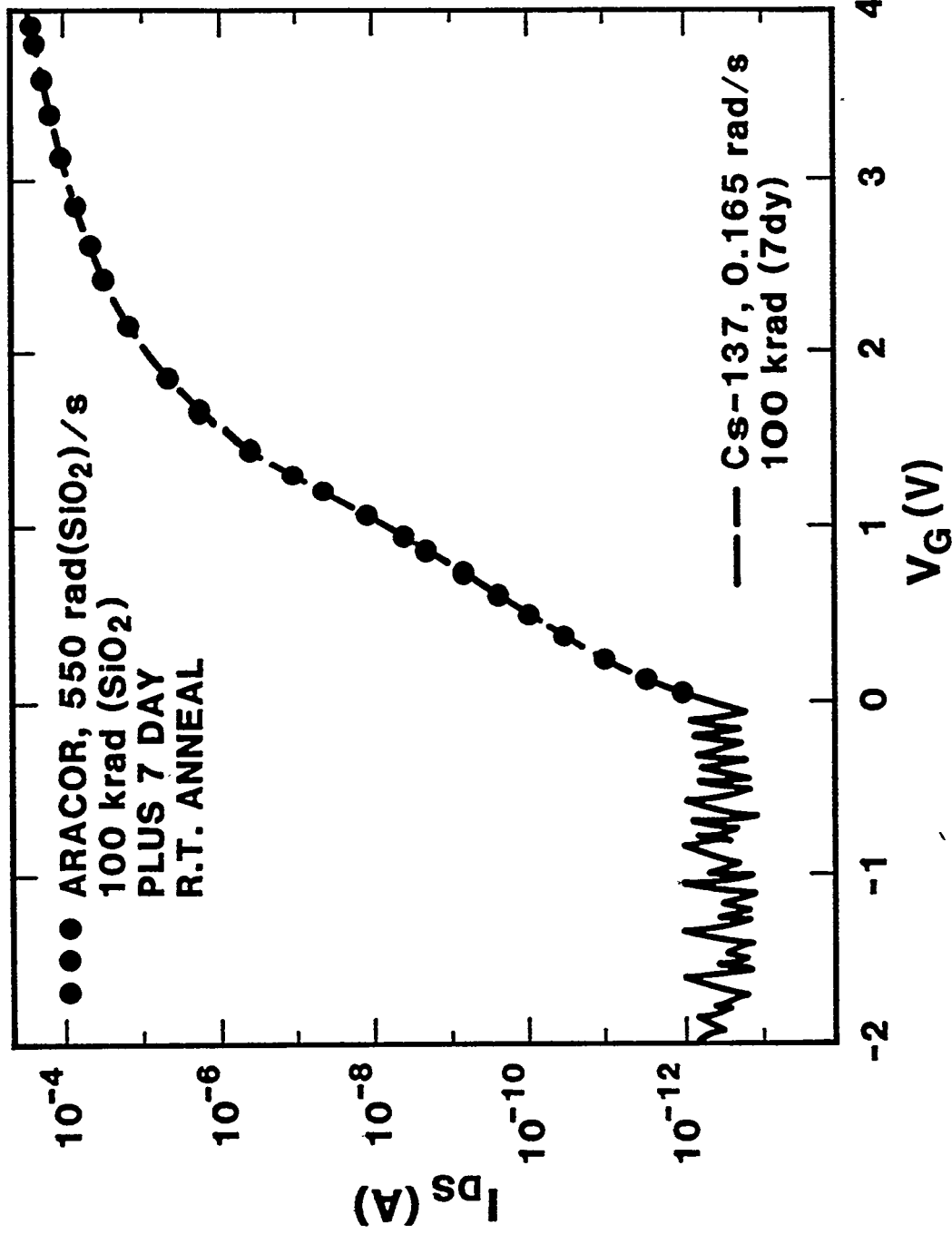
- ARACOR, 550 rad(SiO_2)/s
  100 krad (SiO_2)
  PLUS 7 DAY
  R.T. ANNEAL

— Cs-137, 0.165 rad/s
  100 krad (7dy)

V_G (V)

I_{DS} (A)

Fig. 8

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ΔVot vs. POSTIRRADIATION ANNEALING TIME FOR VARYING DOSE-RATE EXPOSURES ~100 krad N-ch (6 V) t_{ox}=600 Å

Cs-137 (0.05 rad/s)

Cs-137 (0.165 rad/s)

X-ray, 52 rad (SiO_2)/s

X-ray, 5550 rad (SiO_2)/s

LINAC, 2 PULSES, 6 x 10^9 rad (SiO_2)/s

ΔVot (V)

t (s)

Fig. 9

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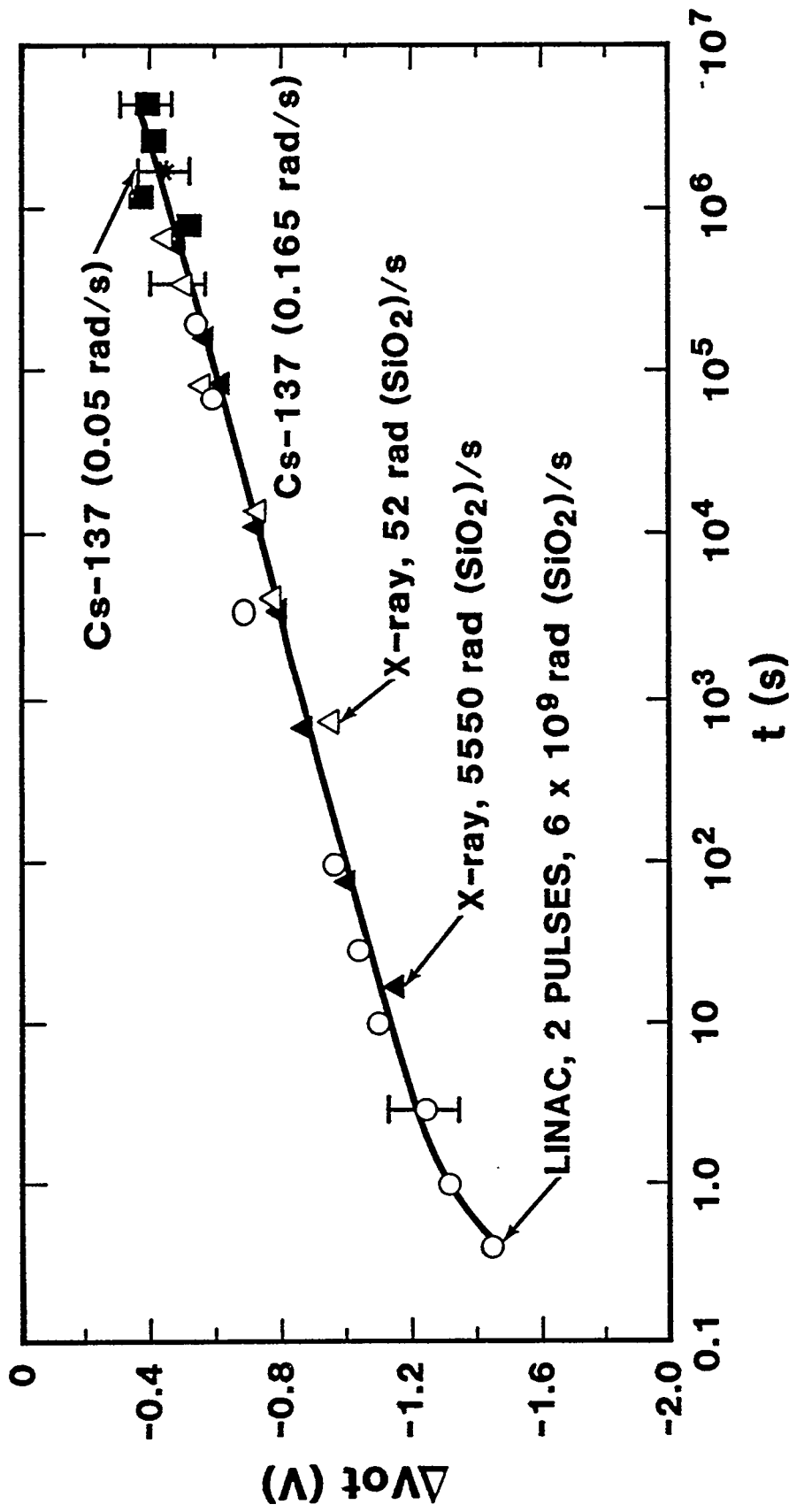
ΔVit vs. POSTIRRADIATION ANNEALING TIME FOR VARYING DOSE-RATE EXPOSURES

100 krad   N-ch (6V) t_{ox} = 600Å
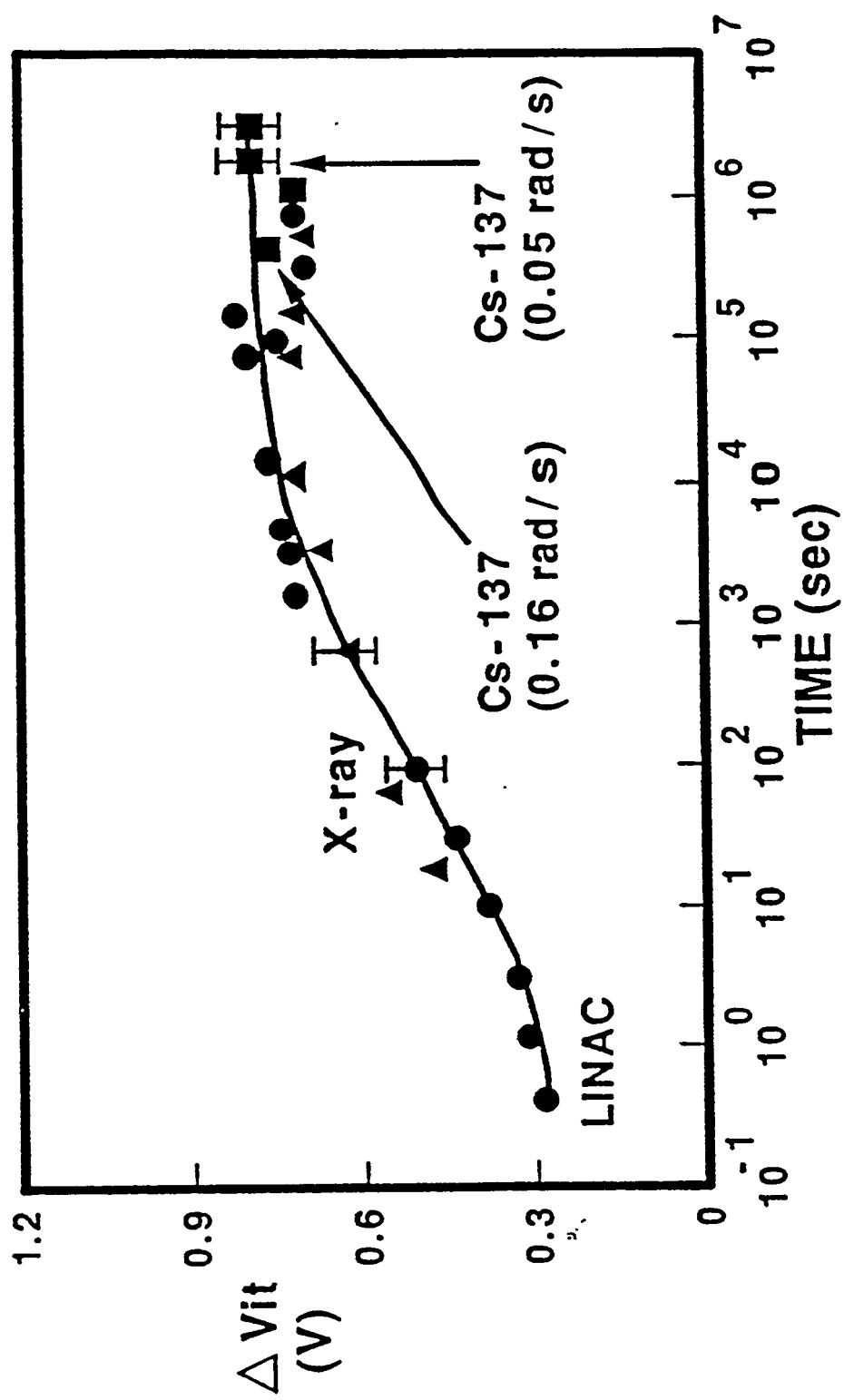
Fig. 10

Fig. 11

Fig. 12

Fig. 13

59
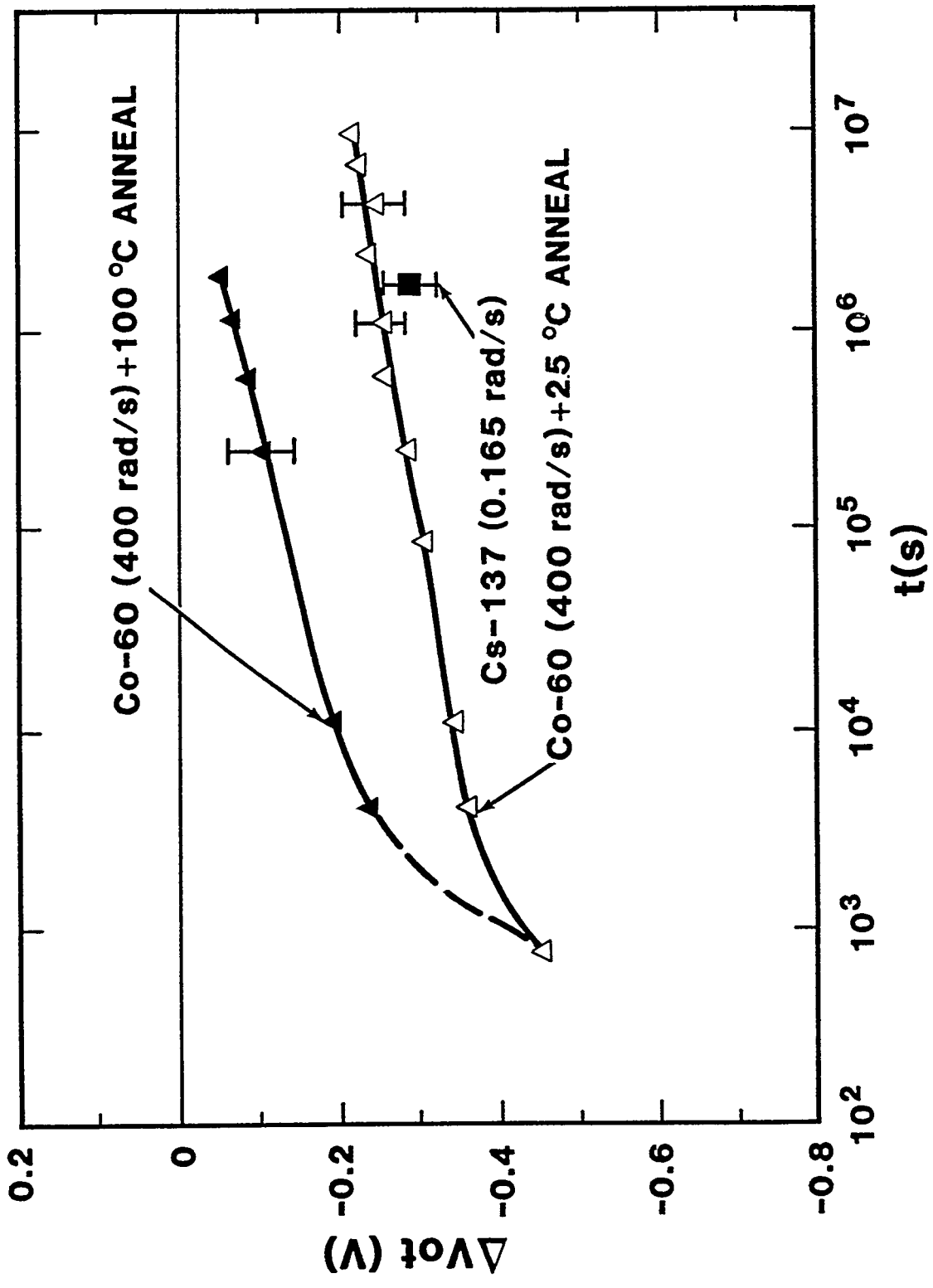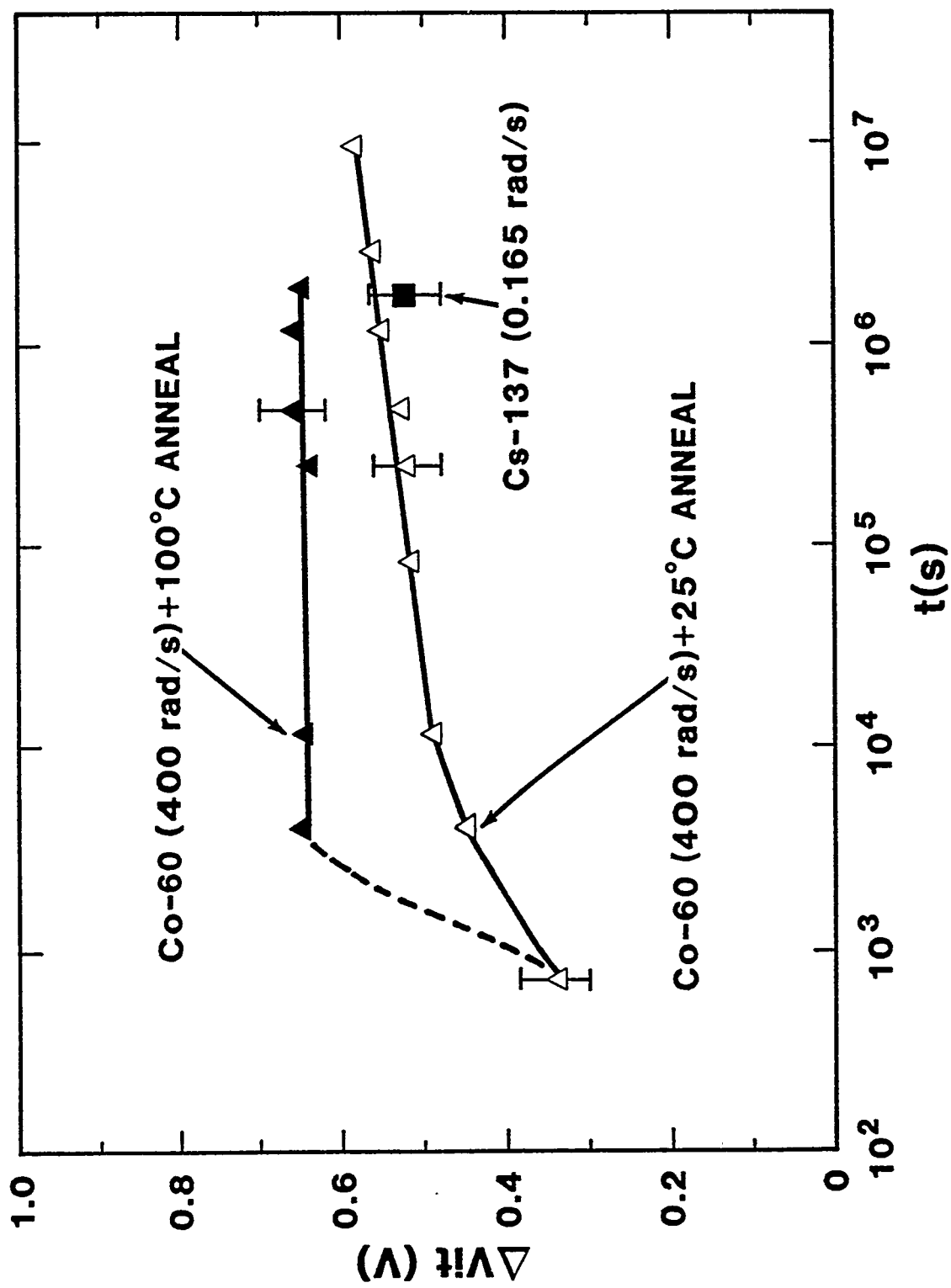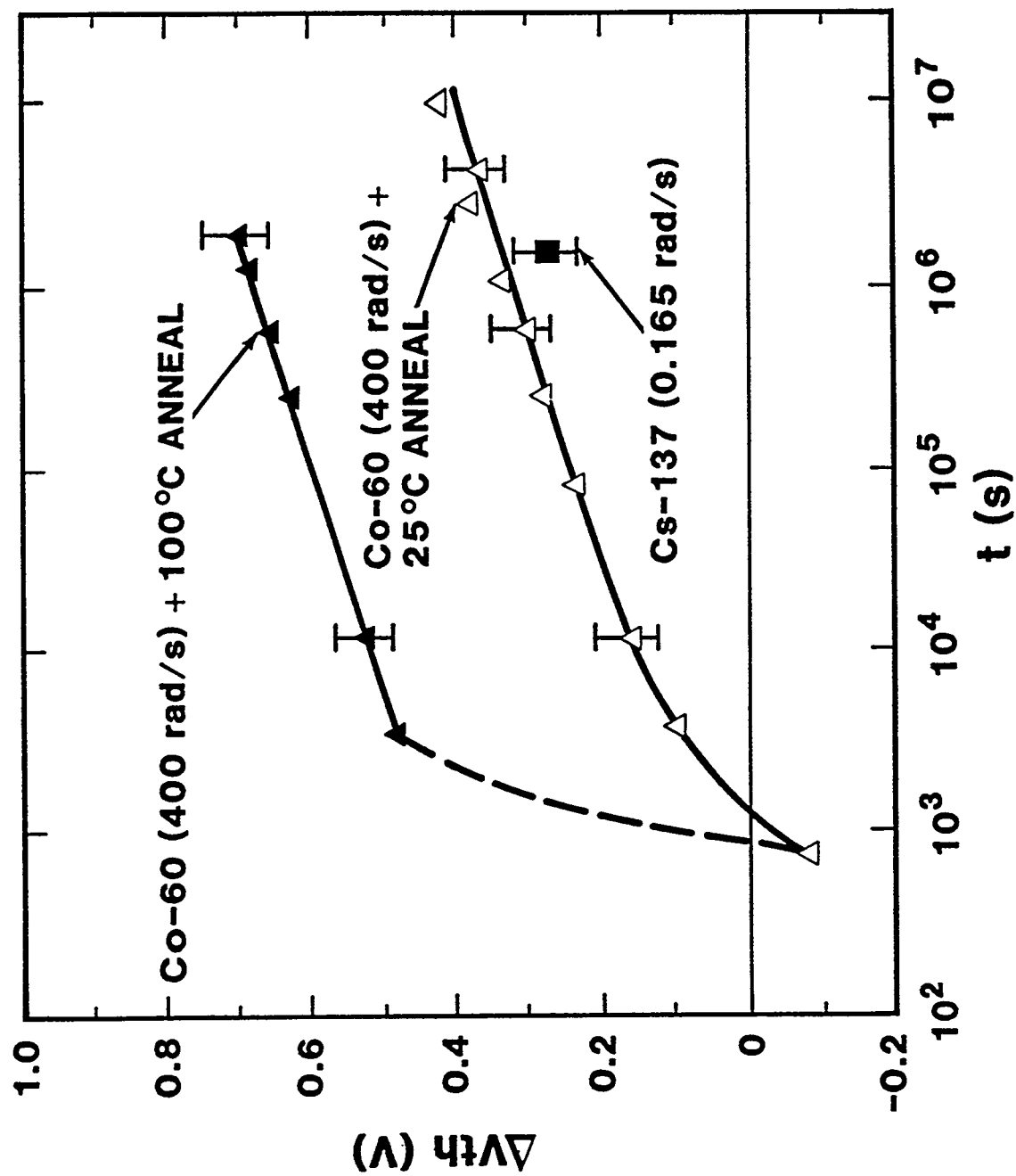
EXAMPLE: SPACE APPLICATION.
Co-60 EXPOSURE To ~1.5 TIMES SPEC.
PLUS ONE WEEK 100°C ANNEAL
(Pass/Fail)

Fig. 14

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DMF/PSW/JRS 7/88

Fig. 15

69
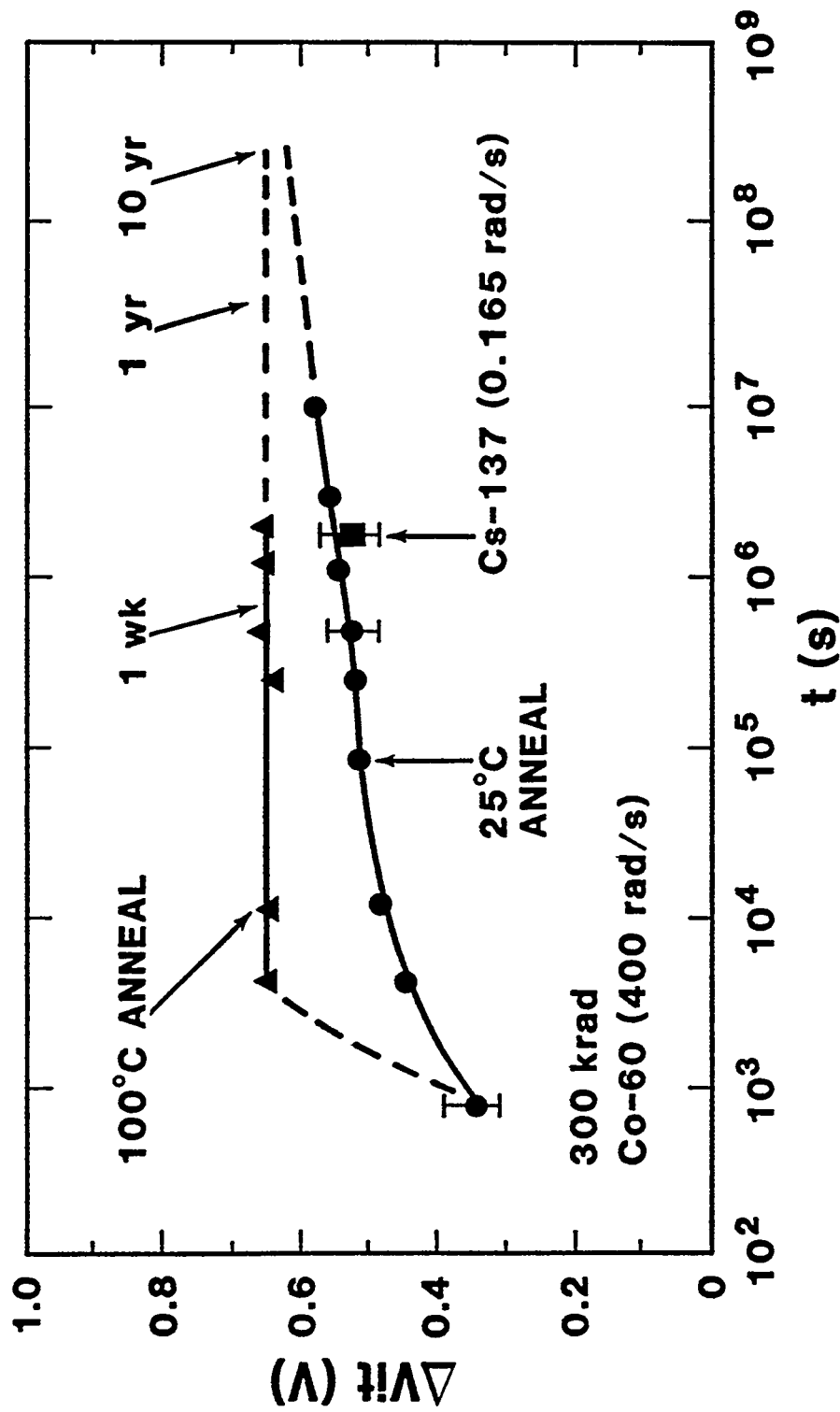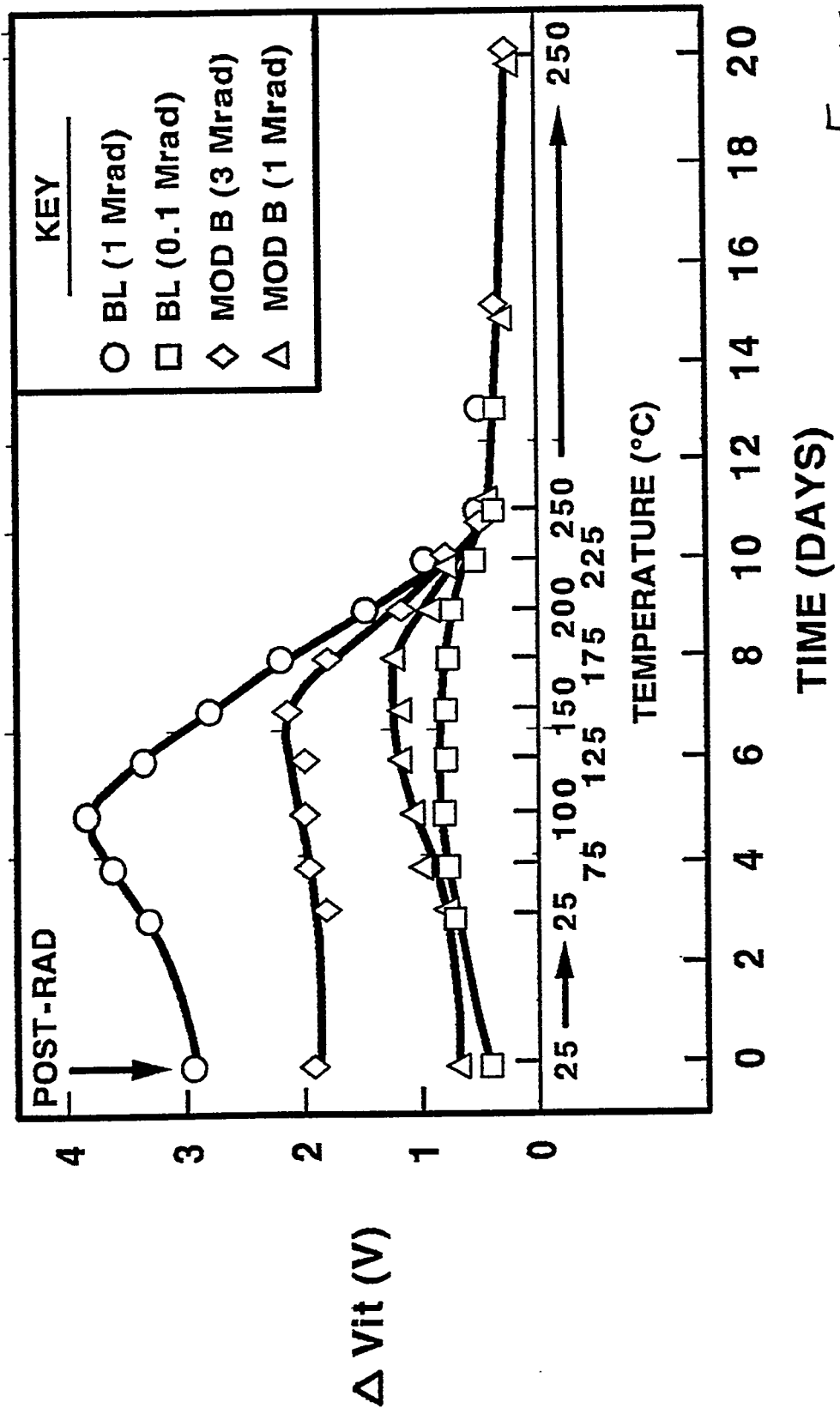
LEAKAGE AS A FUNCTION OF DOSE,
DOSE RATE, AND ANNEALING TIME AND
TEMPERATURE FOR OKI TRANSISTORS

OKI
Bias = 5 V
t_{ox} = 50 nm

□ 6k, Co-60, 200 rad/s, 25°C Anneal
△ 6k, Co-60, 2 rad/s
○ 6k, Cs-137, 0.02 rad/s
◆ 30k, Co-60, 240 rad/s + 100°C Anneal

Fig. 6

⊞ Sandia National Laboratories

DMF/LCR 7/89

TA0034.02.08
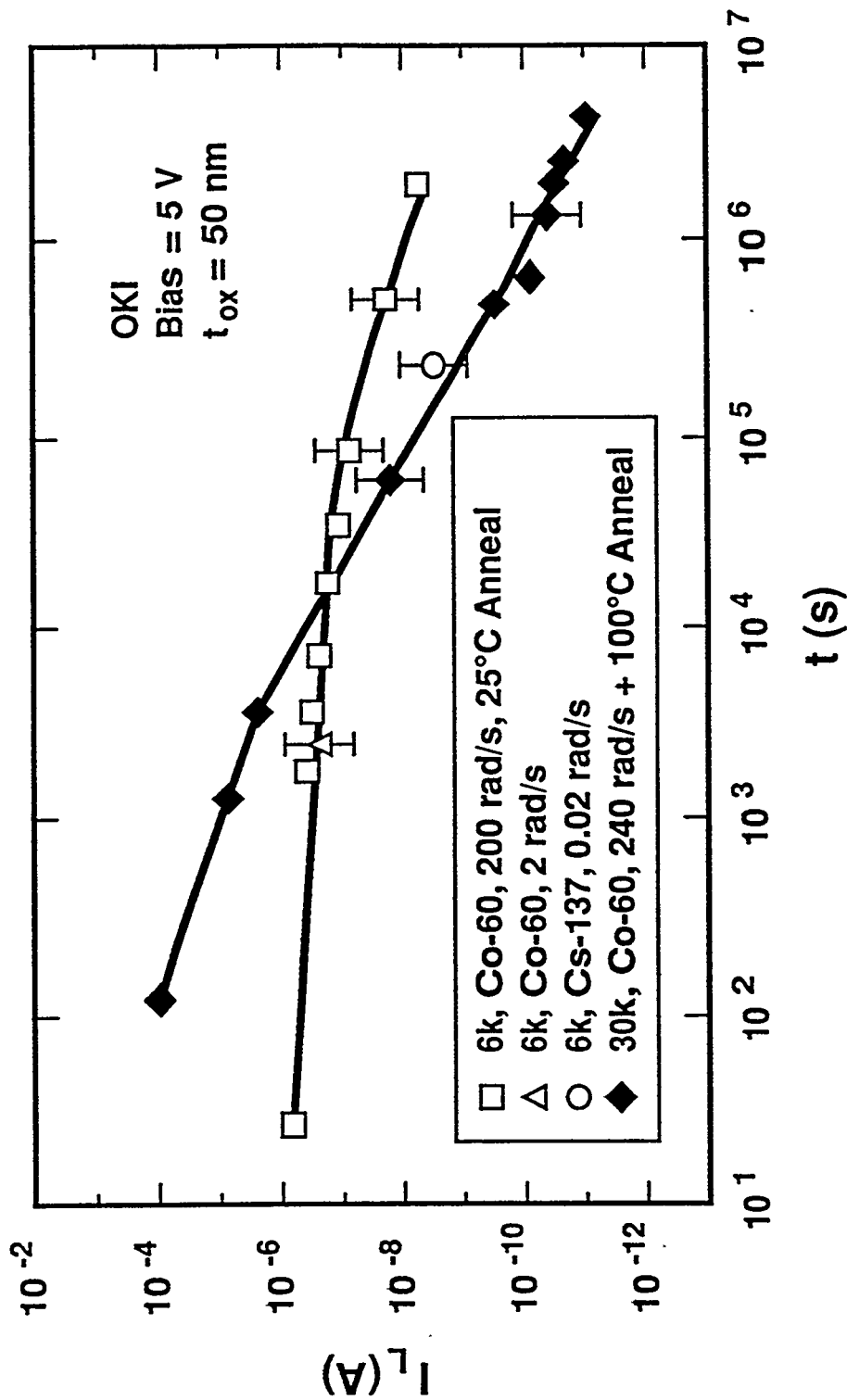
PRESENT MIL-STD-883D, METHOD 1019.4
ADDRESSES SPACE/ACCELERATOR THREATS

Sandia National Laboratories

Accelerator

SPACE

"Rebound"

LAB

1019.4

50

300

WEAPON

Typical Dose Rates (rad(Si)/s)

10^{-6} 10^{-3} 10^{0} 10^{3} 10^{6} 10^{9} 10^{12}
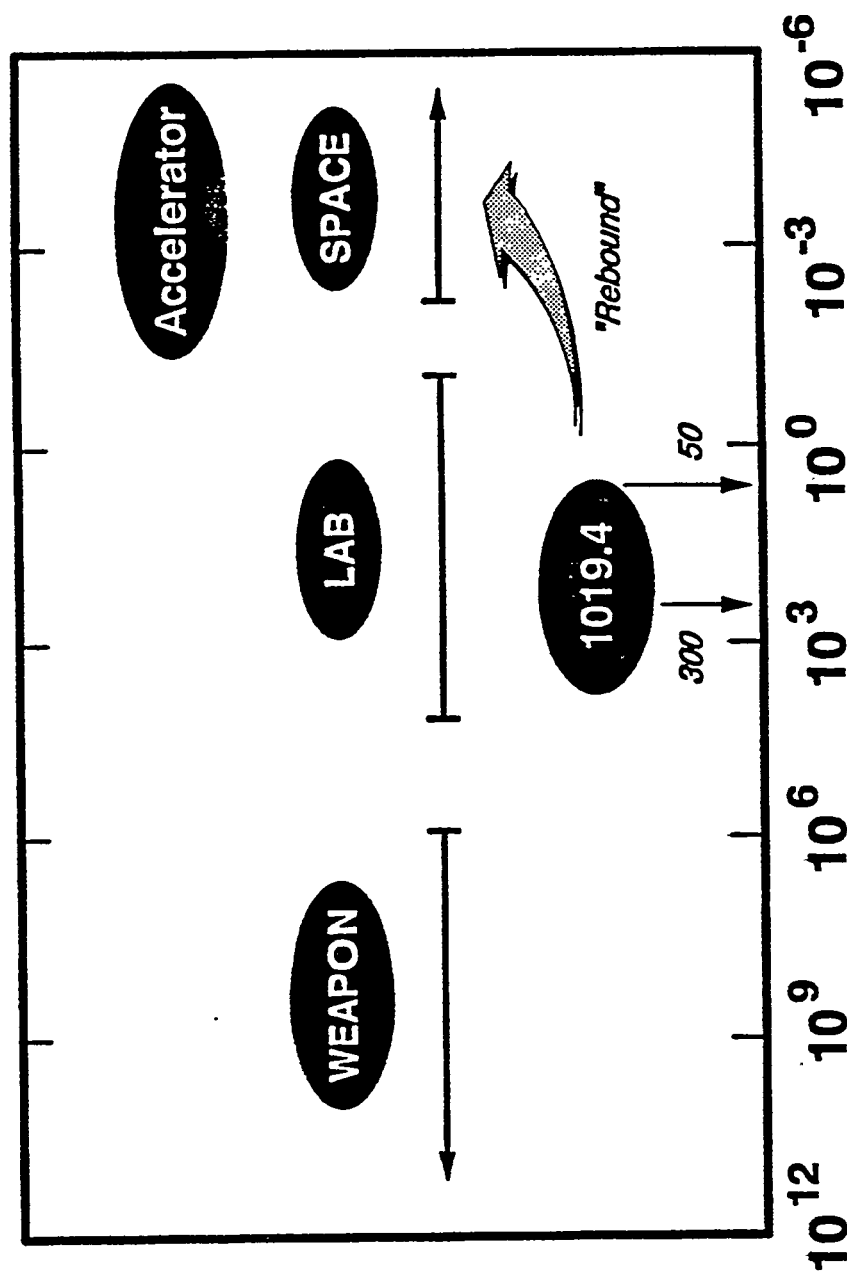
Fig. 17

MIL-STD 883D Method 1019.4 Test Flow

Dose > 5 krad(Si) or TDE Important

```
┌─────────────────────────────┐
│  Irradiate to spec level    │
│   50 - 300 rad(Si)/s        │
└─────────────────────────────┘
              │
              ▼
      ┌─────────────────┐
      │ Electrical Test │
      │     < 2 hr      │
      └─────────────────┘
              │
              ▼
          ◇ Pass ? ◇ ──No──►  ┌──────────┐
                              │  Reject  │
                              │  Parts   │
        Yes                   └──────────┘
              │
              ▼
┌─────────────────────────────┐
│ Irradiate + 50% spec level  │
│   50 - 300 rad(Si)/s        │
└─────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│      Biased Anneal          │
│    168 hr @ 100° C          │
└─────────────────────────────┘
              │
              ▼
      ┌─────────────────┐
      │ Electrical Test │
      │     < 2 hr      │
      └─────────────────┘
              │
              ▼
┌──────────┐          ┌──────────┐
│  Parts   │◄──Yes── ◇ Pass ? ◇ ──No──► │  Reject  │
│   OK     │                            │  Parts   │
└──────────┘                            └──────────┘
```
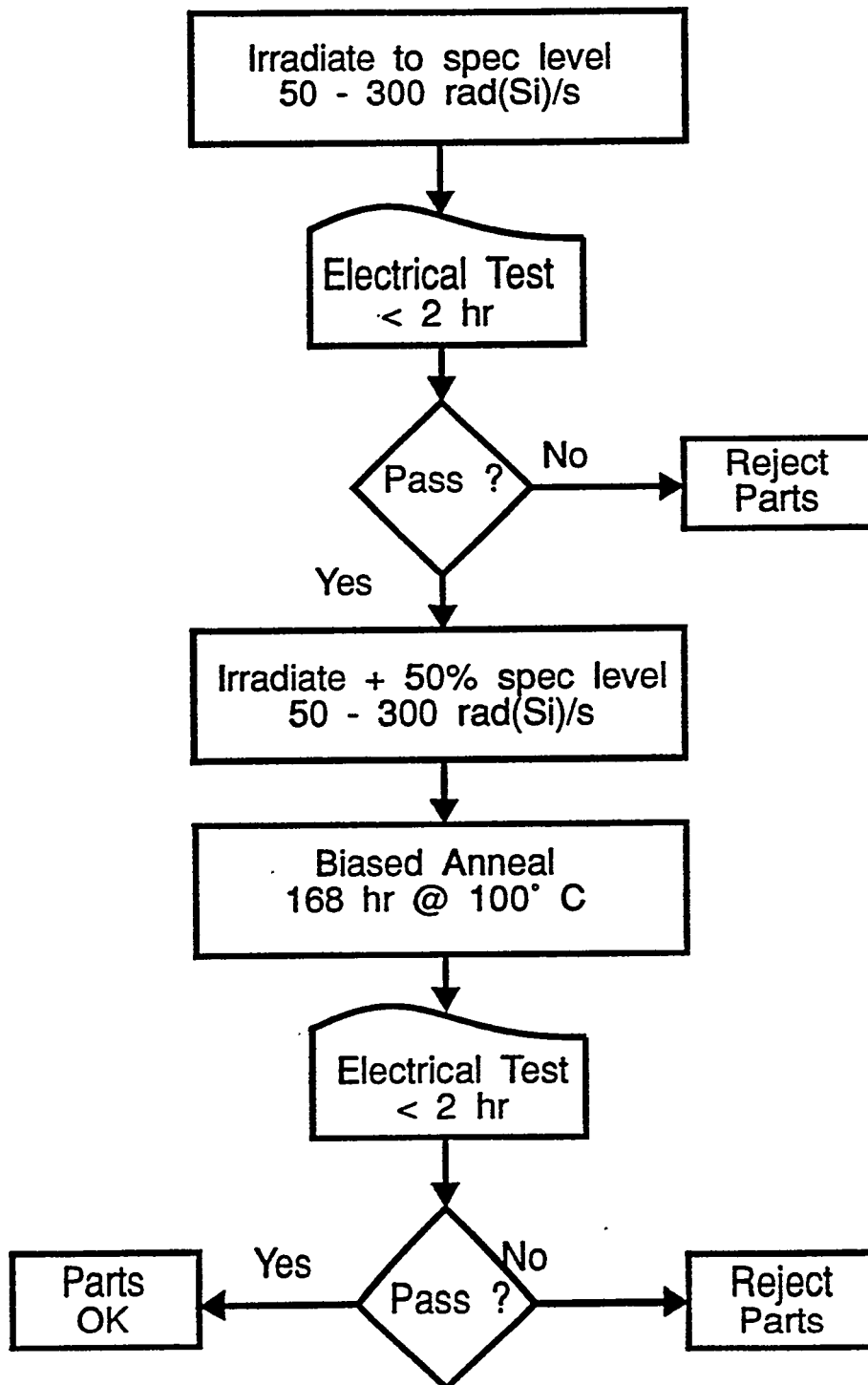
Fig 18

N-CHANNEL THRESHOLD
VOLTAGE SHIFT vs RADIATION and ANNEAL

G1916A/W22   Co-60 (1.0 Mrad SiO_2)

t_{ox}=320Å

Fig. 19

DMF 1/87

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Fig. 20

50 kHz

0 V

10 V

Co-60
19.6 krad (SiO₂)/min
48 nm OXIDE

DOSE [Mrad (SiO₂)]

$\Delta V_{th}(V)$
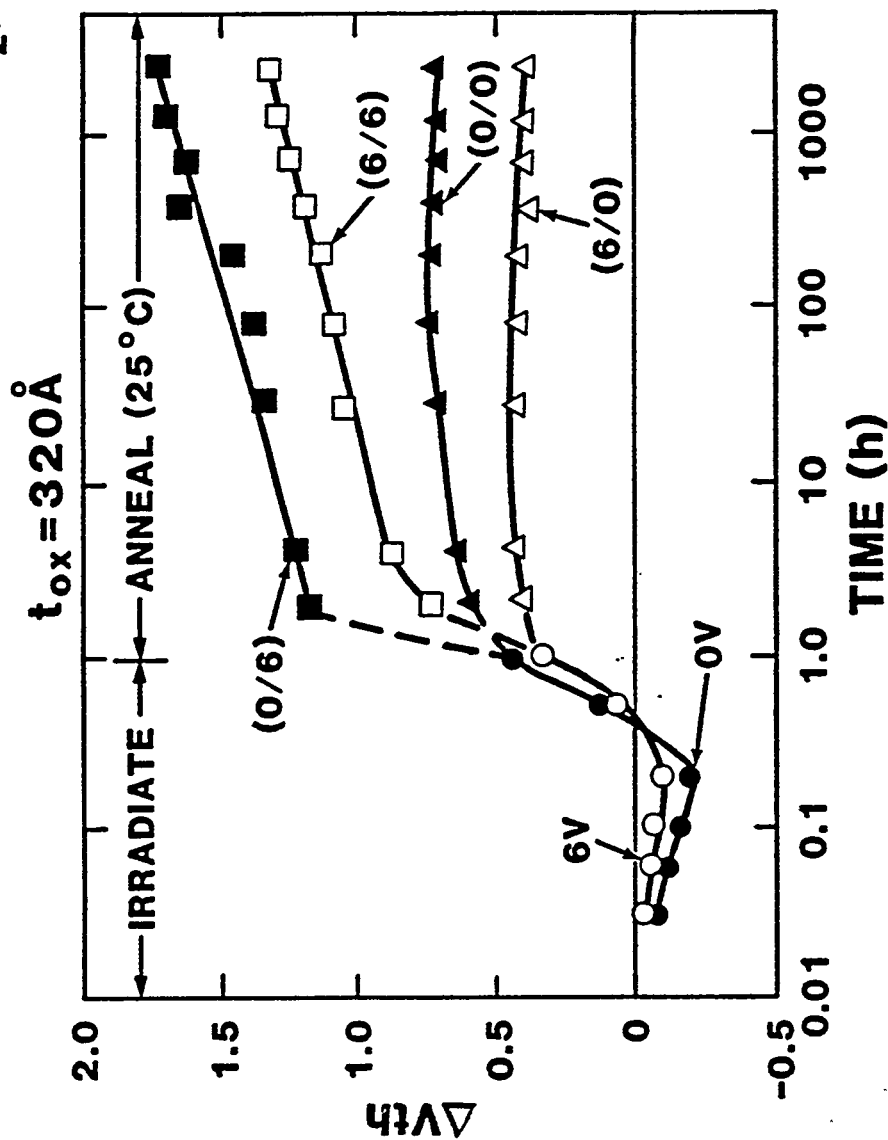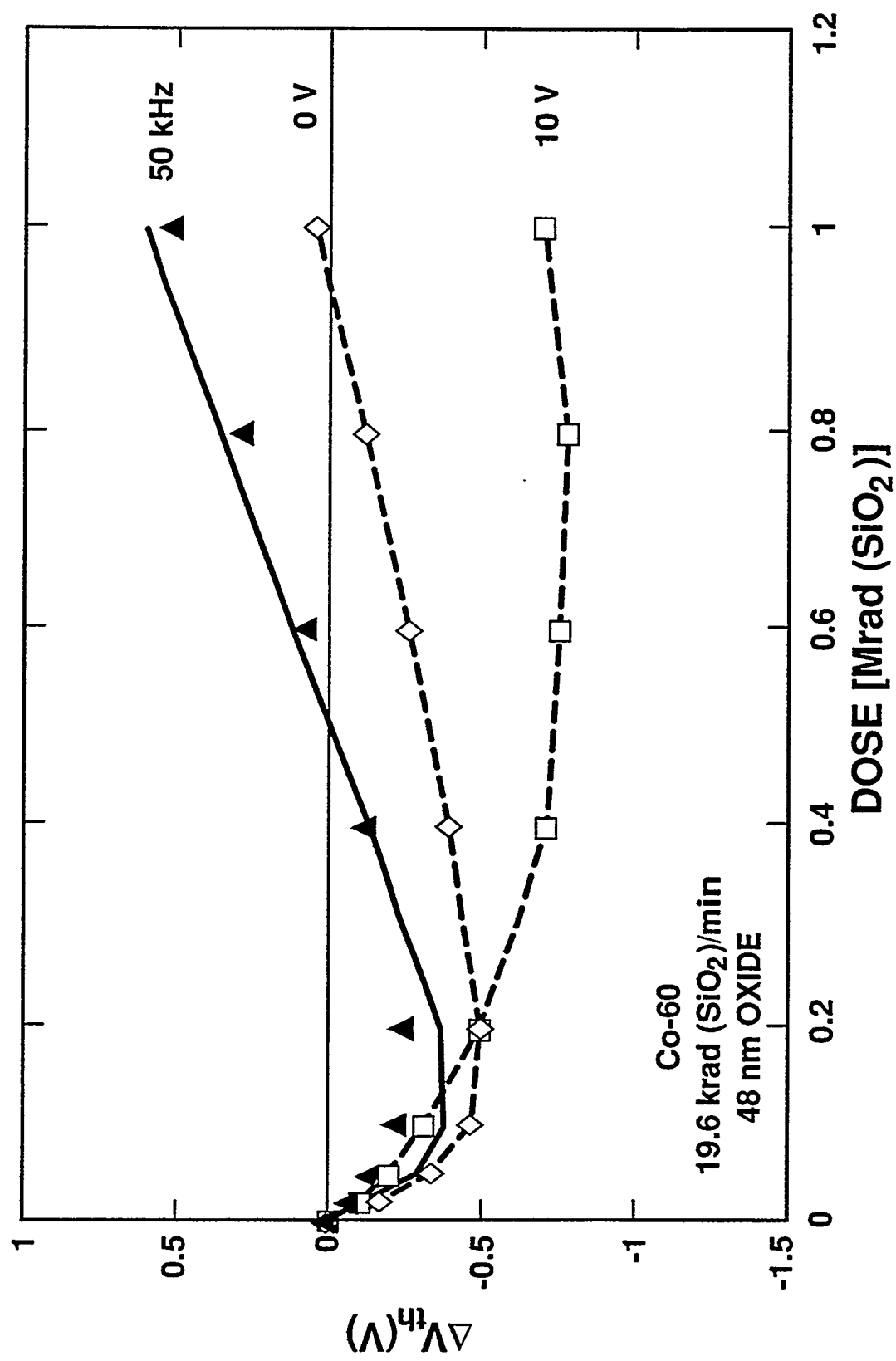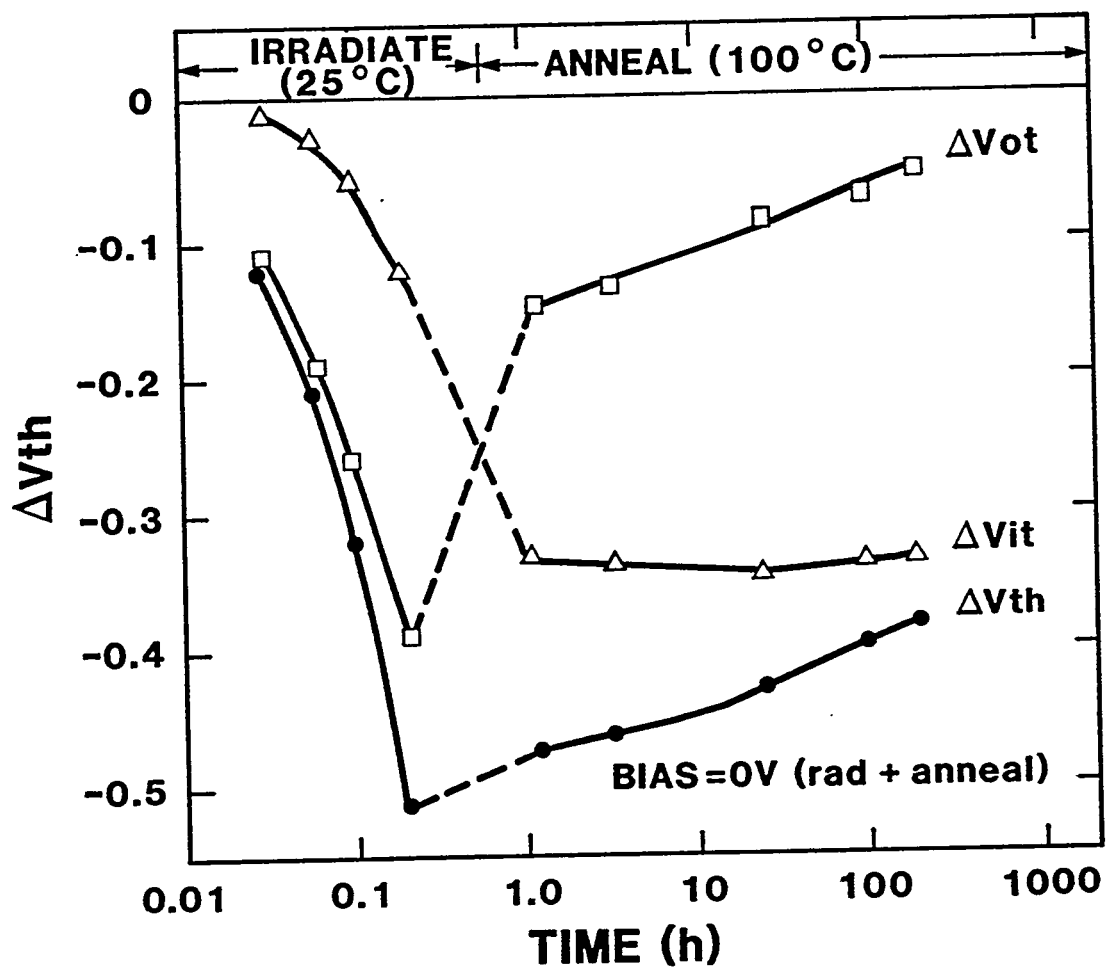
Fig. 21

ΔVit vs RADIATION and ANNEAL (N-Channel)

G1916A/W22 Co-60 (200 krad SiO_2)

t_{ox} = 320Å

RAD 25°C

ANNEAL (100°C)

(0/6)
(6/6)
(0/0)
(6/0)

6V

0V

ΔVit (V)

1.0   0.8   0.6   0.4   0.2   0

TIME (h)

0.01   0.1   1.0   10   100   1000
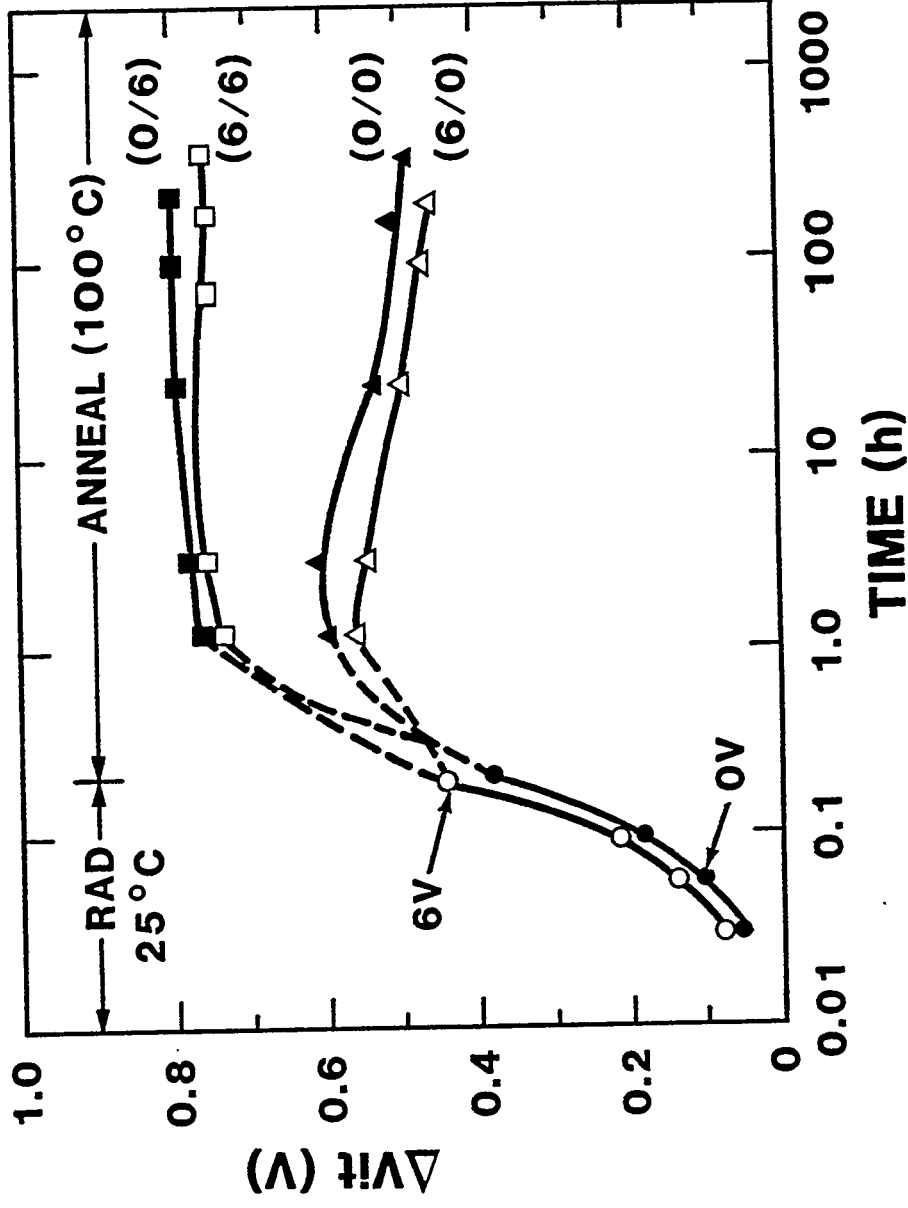
Fig. 22

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READ ACCESS TIME VERSUS DOSE

t_{ox} = 31 nm
V_{DD} = 5 V
0.2 rad (SiO_2)/s
Cs - 137

Rebound
Overtest

Rebound
Overtest

SA3240
16 k SRAM

400

300

200

100

t_{rd}, ns

0
PRE

0.1

1

10

Dose, Mrad(SiO_2)
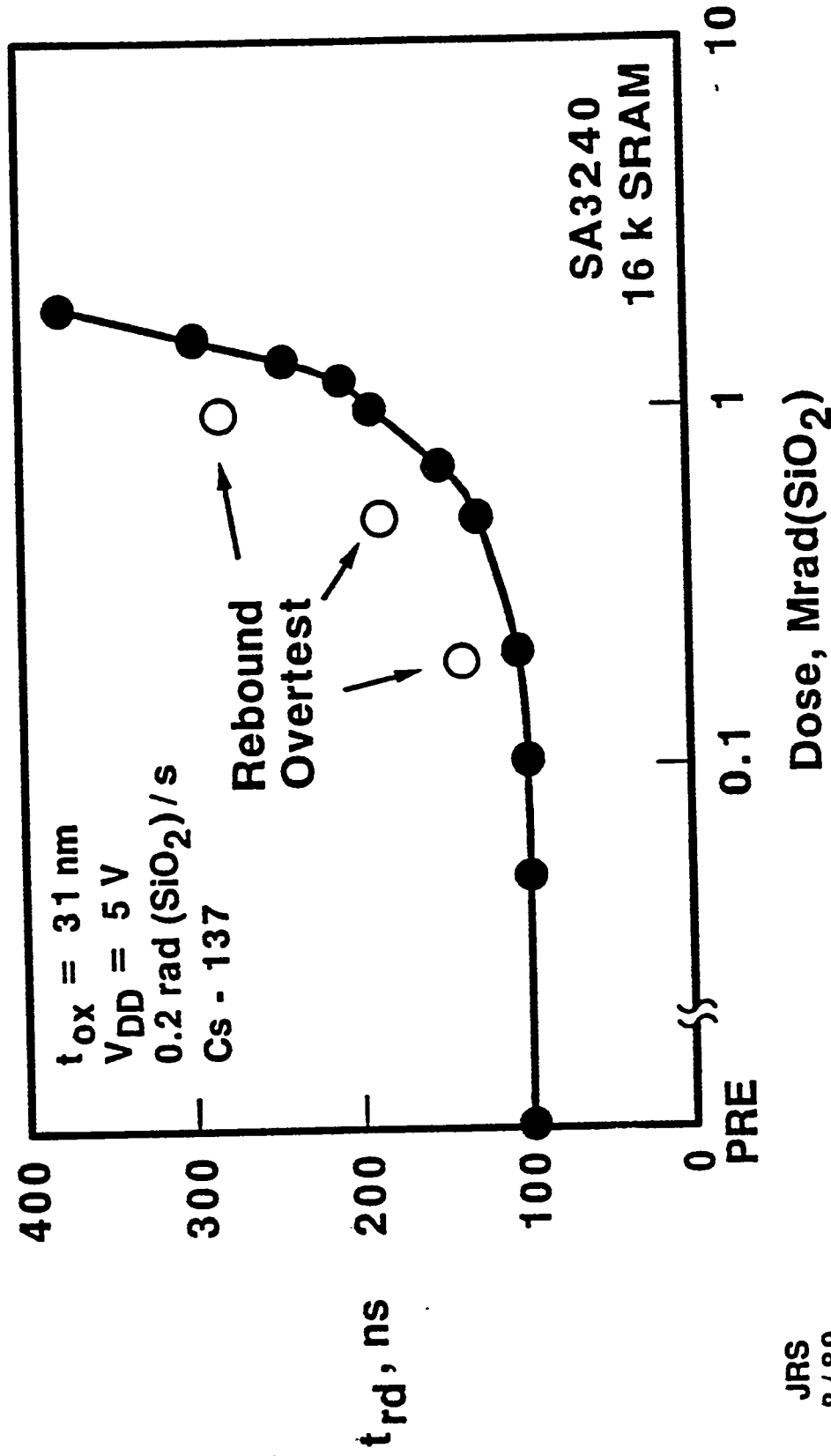
Fig. 23

JRS
8/89

89N2000.40

PROJECTED MAXIMUM REBOUND VOLTAGE
20% Interface-Trap Generation Efficiency

$$\Delta V_{it}(V) = (q/\epsilon_{ox}) K_g\, f_y\, D\, (t_{ox})^2\, f_{it}$$

80% Charge Yield

MAX POSITIVE N-ch $\Delta V_{th}(V)$

DOSE [krad(SiO$_2$)]

100 nm

50 nm

20 nm

10 3 1 0.3 0.1 0.03 0.01
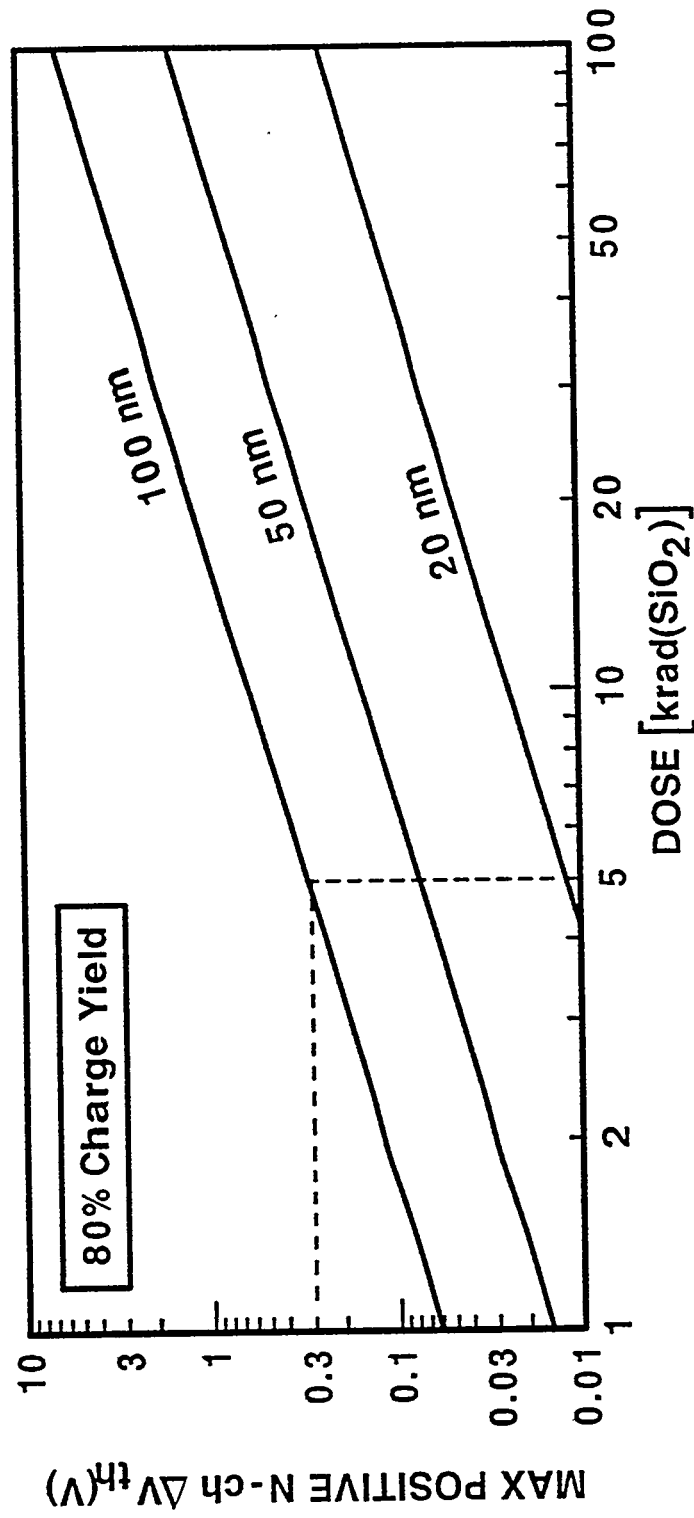
1 2 5 10 20 50 100

After McGarrity, IEEE Trans. Nucl. Sci. 27, 1739 (1980)

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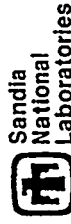
Fig. 24

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91B2000.30

Failure Dose Depends Differently on Dose Rate for Commercial Devices Parts Fail Due to Oxide Charge

OKI 81C55

SGS4007

HM6504

1019

Failure Dose [krad(Si)]

Dose Rate [rad(Si)/s]
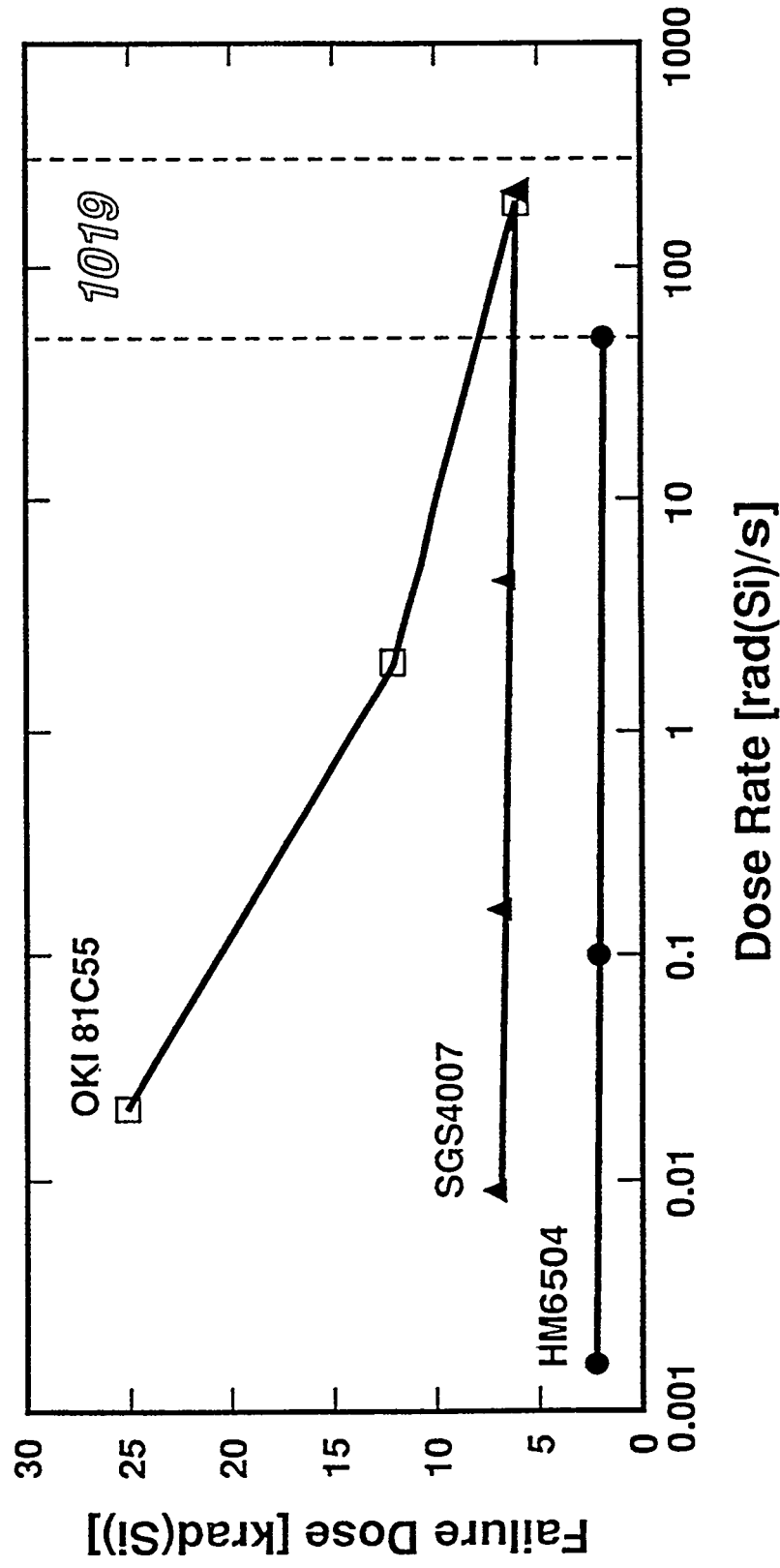
Fig. 25

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Albuquerque, New Mexico

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Annealing Rates Vary Widely For Commercial 4007s
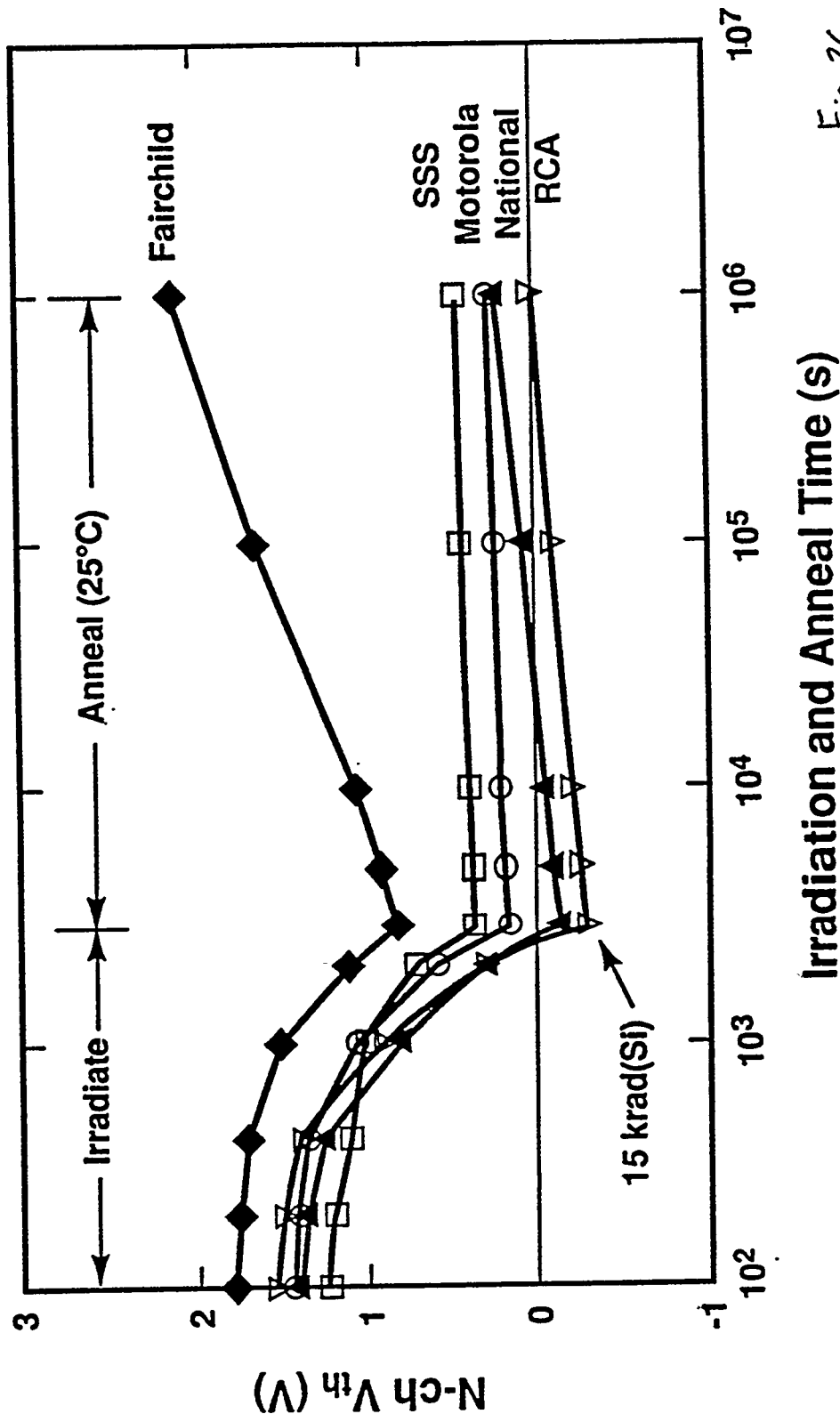
N-ch V_{th} (V)

Irradiation and Anneal Time (s)

Fairchild

SSS
Motorola
National
RCA

Anneal (25°C)

Irradiate

15 krad(Si)

Fig. 26

Sandia National Laboratories
Albuquerque, New Mexico

PSW 7/83

ROOM-TEMPERATURE ANNEAL vs. LOW DOSE
RATE RESPONSE FOR VARYING ANNEAL RATES

Based on Linear Response Analysis

Low Dose Rate

A: 5% per decade
B: 10% per decade
C: 15% per decade

Co-60 + RT Anneal

30 yr   1 wk   1 dy   1 hr

TIME (Seconds)

GATE OX V_{th}(V)

FIELD OX V_{th}(V)

Fig. 27

Sandia
National
Laboratories
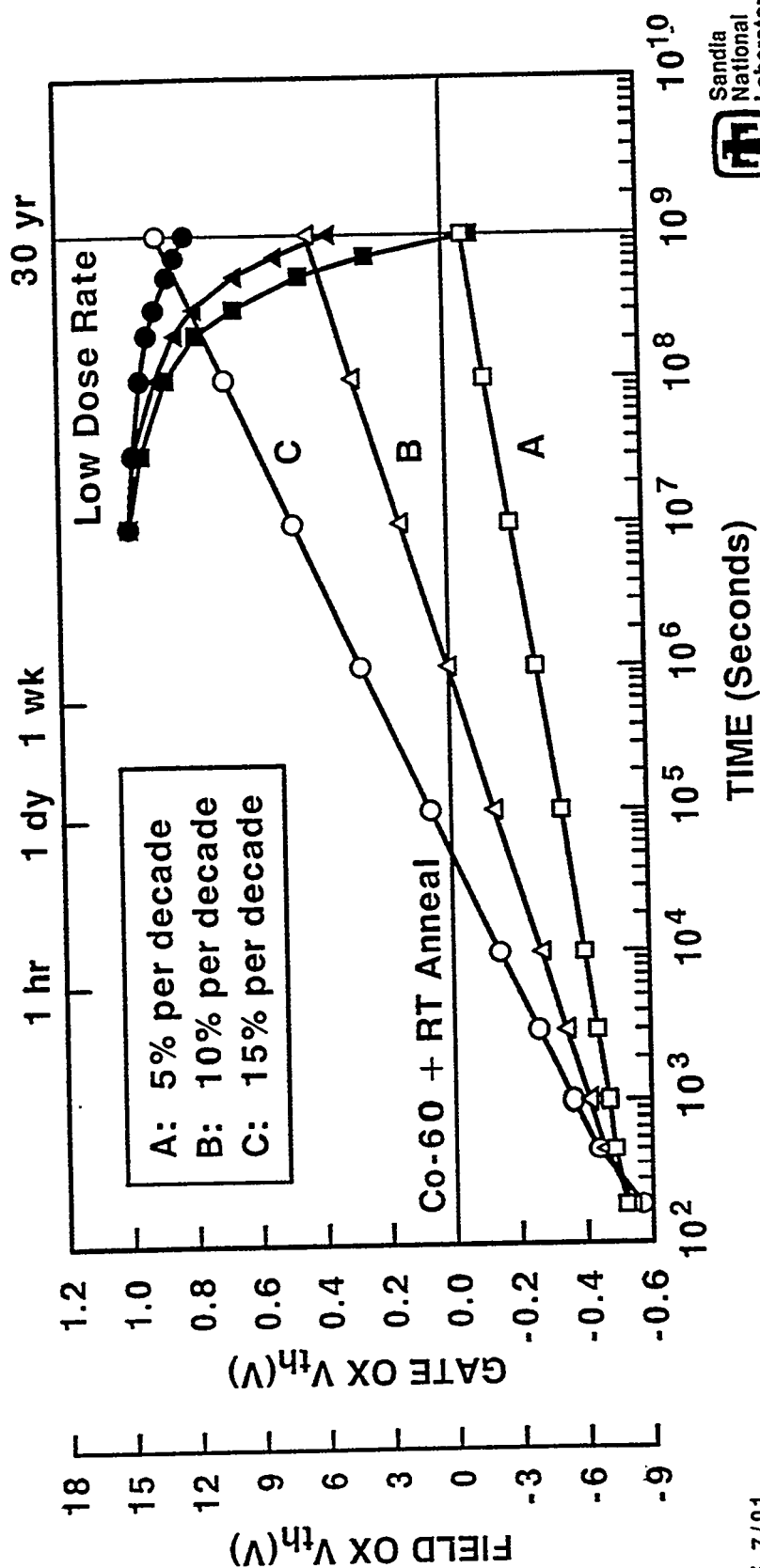
DMF 7/91
91B2000.36

Amount by Which Co-60 Rad. + RT Ann'l Overpredicts Low Dose Rate V_{th} due to Hole Trapping vs. Annealing Rate

Linear Response Analysis
V_{th} Shifts due to N_{ot}
MOS devices

1-mi Ann'l
1-hr Ann'l
1-dy Ann'l
1-wk Ann'l

Amount of Overprediction

Annealing Rate (per decade of time)

Fig. 2g
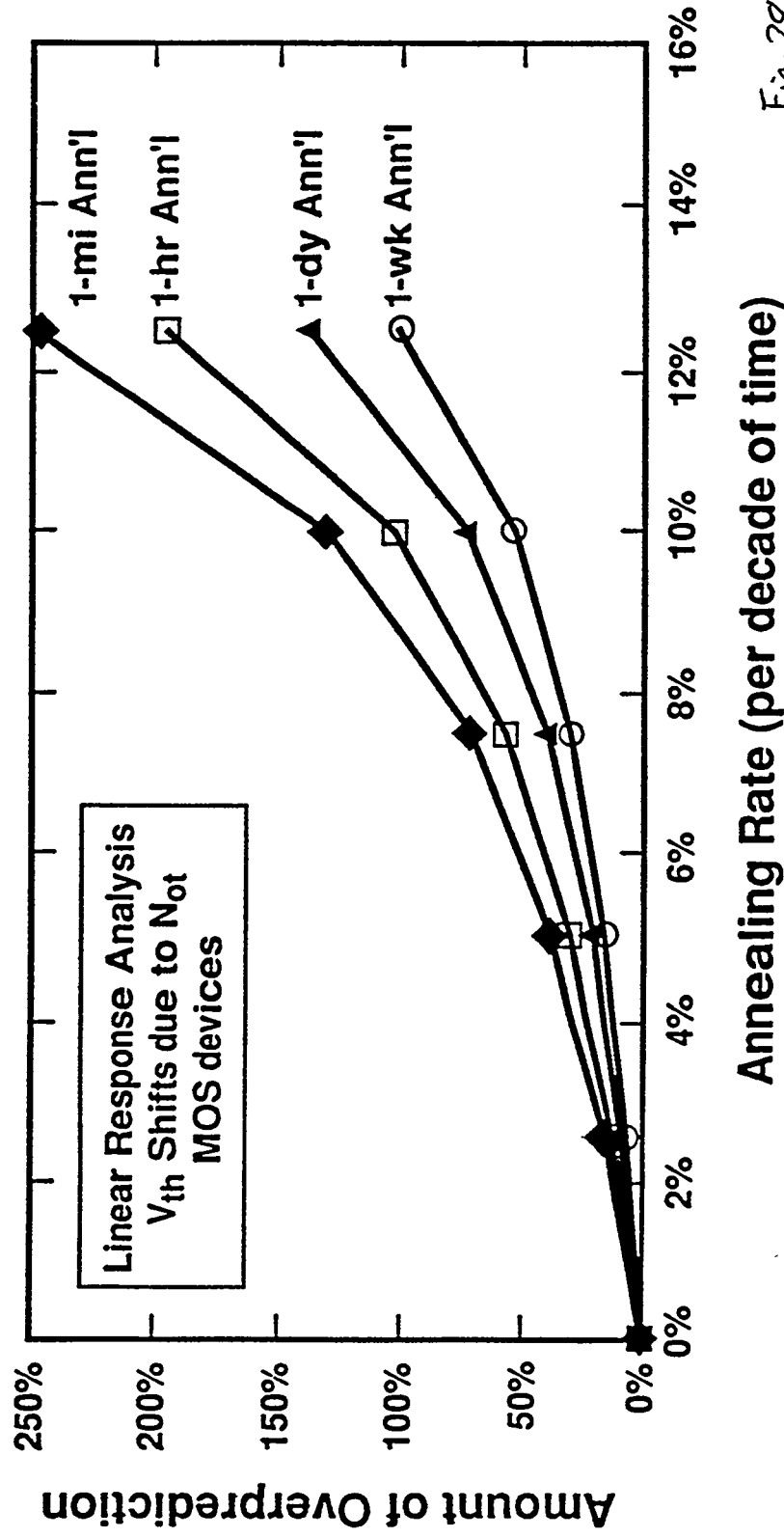
Sandia National Laboratories
Albuquerque, New Mexico

DMF 2/91

TEST FLOW FOR HIGHER DOSE SYSTEMS
Illustrative Example

Dose > 5 krad
* or *
Gate Ox > 100 nm

Co-60 Rad & Test
50-300 rad(Si)/s

PASS

Rebound Test
per 1019.4

FAIL

OPTION TO
CONTINUE

Room-Temperature
Anneal & Test

FAIL

FAIL

Duration < (Spec Dose)/Max System Rate

PASS

Rebound Test per 1019.4

Fig. 29

80
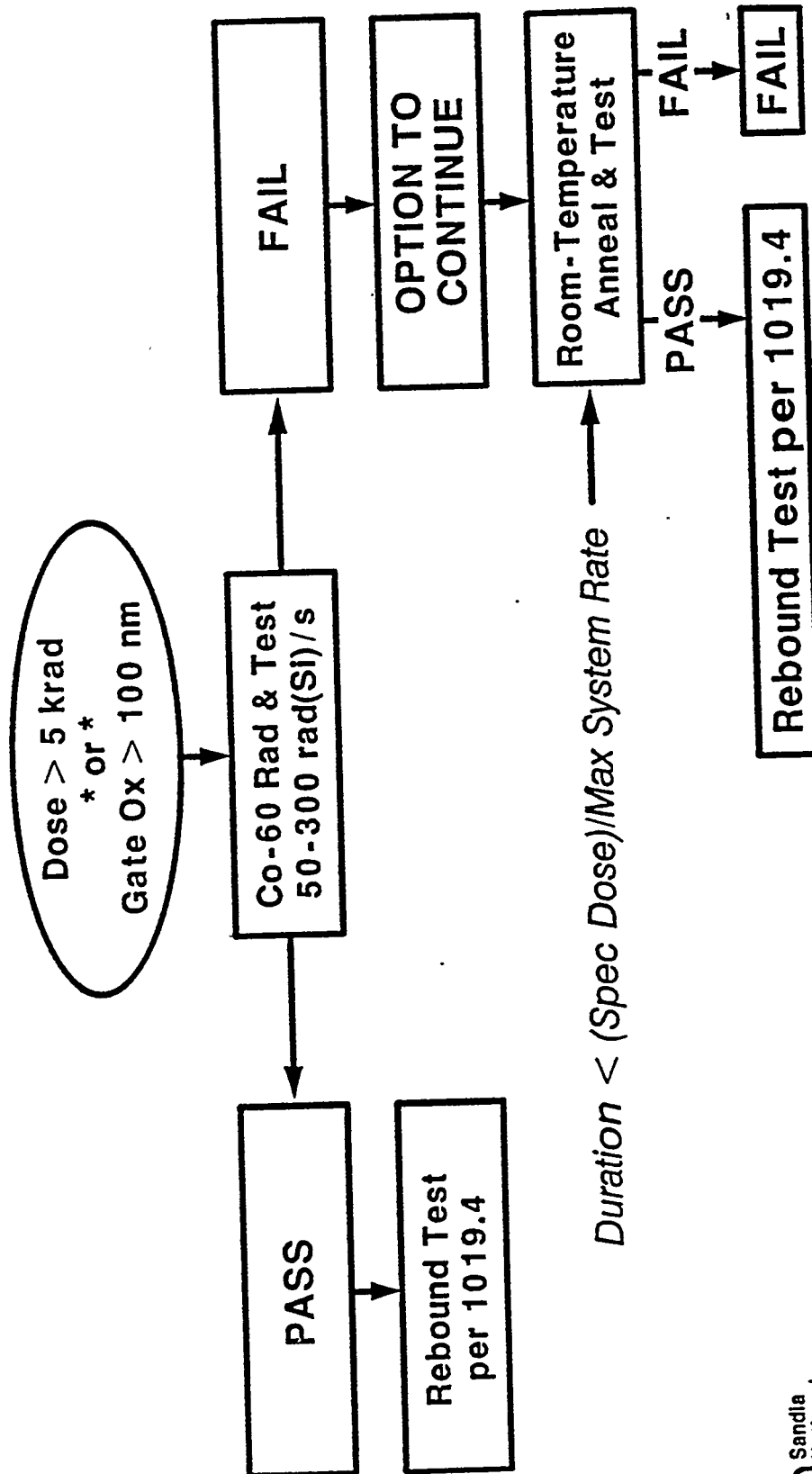
Dose Rate Dependence of Field Oxide Induced IC Leakage Current

Fig. 30

CHARGE YIELD FOR 10-keV X-RAY

Legend:
- ○ Benedetto and Boesch (1986)*
- ◇ Dozier and Brown (1980)*
- ▨ 47.5 nm oxide
- ▨ 60 nm oxide
- ■ 105 nm oxide
- ▨ 350 nm oxide

X-axis: E_{ox} (MV/CM)

Y-axis: Fraction of Unrecombined Holes
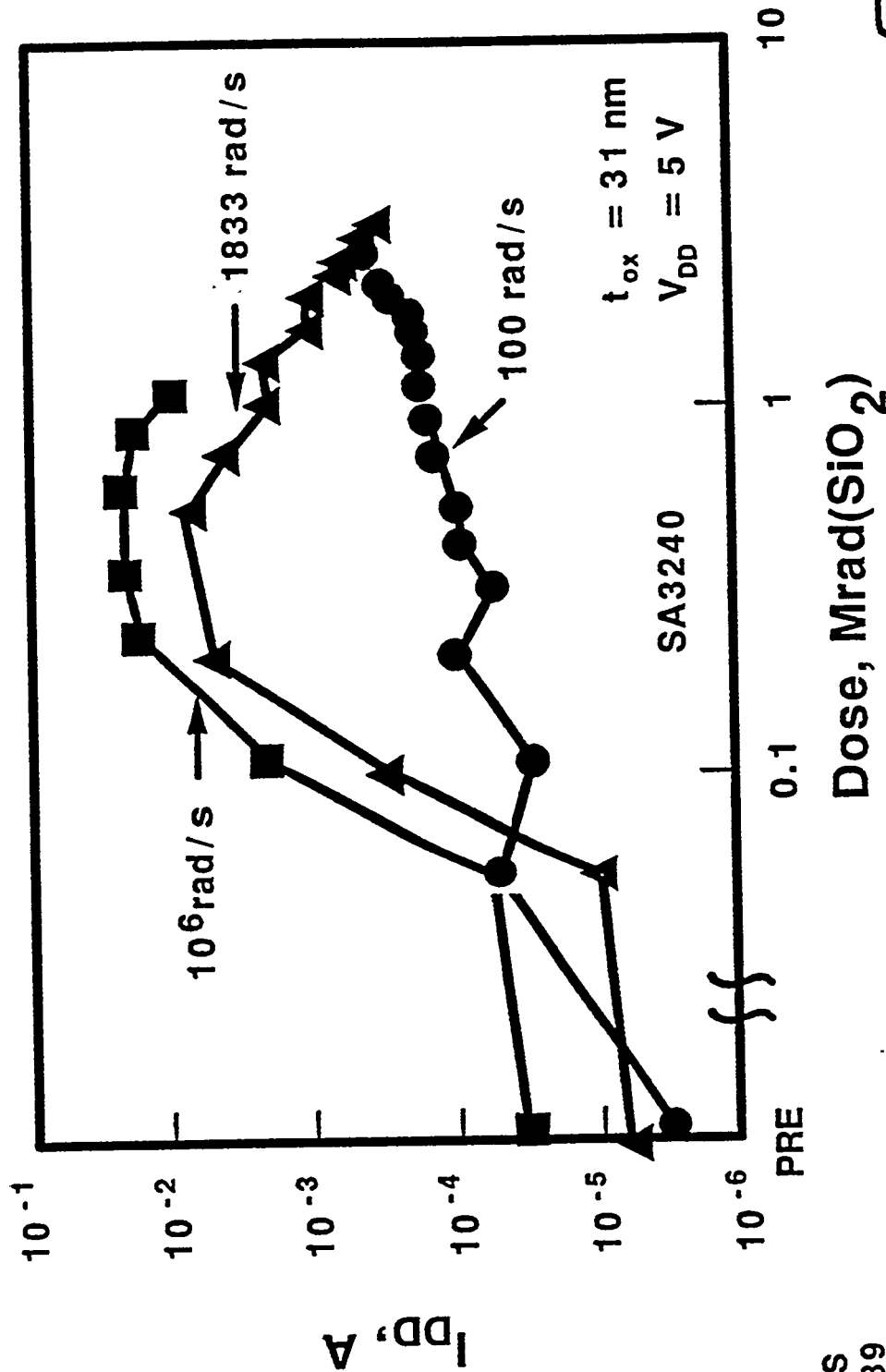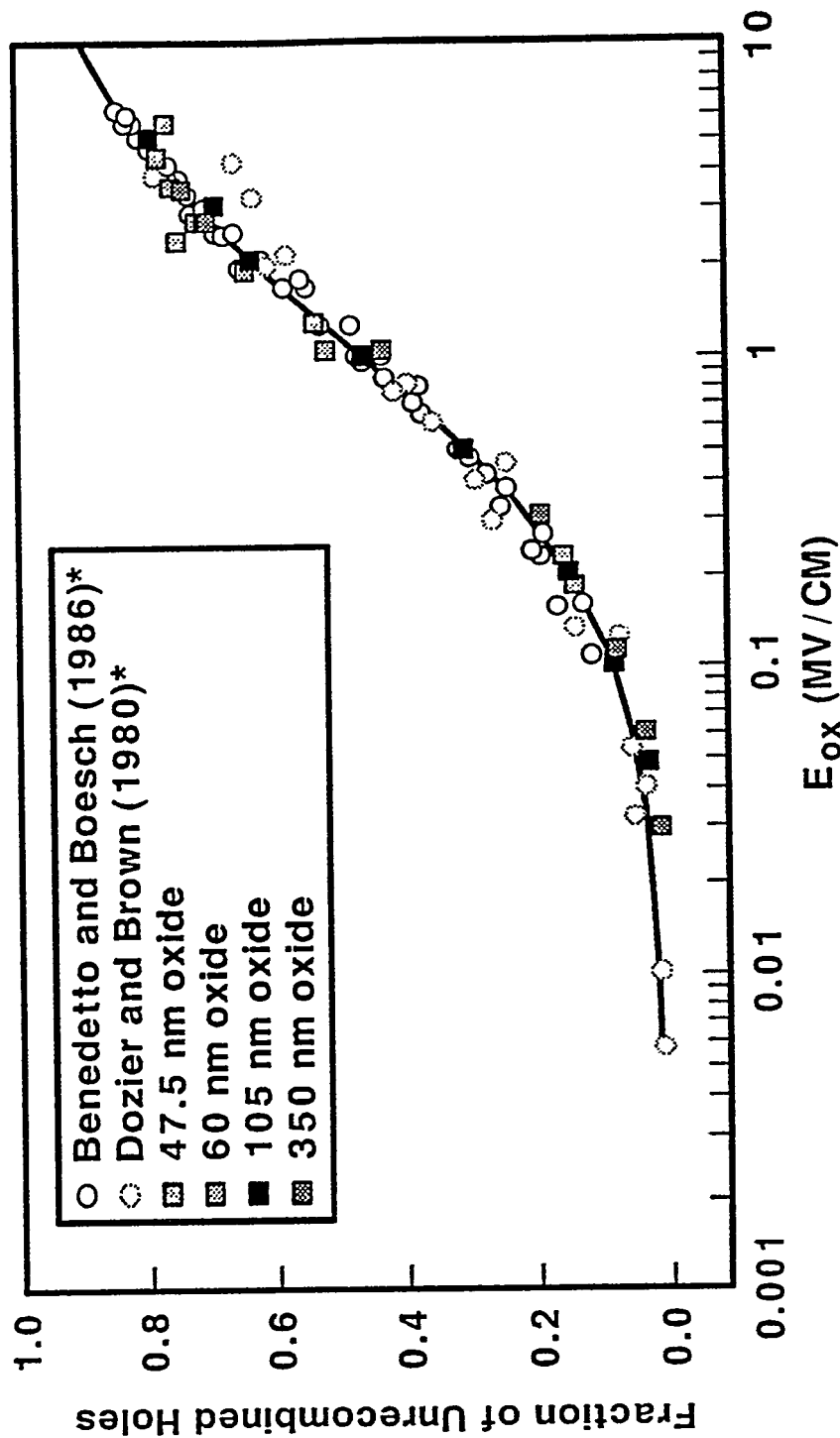
*After C. M. Dozier et al., IEEE Trans. Nucl. Sci. NS-34, 1535 (1987)

Fig. 31

Sandia National Laboratories
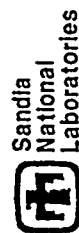
LOW-TEMPERATURE CHARGE YIELD FACTORS OF SROUR AND CHIU AGREE WITH THIS WORK

Srour and Chiu (1977)
- ■ 91 nm oxide

This Work
- 47.5 nm oxide
- 60 nm oxide
- 105 nm oxide
- 350 nm oxide

Fraction of Unrecombined Holes

E_{ox} (MV/cm)

Fig. 32

83
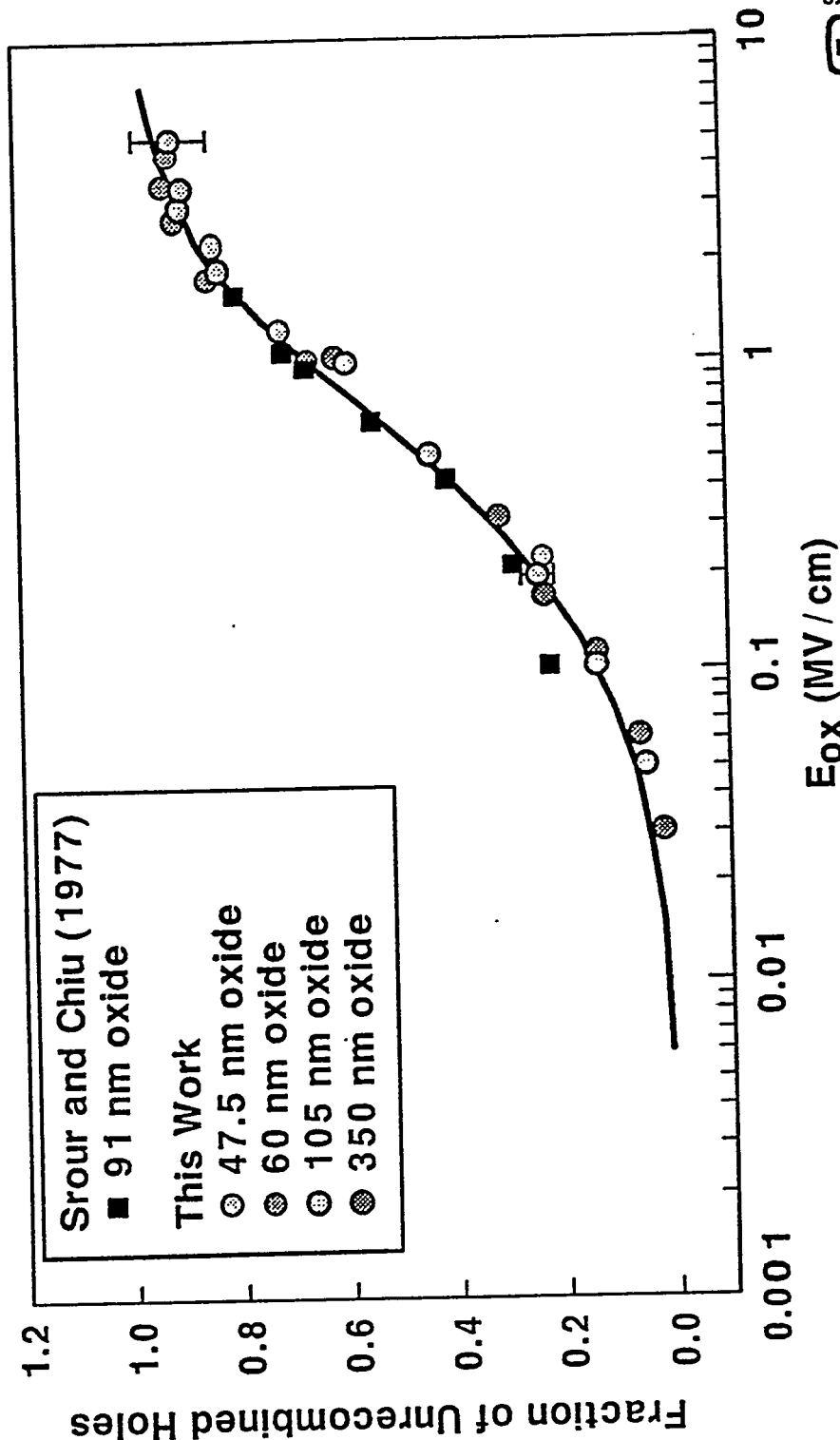
RATIO OF 10-keV X-RAY TO Co-60 OXIDE-TRAPPED CHARGE

Fig. 33

E_{ox} (MV/cm)

ΔV_{ot} (X-ray)/ΔV_{ot} (Co-60)

DEF = 1.4

DEF = 1.0

○ t_{ox} = 105 nm Poly Gate
● t_{ox} = 350 nm Metal Gate

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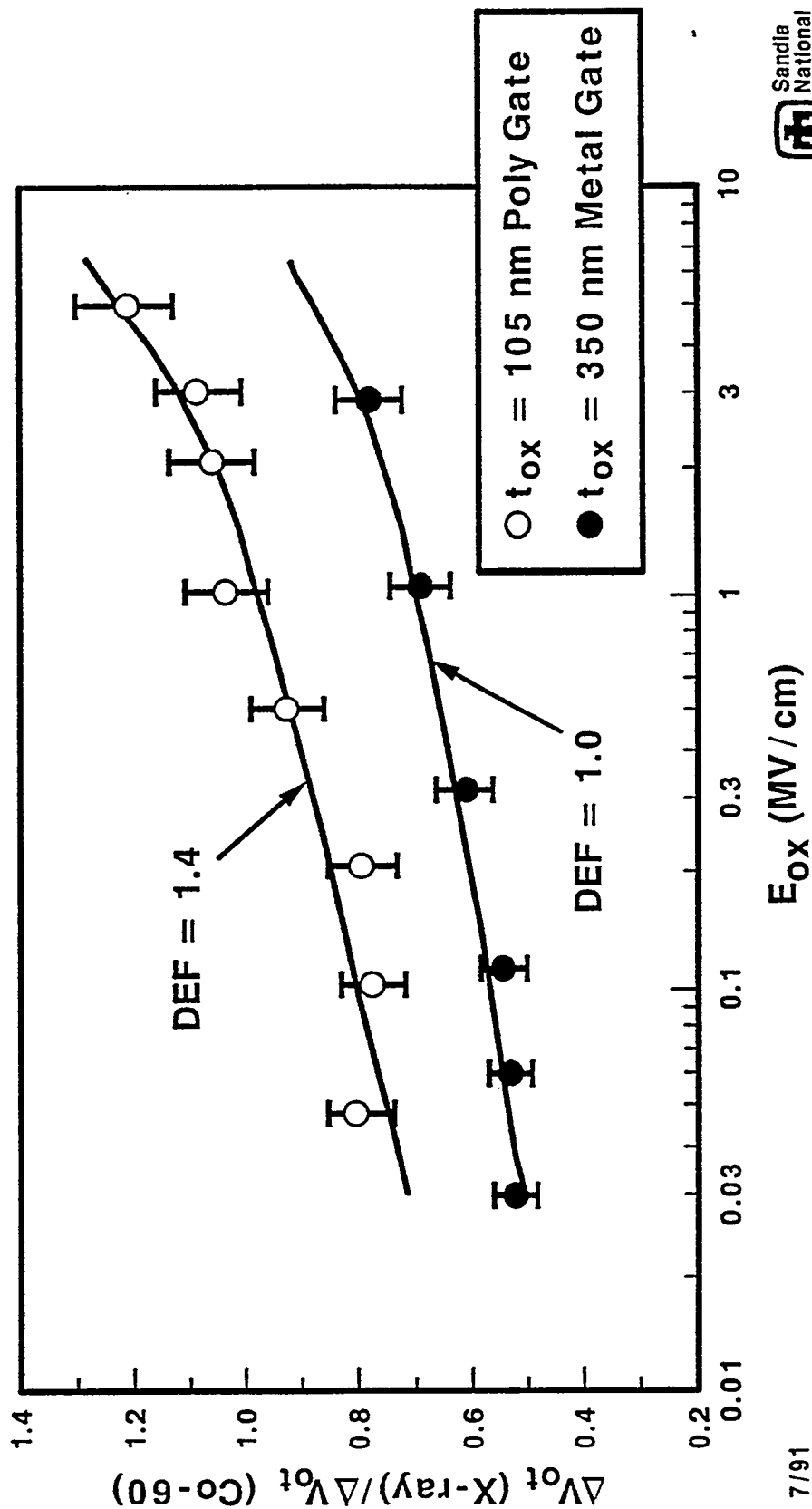
FACTORS DETERMINING "WORST-CASE" RADIATION BIAS
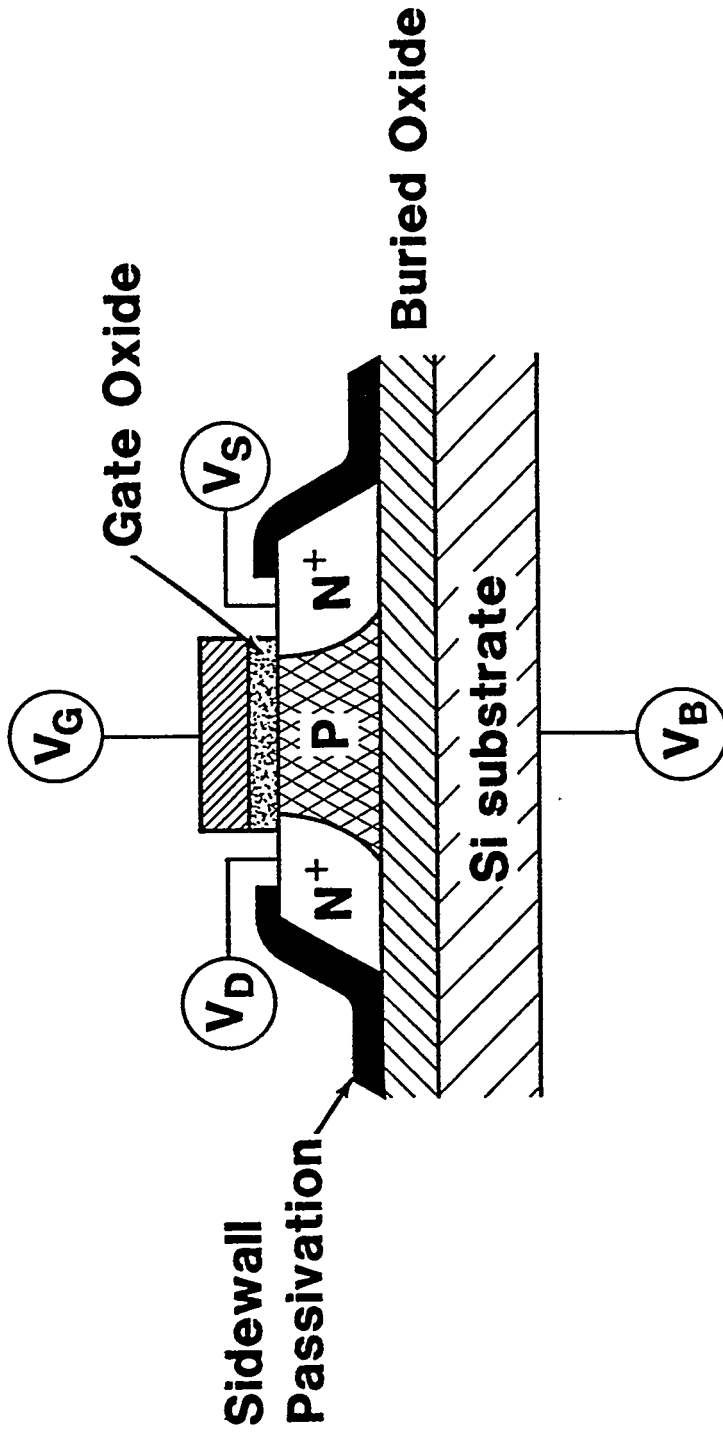
Fig. 34

1. Three SOI insulators, with different thicknesses, that vary for different technologies.

2. V_G, V_D, V_S, V_B (floating body)

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BACK–GATE Vth vs DOSE
SIMOX ($t_{ox} \cong 4000$ Å)

X-Ray

Co–60

DOSE [krad (SiO_2)]

$V_{BG} = 0$ V
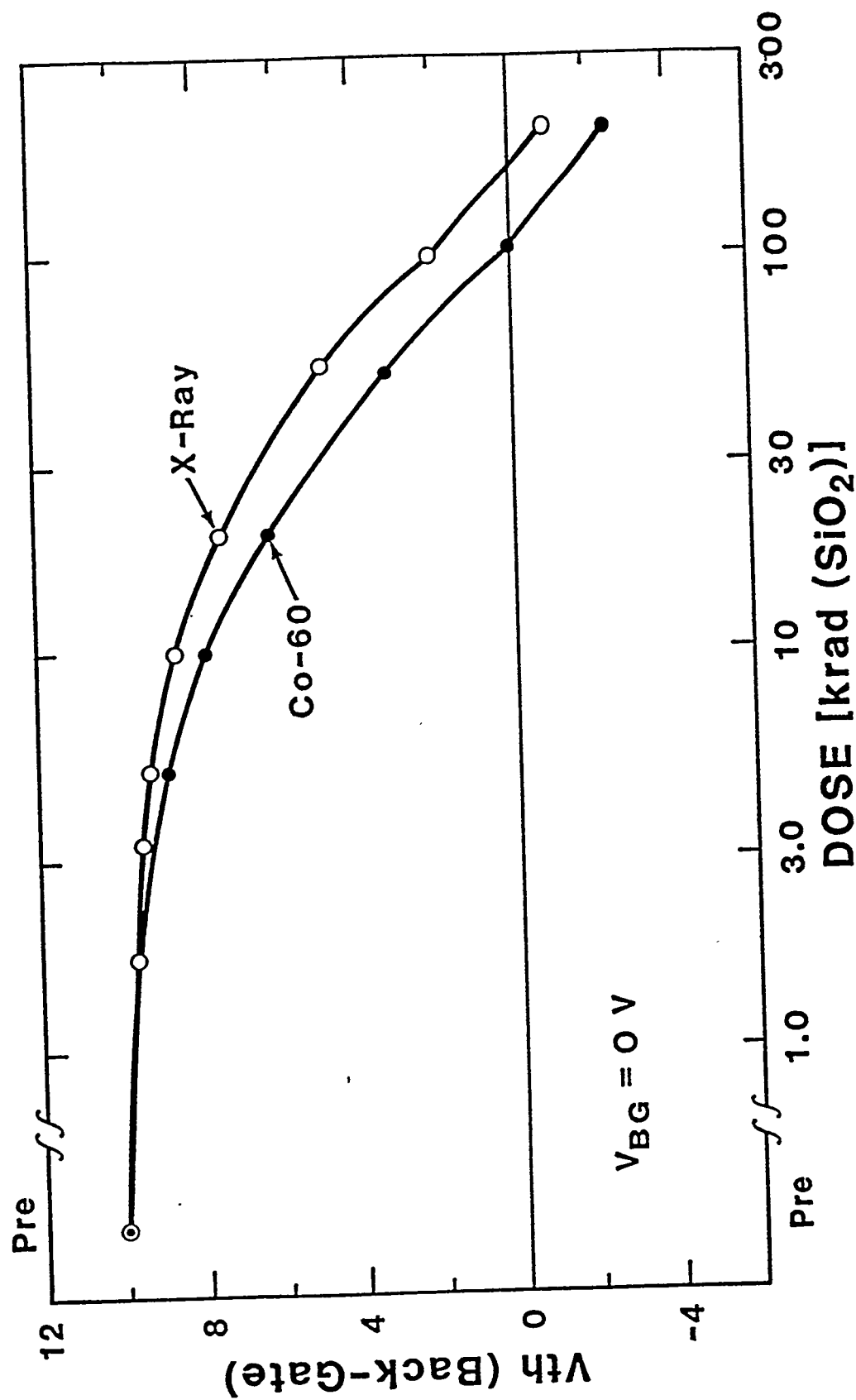
Vth (Back-Gate)

Fig. 35

DMF 11/87

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BACK-GATE Vth vs DOSE
ZMR ($t_{ox} \cong 20,000\text{Å}$)

X-Ray

Co-60

$V_{BG} = 0$ V

Pre

DOSE [krad (SiO_2)]

Vth (Back-Gate)

Pre
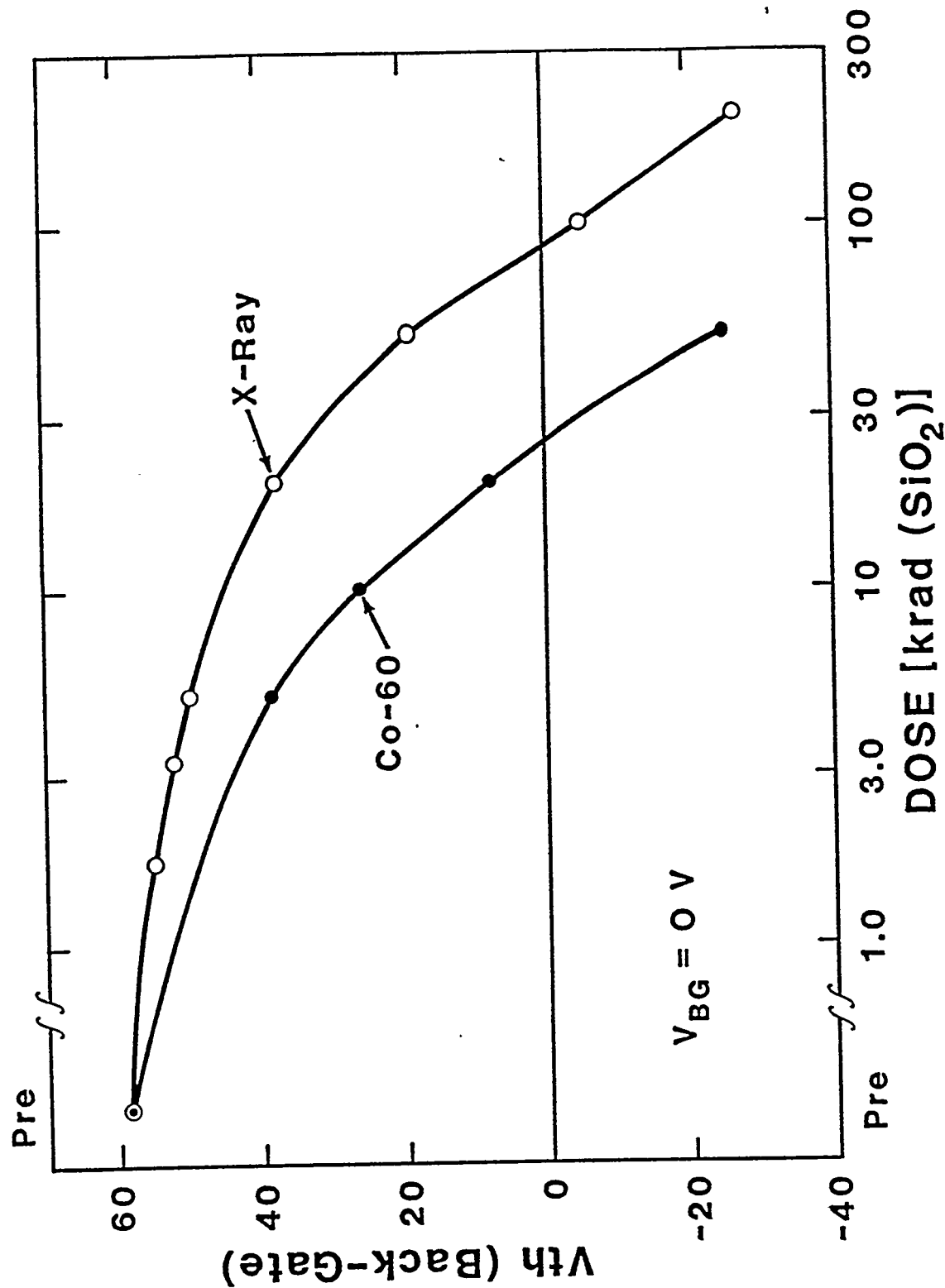
Fig. 36

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87

EXAMPLE: "STRATEGIC" APPLICATION
X-RAY EXPOSURE AT DOSE RATE $\gtrsim$ 2000 rad (SiO$_2$)/s
to 2-3 TIMES SYSTEM SPECIFICATION

(Pass/Fail)

LINAC, 1 Pulse, 6x10^9 rad/s

50 krad

Equal $\triangle$Vth

X-ray, 5550 rad (SiO$_2$)/s

100 krad

$\triangle$Vth (V)

0.8   0.4   0   -0.4   -0.8   -1.2   -1.6

TIME (sec)

10^{-4} 10^{-3} 10^{-2} 10^{-1} 10^0 10^1 10^2 10^3 10^4 10^5

88H2000.49

Fig. 37

88

Fig. 32
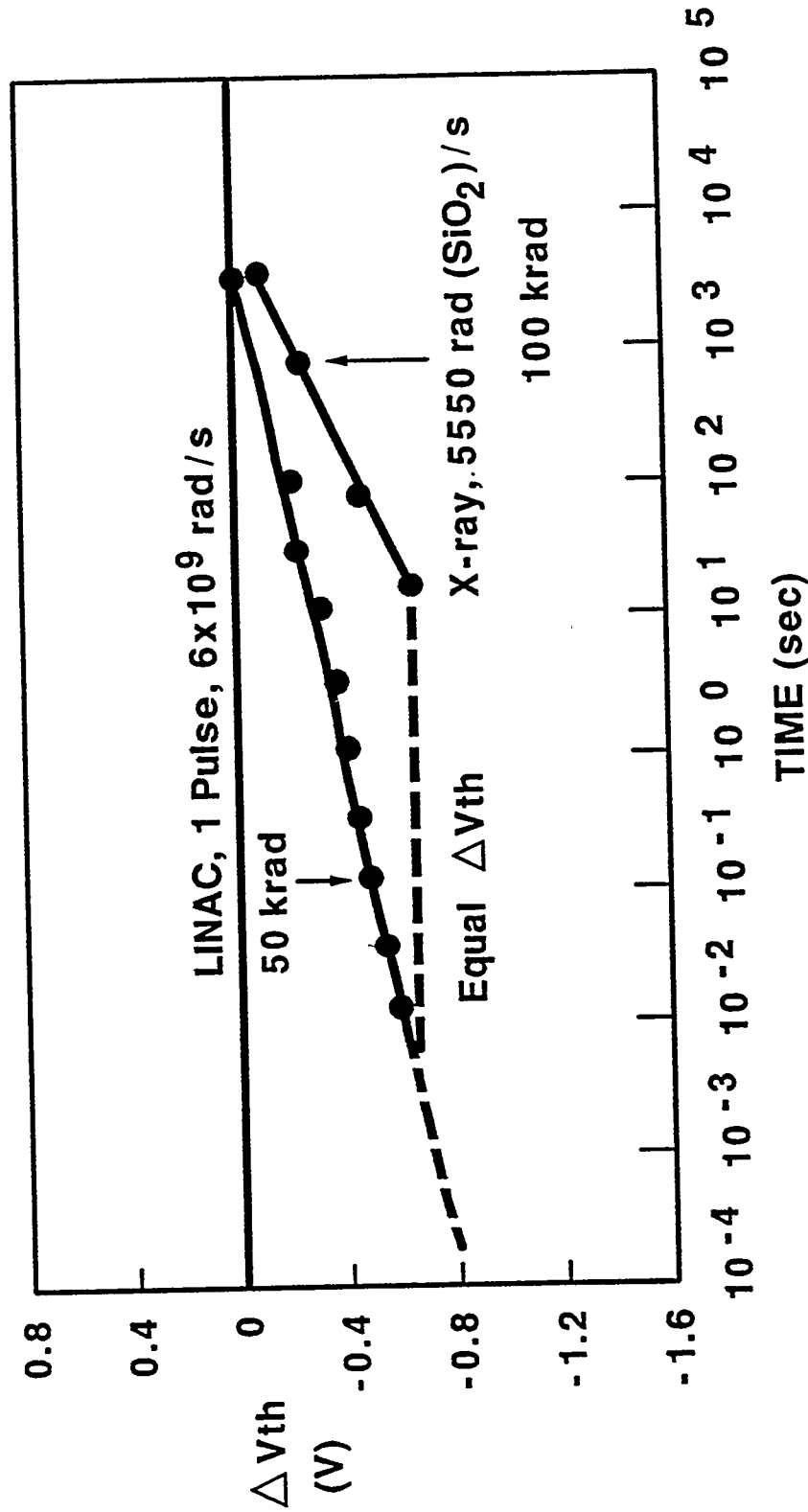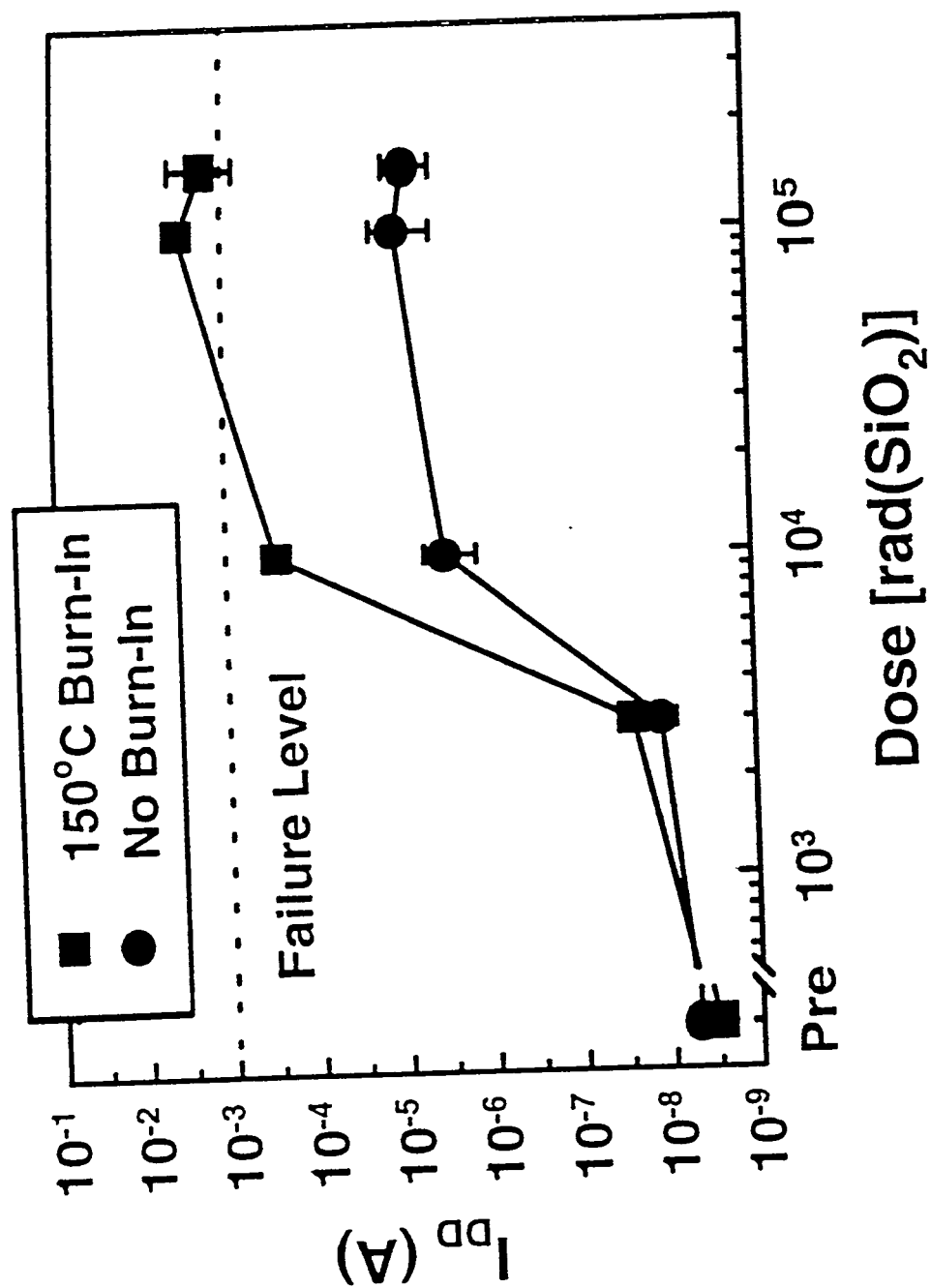
LEAKAGE CURRENTS IN BIPOLAR DEVICE STRUCTURE

N+

P BASE

N EPITAXIAL

② COLLECTOR TO EMITTER CHANNELING ON WALLED EMITTERS

N+ BURIED LAYER

RECESSED FIELD OXIDE

P+

INCREASED SIDEWALL CURRENTS

③

P SUBSTRATE

① BURIED LAYER TO BURIED LAYER CHANNELING

P BASE

N+ BURIED LAYER

Fig. 39

90
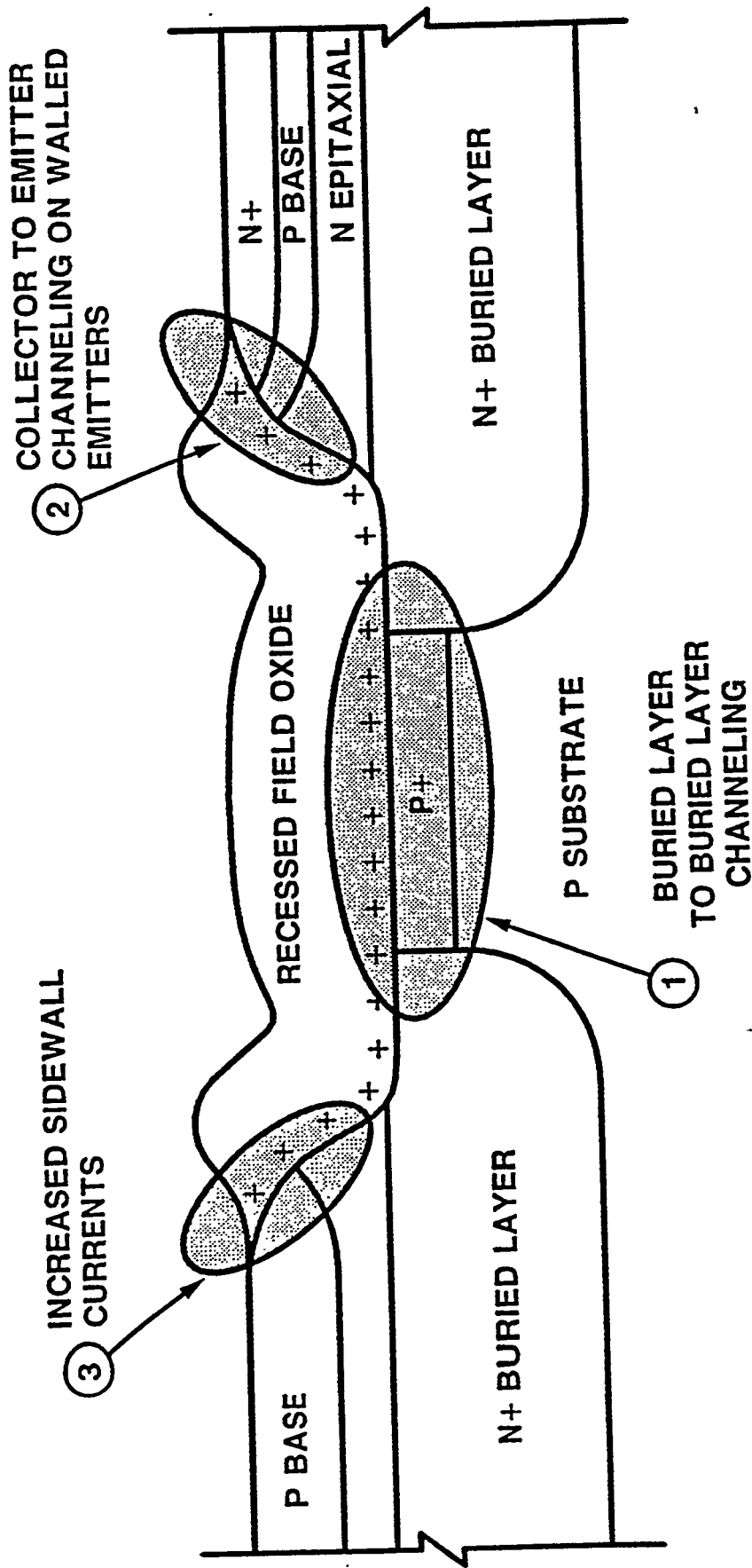
Modern BiCMOS BJTs
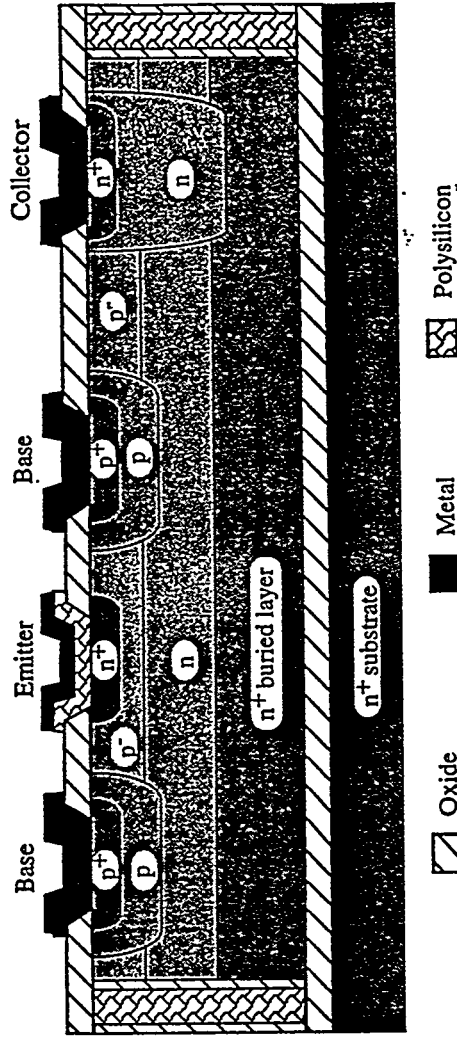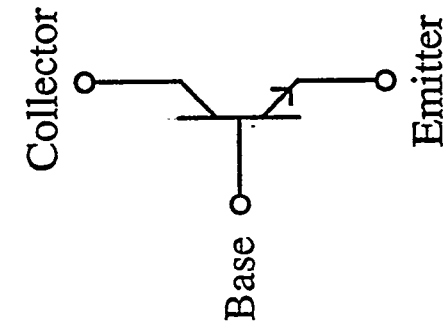
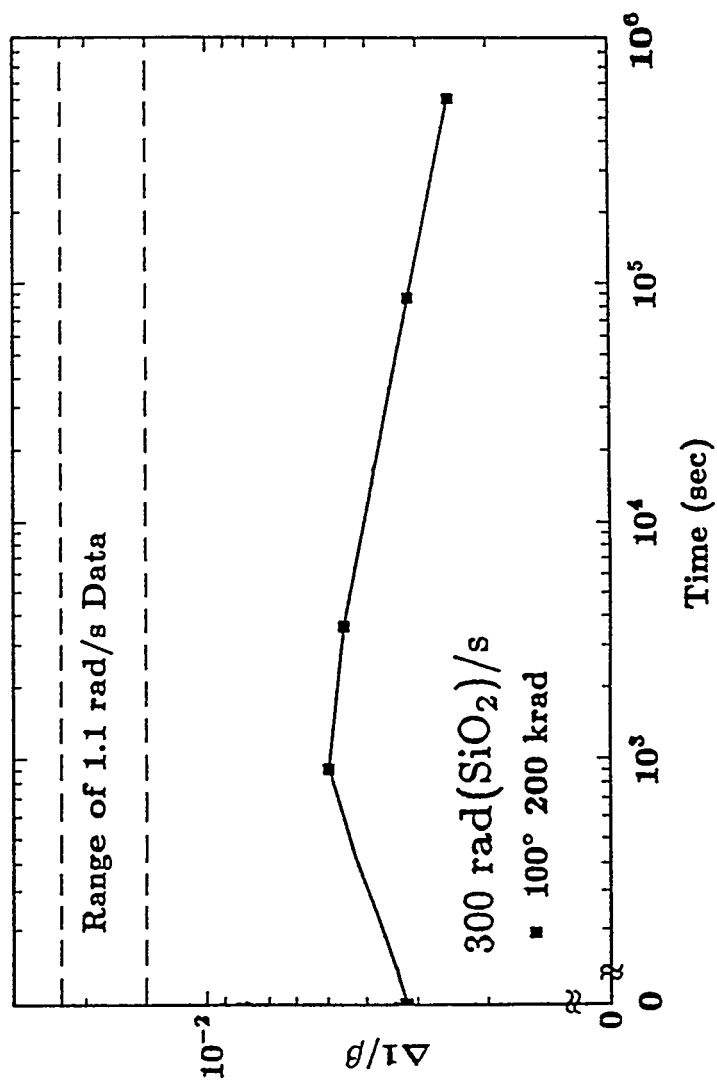| Emitter-Base Junction Depth | $0.3 \ \mu m$ |
| Intrinsic Base Surface Doping | $9.0 \times 10^{17} \ cm^{-3}$ |
| Oxide Thickness | $5450 \ \mathring{A}$ |

Fig. 40

Enlow et al., 1991: ADI RBCMOS (Development)
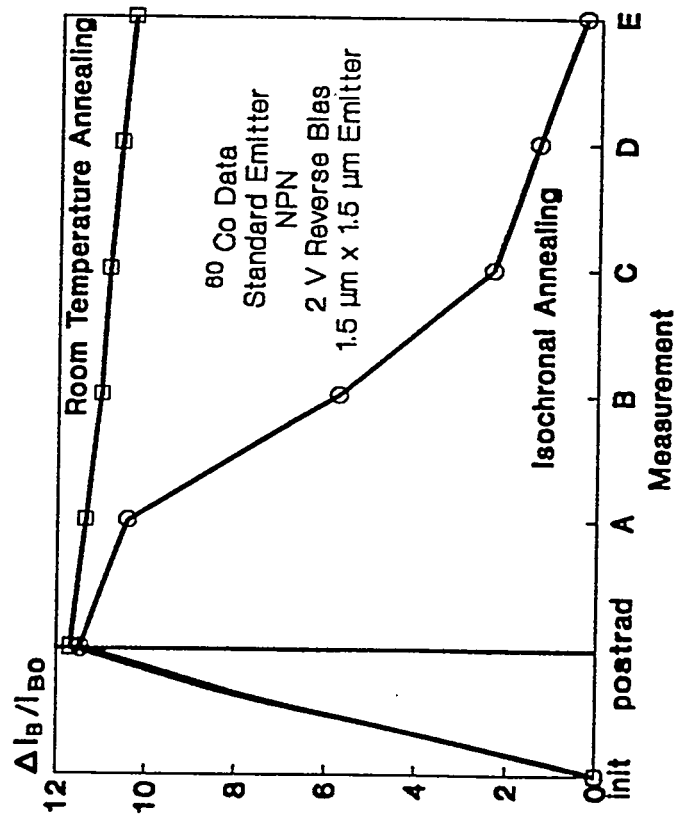
Fig. 41

Nowlin et al., 1993: ADI XFCB

Room Temperature Annealing

80 Co Data
Standard Emitter
NPN
2 V Reverse Bias
1.5 μm x 1.5 μm Emitter

Isochronal Annealing

$\Delta I_B / I_{BO}$

Measurement

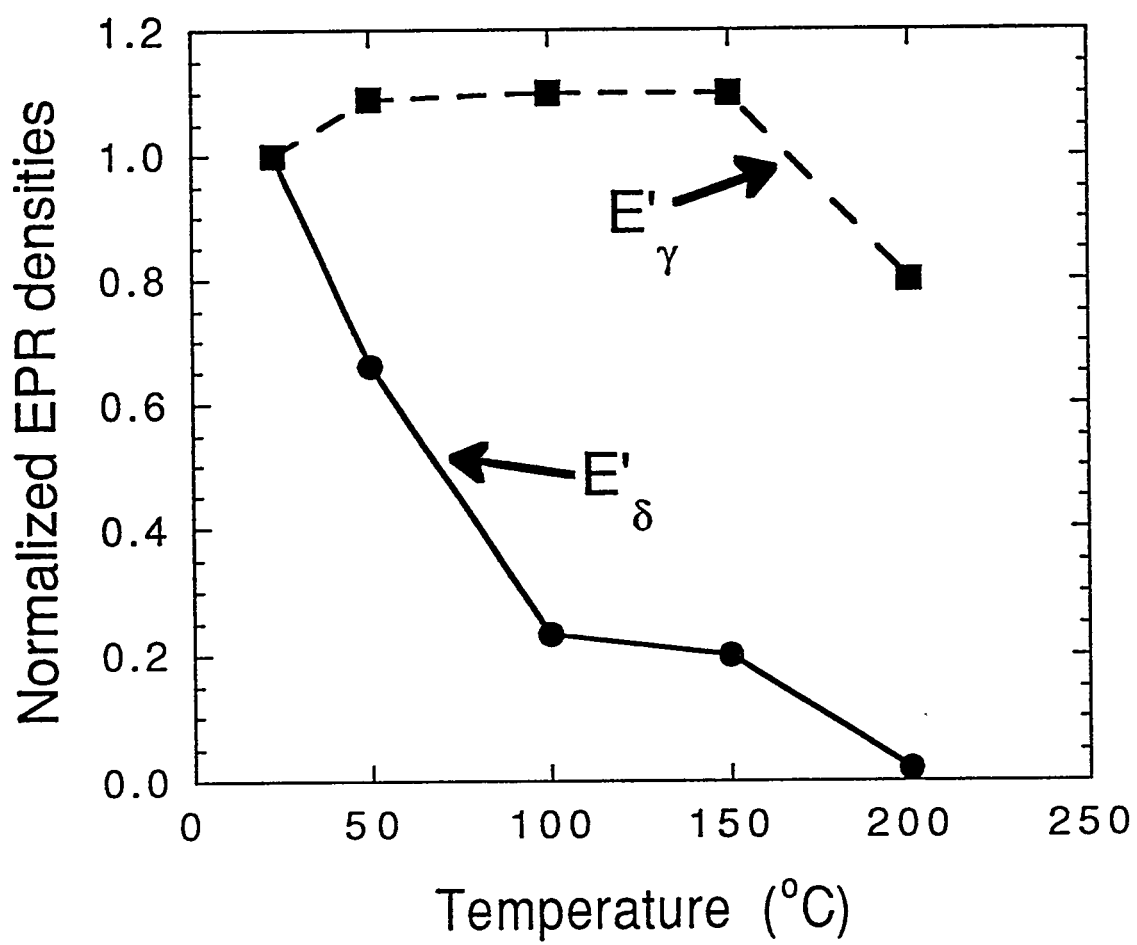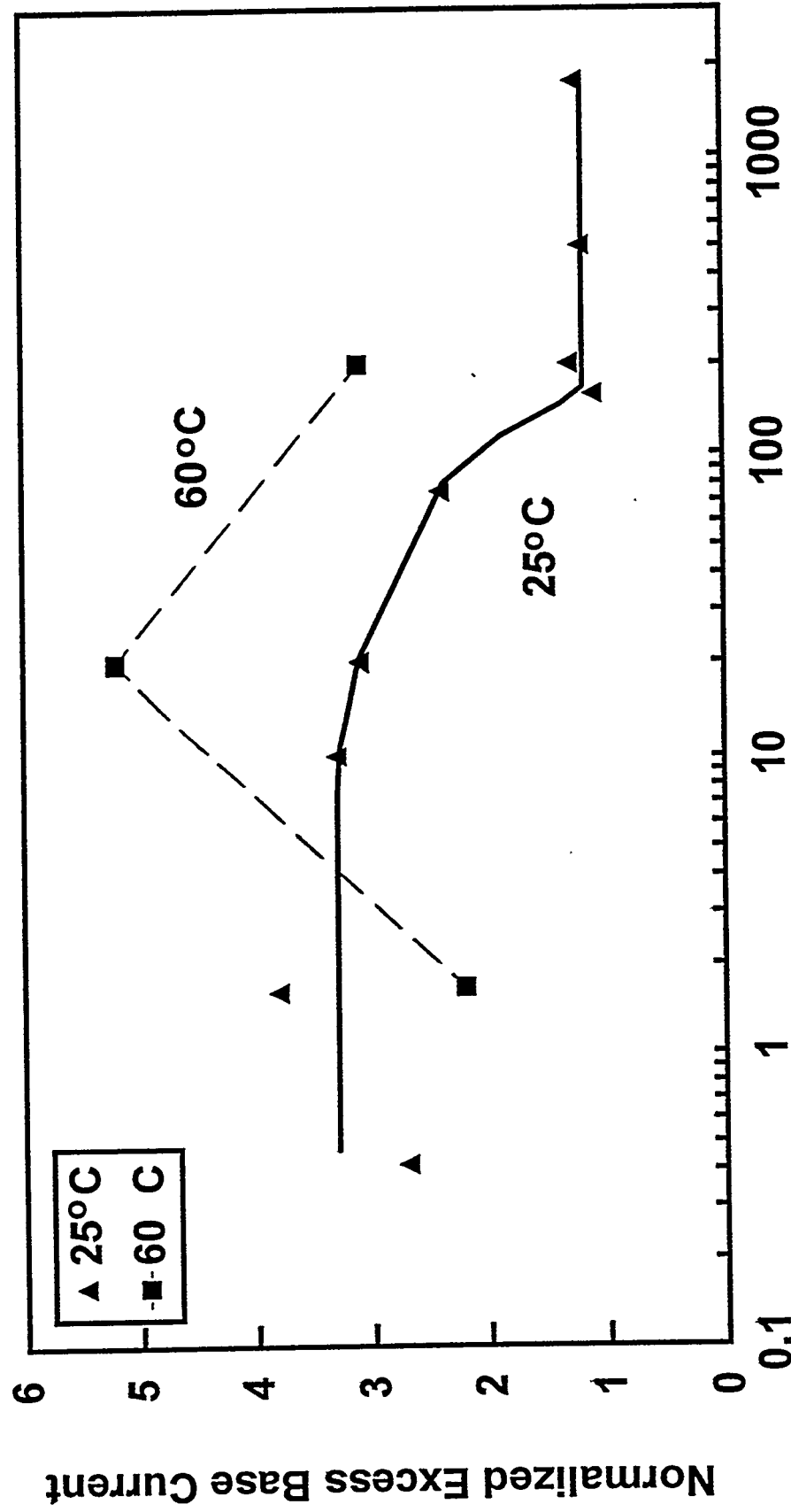init postrad A B C D E

Fig. 42

93

Fig. 43

60°C Rad @ Rates > 20 rad/s Enhances Damage for ADI XFCB Devices, but Lower Rate, High-T Rad Risks Annealing

0 V Rad to 300k; $V_{BE} = 0.6$ V

Dose Rate [rad(SiO_2)/s]

Normalized Excess Base Current

Legend:
- ▲ 25°C
- ■ -60 C

DMF/RNN 7/94

Nowlii   Fig. 44

Nowlii

IS, 1686
SREC

95

JPL

NEW RESULTS FOR LM324 Op-Amp

Johnston et al., 1994 IEEE Trans. Nucl. Sci.

Fig. 45

96
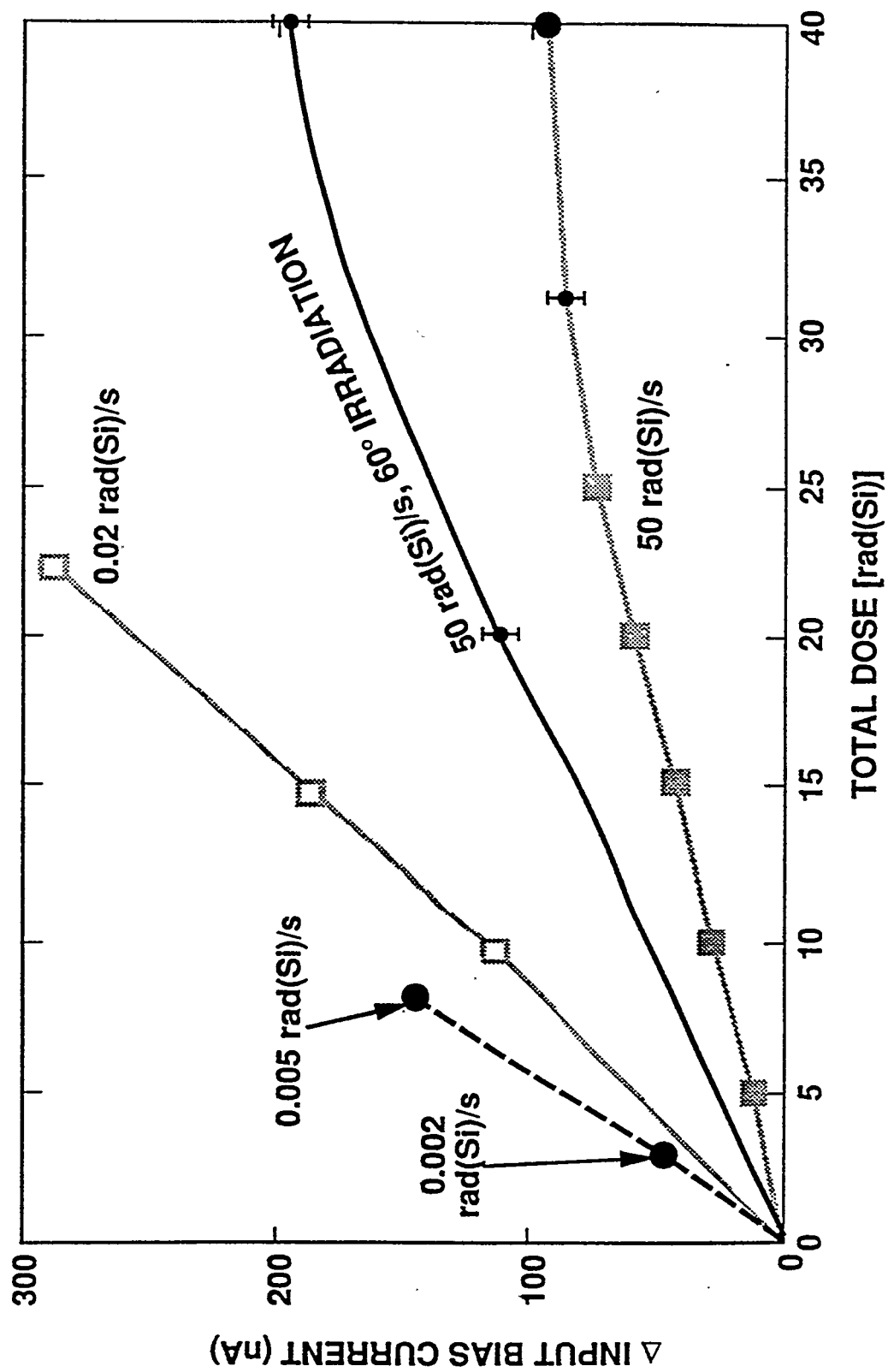
QML IMPLEMENTATION: KEY CORRELATIONS
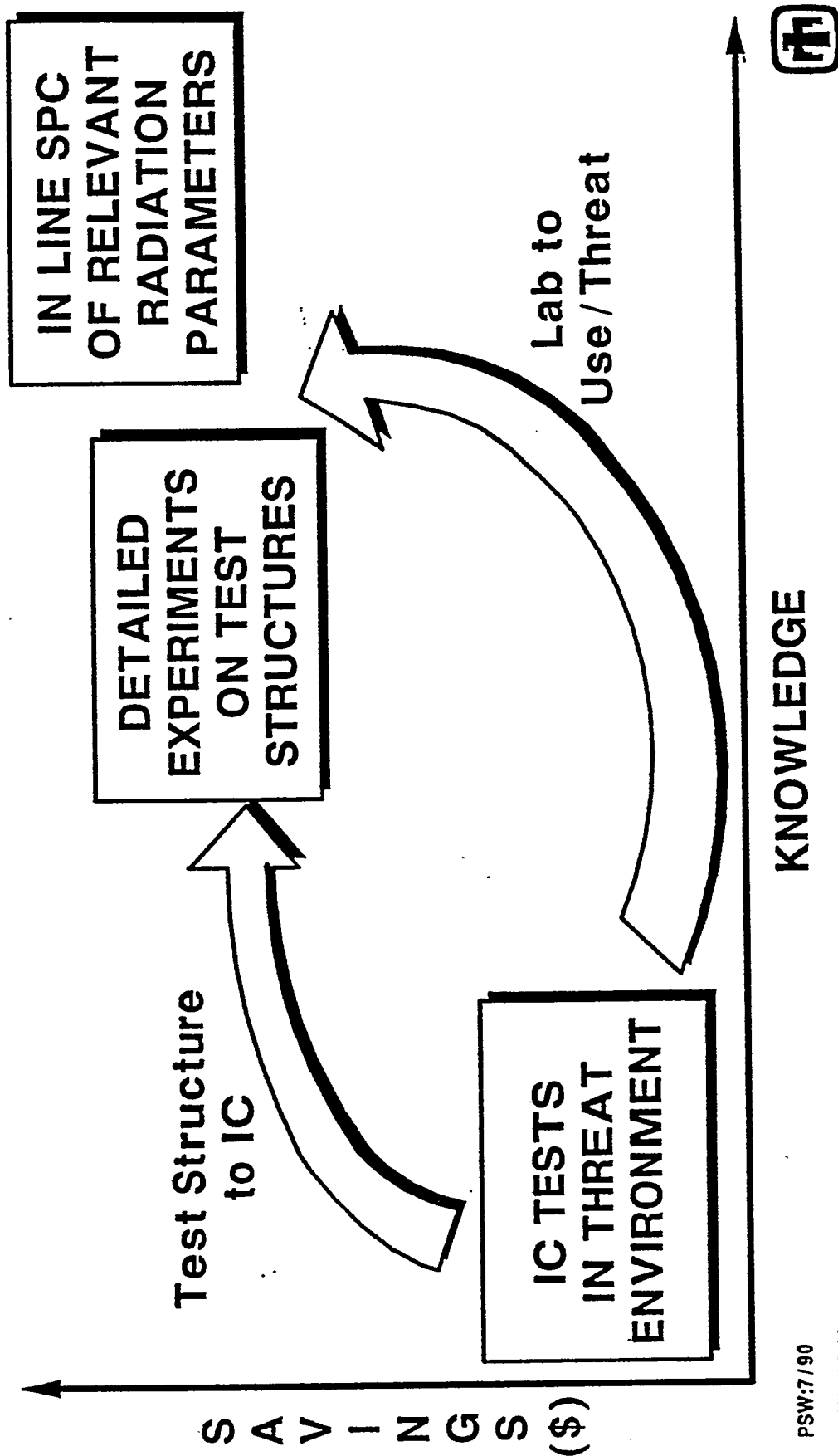
IN LINE SPC
OF RELEVANT
RADIATION
PARAMETERS

DETAILED
EXPERIMENTS
ON TEST
STRUCTURES

Lab to
Use / Threat

Test Structure
to IC

IC TESTS
IN THREAT
ENVIRONMENT

KNOWLEDGE

S A V I N G S ($)

Fig. 46

CONTROL CHART FOR ΔV_{it} & ΔV_{ot} FROM SNL 4/3-μm TECHNOLOGY

10 keV X Rays
500 krad (Si)

ΔV_{it}

UCL = 0.58

LCL = 0.23

ΔV_{ot}

LCL = -0.99

UCL = -1.74

X bar, moving R plot

Voltage Shift (volts)

Gate Oxidation Date

12/84   12/85   12/86   12/87   12/88

Fig. 47

PSW:7/90
90H2000.40

98

SPC OF ΔV_{it} FOR SPACE APPLICATIONS

Sandia 4 / 3 -µm Technology
500 krad(SiO$_2$)

UCL

LCL
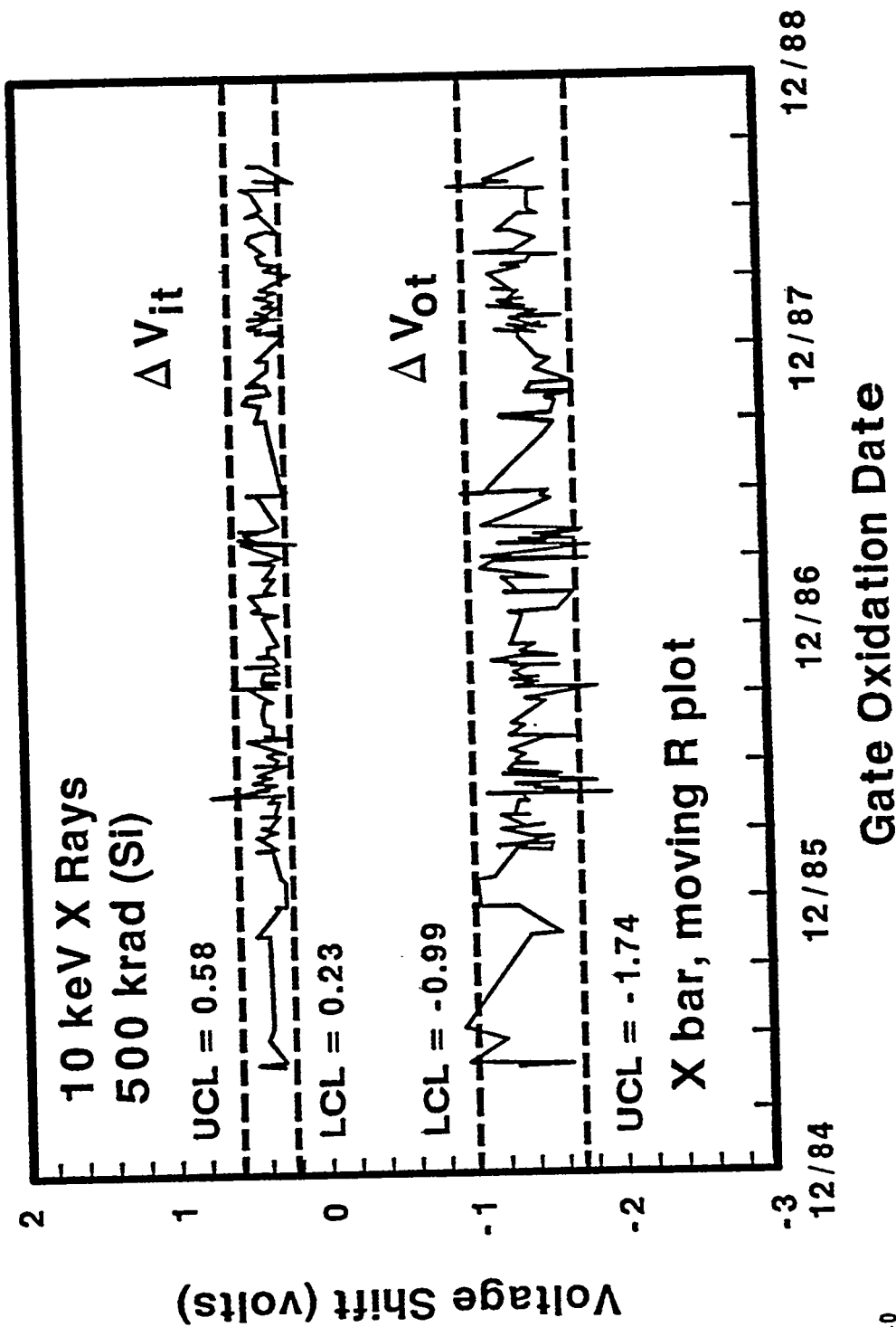
ΔV_{it} (Volts)
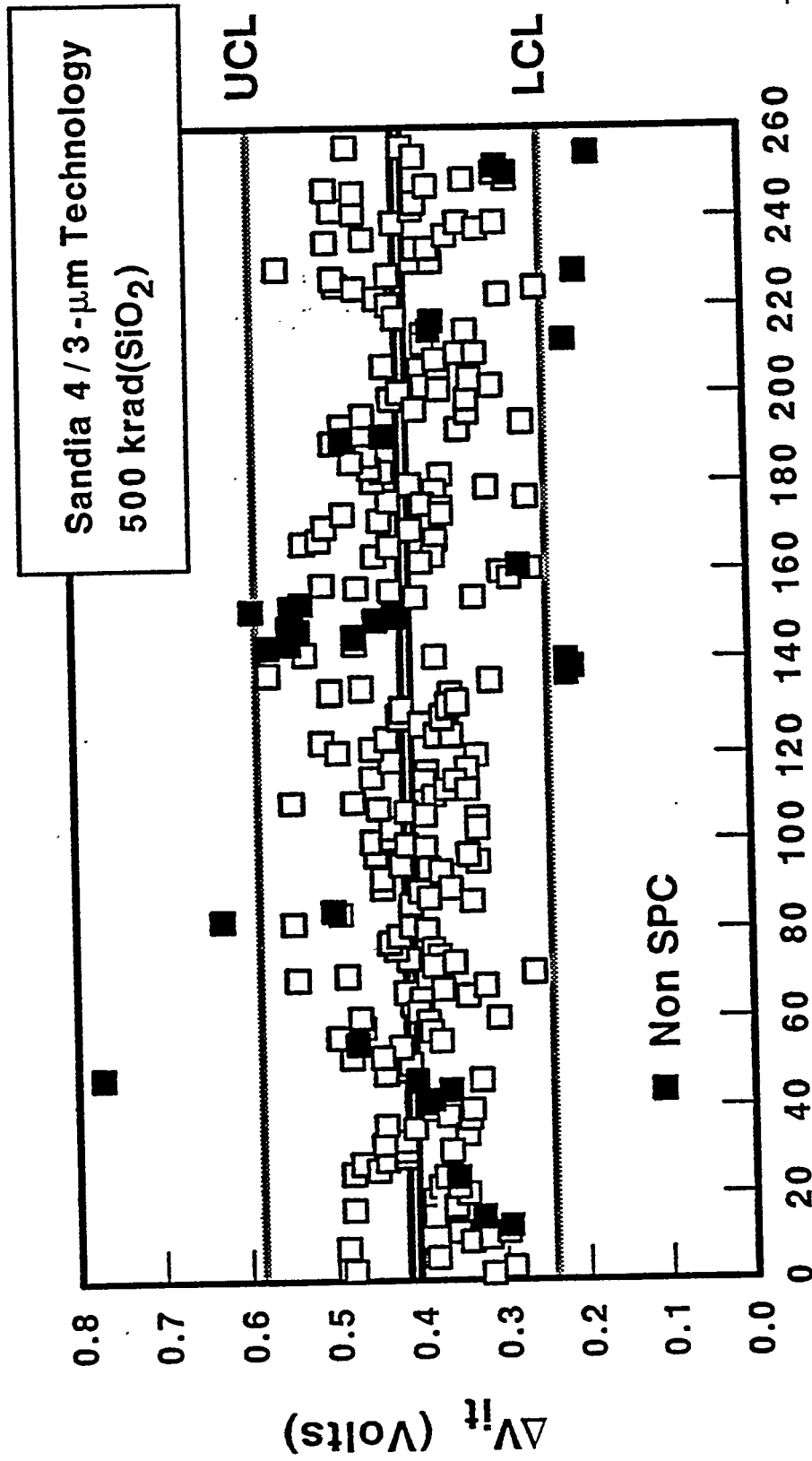
Consecutive Lots Processed

■ Non SPC

PSW:7/90

90H2000.52

Fig. 46

99

CHANGE IN "READ" TIMING VERSUS ΔV_{it}

SA3001
2k SRAM
n-Channel

0.20 rad(Si)/s
+10V

ΔV_{it} (Volts)

Δt_{RD} (ns)
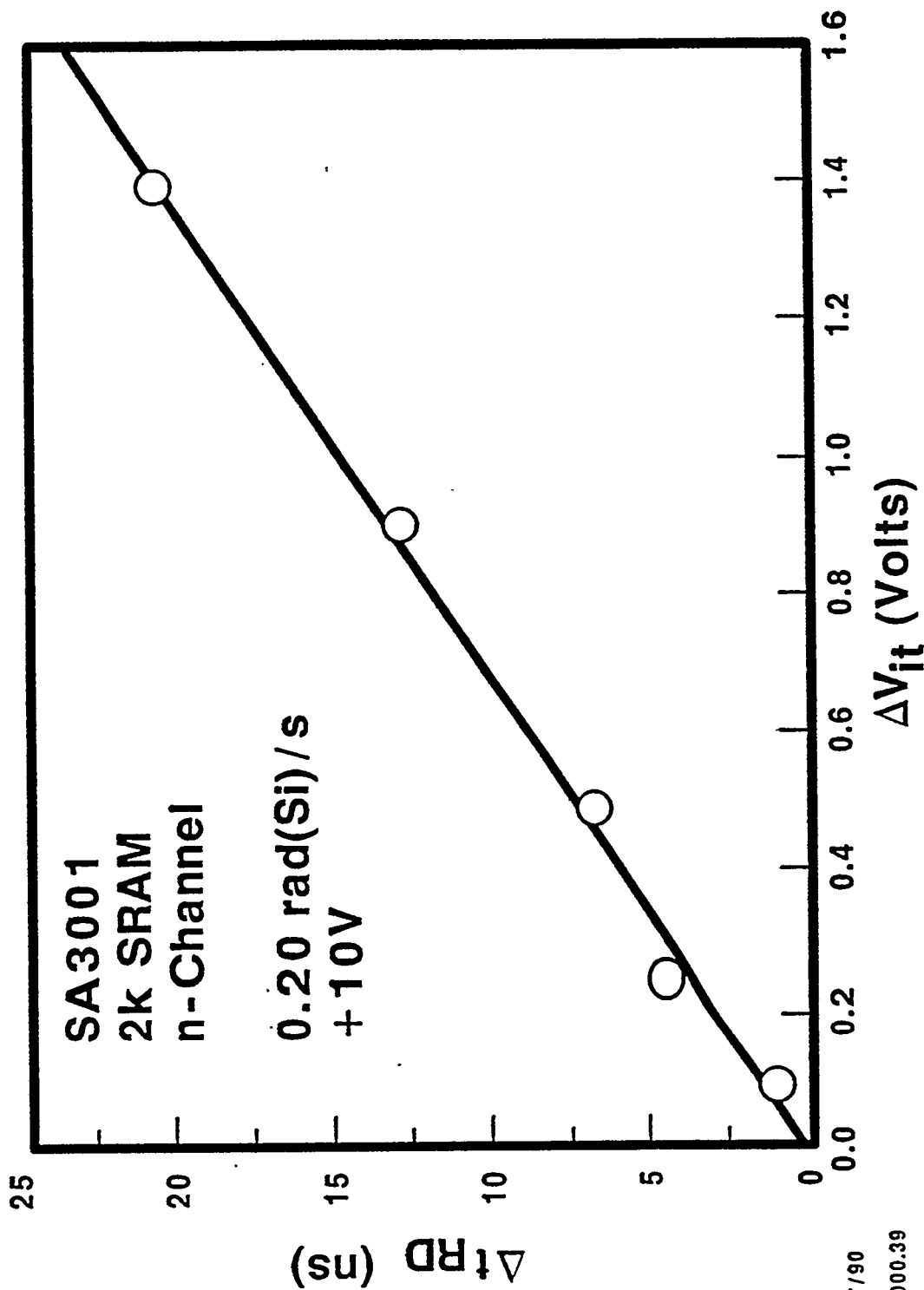
Fig. 49

PSW:7/90

90H2000.39

PREIRRADIATION 1/f NOISE MEASUREMENTS PREDICT RADIATION INDUCED OXIDE CHARGE

PREIRRADIATION NOISE POWER

POSTIRRADIATION OXIDE-TRAP CHARGE

$K \ (V^2)$

$-\Delta V_{OT} \ (V)$

D. M. Fleetwood and J. H. Scofield, Phys. Rev. Lett. 64, 579 (1990)

Sandia National Laboratories

JHS/DMF 9/89

Fig. 50