

Oblique Patterned Etching of Vertical Silicon Sidewalls

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Abstract: A method for patterning on vertical silicon surfaces in high aspect ratio silicon topography is presented. A Faraday cage is used to direct energetic reactive ions obliquely through a patterned suspended membrane positioned over the topography. The technique is capable of forming high-fidelity patterns (100 nm) features, adding an additional fabrication capability to standard top-down fabrication approaches.

Emerging nano-photonic ¹ and nano-opto-mechanical ² applications benefit from fabrication of complex three-dimensional structures. Creation of micrometer scale and sub-micrometer scale structures is a challenging endeavor, with only a handful of techniques capable of producing functional three dimensional structures. Many of the techniques such as direct laser write ^{3,4}, interferometric lithography ^{5,6}, nano-origami ^{7,8} and colloidal self-assembly ⁹ have been used to create a wide array of complex sub-micrometer structures, however the space of achievable structures is typically limited by the constraints of the fabrication approach. Typical top-down semiconductor fabrication approaches excel at creating the two-dimensional structures used in microelectronics, and can be adapted to create three dimensional structures such as micro-electro-mechanical (MEMS) structures and layer-by-layer structures ^{10,11}.

Microelectronic fabrication requires the ability to create sub-micrometer and deep sub-micrometer scale patterns in resist and subsequent transfer of these patterns to the substrate. Plasma-based etching is the dominant etching technique and is used to create contact holes, define transistor gates, and pattern blanket metal layers into patterned interconnects. In plasma etching, a space-charge neutral region of ionized atoms and electrons is created inside the etch chamber. At the cathode, a plasma sheath with a large voltage drop is created, accelerating etchant-species ions out of the plasma toward the surface of the wafer. Upon impact, the material to be etched becomes volatilized and removed via vacuum pump ¹². In most applications, plasma etching occurs through a patterned planar etch mask, either a soft mask such as photoresist or a hard mask such as oxide or nitride, in a direction normal to the wafer or substrate surface. For some next generation applications etching of more complex 3-dimensional structures is required and alternative approaches to traditional top-down plasma based etching are sought.

Rather than being distributed throughout the etch chamber, the electric field responsible for accelerating the ions inside the chamber is concentrated in the narrow “plasma sheath” which conforms to the surface of the substrate. Simply tilting the substrate with respect to the nominal etching direction in an attempt to etch at oblique incidence is unsuccessful in most circumstances because the plasma sheath conforms to the substrate, once again accelerating the ions in the direction normal to the now-tilted substrate surface (Fig. 1(A)). Oblique incidence etching is possible using a Faraday cage to alter the

local plasma sheath, redirecting the energetic ions at an oblique angle with respect to the substrate surface normal (Fig. 1(B)). The plasma sheath conforms to the periphery of the Faraday cage, while inside the cage, the electric field is zero. By selecting a mesh of appropriate dimension, the accelerating electric field can be completely screened inside the cage, while ions accelerated by the plasma sheath are able to penetrate the screen, following their initial trajectory unabated until they strike the sample

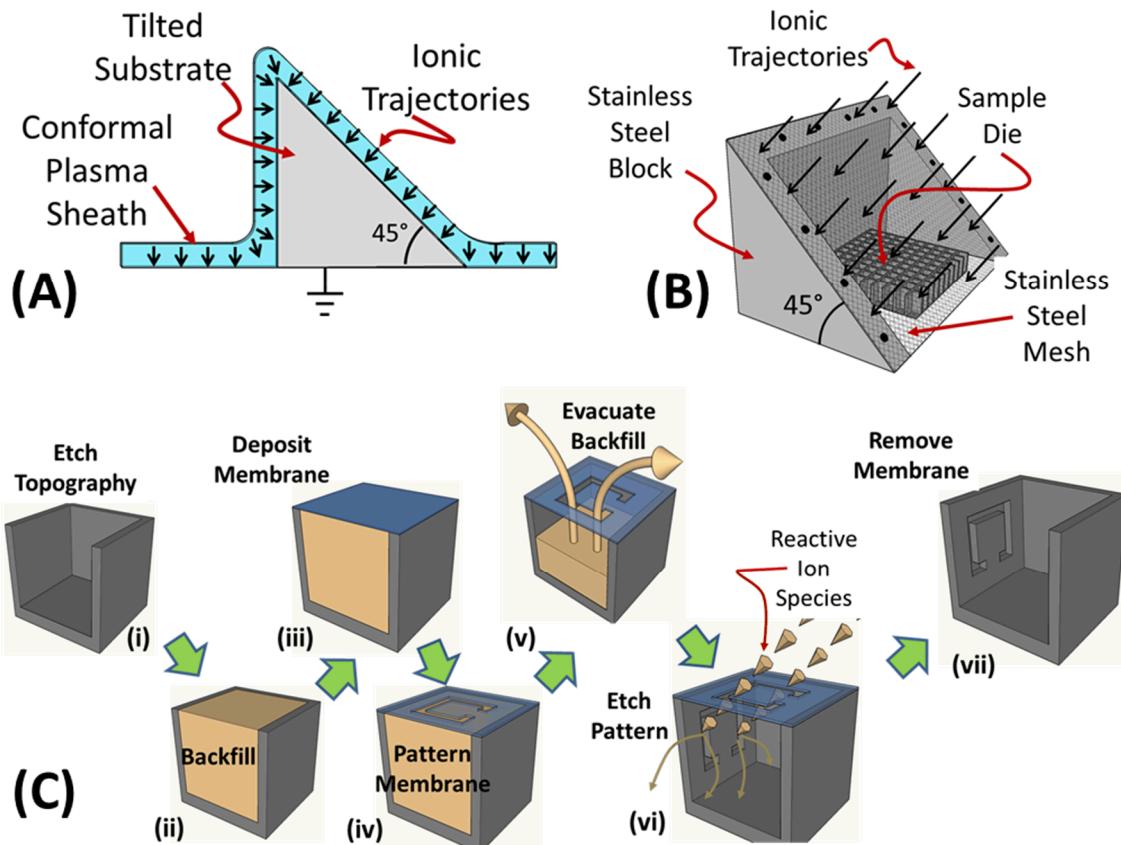


Fig. 1 (A) Schematic diagram showing the conformal plasma sheath directing the etchant species normal to the tilted surface; (B) Isometric view of a Faraday cage with a mesh screen. The Faraday cage redirects the plasma orientation while the screen allows the ions to pass through. The sample rests flat on the floor of the Faraday cage, so that the redirected ions entering through the mesh face are incident at an oblique angle; (C) Schematic diagram of the formation of the suspended patterned membrane;

at an angle defined by the Faraday cage geometry. This technique has been used to perform oblique etching on planar patterns using standard parallel plate etch systems¹³⁻¹⁶. It is also possible to etch in multiple directions simultaneously using Faraday cages with multiple surfaces covered with mesh. In a similar vein, in¹⁷ the authors fabricated a structure directly on top of the substrate to redirect the incident ions obliquely onto the substrate. Here we combine the oblique directionality provided by a Faraday cage with a suspended patterned membrane to demonstrate robust three-dimensional patterned etching of vertical silicon sidewalls, generalizing planar top-down etching into truly three-dimensional subtractive patterning approach.

Recently, we demonstrated membrane projection lithography (MPL) as a method for creation of 3-dimensional metamaterial structures^{18,19} in a polymer material system. In the MPL process, directional metal deposition is performed into unit cells through a patterned, suspended membrane, resulting in the deposition of metal-inclusions on the interior face(s) of the unit cell. MPL is capable of producing high fidelity 3-D inclusions at sub-micrometer dimensions with < 100 nm spatial resolution. The basic MPL process flow is covered in detail in a CMOS compatible material system²⁰, however we provide a brief synopsis of the approach for completeness.

The silicon substrate is patterned into the desired topography using standard deep reactive ion etching (i). A plasma enhanced chemical vapor deposition (PECVD) oxide is then deposited into the silicon topography, filling the cavities and overfilling the etched volume. Chemical mechanical polishing (CMP) is then used to planarize the sacrificial oxide back to top of the silicon(ii). Aluminum nitride is then deposited over the planarized oxide (iii) and patterned with optical lithography and a subsequent planar etch step (iv). The oxide backfill is then removed through the patterned AlN membrane(v) via 49% hydrofluoric acid (HF), yielding the final suspended patterned membrane positioned over the silicon (vi). This patterned membrane serves as a stencil, defining the pattern to be transferred into the vertical sidewall after oblique etching. There is considerable freedom of choice for the silicon topography. For this work, we created dense arrays of both cubic cavities as well as dense arrays of pillars.

A stainless steel block was machined into a 45-45-90 degree wedge with a 1.4 cm x 1.4 cm cavity. Stainless steel mesh (Goodfellow, Inc.) with a wire diameter of 66 μ m, with a grid spacing of \sim 6

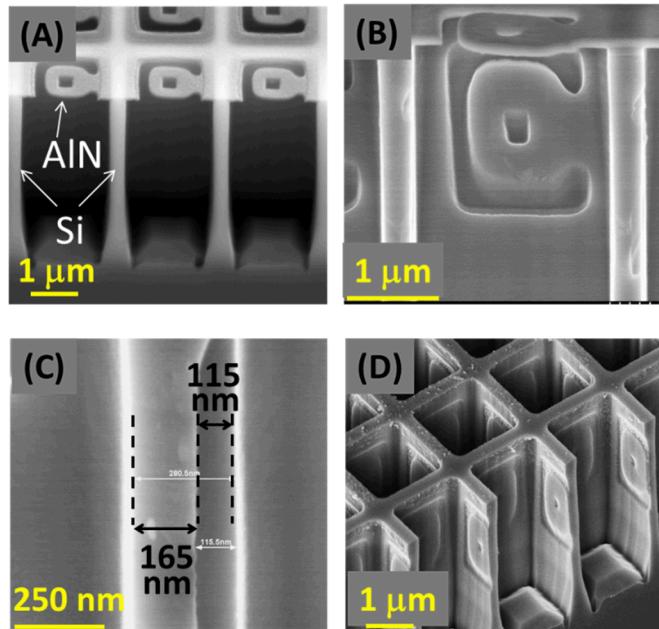


Fig. 2 (A) Cross-section SEM image showing the suspended patterned aluminum nitride membrane over unit cells in high aspect ratio silicon topography; (B) Cross-section SEM image of an etched feature in the vertical silicon wall; (C) Cross-section SEM image showing the etch depth into the wall, where 115 nm of silicon was etched into a 280 nm thick silicon wall; (D) Isometric SEM image showing two consecutive etches after a 90 degree rotation of the sample in the Faraday Cage.

wires/mm and nominal aperture of approximately 100 μ m was used to form the ion-permeable surface

mounted on the edges of the machined 45 degree face of the cage (Fig. 1(B)). The two most common forms of plasma etching are inductively coupled plasma (ICP) etching and reactive ion etching (RIE). We have etched using both etching approaches in multiple different etch systems, although only ICP results are shown here.

Fig. 2(A) shows an SEM image of the high-aspect ratio silicon structure prior to etching the vertical surface. The structure consists of a two-dimensional array of rectangular parallelepiped ($2 \mu\text{m} \times 2\mu\text{m} \times 4 \mu\text{m}$) cavities with a $2.3 \mu\text{m}$ period etched into the silicon substrate. Because the topography has been CMPed flat after the oxide backfill, the membrane can be patterned using a variety of methods, including high NA immersion optical lithography, e-beam, interferometric lithography, directed self-assembly, etc. One of the few constraints is that the final pattern must be self-supporting, eliminating patterns with closed loops. In Fig. 2, the AlN membrane is patterned into a “C” shape with a central dot, with as-drawn mask dimensions of $1.5 \mu\text{m} \times 1.5 \mu\text{m}$ and a 300 nm linewidth. Three unit cells of a dense array of similar unit cells are shown. All processing on these samples occurred at the wafer scale on a 150 mm silicon fabrication line. A 248 nm optical scanner was used for the lithography. Prior to oblique etching, the wafer was diced to fit into the Faraday cage and the sacrificial oxide evacuated using HF and the samples were dried.

A PlasmaTherm Versaline ICP RIE with a Cl_2/Ar mixture (20 sccm, 20 sccm), background pressure of 10 mTorr, RF (13.56 MHz) ICP power of 500 W and 50 W of DC bias was used to etch the silicon. The cross-section SEM in Fig. 2(B) shows the transfer of the membrane pattern into one vertical face in the interior of the unit cell after 300 seconds of etching. Fig. 2(C) shows a cross-section SEM of the etched wall, where 115 nm of the 280 nm thick wall was etched, yielding an etch rate of 3.8 A/s . (Note: the etch parameters have not been optimized for etch rate). In Fig. 2(D), two shorter consecutive etches were performed with a 90 degree rotation of the sample between etches so that two adjacent faces of the unit cell have been decorated. Additionally, in Fig. 2(D), the AlN membrane was removed in a basic SC1 clean, a standard CMOS cleaning solution (10:1:1, $\text{H}_2\text{O}:\text{HN}_3\text{OH}:\text{H}_2\text{O}_2$). No apparent degradation of the AlN mask was evident after 600 s of combined etching. Samples appear uniform by eye over the entire cm die.

In Fig. 3(A-D) we show MPL-Etching results on the external faces of silicon pillars, demonstrating that the approach is quite versatile. In Fig. 3(A), a single cross is etched into the vertical face of the pillar. The distortion of the cross is a faithful representation of the distorted membrane pattern, due to the difficulties in resolving these deep sub-micrometer features using the available optical stepper. Fig. 3(B) shows a pillar with 2 consecutive etches performed after a 90 degree rotation of the sample. Again, no obvious degradation of the mask pattern is evident. Fig. 3(C) shows isolated dots while Fig. 3(D) shows parallel dashes. The smallest dimension in both of these patterns is approximately 100 nm.

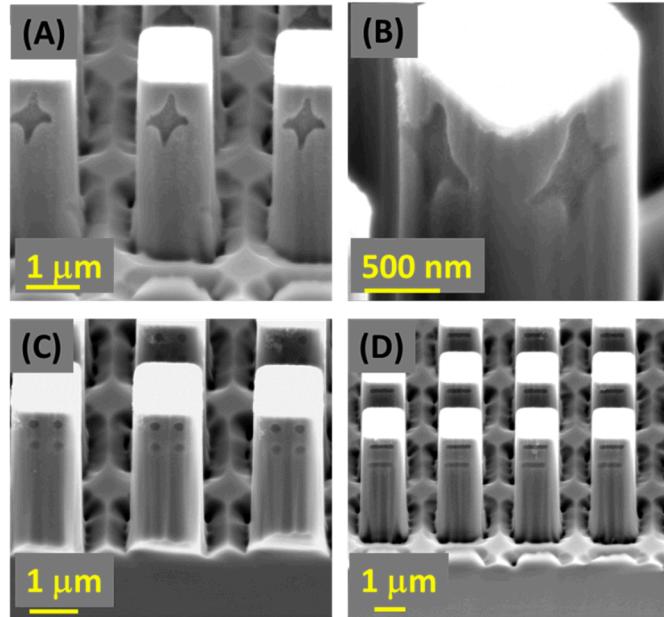


Fig. 3 (A) Oblique SEM image of silicon pillars patterned with a cross on a single side; (B) Oblique SEM image of a pillar patterned on multiple sides; (C) Oblique SEM image of pillars with ~ 100 nm isolated etched features; (D) Oblique SEM image of ~ 100 nm etched dashes.

Given the success of the MPL approach as a deposition technique, the success of an MPL-based etching approach might seem assured. One significant difference between deposition in an e-beam evaporator and a plasma etch chamber is the ambient pressure. In a metalevaporator, metal is deposited somewhere between 10^{-7} Torr - 10^{-6} Torr, while typical etch pressures range from 10^{-3} Torr- 10^{-1} Torr. One of the metrics which is used to assess etch quality is resolution. The increased pressure inside the etch chamber could possibly affect this by causing gas phase collisions in the volume of the Faraday cage, resulting in redirection of the incident etchant species even in the absence of applied field. While we are currently performing experiments to quantify the resolution of this technique, the SEM images in Fig. 3C,D demonstrate that resolving patterns with dimensions on the order of 100 nm is possible. We also need to establish limits on the pattern density, i. e. how close together can two minimum-resolution features be placed on the vertical wall. Pattern density can be expected to be a function both of the in-chamber gas-phase scattering as well as the limits of the structural integrity of the membrane in areas with narrow cross section. In addition, etching occurs into the vertical wall at the angle prescribed by the Faraday cage, and in principle, should follow that trajectory. This inevitably results in an angled sidewall, seen at the top of the cross-section SEM of Fig. 2C. For short etches, for instance to break through a thin film on the sidewall, the angling of the etched sidewall will have negligible impact. For deeper etches such as a through-wall etch, this angled sidewall will be more apparent, similar to that seen in references¹³⁻¹⁶.

Demonstration of the ability to etch complex patterns into high aspect ratio structures has the potential to impact a wide variety of next generation micro and nano structured research. In structured electromagnetic research, complementary metamaterials are formed following Babinet's principal where continuous metallic films are patterned with clear openings in the form of split ring resonators or other resonant structures. Where the standard resonators operate on the electric field, the CMM

resonators operate on the magnetic field (or vice versa). For non-metallic structured electromagnetic materials, researchers are using solid prisms of high index semiconductors formed into dielectric resonators with significantly lower loss than metallic resonator based metamaterials. The quality factor (Q-factor) of these structures is dramatically impacted by the shape and symmetry of the dielectric resonator. The patterned etch presented here could be used to dress the faces of the dielectric resonator with structure to modify the Q-factor or alternatively, complete low-index (air) dielectric resonators could be formed in the high index background, forming complementary dielectric metamaterials.

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- [1] A. M. Jones, C. T. DeRose, A. L. Lentine, D. C. Trotter, A. L. Starbuck, R. A. Norwood, *Opt. Exp.*, **21**, 12002 (2013).
- [2] H. Shin, J. A. Cox, R. Jarecki, A. Starbuck, Z. Wang, and P. T. Rakich, *Nat. Comm.* **6**, 6427 (2015).
- [3] J. K. Gansel, M. Thiel, M. S. Rill, M. Decker, K. Bade, V. Saile, G. von Freymann, S. Linden, and M. Wegener, *Science*, **325**, 1513 (2009).
- [4] M. S. Rill, C. Plet, M. Thiel, I. Staude, G. von Freymann, S. Linden, and M. Wegener, *Nat. Mater.*, **7**, 543 (2008).
- [5] D. B. Burckel, C. M. Washburn, A. K. Raub, S. R. J. Brueck, D. R. Wheeler, S. M. Brozik and R. Polksy, *Small*, **5**, 2792 (2009).
- [6] X. Xiao, T. E. Beechem, M. T. Brumbach, T. N. Lambert, D. J. Davis, J. R. Michael, C. M. Washburn, J. Wang, S. M. Brozik, D. R. Wheeler, D. B. Burckel and R. Polksy, *ACS Nano*, **6**, 3573 (2012).
- [7] J. H. Cho and D. H. Gracias, *Nano Lett.*, **9**, 4049 (2009).
- [8] J. H. Cho, M. D. Keung, N. Verellen, L. Lagae, V. V. Moshchalkov, P. Van Dorpe, and D. H. Gracias, *Small*, **7**, No. 14, 1943 (2011).
- [9] Y. A. Vlasov, X. Z. Bo, J. C. Sturm, and D. J. Norris, *Nature*, **414**, 289 (2001).
- [10] J. G. Fleming, S. Y. Lin, I. El-Kady, R. Biswas, and K. M. Ho, *Nature*, **417**, 52 (2002).
- [11] J. Valentine, S. Zhang, T. Zentgraf, E. Ulin-Avila, D. A. Genov, G. Bartal, and X. Zhang, *Nature*, **455**, 376 (2008).

[12] S. A. Campbell, The Science and Engineering of Microelectronic Fabrication (Oxford University Press, New York, 1996).

[13] G. D. Boyd, L. A. Coldren and F. G. Storz, *Appl. Phys. Lett.*, **36**, 583 (1980).

[14] B. Cho, S. Hwang, J. Ryu, I. Kim, and S.H. Moon, *Electrochem. And Solid State Lett.* **2**, 129 (1999).

[15] J.-K. Lee, S.-H. Lee, J.-H. Min, I.-Y. Jang, C.-K. Kim, and S.H. Moon, *J. Electrochem. Soc.* **156**, D222 (2009).

[16] M.J. Burek, N.P. de Leon, B.J. Shields, B.J.M. Hausmann, Y. Chu, Q. Quan, A.S. Zibrov, H. Park, M.D. Lukin, and M. Lončar, *Nano Lett.* **12**, 6084 (2012).

[17] S. Takahashi, K. Suzuki, M. Okano, M. Imada, T. Nakamori, Y. Ota, K. Ishizaki, and S. Noda, *Nat. Mater.* **8**, 721 (2009).

[18] D. B. Burckel, J. R. Wendt, G. A. Ten Eyck, A. R. Ellis, I. Brener, and M. B. Sinclair, *Adv. Mater.*, **22**, 3171 (2010).

[19] D. B. Burckel, J. R. Wendt, G. A. Ten Eyck, J. C. Ginn, A. R. Ellis, I. Brener, and M. B. Sinclair, *Adv. Mater.*, **22**, 5053 (2010).

[20] D. B. Burckel, P. J. Resnick, P. S. Finnegan, M. B. Sinclair and P. S. Davids, *Opt. Mater. Expr.*, **5**, 2231 (2015).