

Challenges in LTCC

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Challenges are Two-Fold

- From the Dictionary:
 - ...by its nature or character serves as a call to ... special effort.
 - I read this as “Opportunities in LTCC”
 - Novel applications
 - “out of the box”
 - Difficulty in...an undertaking that is stimulating...
 - I read this as “Limitations in LTCC”
 - Emphasis: performance, cost, schedule, reliability



Novel Applications- the Path Includes:

- Shaping (bending, rolling, molding, applique)
- Sacrificial Volume Materials (SVM)
- Multi-purpose (fluidic, electrical, mechanical, chemical, sensors)



“Flat Boards”-

The path includes:

- Shielding
- Thermal issues
- Shrinkage tolerance vs. high-density circuitry
- High Frequency
 - Location of RF ground planes, features
- Cavities, holes, valleys, ledges
- Assembly



Marketplace

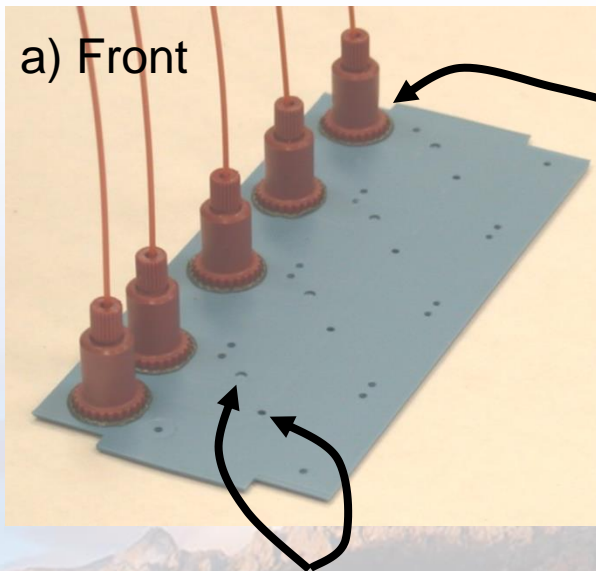
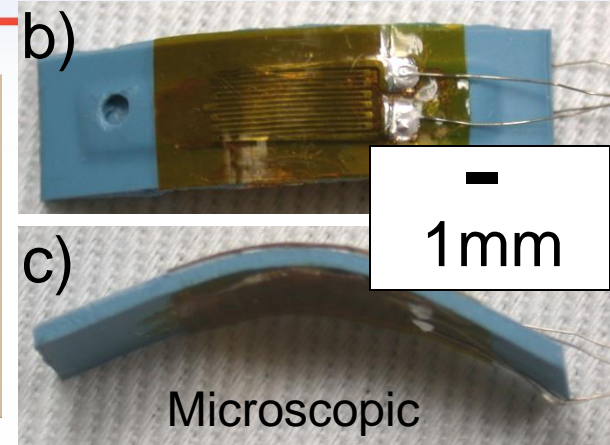
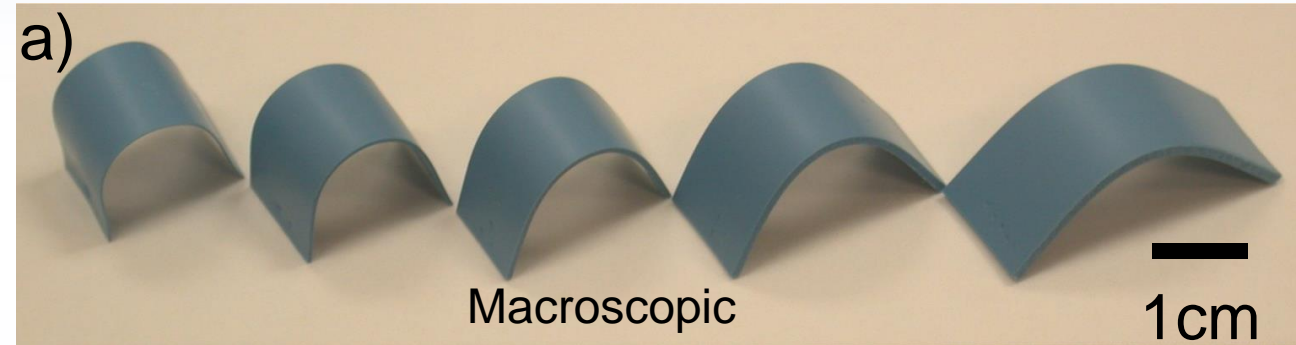
- Drive toward finer features, larger panels, lower cost.
- Maintain high quality, reliability.
- Competing technologies present risk of defection.



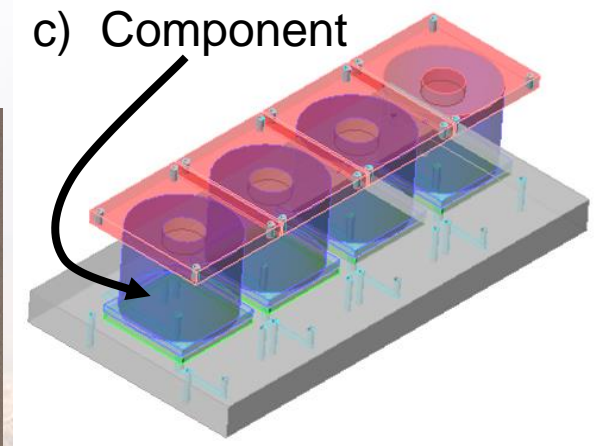
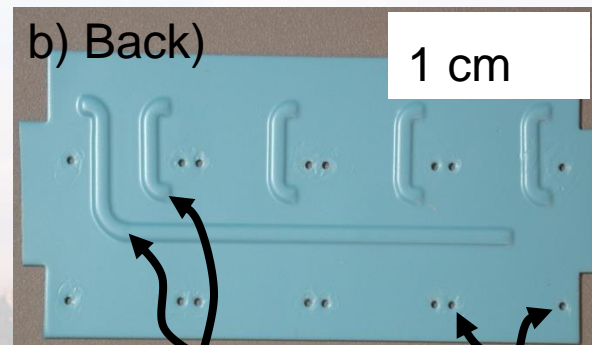
Outline

- Review novel processing
 - Shapes
 - Sacrificial materials
 - MEMS applications
- Review MCM structures & processing
- Conclusions

Shaped Structures

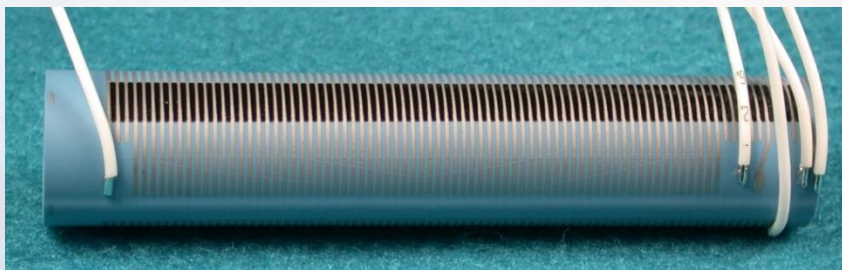
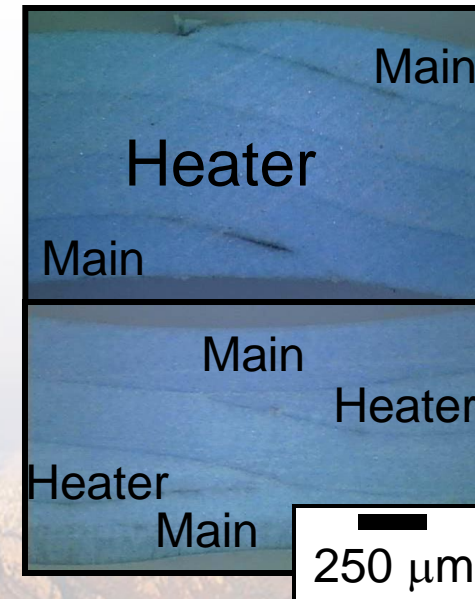
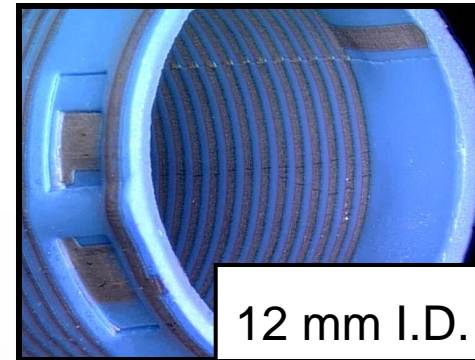
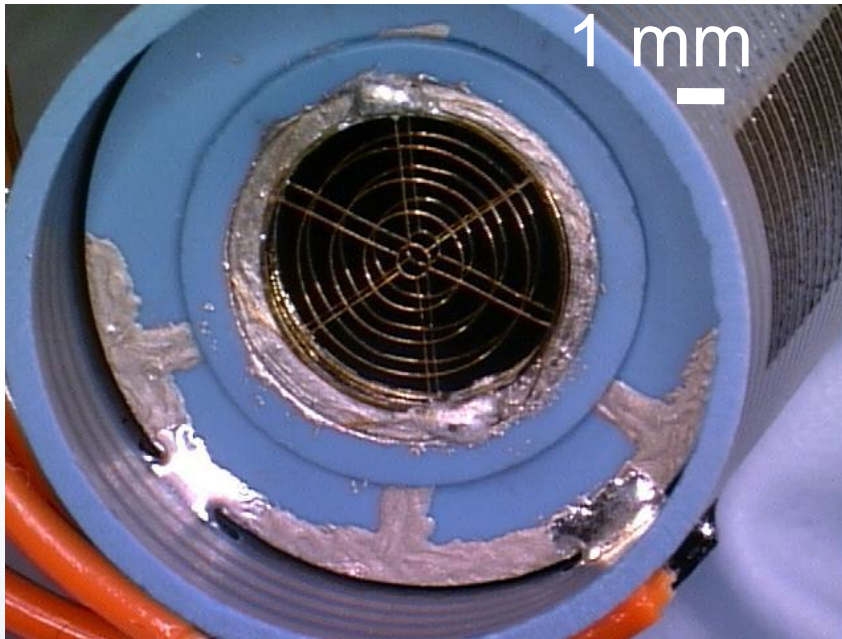


Commercial ports



Forming of LTCC to Unconventional Requirements

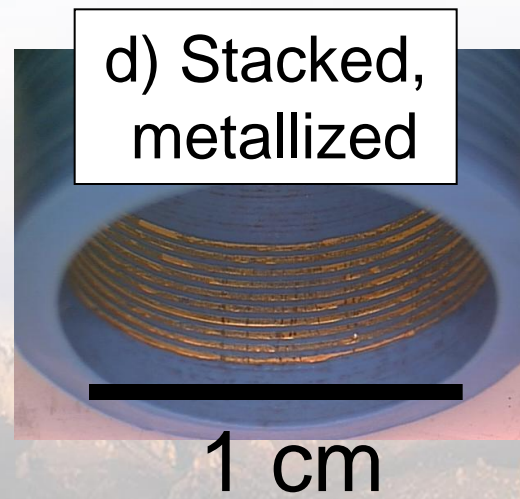
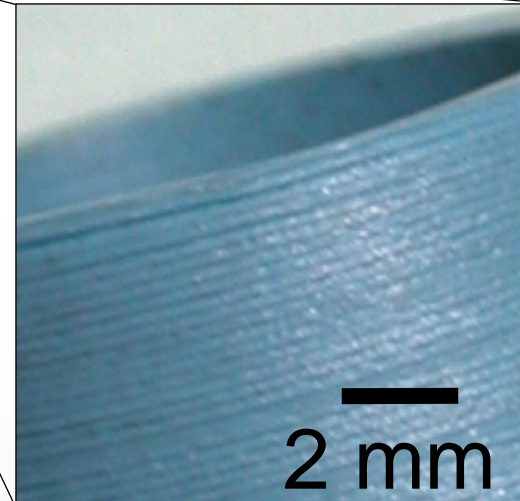
Rolled ion mobility spectrometer (IMS) drift tube



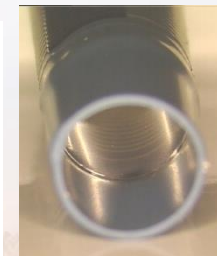
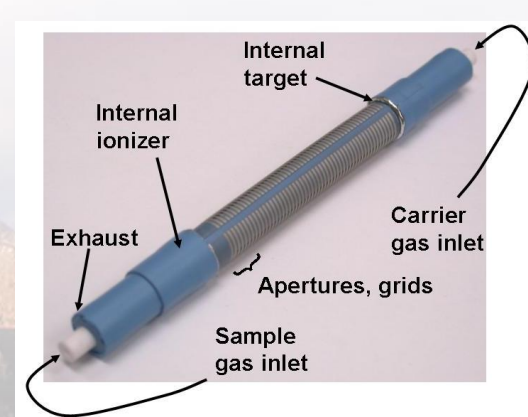
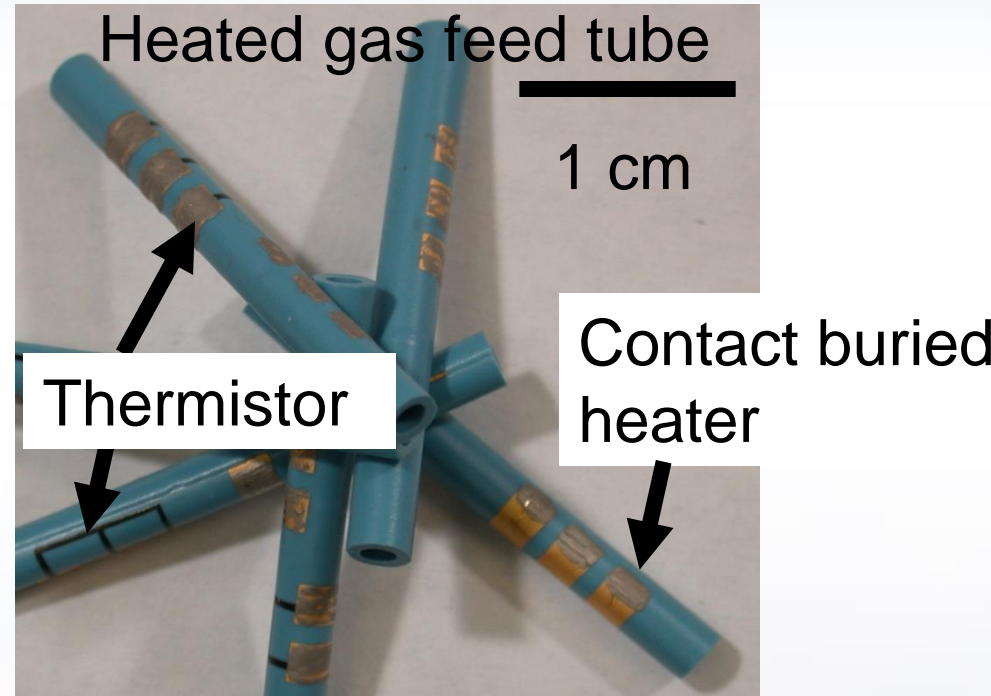
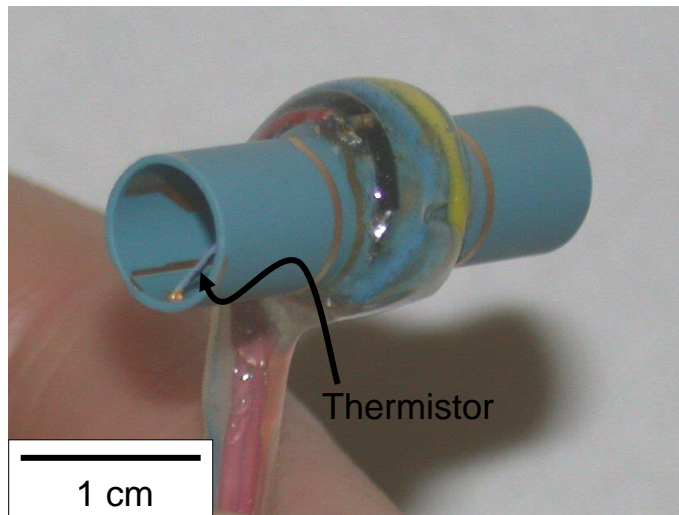
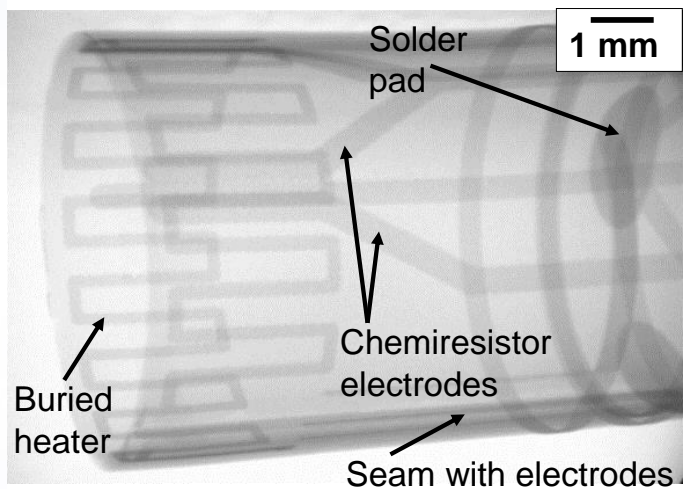
1 cm

250 μm

Stacking to 300 layers

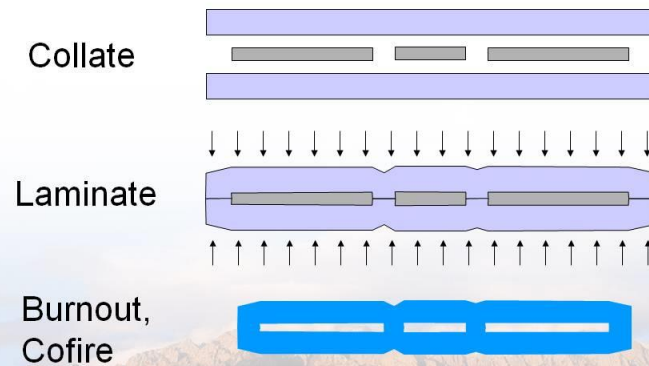


Tubular Devices



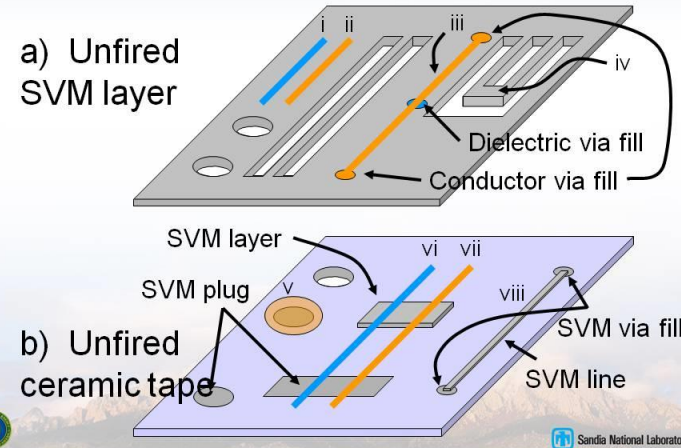
Novel Structures 1: SVM

SVM Technique



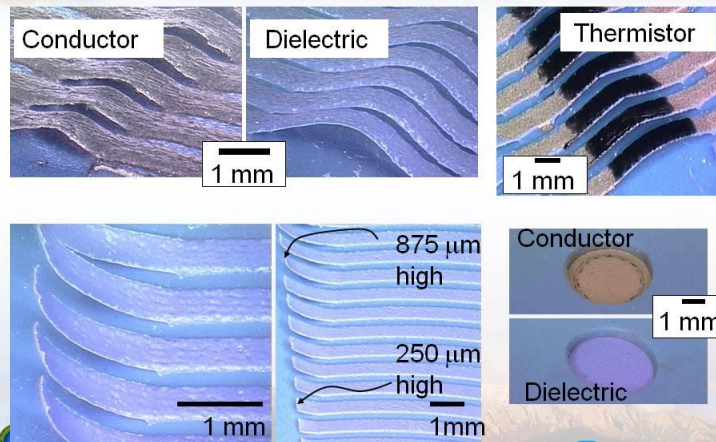
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SVM / LTCC Tape / Thick Film Combinations



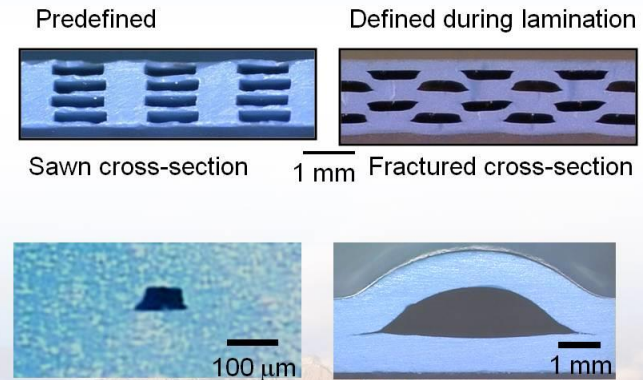
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Suspended Thick Film



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Meso/Micro-Scale Channels

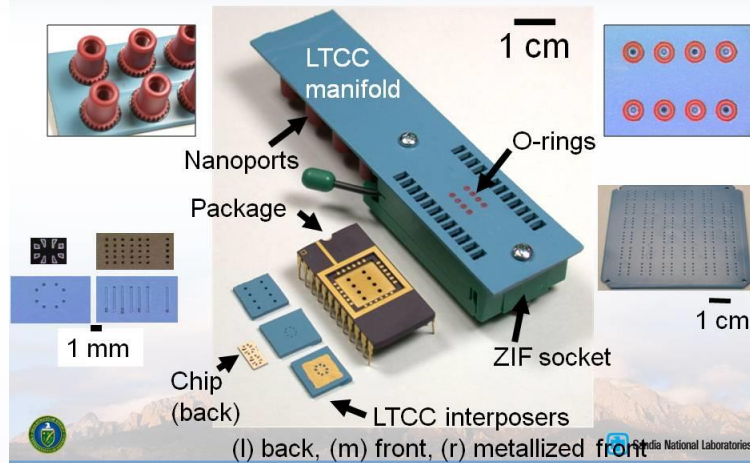


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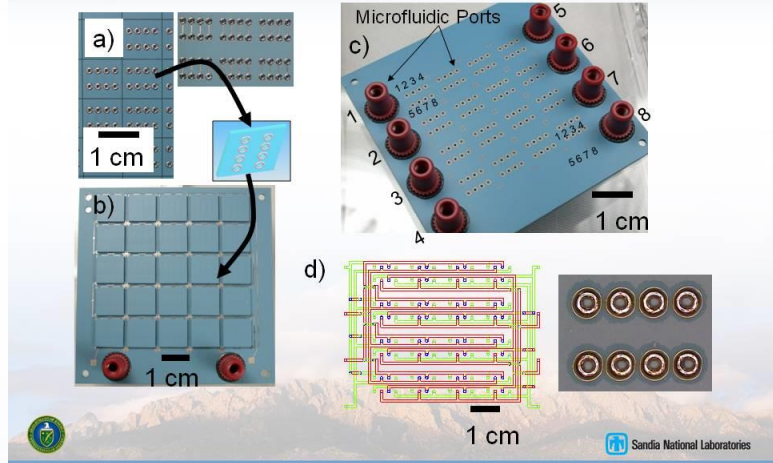
laboratories

Novel Structures 2: Channels

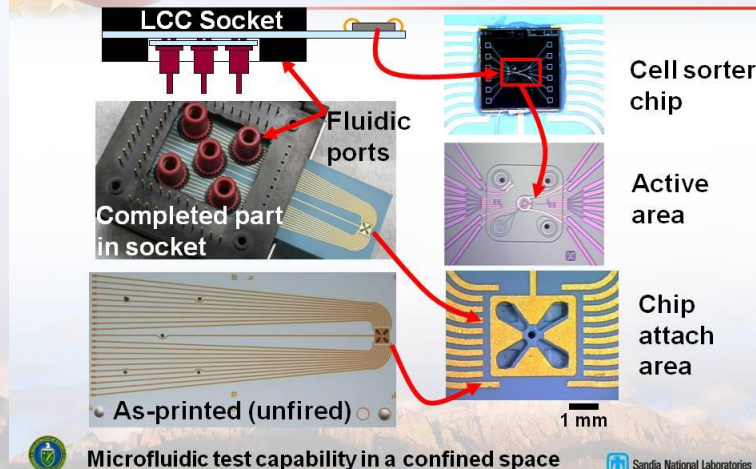
Test Manifold



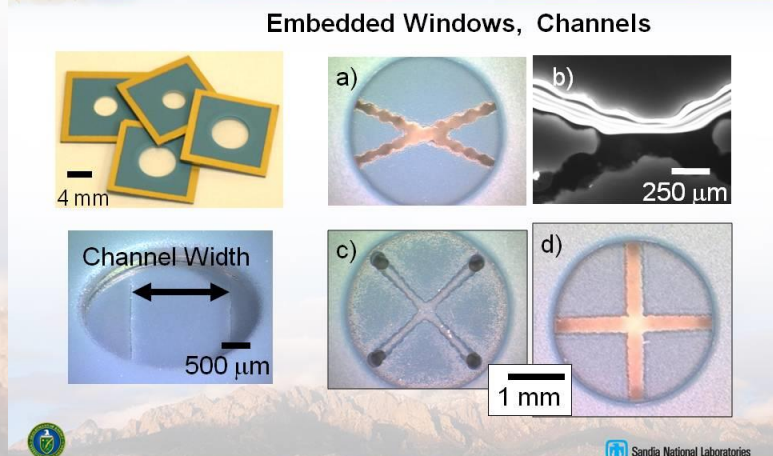
Modular Microfluidic Standard Components



Biological Cell Sorter



View Ports

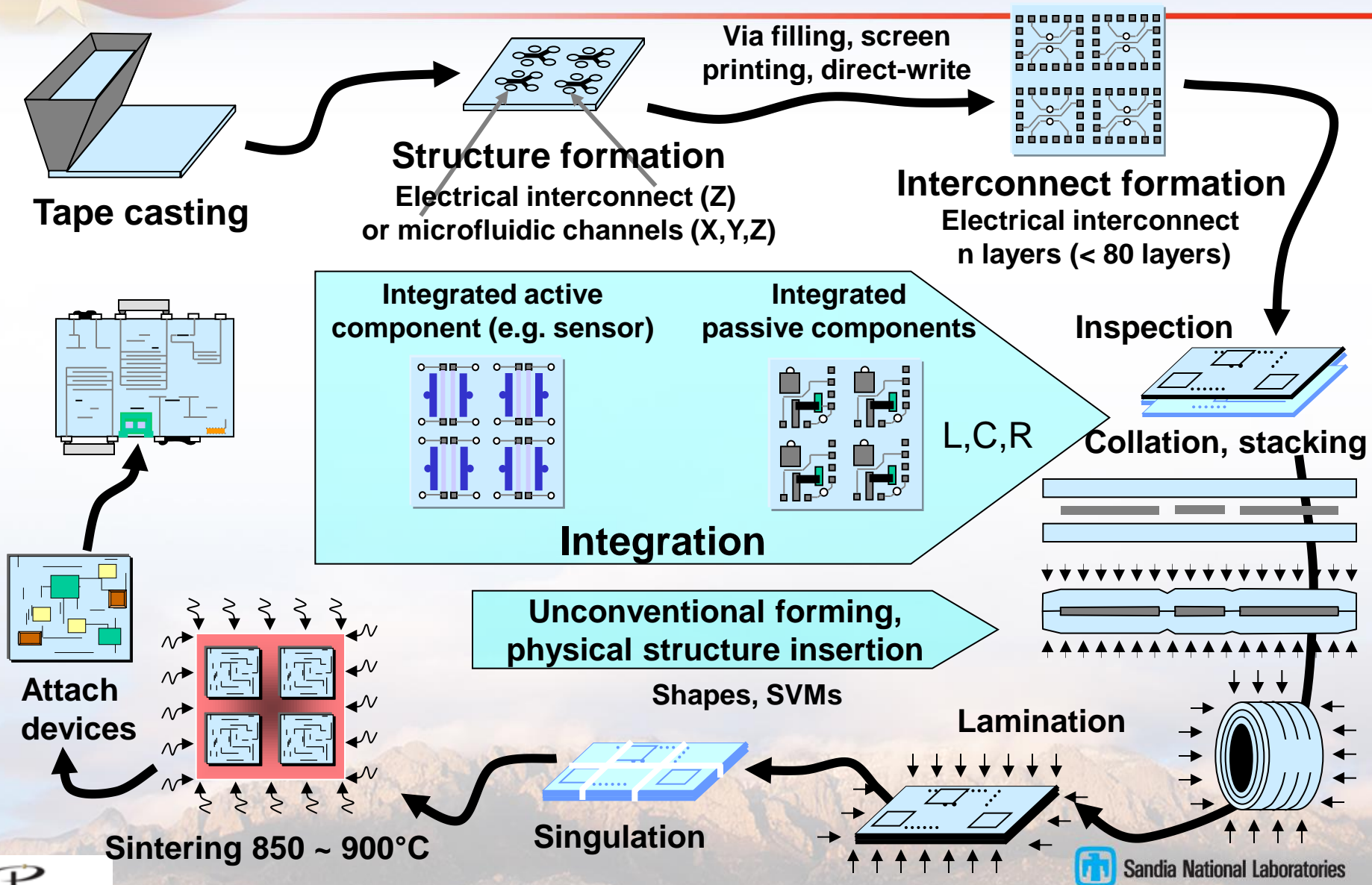




Process Flow for LTCC

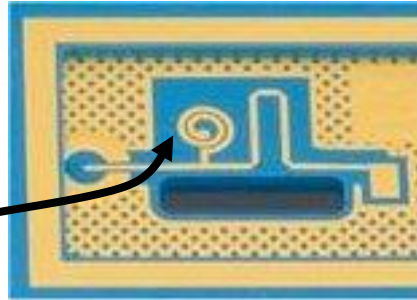
- Storage
- Conditioning
- Preparation
- Z-axis channels (vias)
- X-Y axis features (other axes)
- Collation
- Lamination
- CoFiring
- Post-Processing

LTCC Processing

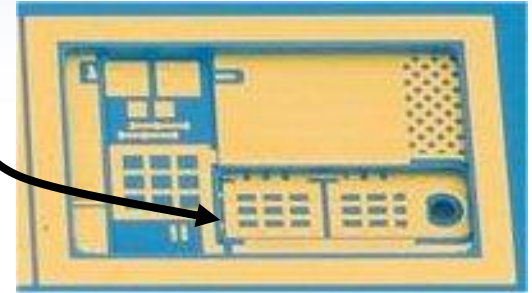


Planar MCM Features

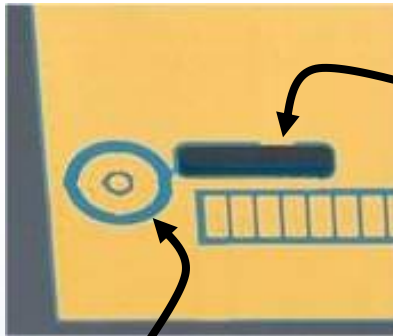
Integral
limiter



Multiple
cavity
levels



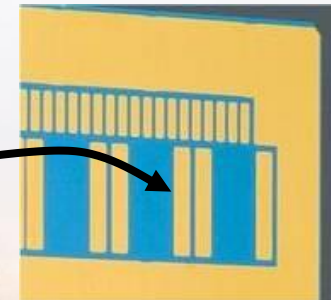
Cutouts for
high-power
devices



Connectors

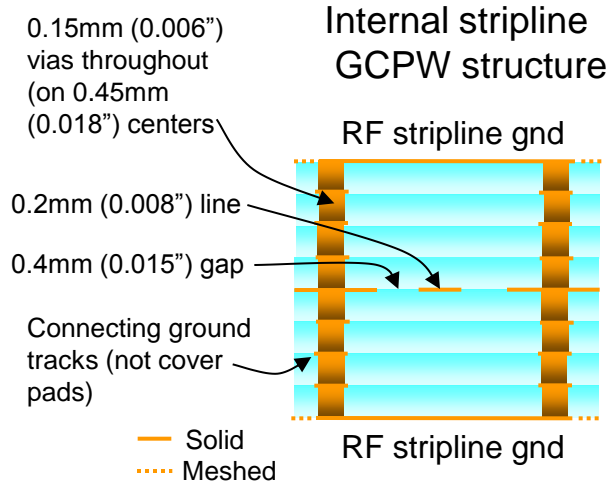


Discrete
component
pads

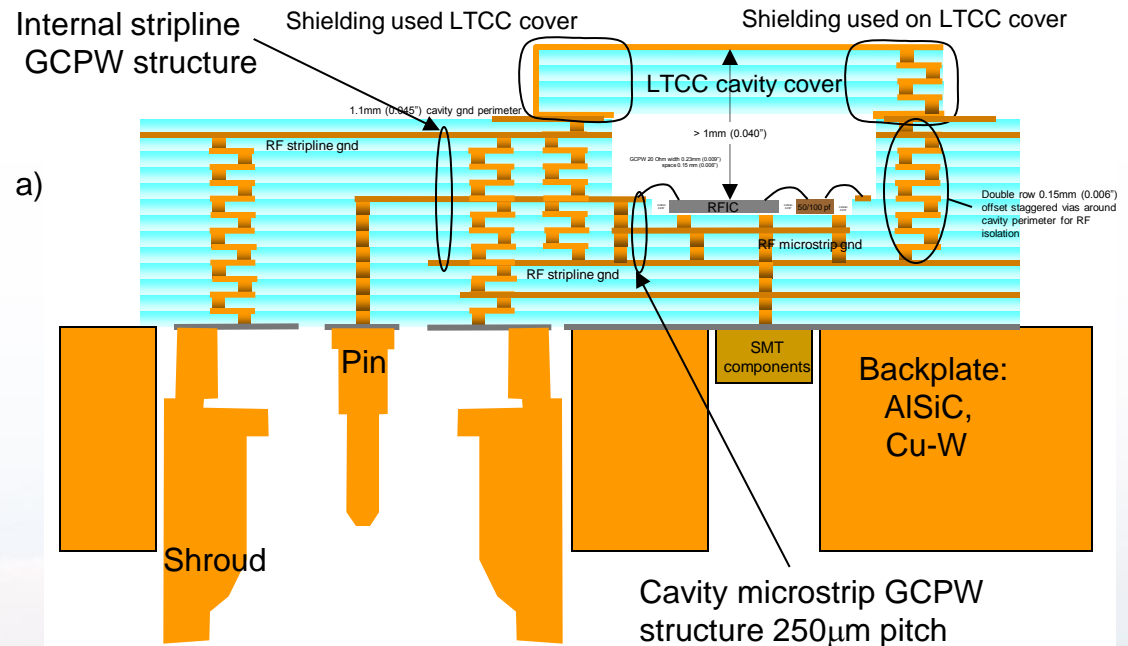
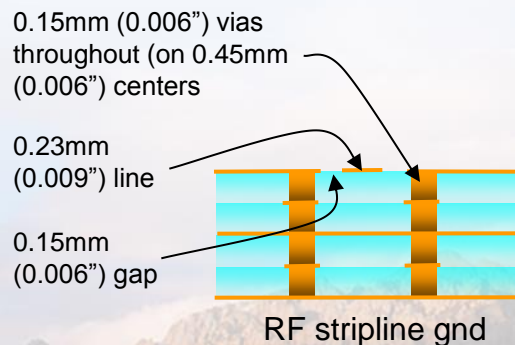


1 cm

MCM: Sectional View



Cavity microstrip GCPW
structure 250μm pitch



Well-suited to RF features; stripline, microstrip.



Structuring

- Punching
- Milling (unfired or fired)
- Laser-ablation (unfired or fired)

Designed Experiment: Punching

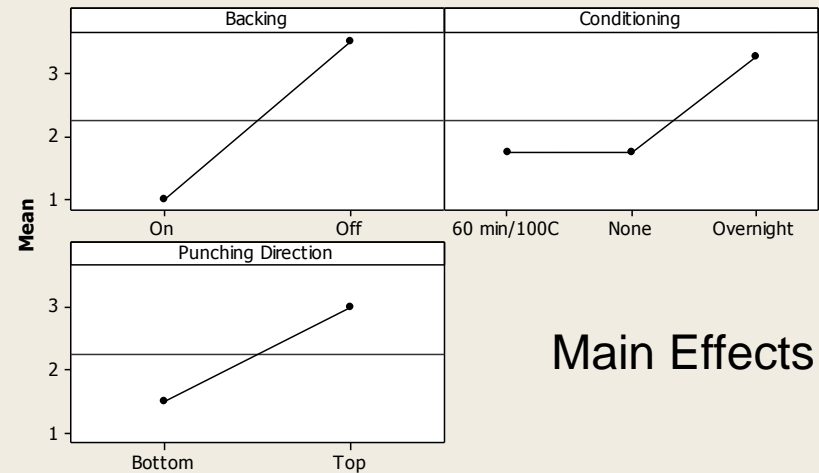
Experimental Matrix

Std Order	Run Order	Backing	Conditioning	Punch Direction	Surface Cracks	Bore Cracks	Perim. Surf. Def.	Ceramic Debris	Entrained Backing	Overall
1	1	On	1h@100°C	Bot	1	1	1	7	4	14
2	10	On	1h@100°C	Top	1	10	7	1	7	26
3	2	On	None	Bot	1	1	4	4	1	11
4	4	On	None	Top	1	1	7	1	1	11
5	6	On	16h@20°C	Bot	1	1	1	4	4	11
6	11	On	16h@20°C	Top	1	7	7	1	1	17
7	9	Off	1h@100°C	Bot	1	4	4	4	1	14
8	3	Off	1h@100°C	Top	4	4	7	4	1	20
9	5	Off	None	Bot	1	4	4	4	4	17
10	8	Off	None	Top	4	10	4	1	1	20
11	7	Off	16h@20°C	Bot	4	7	4	7	1	23
12	12	Off	16h@20°C	Top	7	10	10	1	1	29

With respect to Surface Cracking

Main Effects Plot for Surface Cracks

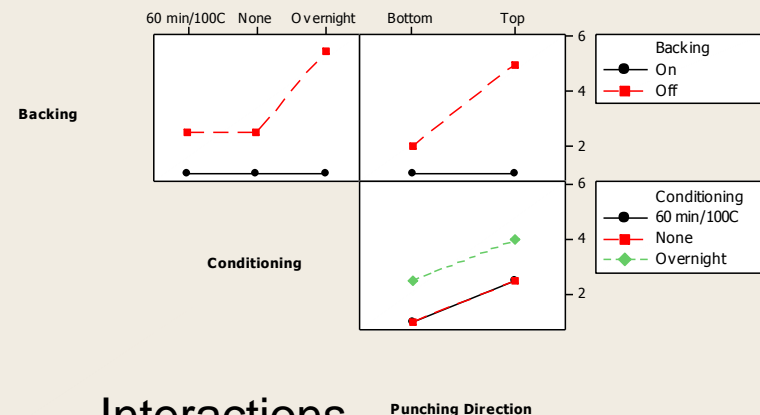
Data Means



Main Effects

Interaction Plot for Surface Cracks

Data Means



Interactions

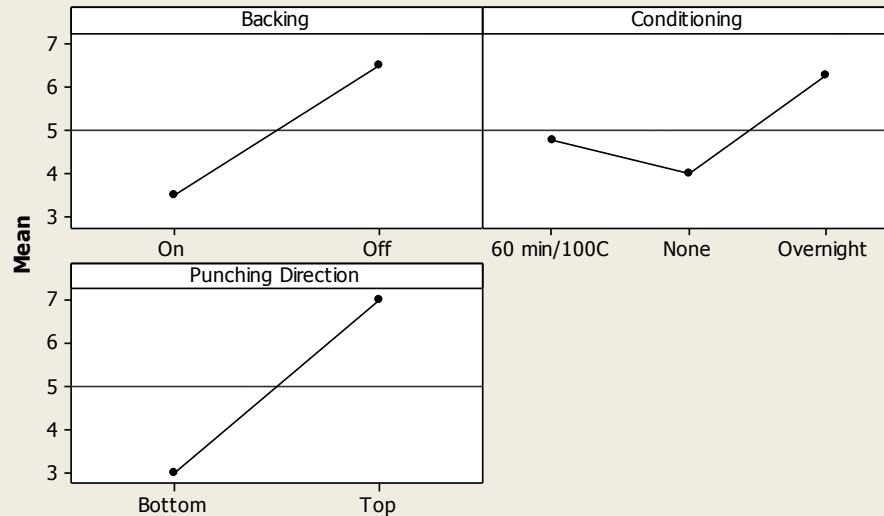
Punching Direction

Designed Experiment: Punching

With respect to Bore Cracking

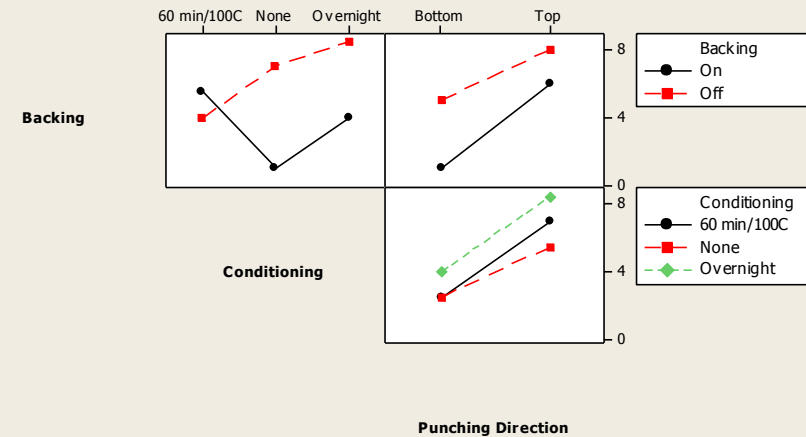
Main Effects Plot for Bore Cracks

Data Means



Interaction Plot for Bore Cracks

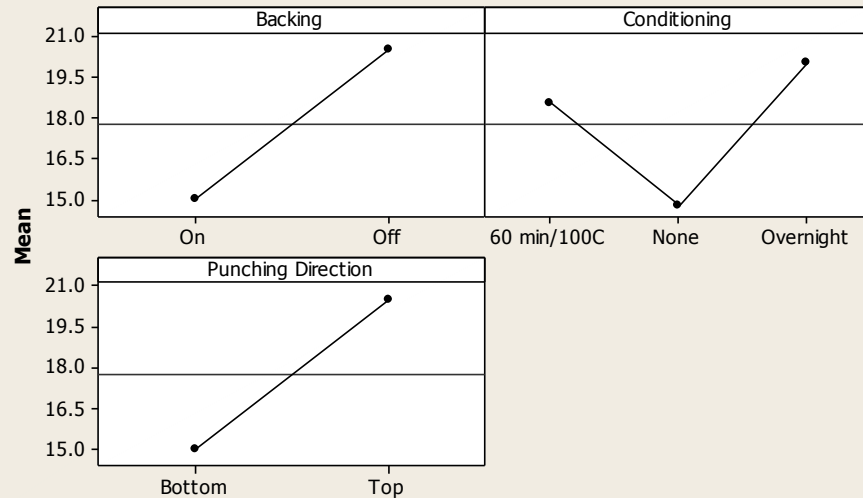
Data Means



Overall Punching

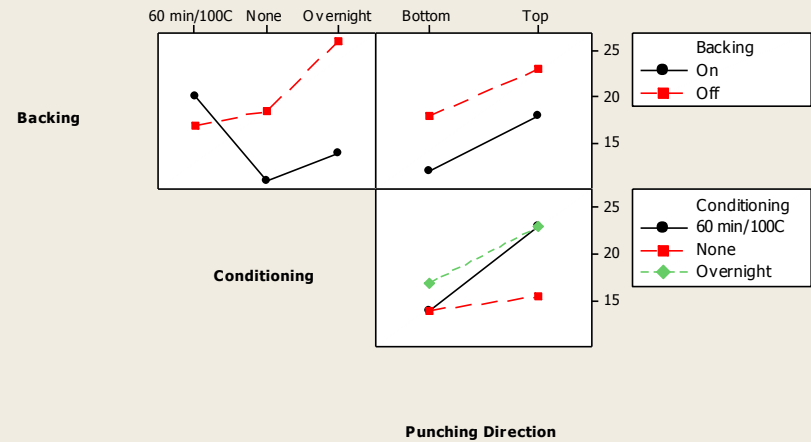
Main Effects Plot for Overall

Data Means



Interaction Plot for Overall

Data Means



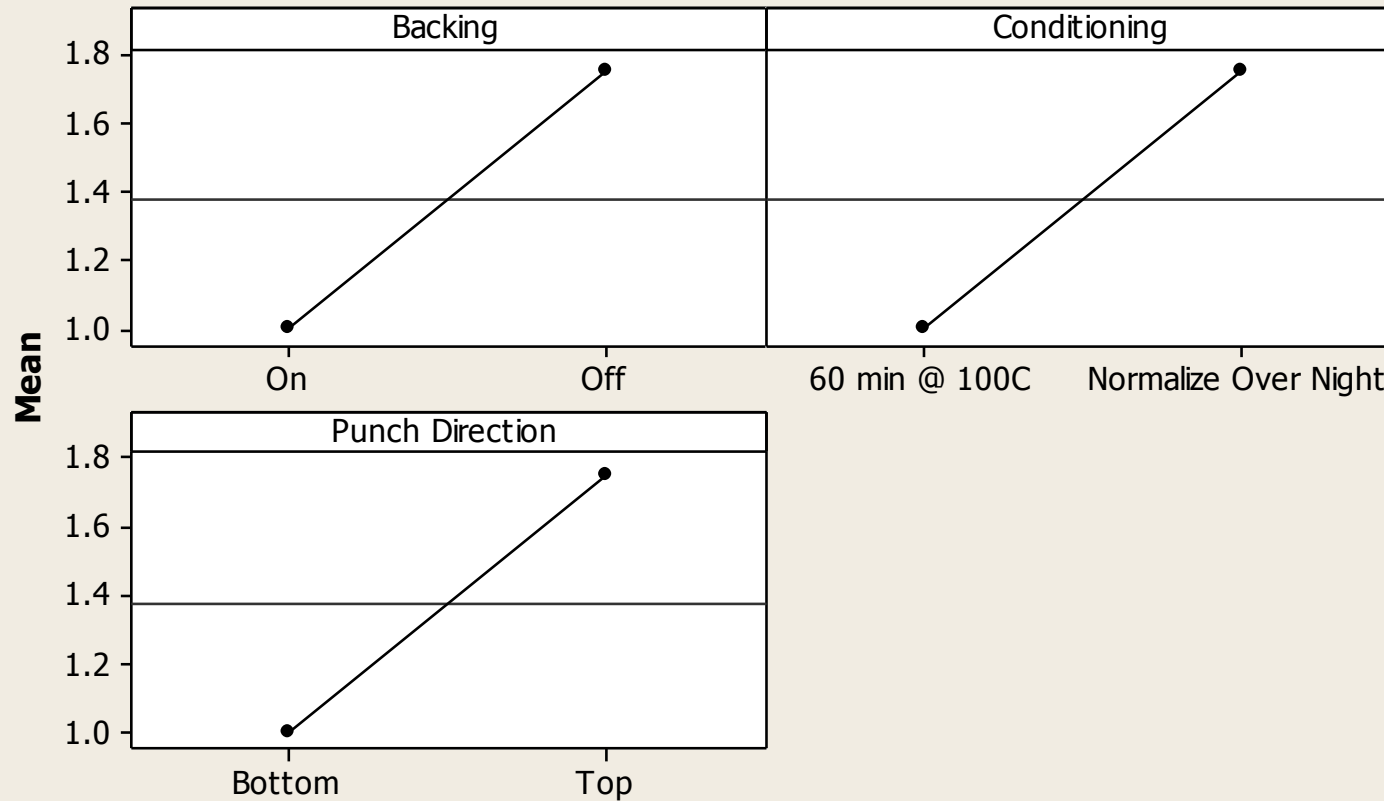
Designed Experiment: Punch #2

	Order	Back.	Cond.	Dir.	Surf.	Bore	Def	Debris
5	1	on	1h@100C	top	1	4	4	1
1	2	on	1h@100C	bottom	1	1	4	4
4	3	off	16h@20C	bottom	1	4	1	4
6	4	off	1h@100C	top	1	4	1	4
7	5	on	16h@20C	top	1	4	4	1
3	6	on	16h@20C	bottom	1	1	1	4
8	7	off	16h@20C	top	4	4	1	4
2	8	off	1h@100C	bottom	1	4	1	1

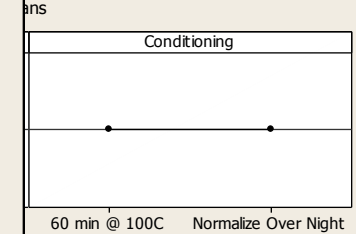
Main Effects and Interactions

Main Effects Plot for Surface Cracks

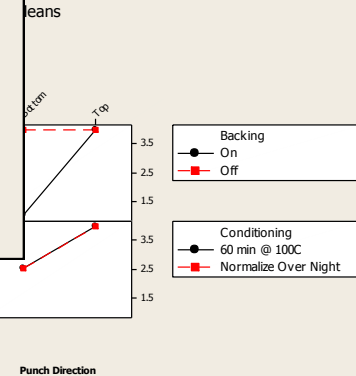
Data Means



for Bore Cracks

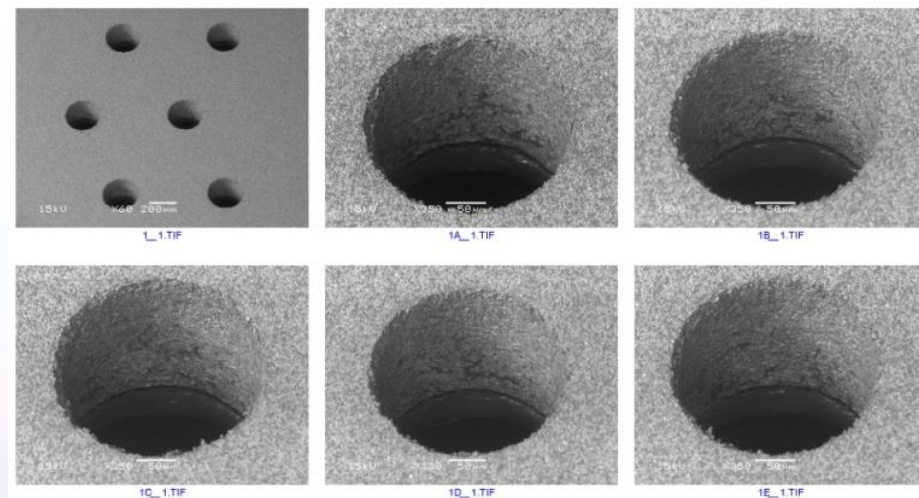
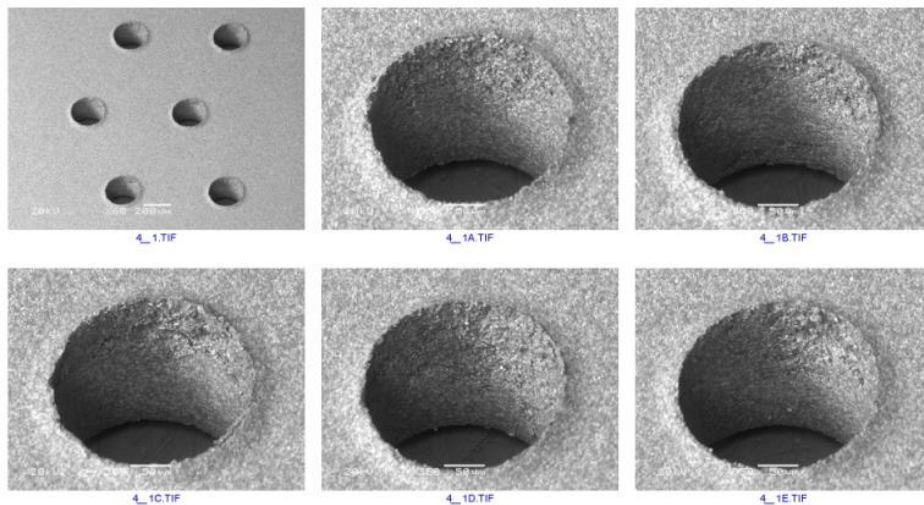


for Bore Cracks





Examples

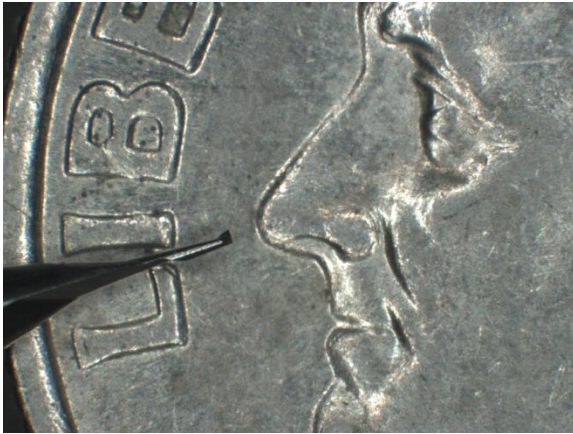




Milling

- Why Mill Unfired Tape?
 - The best mold insert possible!
 - Superior to
 - Metal, elastomer,
- Metallized cavity floors/walls
 - Sense-mode machining
- Drawbacks to Milling
 - Machining rates/material behavior
 - Dulling of tools from a ceramic/glass loaded polymer
 - Not much different than sandpaper

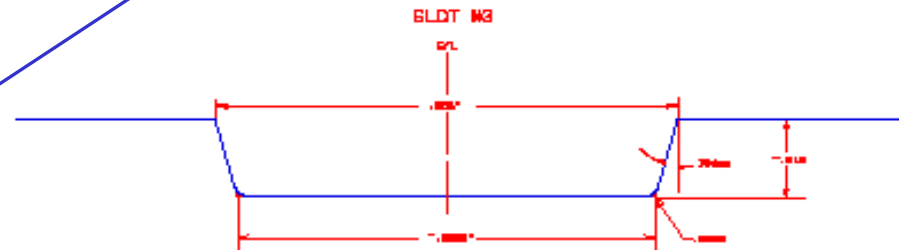
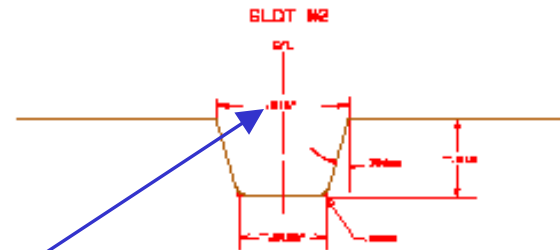
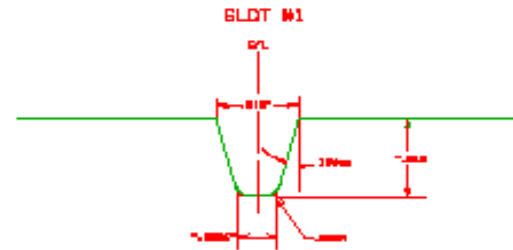
Schmoll Tooling



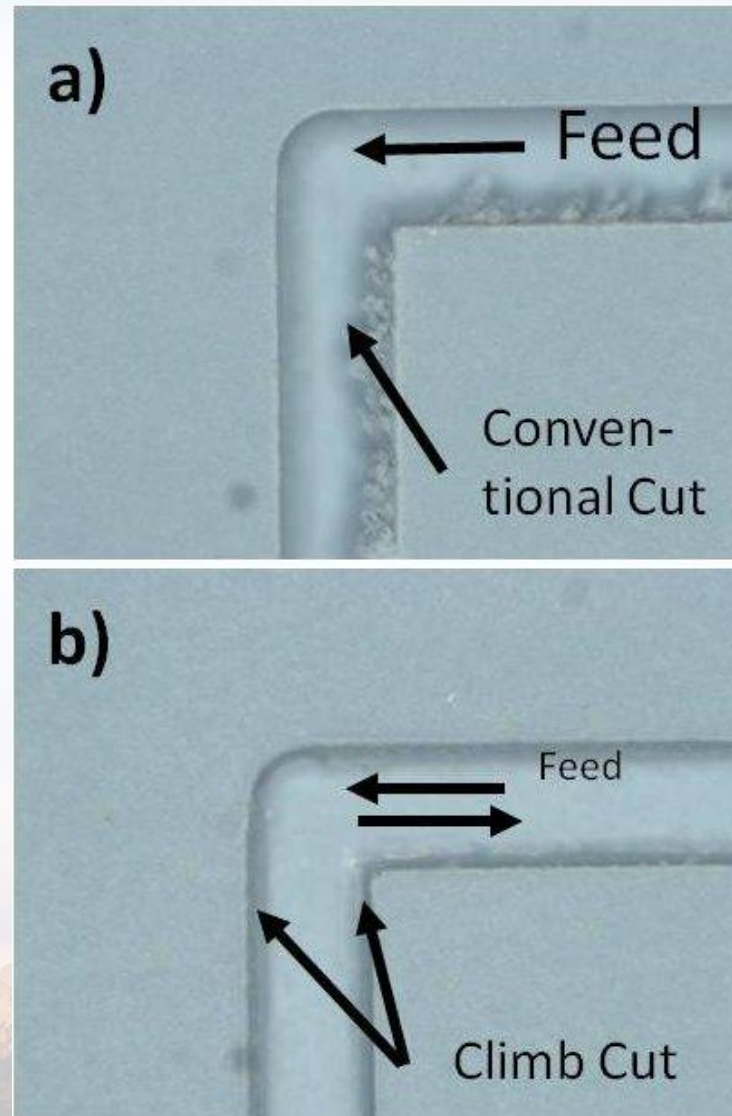
.010" Ø Single Flute End Mill



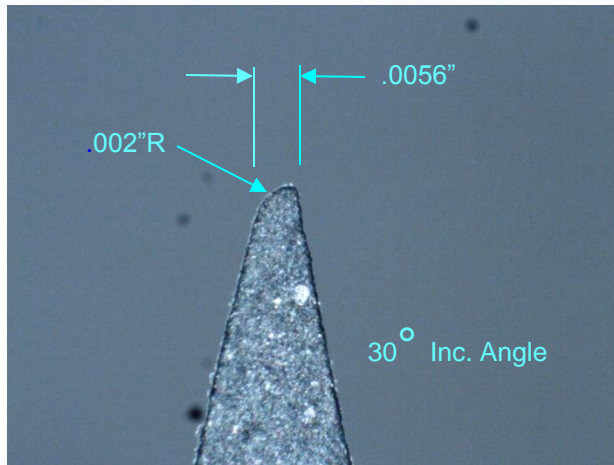
Pantograph Style Tool



Green Machining

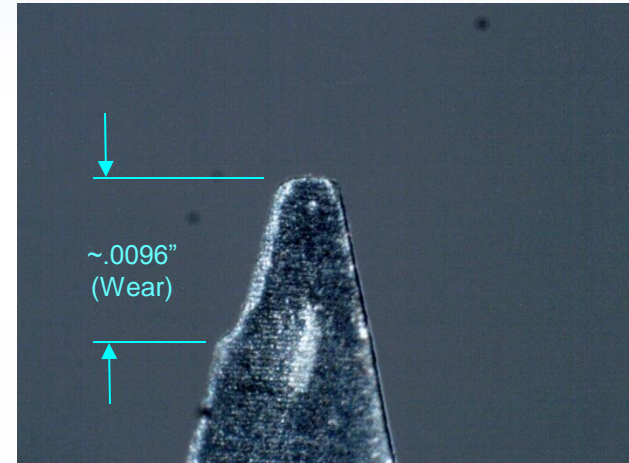


Tool Wear – Engraving Cutters

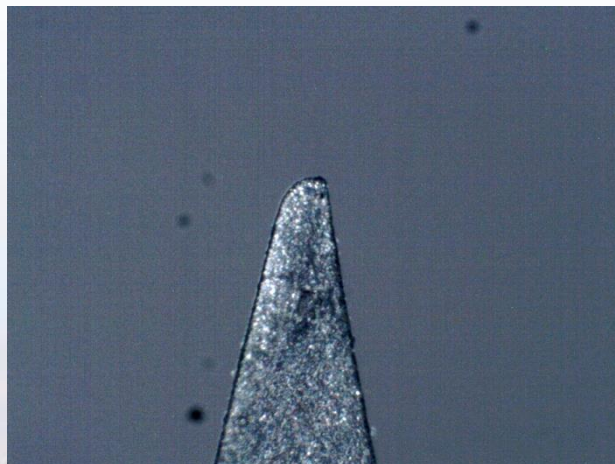


Unused CVD .010" Ø Pantograph Tool

(115x)



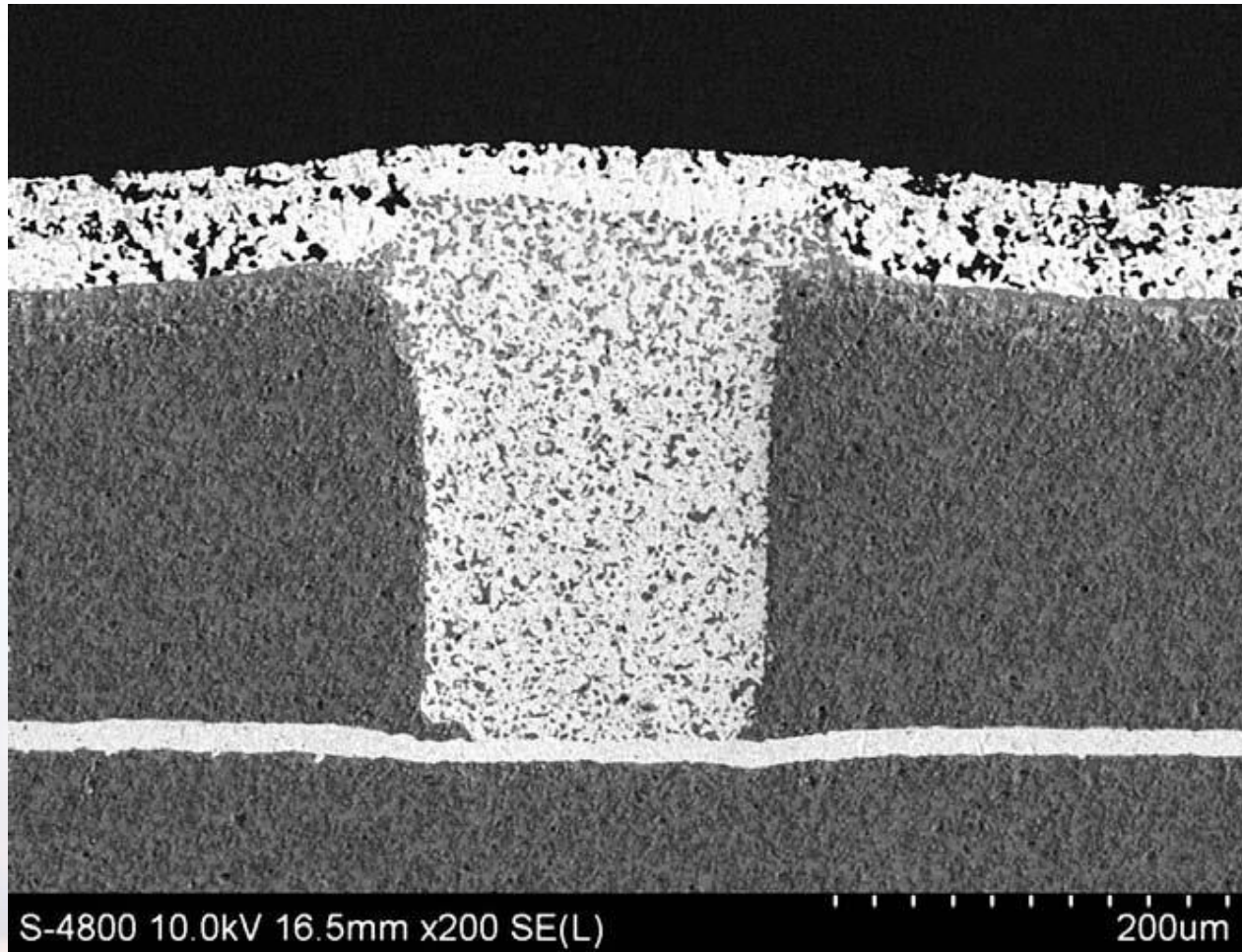
Worn non-Coated .010" Pantograph Tool after Milling ~400 linear inches



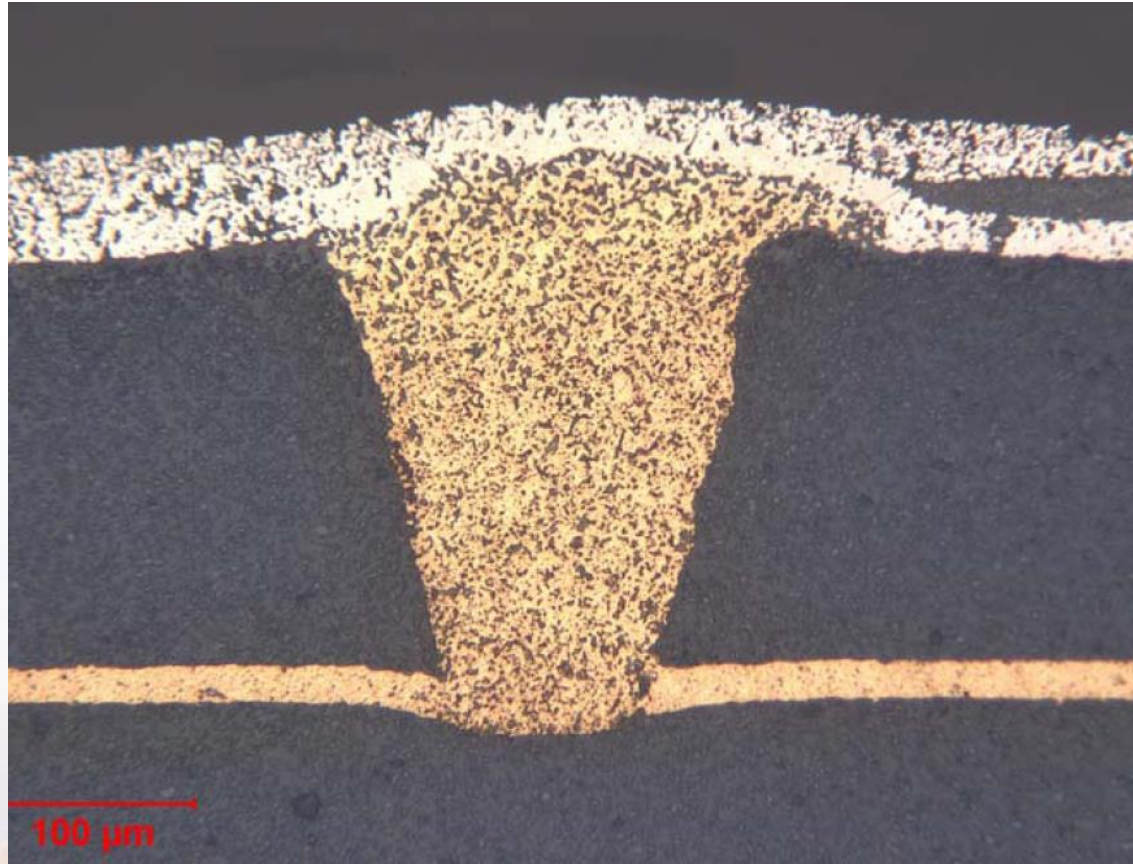
Used CVD COated Pantograph Tool after Milling ~2400 linear inches

- CVD Diamond Coating 8-10 micron thick Grown" . Directly on Micro-Grain Carbide Tool
- Hardness (88-98 GPa) & COF (.05 - .3) = Diamond
- Provides 50x Cutter Life
- Non-Conductive - Does Not Support Conductive . (Sensing) Depth Control
- Investigate: Boron Ion Doping of Diamond Coating Cryogenic Treatment (Tempering)

Cross Section: Mill to GP



Cross Section: Angled Walls

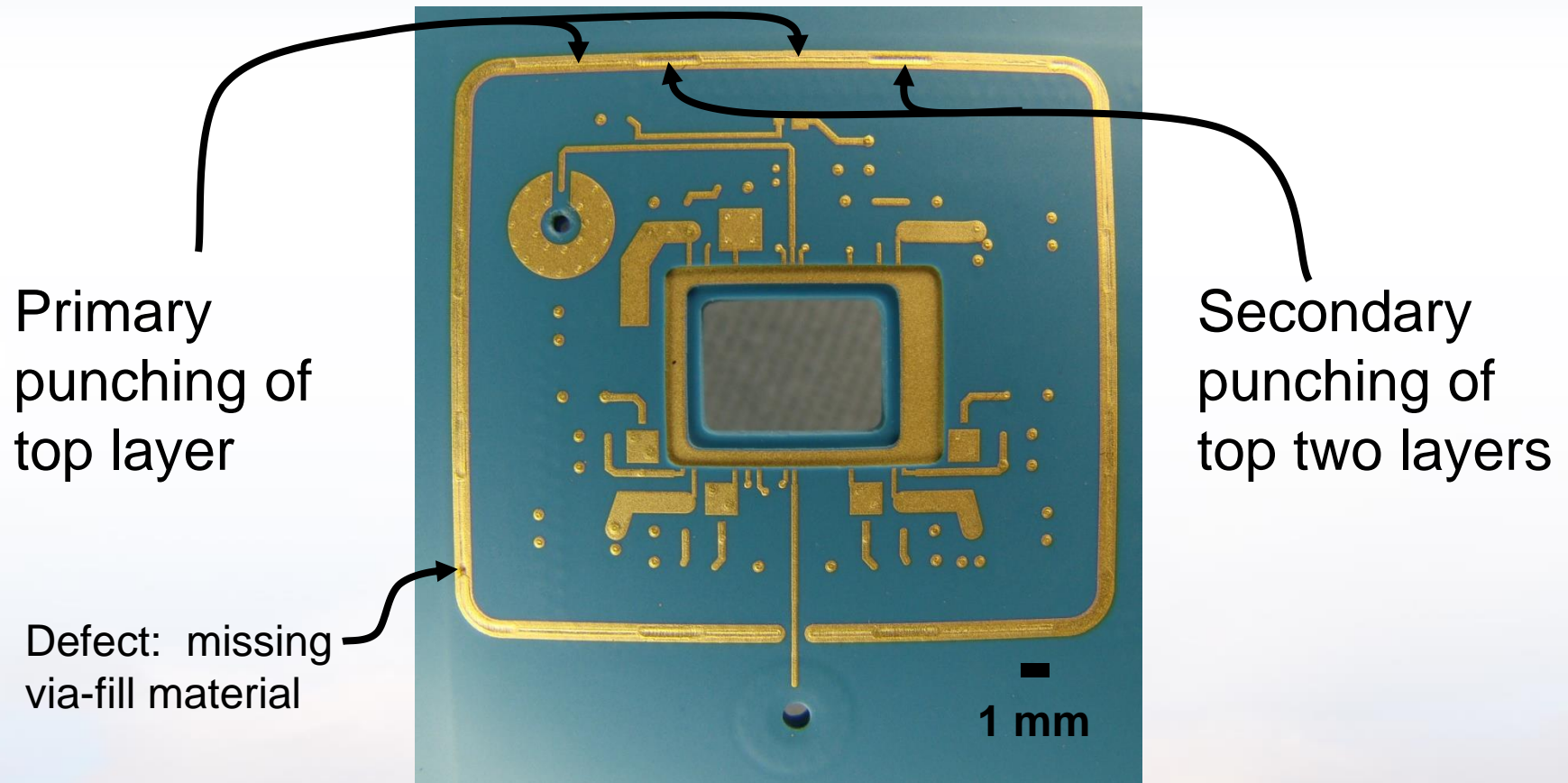


Milling Tool



Fired Solid Wall

(eight layer test fixture)



Solid wall covered by cofired barrier layer; No cracks.



Kansas City Plant
National Security Agency



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Applications of Laser Etching

- Definition of conventional circuitry
- Minimal etching approach
- Definition of unfired circuitry
- Depth engraving to a buried ground plane



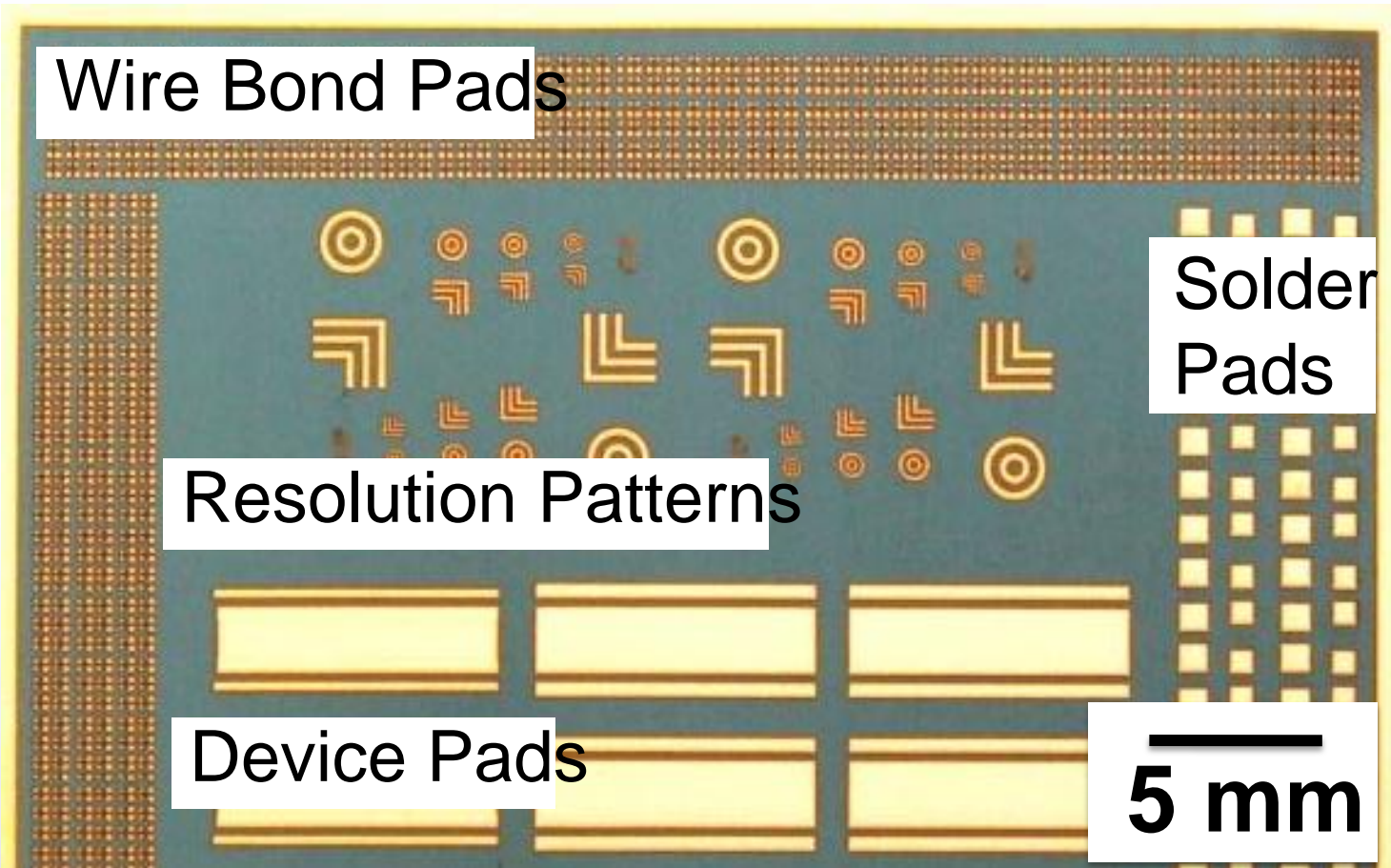
Wire Bond Pads

Solder
Pads

Resolution Patterns

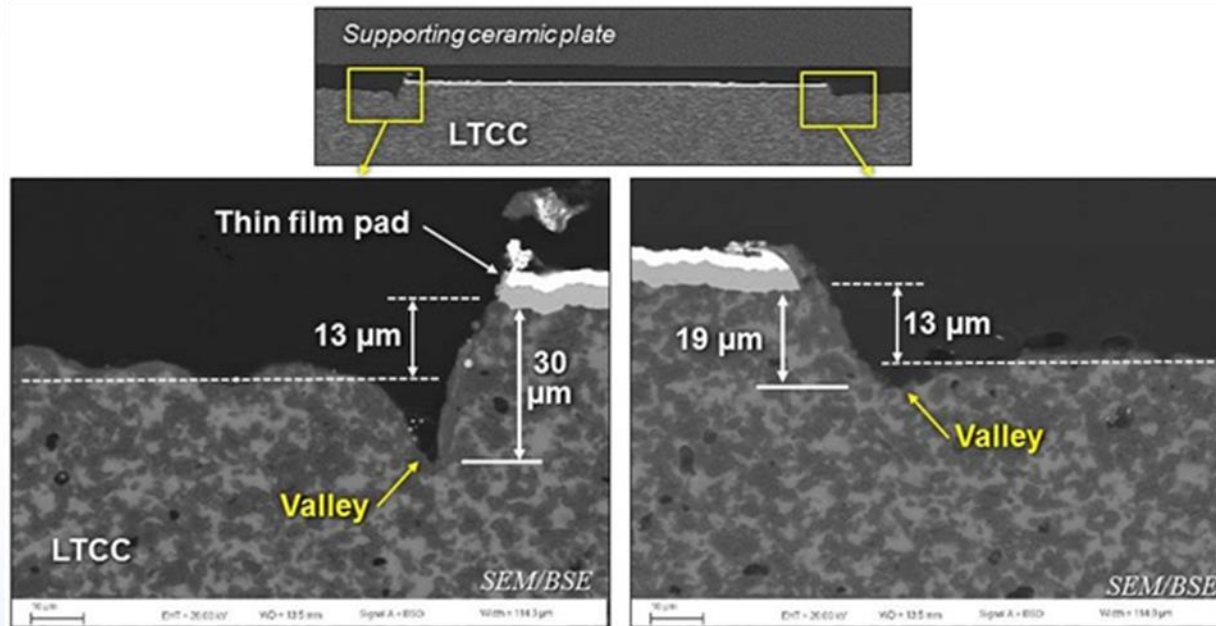
Device Pads


5 mm



- LPKF U1 UV Laser
- SEM/SE and BSE images follow  Sandia National Laboratories

Phase Three



U3 process parameters:

- 6.67 watts laser power
- 15 μm beam spot size
- 12 μm beam pulse width
- 250 mm/s travel speed
- One hatch/contour pattern

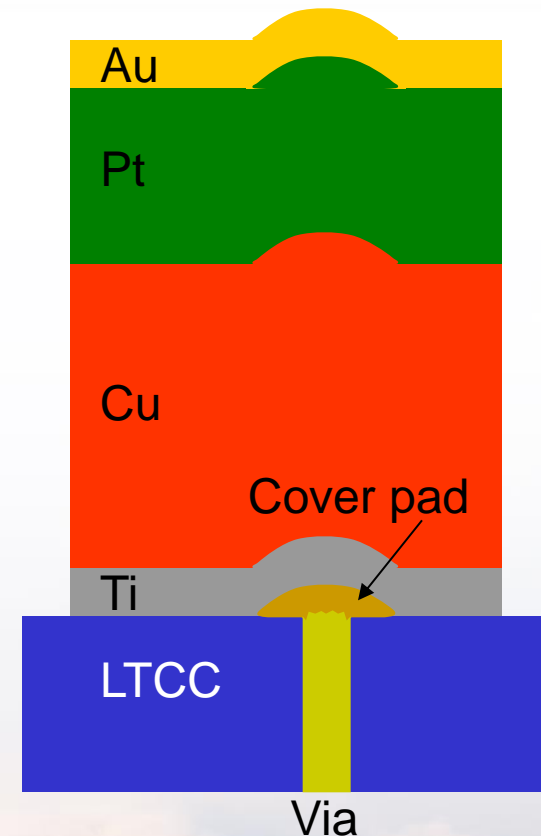


The Bane of LTCC

- Shrinkage – not so bad
- Shrinkage tolerance is the problem!
- Design rules
- Fabrication practices
- Production quantities

Thin Film Multilayer

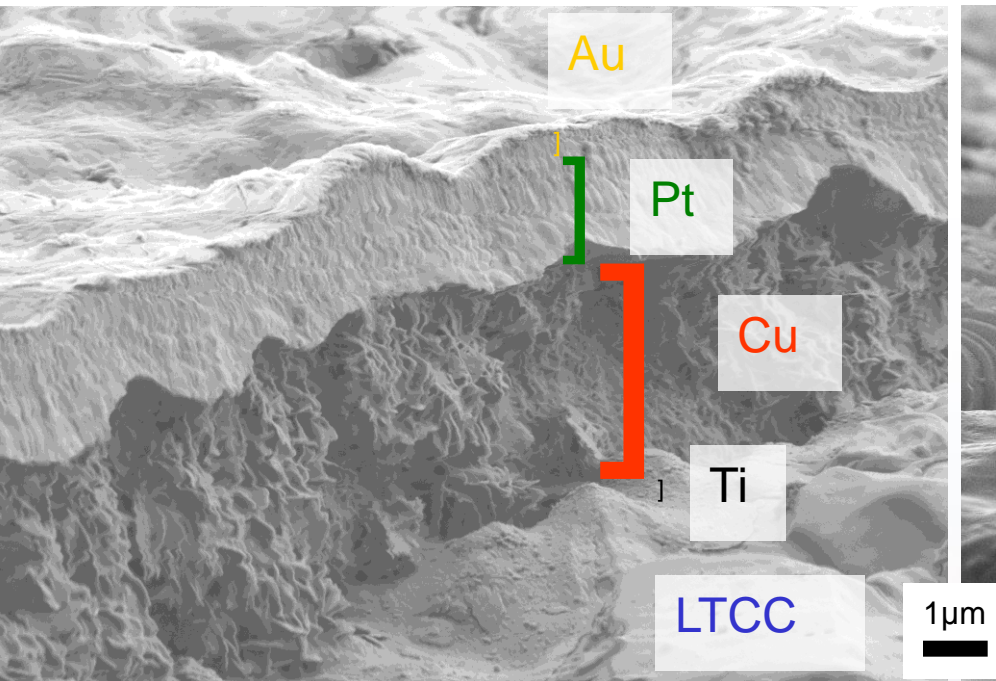
- Goal: single thin film material that satisfies all requirements:
 - Solder connectivity;
 - Wire bond connectivity;
 - RF conductivity;
 - Adhesion.
- Solution: Ti/Cu/Pt/Au multilayer (total $6.45\mu\text{m}$):
 - $0.2\mu\text{m}$ Ti \Rightarrow adhesion;
 - $4.0\mu\text{m}$ Cu \Rightarrow RF conductivity, pure metal;
greater than 2 times skin depth at
single digit GHz;
 - $2.0\mu\text{m}$ Pt \Rightarrow robust solder connectivity;
barrier for cross-diffusion of Cu
and Au or Sn;
 - $0.25\mu\text{m}$ Au \Rightarrow wire bond connectivity;
wetting for solder connectivity;
keeps layers inert over time;
 - Thick film cover pads over vias for topography
issues;



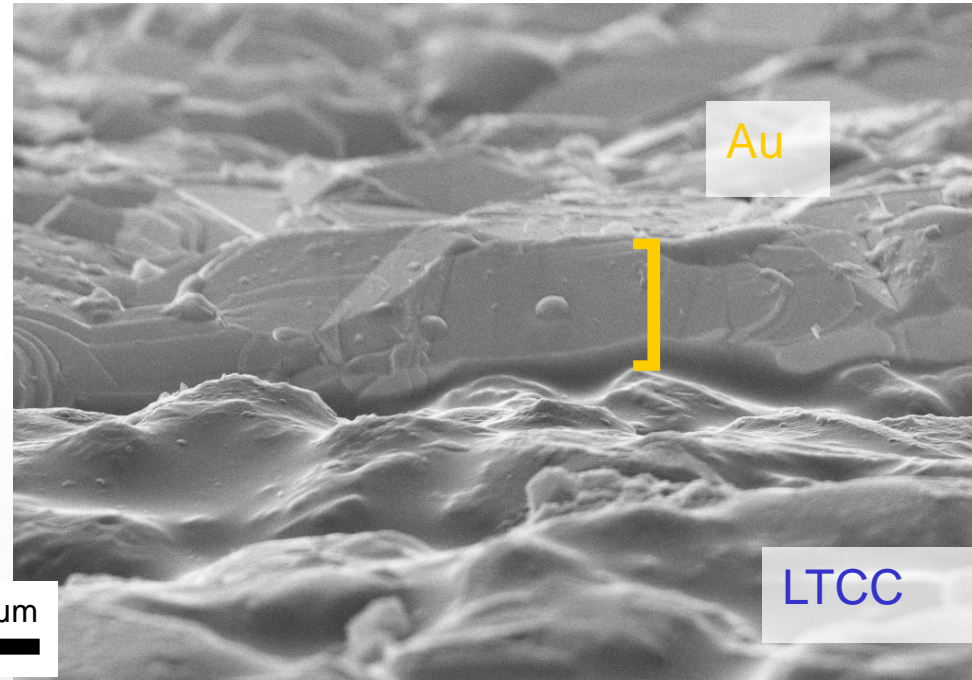
Thin Film Cross Section
(not to scale)



Thin Film vs. Thick Film



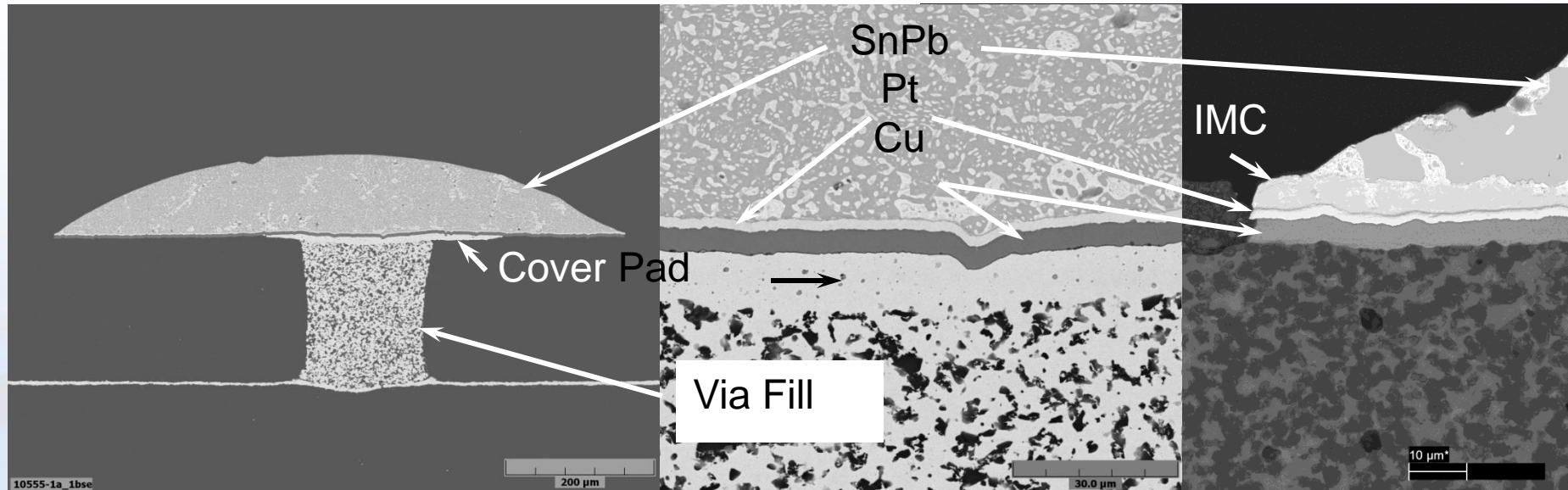
Thin film line edge



Thick film line edge

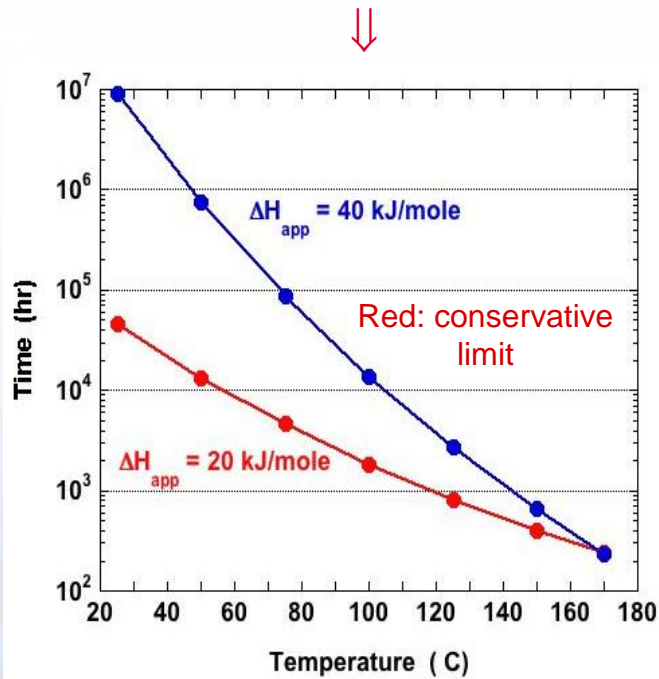
SnPb Solder Connectivity

- Thin film surface wets extremely well.
- SnPb dissolves Au, forms intermetallic layer (IMC) with Pt.
- Solder joints exhibit excellent strength:
 - Shear test:
 - 0402 from 4.2lbs as soldered to 3.2lbs after aging at 170°C for 25 days;
 - 0603 from 6.0lbs as soldered to 4.6lbs after aging at 170°C for 25 days;
 - Sebastian-like pull test:
 - Soldering at 214°C: 35lbs after 15s up to 37lbs after 120s;
 - Soldering at 290°C: 27lbs after 15s down to 22lbs after 120s;
 - Approximately 24lbs constant after 1 to 15 5s solder-dipping cycles at 290°C.

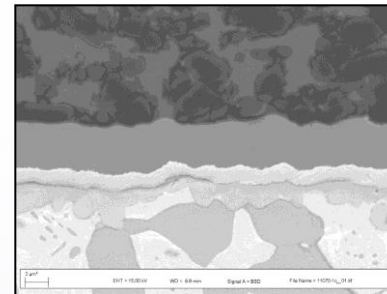


SnPb Solder Solid State Aging

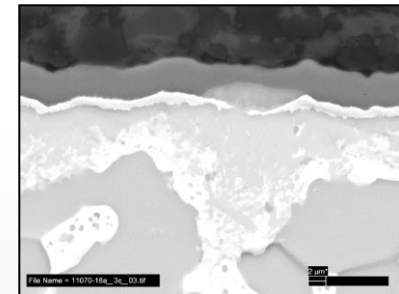
- Temperatures between 55°C and 170°C.
- Times between 2 and 25 days (longer times still under evaluation).
- Without solder: thin film layer thicknesses constant.
- With solder:
 - Breakdown of thin film structure at 170°C between 10 and 25 days;
 - Adhesion not lost after 25 days at 170°C;
 - Assume aging limit is 10 days at 170°C.



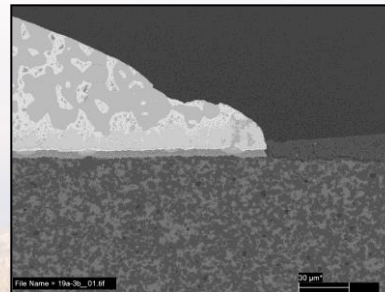
Lifetime limit based on temperature



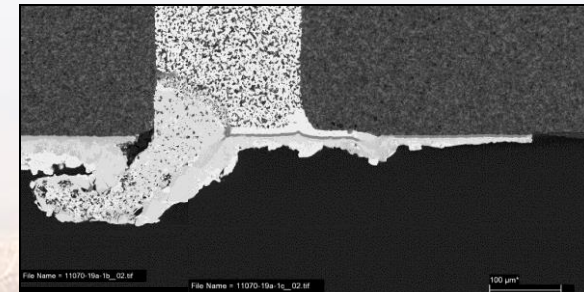
135°C, 10 days
large solder amount



170°C, 10 days
large solder amount



170°C, 25 days, edge,
small solder amount



170°C, 25 days, large solder amount



Benefits from Thin Film on LTCC

- Increased reliability.
- Robust in assembly.
- Versatile in assembly, multifunctional single metallization for soldering and wire bonding.
- Superior reworkability, hand soldering.
- Superior electrical and RF performance.
- Finer Lines and Spaces, smaller geometry.
- Enables higher frequencies.
- Positioning for thin film passives (e.g. Band Pass Filter (BPF), capacitors).
- Open to further development, e.g.:
 - AuSn soldering;
 - Fully integrated thin film passives.



Bulk Inclusions

- EMI shielding structures
- Heat sinks
- Filters
- Familiar problem: What metamaterial achieves primary purpose while remaining integral to structure?
 - Adequate thermal conductivity with proper CTE?
 - Cofirable
 - Assembly (post-processing)



Adaptive Techniques

- Laser direct imaging
- Laser ablation
- Additive manufacturing-direct write
- Relaxed design rules



Summary

- Structuring techniques continue to progress.
- Shrinkage tolerance control is paramount.
- Thin films are effective, if not conventional



Thank you for your attention