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Improving the Sandia Test Protocols with Advanced Inverter Functionality Testing of INV3, FW21, VV11, and L/HVRT

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Abstract

Sandia National Laboratories has created a test protocol for IEC TR 61850-90-7 advanced distributed energy resource (DER) functions, titled "Test Protocols for Advanced Inverter Interoperability Functions," often referred to as the Sandia Test Protocols. This document is currently in draft form, but has been shared with stakeholders around the world with the ultimate goal of collaborating to create a consensus set of test protocols which can be then incorporated into an International Electrotechnical Commission (IEC) and/or Underwriters Laboratories (UL) certification standard. The protocols are designed to ensure functional interoperability of DER (primarily photovoltaic (PV) inverters and energy storage systems) as specified by the IEC technical report through communication and electrical tests. In this report, Sandia exercises the electrical characterization portion of the test protocols for four functions: constant power factor (INV3), volt-var (VV11), frequency-watt (FW21), and Low and High Voltage Ride Through (L/HVRT). The goal of the tests reported here was not to characterize the performance of the equipment under test (EUT), but rather to (a) exercise the draft Sandia Test Protocols in order to identify any revisions needed in test procedures, conditions, or equipment and (b) gain experience with state-of-the-art DER equipment to determine if the tests put unrealistic or overly aggressive requirements on EUT operation. In performing the work according to the current versions[1] of the protocols, Sandia was able to identify weaknesses in the current versions and suggest improvements to the test protocols.

[1] The versions of the test protocols used for this testing were:
INV1: Version 2.2 from 17 July 2013
VV11: Version 2.3 from 1 Aug 2013
FW21: Version 4.0 from 1 Aug 2013
L/HVRT: Version 2.0 from 10 May 2013

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NOMENCLATURE

AC	Alternating Current
CT	Current Transformer
DC	Direct Current
DER	Distributed Energy Resource
DETL	Distributed Energy Technologies Laboratory
DOE	Department of Energy
EUT	Equipment Under Test
Hz	Hertz
IEC	International Electrotechnical Commission
I-V curve	Current-Voltage Curve (of a PV module, string or array)
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
kW	Kilowatt
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracker
PV	Photovoltaic
RLC	Resistive/Inductive/Capacitive
SNL	Sandia National Laboratories
UL	Underwriters Laboratories, LLC
V_{OC}	Open Circuit voltage

1. INTRODUCTION

Sandia National Laboratories has created test protocols for interoperability functions defined in IEC TR 61850-90-7 [1]. The Sandia Test Protocols ("Test Protocols for Advanced Inverter Interoperability Functions") [2, 3] provides a recommended set of instructions to certify DER products to new international interoperability requirements. The types of advanced DER interoperability functions and modes are included in Table 1.

Table 1: Interoperability functions and modes.

Command/ Request	Function	General Category
INV1	Connect/Disconnect	Immediate control functions
INV2	Adjust Max Generation Level	
INV3*	**Adjust Power Factor**	
INV4	Charge/Discharge Storage	
INV5	Pricing Signal for Charge/Discharge of Storage	
VV11*	**Volt-Var Mode**	Volt-var management modes
VV12	Volt-Var Mode	
VV13	Volt-Var Mode	
VV14	Volt-Var Mode	
FW21*	**Frequency-Driven Active Power Reduction**	Frequency-watt management modes
FW22	Frequency-Driven Active Power Modification	
TV31	Dynamic Reactive Power Support	
L/HVRT*	**Low/High Voltage Ride Through**	Voltage Ride Though
WP41	Feed-in Power Controls Power Factor	Watt-power factor behavior modes
WP42	Feed-in Power Controls Power Factor	
VW51	Generation to Smooth Voltage Variations	Voltage-watt management modes
VW52	Charging to Smooth Voltage Variations	
TMP	Temperature Mode Behavior	
PS	Signal Mode Behavior	
DS91	Modify DER Inverter Settings	Parameter setting and reporting
DS92	Event/History Logging	
DS93	Status Reporting	
DS94	Time Synchronization	

*Commands/Requests in **BOLD** were tested for this report.

At this point, some PV inverter manufacturers are including these functions in their products and the California Public Utilities Commission is considering inclusion of some of them in new Rule 21 requirements. Sandia National Laboratories, in collaboration with a manufacturer, is beginning to test the electrical characterization of some of these functions in order to:

1. Gain hands-on experience exercising the protocols
2. Learn limitations of current inverter product designs
3. Improve the Test Protocols by identifying problems with the current draft versions

Most of the test protocols are designed with two separate sections. The first section deals with *communications* from a utility simulator to the EUT and tests the interoperability of the EUT. The other section focuses on *electrical behavior characterization* of the EUT to verify the *communications* were successful. Standardized translation software from utility commands/ requests to the EUT is still under development so the *communications* elements of the test protocols were not included in these tests for this report. Only the results from the *electrical behavior characterization* are included. Furthermore, the Sandia Interoperability Test Protocols must be expanded to fully characterize the interoperability section. While the electrical tests are designed to verify the interoperability command that was sent by the utility and successfully received by the EUT, incorrectly formatted commands, incomplete commands, and erroneous commands, must also be tested to ensure robust interoperability communications.

This technology is just becoming available, so not all the functions and modes were able to be tested—or tested across the full range of test conditions—because of limitations in the software and hardware of the inverter DER. However, in order to continue the development of the Sandia Test Protocols, a subset of the functions were exercised for this report, including constant power factor (INV3), volt-var (VV11), frequency-watt (FW21), and Low and High Voltage Ride Through (L/HVRT). In many test cases, the EUT did not have the capability to perform all the recommended tests, so revised test matrices were established. This was not considered a major setback, because the goal of the tests was to improve the Sandia Test Protocols, not to characterize the EUT. In the future, more functions and modes will be available from commercial products and more thorough testing of the DER can be completed.

2. INV3 – CONSTANT POWER FACTOR TESTS

The INV3 function sets the power factor in response to a command from the utility controller or a combination of local conditions, modes, schedules, etc. A ramp rate and a delay time before starting may also be included. A timeout period may be included for reverting to the default state of the EUT if no additional INV3 commands are received.

2.1 Function Capability Table and Test Matrix for INV3

The following parameters were included in the EUT:

- *Requested power factor* – This value is entered into the front panel of the inverter. The value ranges from 0.85 capacitive (overexcited) to 0.85 inductive (underexcited).
- *Requested ramp time* – Not included with this inverter. The internal default value was used.
- *Time window* – Not included with this inverter. The default value of 0 was used.
- *Timeout period* – Not included with this inverter.

Based on these capabilities, the Test Matrix shown in Table 2 was used to test the inverter. Items crossed out reflect lack of availability. Default values that are built into the EUT internally have replaced numerical values for Ramp Rate, Time Window, and Timeout Period because the Sandia Test Protocols indicate that if the EUT does not have certain functionality (e.g., ramp rate control), default, internal values will be used. These values are built into the EUT by the manufacturer and therefore never input into the EUT (or sent via interoperability communication from the utility simulator.)

Table 2: Test Matrix for INV3.

~~Max Power (INV2)~~ ~~(% nameplate)~~	Power Factor (INV3)	Ramp Rate (% nameplate watts/sec)	Time Window (seconds)	Timeout Period (seconds)
~~100~~ N/A	1.00	Default	~~0 sec~~ Default	Default
~~50~~ N/A	MinPFOverAval (0.85 Overexcited)	Default	~~60~~ Default	~~600~~ Default
~~50~~ N/A	MinPFUnderAvail (0.85 Underexcited)	Default	~~300~~ Default	Default
~~100~~ N/A	0.5 + MinPFOverAval/2 (0.93 Overexcited)	~~10~~ Default	Default	Default
~~100~~ N/A	0.5 + MinPFUnderAvail/2 (0.93 Underexcited)	Default	Default	~~1800~~ Default

The INV2 function was not invoked because there is already a dynamic irradiance profile and INV2 has not been characterized. If multiple functions are running at the same time, it will be more difficult to determine which function causes undesirable results. This column will be removed from the Sandia Test Protocols with the next version.

2.2 Laboratory Setup

The 3 kW inverter EUT was connected to a single power supply (5 kW_{dc}) from the 20 kW PV simulator. The PV simulator was configured with two strings of 20 75-W Si modules. The

temperature in the simulator was adjusted to provide 3000 W_p of DC power at the MPP. An irradiance profile (which scales linearly to maximum DC power available) was built into the dynamic function of the PV simulator to create the power levels shown in Figure 1.

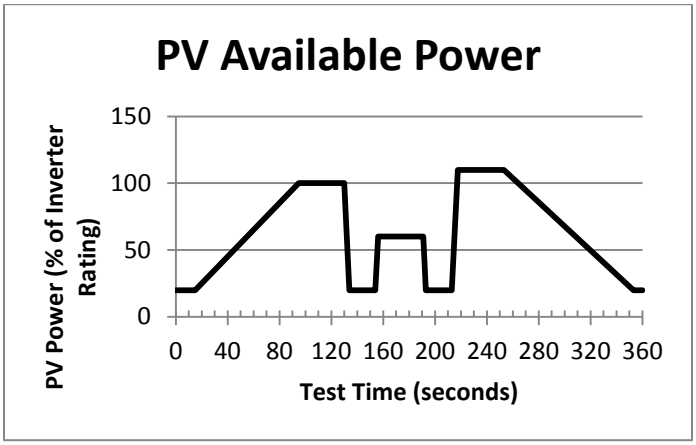


Figure 1: INV3 dynamic power profile. For details see Sandia Test Protocols.

The inverter EUT was connected to a 180 kW grid simulator (240 V, 60 Hz nominal at the EUT). This is not necessary for this test, but was chosen because it would allow for a quick transition to the other functions which require AC frequency and voltage modifications. Additionally, the use of the grid simulator guarantees repeatable testing with strict control over the grid frequency and voltage. The test configuration is shown in Figure 2.

The following data were collected during the tests:

1. DC Current
2. DC Voltage
3. AC Current
4. AC Voltage

The following were calculated in real time and recorded based on the measured signals using a program in National Instruments LabVIEW:

1. Power factor
2. Watts
3. VA
4. Vars

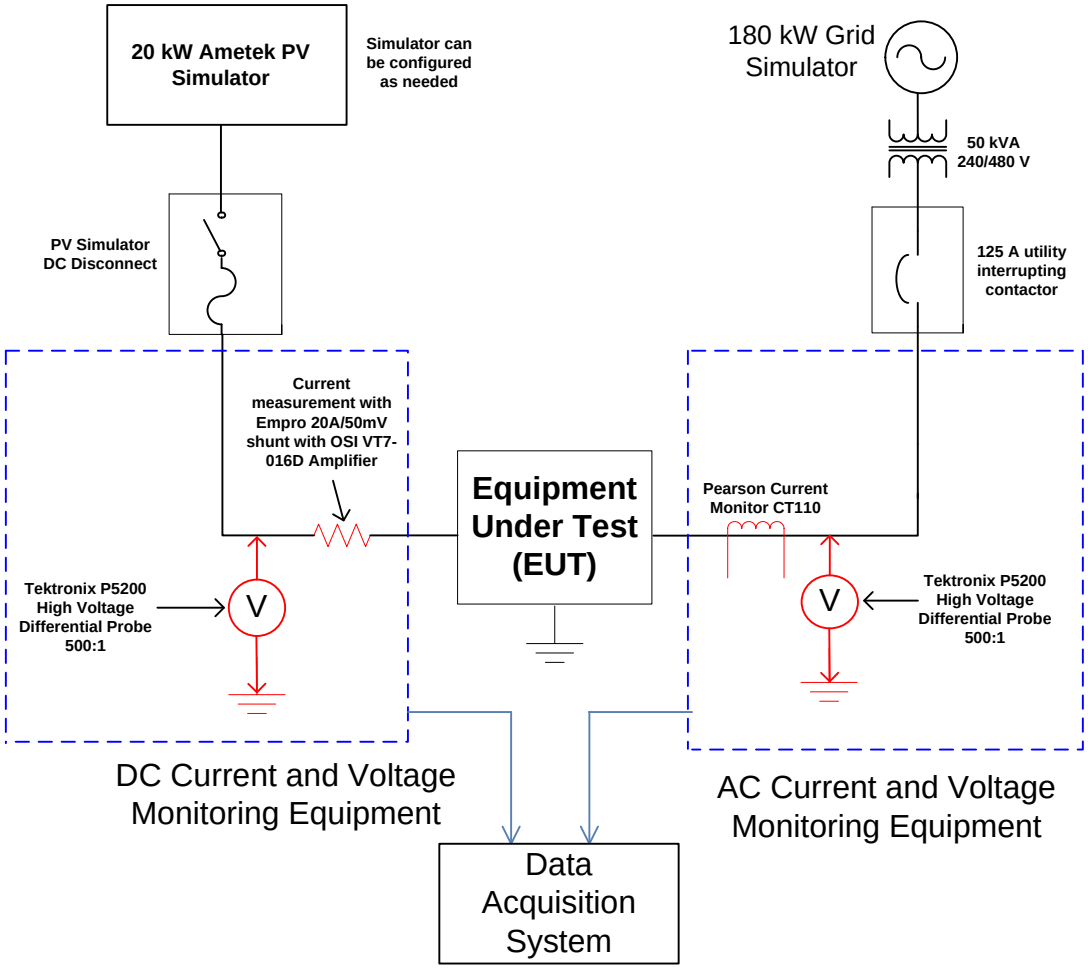


Figure 2: Configuration for INV3 Testing.

2.3 Test Procedure

The communications (interoperability) portion of the test was not performed, so only the Electrical Behavior Characterization steps were completed, as shown in Table 3. The steps taken for each of the tests listed in the Test Matrix in Table 2 were as follows:

1. The Data Acquisition System was started with data collection every 1 second.
2. The PV simulator output was set to 20% of the EUT DC power rating by setting the PV simulator irradiance to 200 W/m^2.
3. The power factor was entered into the EUT through the front panel of the inverter.
4. The inverter was allowed to come up to a steady state power level.
5. The dynamic irradiance curve in Figure 1 was simulated by the PV simulator.
6. The next power factor setpoint in the test matrix was entered into the EUT.
7. Steps 4-6 (above) were repeated until all five tests were completed.

Table 3: INV3 Test Protocol Sequence.

	Step	Task	Function	Notes
Electrical Behavior Characterization	**6**	~~Verify command was successfully executed. (DS92 and DM).~~ Conduct the test while varying input PV power according to Table A3-3, Figure A3-1.	–	Monitor output power factor level to determine if output is adjusted correctly. Measure power and power factor Determine ramp rate of response Record time For three-phase EUTs observe all three phases.
	7	Repeat test with optional parameters (Table A3-4). Each test should be repeated until behavior of the inverter is reasonably understood.	–	
Analysis	**8**	Characterize EUT's response.	**DS92; DM**	Determine how command was executed. Verify compliance with time window, ramp rate, time delay, as appropriate

2.4 Test Results

The INV3 testing took roughly one hour to conduct using the front panel of the inverter to enter the new PF setpoints. The results from the test can be seen in Figure 3. The Sandia Test Protocol does not have a pass/fail criterion for any of the tests because this is a pre-certification test standard, but this testing and data can be used for determining whether this EUT was successful with the INV3 function if performance requirements are established.

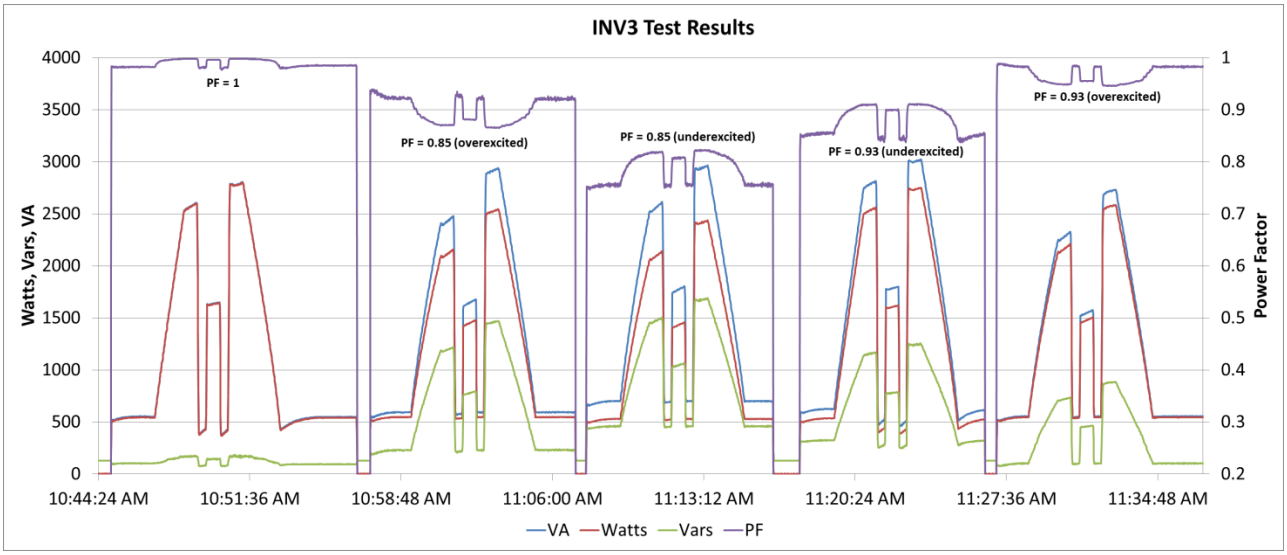


Figure 3: INV3 test results.

2.5 Recommendations for the INV3 Test Protocol

Based on these tests, Sandia identified minor changes to the test protocol. These changes include:

1. The Max Power (INV2) column in the Test Matrix should be deleted.
2. Under Section A3.2, there should be no allowance for testing with real PV since the dynamic PV profile would not be possible.
3. In Section A3.2, the utility (grid) simulator is required to run for 5 minutes at the nominal voltage *before* the communication command is sent. In the case of this inverter, changing the INV3 level requires the inverter to restart power production, so it is an inefficient use of time to have the 5 minute delay before interoperability functions are sent. In these tests, a reasonable level of steady-state operation of the EUT was established before running the dynamic irradiance profile. Steady-state operation must be defined (e.g., <1% power change in 1 minute), but this is a more appropriate starting criterion.

Other comments about INV3 testing, results, and data collection.

1. The PV simulator used for this test only allowed whole seconds between data points, so the 217.5 second data point was moved to 218. This should have little bearing on the test results or pass/fail criteria, but limitations in test equipment must be addressed as they come to light.
2. There are some quick transients but they seem to be sufficiently captured with the 1 second recorded data. Thus, saving data at 1 sample/sec appears to be sufficient. However, data sampling rates of much higher levels (e.g., 24 kHz) are required for the calculation of vars and power factor.

3. VV11 – VOLT-VAR MODE

This function defines how an inverter will provide reactive power (var) support to the grid. In the VV11 mode, the EUT provides a certain percentage of available vars, based on the system (grid) voltage. In this mode, EUT will be provided with a sequence of (voltage, reactive power) pairs that describe the volt/var setpoints. This sequence of points defines a set of voltage levels and their corresponding reactive power levels as a percentage of available reactive power range.

3.1 Function Capability Table and Test Matrix for VV11

The following parameters were included in the EUT:

- *VV11 initiation (var support with no impact on watts) with an Array of (V,Q) pairs* – These arrays (VV11 curves) were entered into the front panel of the inverter.
- *Requested ramp time* – Not included with this inverter. The internal default value was used.
- *Time window* – Not included with this inverter. The default value of 0 was used.
- *Timeout period* – Not included with this inverter.

Based on these capabilities, the Test Matrix shown in Table 4 was used to test the inverter. The yellow test was added to the sequence because it was deemed necessary to test the EUT at rated power; a true VV11 function with watt-priority will not source any vars when operating at 100% of rated power. Items crossed out reflect that ramp rates, random time window delay, and time options were not tested because the EUT did not have this functionality.

Table 4: Test Matrix for VV11. The yellow test was added to the sequence.

Test	EUT Initial Operating State	Volt/Var Initiation	Volt/Var [V,Q] Array				Requested Ramp Time (% VArAval/s)	Time Window (seconds)	Timeout Period (seconds)
1	100% rated power, unity power factor	Binary, 1	V1	97	Q1	50	-	-	-
			V2	99	Q2	0			
			V3	101	Q3	0			
			V4	103	Q4	-50			
2	50% rated power, unity power factor	Binary, 1	V1	97	Q1	50	-	-	-
			V2	99	Q2	0			
			V3	101	Q3	0			
			V4	103	Q4	-50			
3	90% rated power, unity power factor	Binary, 1	V1	97	Q1	50	~~10~~ Default	-	-
			V2	99	Q2	0			
			V3	101	Q3	0			
			V4	103	Q4	-50			
~~4~~	~~50% rated power, unity power factor~~	~~Binary, 1~~	~~V1~~	~~97~~	~~Q1~~	~~50~~	~~-~~	~~60~~	~~-~~
			~~V2~~	~~99~~	~~Q2~~	~~0~~			
			~~V3~~	~~101~~	~~Q3~~	~~0~~			
			~~V4~~	~~103~~	~~Q4~~	~~-50~~			
5	30% rated power, unity power factor	Binary, 1	V1	97	Q1	50	-	-	~~300~~
			V2	99	Q2	0			
			V3	101	Q3	0			
			V4	103	Q4	-50			
~~6~~	~~50% rated power, unity power factor~~	~~Binary, 1~~	~~V1~~	~~97~~	~~Q1~~	~~50~~	~~10~~	~~60~~	~~500~~
			~~V2~~	~~99~~	~~Q2~~	~~0~~			
			~~V3~~	~~101~~	~~Q3~~	~~0~~			
			~~V4~~	~~103~~	~~Q4~~	~~-50~~			

7	50% rated power, unity power factor	Binary, 1	V1	97	Q1	100	~~10~~ Default	~~60~~ Default	~~500~~ Default
			V2	99	Q2	0			
			V3	101	Q3	0			
			V4	103	Q4	-100			
8	50% rated power, unity power factor	Binary, 1	V1	95	Q1	50	~~10~~ Default	~~60~~ Default	~~500~~ Default
			V2	98	Q2	0			
			V3	102	Q3	0			
			V4	105	Q4	-50			
9	50% rated power, unity power factor	Binary, 1	V1	80	Q1	100	~~10~~ Default	~~60~~ Default	~~500~~ Default
			V2	95	Q2	0			
			V3	105	Q3	0			
			V4	120	Q4	-100			

Test 4 and Test 6 were not conducted because they were the same as Test 2 without the optional parameters.

3.2 Laboratory Setup

The 3 kW inverter EUT was connected to a single power supply (5 kW_{dc}) from the 20 kW PV simulator. A configuration of two strings of 20 75-W Si modules was selected. The temperature was adjusted in the simulator to provide 3000 W_p of DC power at the MPP.

The EUT was connected to a 180 kW Grid Simulator to provide the AC power (240 V, 60 Hz nominal at the EUT). A transient voltage profile was built for the grid simulator as shown in Figure 4. This profile was designed to represent voltages that could exist on a distribution feeder for extended durations in which volt-var support would be beneficial. ANSI C84.1 Range A (Normal) allows for +/- 5% of voltage at the service and +4.2/-8.3 at the utilization. Based on these levels, the voltage magnitude in the profile was selected to be approximately the same at +/-6%. The symmetry of the surge and sag was for convenience and ease of comparing the EUT in over- and under-excited operation. The step changes were included in the profile to determine the response time for the EUT and the ramps determine the ability to track the voltage changes.

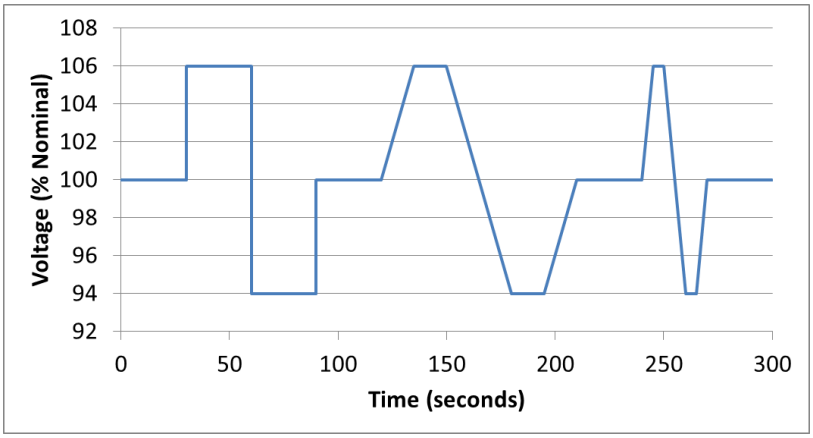


Figure 4: VV11 dynamic grid voltage profile. For details see Sandia Test Protocol.

3.3 Test Procedure

The communications (interoperability) portion of the test could not be performed without additional hardware, so only the Electrical Behavior Characterization steps shown in Table 5 were completed. The steps taken for each of the tests in the Test Matrix in Table 4 were as follows:

1. The Data Acquisition System was started with data collection every 1 second.
2. The PV simulator output was set to the "EUT Initial Operating State" DC power by setting the PV simulator irradiance.
3. The volt/var (V,Q) pairs were entered into the EUT through the front panel of the inverter.
4. The inverter was allowed to come up to a steady state power level with the grid voltage at the nominal level.
5. The dynamic voltage curve in Figure 4 was simulated by the PV simulator.
6. The next VV11 curve from the test matrix was entered into the EUT.
7. Steps 4-6 (above) were repeated until all tests were completed.

Table 5: VV11 Test Protocol Sequence.

	Step	Task	Function	Notes
Electrical Behavior	6	Verify command was successfully executed by varying the voltage profile using the grid simulator and output values of the PV simulator specified in: • Figure A6-4 for VV11 • ~~Table A6-5 for VV12~~ • ~~Table A6-6 for VV13~~ • ~~Unity power factor output for VV14~~		Monitor and record electrical output of EUT. • Grid RMS Voltage • Active power • Reactive power
	7	Repeat test with varying parameters as described in: • Table A6-4 for VV11 • ~~Table A6-5 for VV12~~ • ~~Table A6-6 for VV13~~ Each test should be repeated until behavior of the EUT is reasonably understood. ~~Test the time out period by rerunning the test profile in Figure A6.4.~~	–	
Analysis	8	Characterize EUT response.		Determine if command was executed correctly.

3.4 Test Results

VV11 testing required approximately 10 minutes per test, so 90 minutes should be allocated to conduct all nine tests in the Test Matrix. The results from Tests 1 and 2 are shown in Figure 5; the results from Test 3 are in Figure 6; and the results from Tests 5, 7, 8 and 9 are in Figure 7. (Note that the ripple on the grid voltage in the figures is a known measurement problem and not representative of actual fluctuations in grid voltage.) The Sandia Test Protocol does not have a pass/fail criterion for any of the tests, but the general trends can be seen in the results. It should

also be noted that the data acquisition system reports both over- and under-excited vars as positive values.

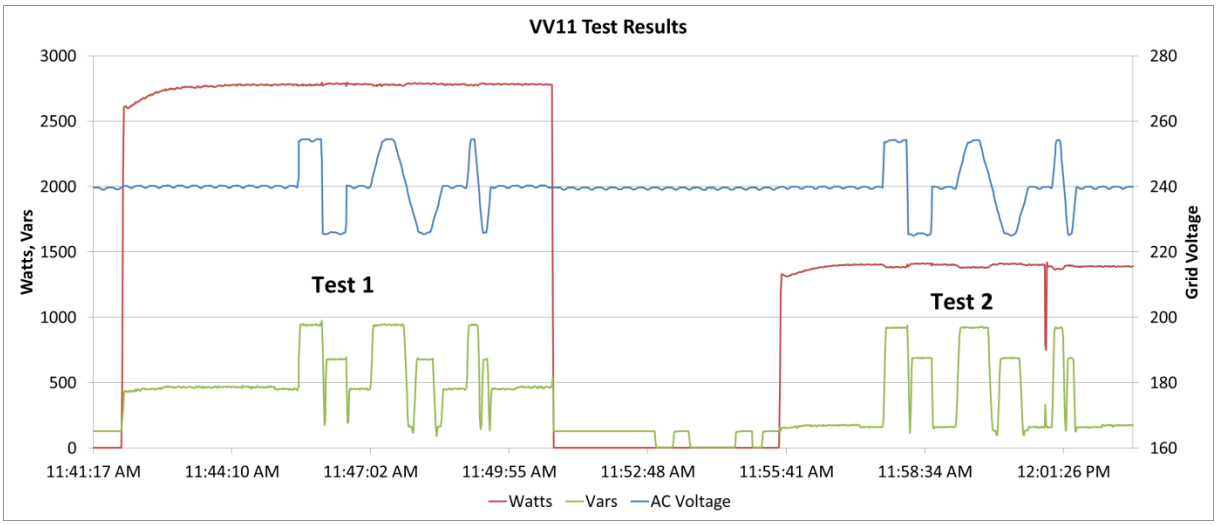


Figure 5: VV11 test results, Tests 1-2.

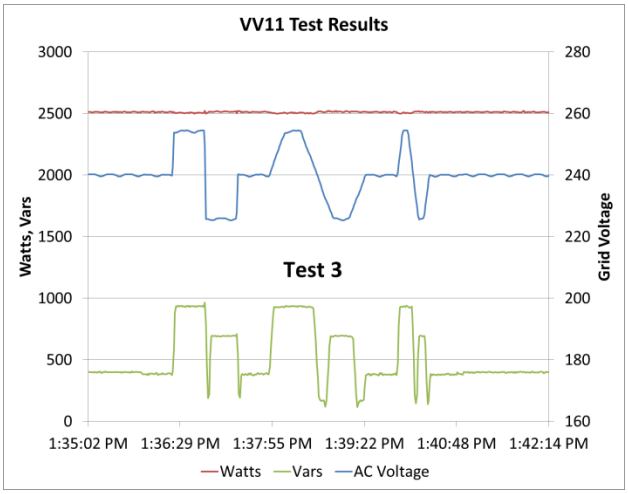


Figure 6: VV11 test results, Test 3.

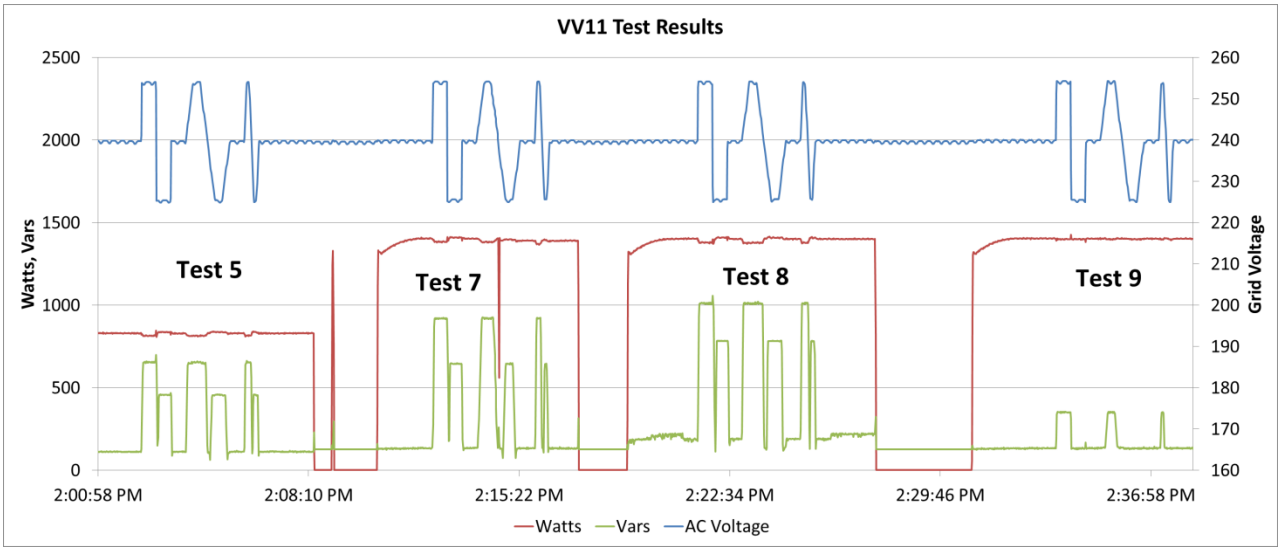


Figure 7: VV11 test results, Tests 5, 7, 8 and 9.

3.5 Recommendations for the VV11 Test Protocol

Based on these tests, Sandia identified a few necessary changes to the test protocol:

1. Section A6.2 (Test Precursors), the Utility (Grid) Simulator is required to run for 5 minutes at the nominal voltage *before* the VV11 command is sent. This is unnecessary and will be removed from the Test Protocols. Arguably this could bring the EUT up to operating temperature before testing the VV11 function, but in nearly every case the inverter will have already been running for other tests or while the test settings are entered into the equipment. I think for the sake of streamlining testing, it is unnecessary.
2. The test can begin as soon as the EUT is at steady-state operation, defined by some metric (e.g., <1% power change in 1 minute).
3. Minor changes to the grammar and style, such as adding test numbers to each of the rows of the Test Matrix.

Other comments about VV11 testing, results, and data collection.

1. The volt/var test profile is excellent for characterizing the behavior of the EUT in a reasonable amount of time. The step changes and a couple ramp rates seem to be sufficient to verify the functionality of the EUT.
2. Saving data at 1 sample/sec appears to be sufficient for this test. However, data sampling rates of much higher levels (e.g., 24 kHz) are required for the calculation of vars and power factor. Although, if active and reactive power transducers are used, this would not be necessary.

4. FW21 – FREQUENCY-WATT MODE

Frequency-watt management of DER is used to mitigate grid frequency deviations by increasing or decreasing power supplied by the DER. Such actions may be taken during emergency conditions, or this capability may be used during normal operations to "smooth" minor frequency variations. FW21 adjusts DER active power output in response to frequency excursions. As frequency rises, active power output of the DER is reduced. As frequency returns to normal, active power output is allowed to increase to original levels.

4.1 Function Capability Table and Test Matrix for FW21

The following parameters were included in the EUT:

- *FW11 initiation* – The array of (F, GP) pairs is defined in this EUT in a different way than the IEC TR 61850-90-7 definitions document prescribes. The first point is fixed at 0.2 Hz from F_{nom} at 0% reduction. The only adjustable parameter is the slope with units of $\%P_{max}$/Hz, as shown in Figure 8.
- *Hysteresis* – Not included with this inverter.
- *Recovery Ramp Rate* – Not included with this inverter.

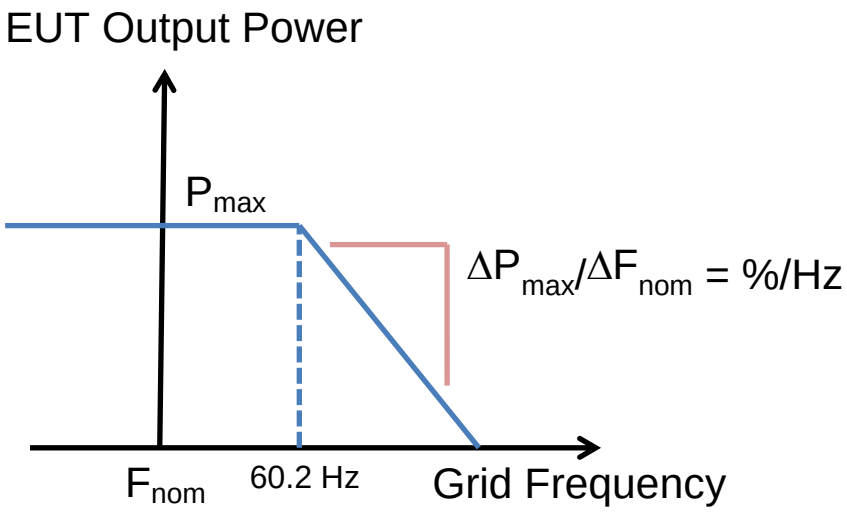


Figure 8: Built-in FW21 curve in the EUT.

Based on these capabilities, the Test Matrix shown in Table 6 was used to test the inverter. The red FW21 tests were not conducted because they required too many (F, GP) setpoints. The green tests were modified in Table 7 in order to test the EUT with the FW21 curve limitations. Other items crossed out reflect not testing for hysteresis or varying ramp rate.

Table 6: Original Test Matrix for FW21.

Test Number	EUT Initial Operating State	Freq/Watt [F, GP] Array				Hysteresis Activation	Hysteresis Reset Value (Frequency)	Recovery Ramp Rate (%Max Power/min)
~~Test 1~~	~~50% rated power, unity power factor~~	~~F_1~~	~~100.3%~~	~~PG_1~~	~~0%~~	——	——	——
		~~F_2~~	~~101.7%~~	~~PG_2~~	~~-15%~~			
		~~F_3~~	~~104.0%~~	~~PG_3~~	~~-80%~~			
~~Test 2~~	~~90% rated power, unity power factor~~	~~F_1~~	~~100.3%~~	~~PG_1~~	~~0%~~	——	——	~~10~~
		~~F_2~~	~~101.7%~~	~~PG_2~~	~~-15%~~			
		~~F_3~~	~~104.0%~~	~~PG_3~~	~~-80%~~			
~~Test 3~~	~~50% rated power, unity power factor~~	~~F_1~~	~~100.3%~~	~~PG_1~~	~~0%~~	~~1~~	~~-~~	——
		~~F_2~~	~~101.7%~~	~~PG_2~~	~~-15%~~			
		~~F_3~~	~~104.0%~~	~~PG_3~~	~~-80%~~			
~~Test 4~~	~~100% rated power, unity power factor~~	~~F_1~~	~~100.3%~~	~~PG_1~~	~~0%~~	~~1~~	~~F_1~~	——
		~~F_2~~	~~101.7%~~	~~PG_2~~	~~-15%~~			
		~~F_3~~	~~104.0%~~	~~PG_3~~	~~-80%~~			
Test 5	100% rated power, unity power factor	F_1	100.5%	PG_1	0%	-	-	-
		F_2	104.0%	PG_2	-50%			
Test 6	100% rated power, unity power factor	F_1	100.5%	PG_1	0%	-	-	~~10~~ Default
		F_2	104.0%	PG_2	-50%			
Test 7	50% rated power, unity power factor	F_1	100.5%	PG_1	0%	~~1~~ Default	-	-
		F_2	104.0%	PG_2	-50%			
Test 8	100% rated power, unity power factor	F_1	100.5%	PG_1	0%	~~1~~ Default	~~F_1~~ Default	-
		F_2	104.0%	PG_2	-50%			

Table 7: Revised Test Matrix for FW21.

Test Number	EUT Initial Operating State	Original Freq/Watt [F, GP] Array				Modified Freq/Watt [F, GP] Array				Actual Value Used in EUT
Test 5	100% rated power, unity power factor	F_1	100.5%	PG_1	0%	F_1	100.33%	PG_1	0%	13.5%/Hz
		F_2	104.0%	PG_2	50%	F_2	104.0%	PG_2	50%	
Test 6	100% rated power, unity power factor	F_1	100.5%	PG_1	0%	F_1	100.33%	PG_1	0%	21.6%/Hz
		F_2	104.0%	PG_2	50%	F_2	104.0%	PG_2	80%	
Test 7	50% rated power, unity power factor	F_1	100.5%	PG_1	0%	F_1	100.33%	PG_1	0%	13.5%/Hz
		F_2	104.0%	PG_2	50%	F_2	104.0%	PG_2	50%	
Test 8	100% rated power, unity power factor	F_1	100.5%	PG_1	0%	F_1	100.33%	PG_1	0%	142.8%/Hz
		F_2	104.0%	PG_2	50%	F_2	101.0%	PG_2	100%	

In tests 6 and 8, the slopes were changed to provide a greater testing range.

4.2 Laboratory Setup

The 3 kW inverter EUT was connected to a single power supply (5 kW_{dc}) from the 20 kW PV simulator. A configuration of two strings of 20 75-W Si modules was selected. The temperature was adjusted in the simulator to provide 3000 W_p of DC power at the MPP.

The EUT was connected to a 180 kW Grid Simulator to provide the AC power (240 V, 60 Hz nominal at the EUT). A transient frequency profile was built for the grid simulator as shown in Figure 9. The largest magnitude of the profile (103% of nominal) was selected based on the new outer must trip IEEE 1547a default limits of 62 Hz (103.3% of nominal). The step changes provide information on maximum response time, and the ramps provide information on the ability of the EUT to track the grid frequency and respond with the proper amount of curtailment.

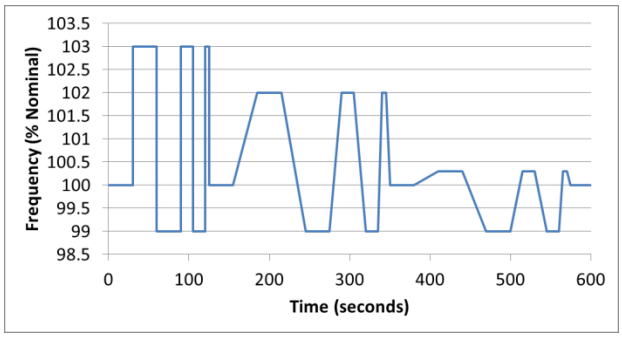


Figure 9: Original dynamic grid frequency profile. For details see Sandia Test Protocol.

Unfortunately, there are also limitations on which frequency trip parameters could be modified in the EUT. The limits are shown in Table 8 with the graphical description of these parameters shown in Figure 10. The default values, 'opened' trip values, and IEEE 1547 requirements are shown in Figure 11. As a result of the fixed upper frequency limits, the dynamic grid frequency profile caused the inverter to shut off when testing FW21. So, to complete some of the FW21 tests, high frequency excursions were significantly reduced, as shown in Figure 12.

Table 8: Default, Opened, and Hard Limits on FRT values in EUT.

Parameter	Default Values	'Opened' Trip Points	Maximum Values
t_{OL}^{max}	9 cycles (0.15 s)	9 cycles (0.15 s)	9 cycles (0.15 s) [limited by t_{IL}^{max}]
F_{OL}^{max}	62.00 Hz (103.7%)	63.00 Hz (105.0%)	
t_{IL}^{max}	9 cycles (0.15 s)	9 cycles (0.15 s)	9 cycles (0.15 s) [unadjustable in firmware]
F_{IL}^{max}	60.48 Hz (100.8%)	60.48 Hz (100.8%)	60.48 Hz (100.8%) [unadjustable in firmware]
t_{OL}^{min}	119 cycles (1.98 s)	255 cycles (0.15 s)	255 cycles (4.25 s) [limited by t_{IL}^{min}]
F_{OL}^{min}	57.00 Hz (95.0%)	57.00 Hz (95.0%)	
t_{IL}^{min}	9 cycles (0.15 s)	255 cycles (4.25 s)	255 cycles (4.25 s) [firmware limit]
F_{IL}^{min}	59.3 Hz (98.8%)	58.50 Hz (97.5%)	

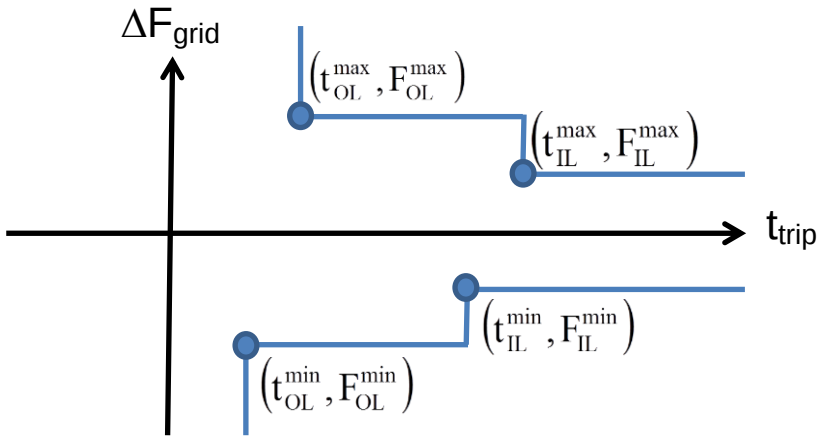


Figure 10: Graphical representation of the frequency trip inner limit (IL) and outer limit (OL) for the EUT.

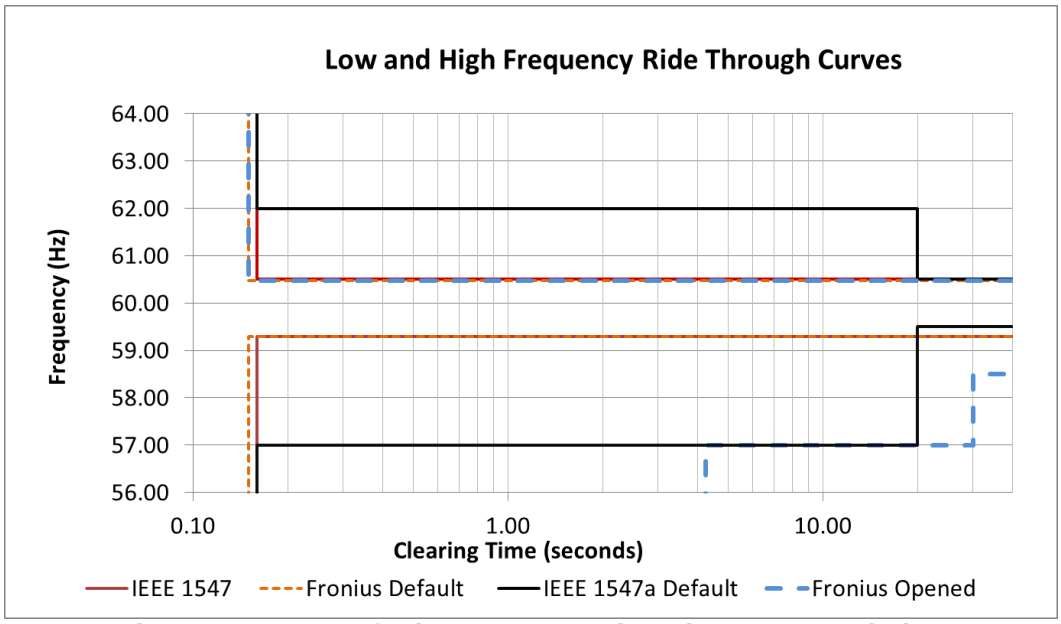


Figure 11: EUT Default, EUT Opened, and IEEE 1547 Limits.

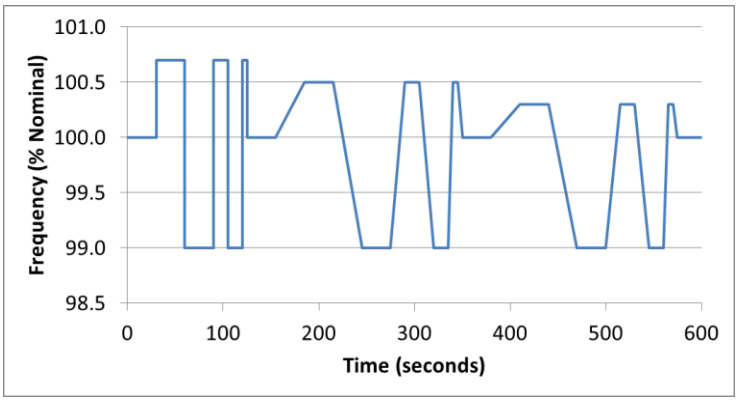


Figure 12: Revised dynamic grid frequency profile.

4.3 Test Procedure

The communications (interoperability) portion of the test was not performed. Only the Electrical Behavior Characterization steps were completed, as shown in Table 9. The procedure taken for each test in the Test Matrix in Table 7 was:

1. The Data Acquisition System was started with 1 second data collection.
2. The PV simulator output was set to the "EUT Initial Operating State" DC power by setting the PV simulator irradiance.
3. The frequency/watt slope was entered into the EUT through the front panel of the inverter.
4. The inverter was allowed to come up to a steady state power level with the grid voltage at the nominal level.
5. The dynamic frequency curve in Figure 12 was simulated by the PV simulator.
6. The next FW21 slope from the test matrix was entered into the EUT.
7. Steps 4-6 (above) were repeated until all tests were completed.

Table 9: FW21 Test Protocol Sequence.

	Step	Task	Function	Notes
Electrical Behavior	6	Verify command was successfully executed by varying the frequency of the grid simulator (Table A7-3 & Figure A7-6) and using the PV simulator outputs of Table A7-4. If the test causes the inverter to trip off, communications need to be re-established with the DS93 command.		Monitor electrical output of EUT. Grid Frequency AC Voltage Active power Reactive power
	7	Repeat test with varying parameters, as specified in Table A7-4, or similar values. Each test should be repeated until behavior of the EUT is reasonably understood.		–
	~~8~~	~~For FW with energy storage, repeat test (steps 1 – 7) with the parameters shown in Table A7-5.~~		
	~~9~~	~~For FW22, use the array of two FW curves as specified in Table A7-6 to re-run steps 1-8~~		
Analysis	10	Characterize EUT's response.	**DS92; DM**	Determine if command was executed correctly.

4.4 Test Results

The FW21 grid simulator test profile is much longer than the VV11 grid simulator test profile. It requires 10 minutes to run the profile, so the total time for each test is close to 15 minutes. The results from Tests 5 and 6 are shown in Figure 13; the results from Test 7 are in Figure 14; and

the results from Test 8 are in Figure 15. The Sandia Test Protocol does not have a pass/fail criterion for any of the tests, but the general trends can be seen in the results. Note that the small ramps at the end of the profile only go up to 100.3% of F_{nom} so there is no power reduction.

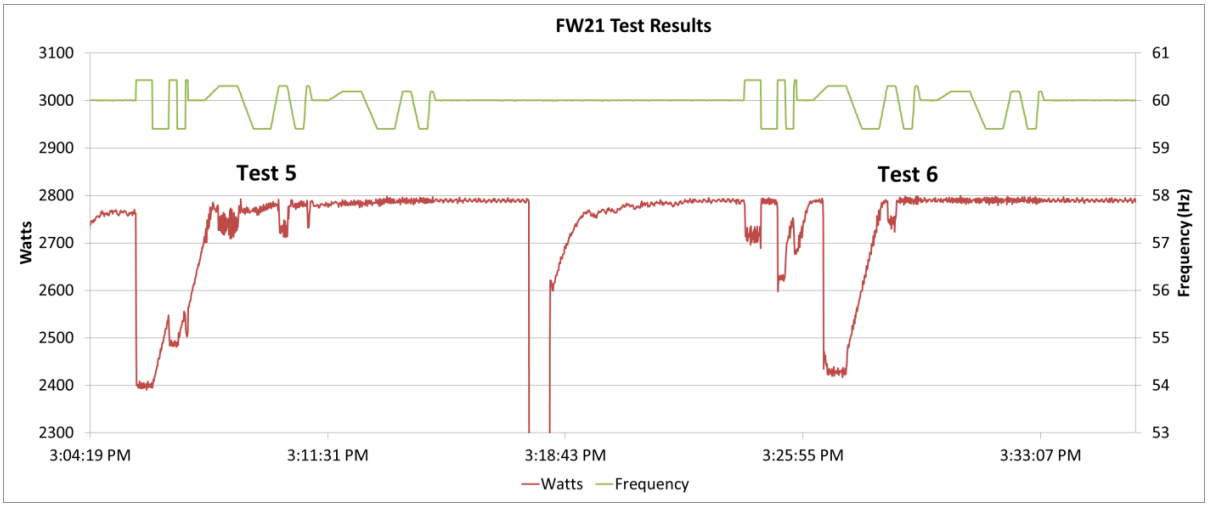


Figure 13: FW21 test results for Tests 5 and 6.

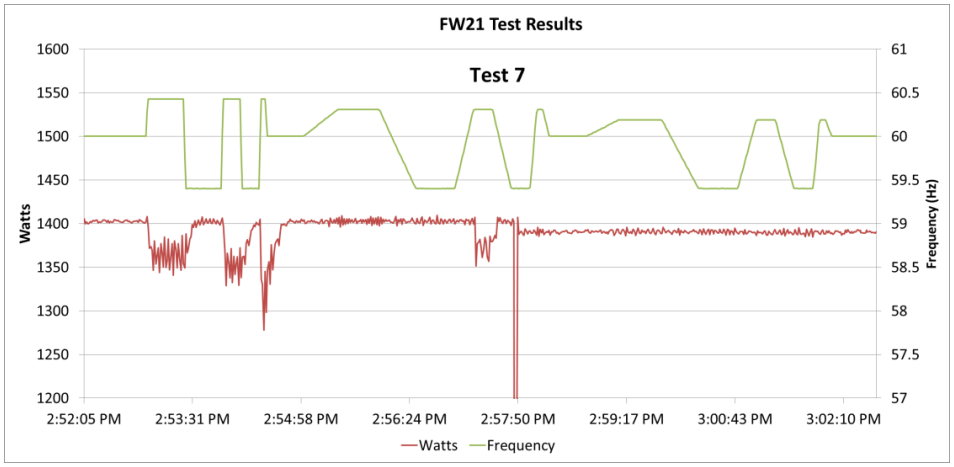


Figure 14: FW21 test results for Tests 7.

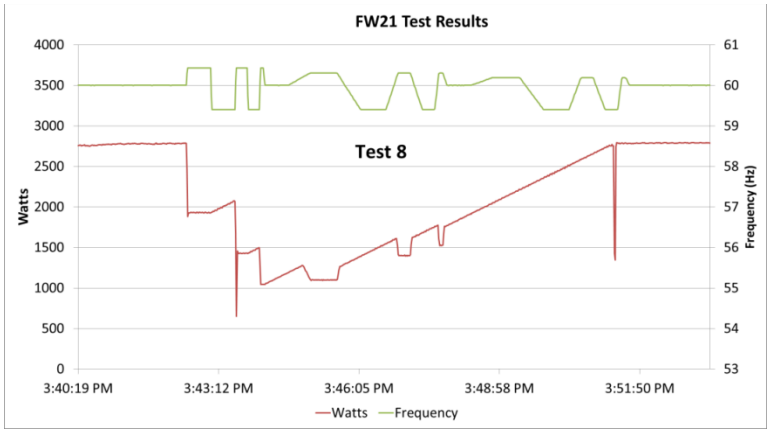


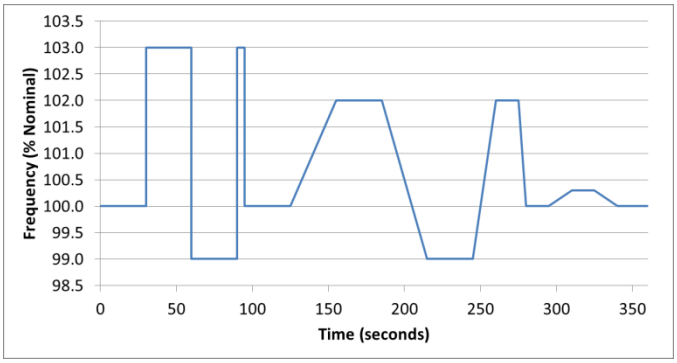
Figure 15: FW21 test results for Test 8.

4.5 Recommendations for the FW21 Test Protocol

Despite the limitations of this particular inverter, Sandia identified a few changes which can improve the test protocol:

1. The test profile seems long (10 minutes). It could be reduced and still provide enough information about the EUT. For instance, transient response information gathered from the step changes is not necessary from three different steps. The same can be said for the larger ramps. Lastly, the final set of small ramps does not exceed the deadband on any of the tests, so only one is necessary to demonstrate that the deadband is functioning. Sandia proposes the following revised Table A7-3 and Figure A7-5:

Time (sec)	Frequency (% nominal)
0	100.0
30	100.0
30	103.0
60	103.0
60	99.0
90	99.0
90	103.0
95	103.0
95	100.0
125	100.0
155	102.0
185	102.0
215	99.0
245	99.0
260	102.0
275	102.0
280	100.0
295	100.0
310	100.3
325	100.3
340	100.0
360	100.0



Revised Test Profile
(Table A7-3 and Figure A7-5)

2. Problems with legacy equipment adhering to IEEE 1547 should be less likely in the future because these new functions will be added to inverter firmware at the same time that IEEE 1547a is being adopted; however the test protocol should not require expanded frequency trip points to perform some FW21 tests. For instance, the first step of the test profile goes up to 103% of F_{nom} (61.8 Hz) for 30 seconds, which exceeds the default

values for IEEE 1547a (as of this writing), but this does not exceed the optional trip limits which can be expanded to 64 Hz (106.7%) for up to 300 s in IEEE 1547a. This could be a problem if the EUTs have fixed values for the 'must trip' frequency ride-through curves that are below 103%. Further, this test should not test the FRT functionality of the device; that will be performed in a separate section of the Sandia Test Protocols. Thus, there appear to be a few different approaches the Test Protocols could take at this juncture:

   a. Open the frequency trip settings up as much as possible and hope that test profile does not trip the device.
   b. Reduce the time at the high frequencies (e.g., only allow excursions above 60.5 Hz for 20 seconds).
   c. Allow for reducing the maximum frequency used in the test (such as was done in this test sequence).

3. The test should begin as soon at the EUT is at steady-state operation, defined by some metric (e.g., <1% power change in 1 minute).
4. The grid frequency should be measured during the test.

Other comments about INV3 testing, results, and data collection.

1. Recording data rates of 1 second appear to be ok for this test, though much higher data collection rates are required to get accurate measurements of the grid frequency.

5. L/HVRT – LOW/HIGH VOLTAGE RIDE THROUGH

For safety reasons (both personnel and equipment), inverters are required to disconnect (i.e., "trip") from the grid during certain conditions. Specific conditions are defined by different standards and vary by region and jurisdictions. Therefore, L/HVRT functions are designed for inverters with the capability to update their voltage ride-through "must remain connected" and "must disconnect" curves based on the needs of the utility or codes/standards of the region.

5.1 Function Capability Table and Test Matrix for L/HVRT

The following parameters were included in the EUT:

- *L/HVRT initiation* command with four sets of point pairs in the form (t_1, V_1, t_2, V_2,…, t_x, V_x) that define the *L/HVRT* zones shown in Figure 16.

  (Note: *Time Window* and *Ramp Rate* are being considered when the EUT returns from a tripped condition, but this is currently not in the Test Protocol.)

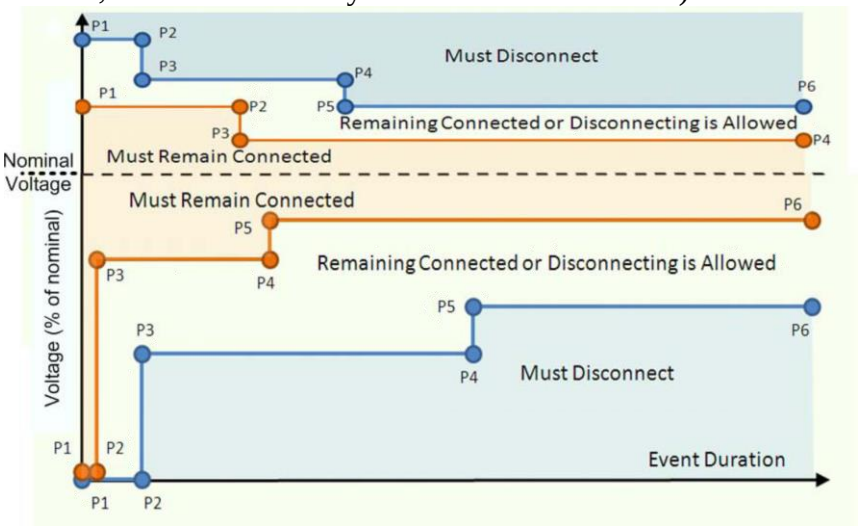


Figure 16: L/HVRT points with zones for "must remain connected," "may remain connected," and "must disconnect."

Based on these capabilities, the Test Matrix shown in Table 10 was used to test the inverter. The shaded red L/HVRT points were not included because there are only two points available for the must trip upper and lower limits available in this EUT. Items crossed out reflect this lack of functionality.

Similar to the FRT, the VRT has specific limits on the types of curves and values that can be entered into the EUT. These limits are shown in Table 11 with a visual representation of the points shown in Figure 17.

Table 10: Test Matrix for L/HVRT. Red values were incorrect in L/HVRT Sandia Test Protocol, Verison 2.0.

Update L/HVRT Command	Must Trip Upper Limit				~~May Trip Upper Limit~~				Must Trip Lower Limit				~~May Trip Lower Limit~~			
(IEEE 1547)	t_1	0.16	V_1	2.00					t_1	0.16	V_1	0.00				
	t_2	0.16	V_2	1.20					t_2	0.16	V_2	0.50				
	t_3	1.00	V_3	1.20					t_3	2.00	V_3	0.50				
	t_4	1.00	V_4	1.10					t_4	2.00	V_4	0.88				
	t_5	30.00	V_5	1.10					t_5	30.00	V_5	0.88				
(Proposed IEEE 1547a 'Open' limits)	t_1	0.16	V_1	2.00	~~t_1~~	~~0.10~~	~~V_1~~	~~2.00~~	t_1	0.16	V_1	0.00	~~t_1~~	~~0.10~~	~~V_1~~	~~0.00~~
	t_2	0.16	V_2	1.20	~~t_2~~	~~0.10~~	~~V_2~~	~~1.17~~	t_2	0.16	V_2	0.45	~~t_2~~	~~0.10~~	~~V_2~~	~~0.50~~
	t_3	1.00/13	V_3	1.20	~~t_3~~	~~12.00~~	~~V_3~~	~~1.17~~	t_3	11.00	V_3	0.45	~~t_3~~	~~10.00~~	~~V_3~~	~~0.50~~
	t_4	1.00/13	V_4	1.10	~~t_4~~	~~12.00~~	~~V_4~~	~~1.07~~	t_4	11.00	V_4	0.60	~~t_4~~	~~10.00~~	~~V_4~~	~~0.70~~
	t_5	30.00	V_5	1.10	~~t_5~~	~~30.00~~	~~V_5~~	~~1.07~~	t_5	21.00	V_5	0.60	~~t_5~~	~~20.00~~	~~V_5~~	~~0.70~~
									~~t_6~~	~~21.00~~	~~V_6~~	~~0.88~~	~~t_6~~	~~20.00~~	~~V_6~~	~~0.92~~
									~~t_7~~	~~30.00~~	~~V_7~~	~~0.88~~	~~t_7~~	~~30.00~~	~~V_7~~	~~0.92~~
(Standard PRC-024-1)	t_1	0.00	V_1	1.20					t_1	0.15	V_1	0.00				
	t_2	0.20	V_2	1.20					t_2	0.15	V_2	0.45				
	t_3	0.20	V_3	1.18					t_3	0.30	V_3	0.45				
	t_4	0.50	V_4	1.18					t_4	0.30	V_4	0.65				
	~~t_5~~	~~0.50~~	~~V_5~~	~~1.15~~					~~t_5~~	~~2.00~~	~~V_5~~	~~0.65~~				
	~~t_6~~	~~1.00~~	~~V_6~~	~~1.15~~					~~t_6~~	~~2.00~~	~~V_6~~	~~0.75~~				
	~~t_7~~	~~1.00~~	~~V_7~~	~~1.10~~					~~t_7~~	~~3.00~~	~~V_7~~	~~0.75~~				
	~~t_8~~	~~4.00~~	~~V_8~~	~~1.10~~					~~t_8~~	~~3.00~~	~~V_8~~	~~0.90~~				
	~~t_9~~	~~30.00~~	~~V_9~~	~~1.10~~					~~t_9~~	~~30.00~~	~~V_9~~	~~0.90~~				

Table 11: Default and firmware limits on VRT values in the EUT.

Parameter	Default Values (IEEE 1547 Compliance)	IEEE 1547a 'Open' Test	PRC-024-1 Test	Maximum Values
t_{OL}^{max}	9 cycles (0.15 s)	9 cycles (0.15 s)	1 cycles (0.016 s)	255 cycles (4.25 s) [limited by t_{IL}^{max}]
V_{OL}^{max}	288 V (120.0%)	288 V (120.0%)	288 V (120.0%)	
t_{IL}^{max}	58 cycles (0.97 s)	58/780 cycles (0.97/13 s)	12 cycles (0.20 s)	255 cycles (0.4.25 s) [firmware limit]
V_{IL}^{max}	264 V (110%)	264 V (110%)	283 V (117.9%)	
t_{OL}^{min}	9 cycles (0.15 s)	9 cycles (0.15 s)	9 cycles (0.15 s)	255 cycles (4.25 s) [limited by t_{IL}^{min}]
V_{OL}^{min}	120 V (50.0%)	108 V (45.0%)	104/108 V (43.3/45.0%)	
t_{IL}^{min}	118 cycles (1.97 s)	255/660 cycles (4.25/11 s)	18 cycles (0.3 s)	255 cycles (4.25 s) [firmware limit]
V_{IL}^{min}	213 V (88.8%)	144 V (60.0%)	144/156 V (60.0/65.0%)	

(**Blue values** were entered because of mistakes in the Sandia Test Protocols, **red values** were limited based on EUT firmware limits, **orange values** were incorrectly entered into the EUT during testing, **black values** are correct.)

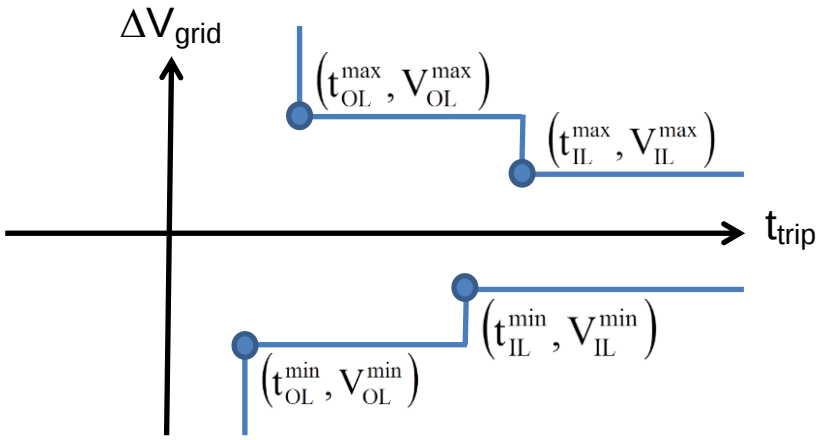


Figure 17: Graphical representation of the voltage trip inner limit (IL) and outer limit (OL) for the EUT.

As explained above, there were limitations with the voltage *must trip* curves. Only two levels (time and voltage) were programmable for the upper and lower voltage *must trip* curves. There was no option for establishing a *must remain connected* curve. Due to these limitations of the EUT, the curves in Table 11 and Figures 18-20 were entered into the EUT for each of the tests. In the case of the NERC PRC-024-1 trip curve, there were errors in V_{OL}^{min} and V_{IL}^{min} entered into the EUT, but since the goal of this work was not to evaluate the EUT, but to improve the Sandia Test Protocol, they were not repeated with the correct values as this has no impact on the validity or evaluation of the test protocol.

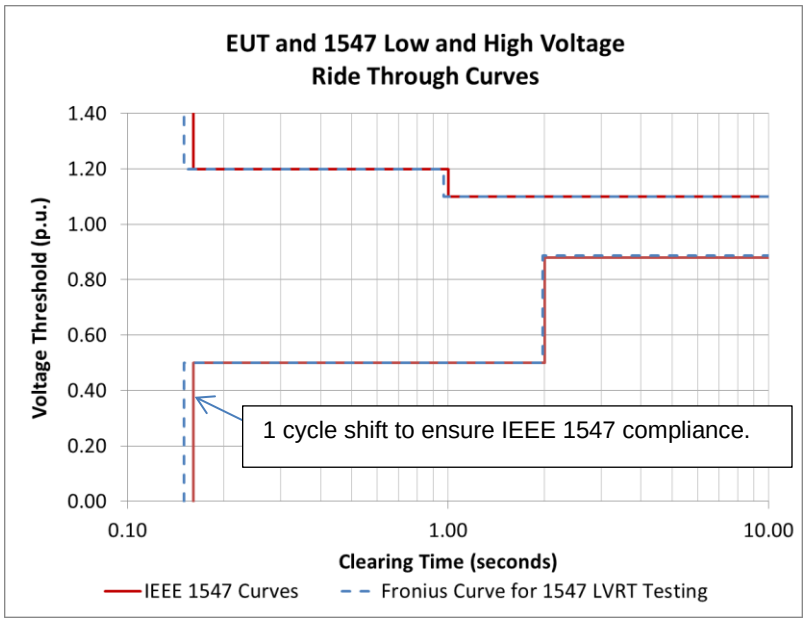


Figure 18: EUT default VRT trip curves and IEEE 1547 limits.

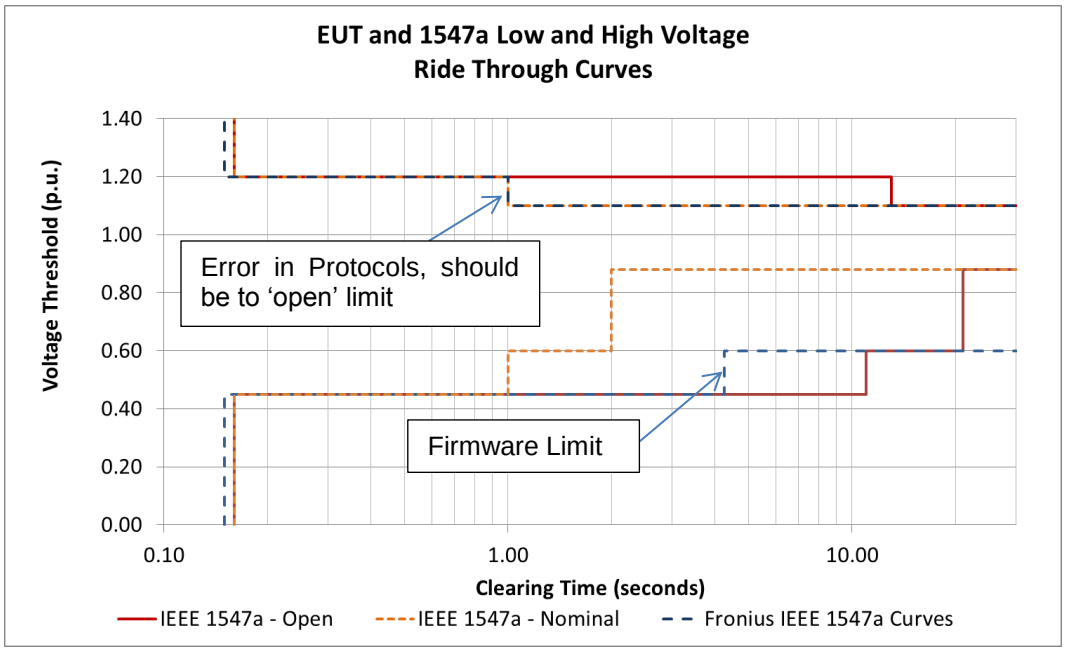


Figure 19: EUT VRT trip curves for IEEE 1547a test.

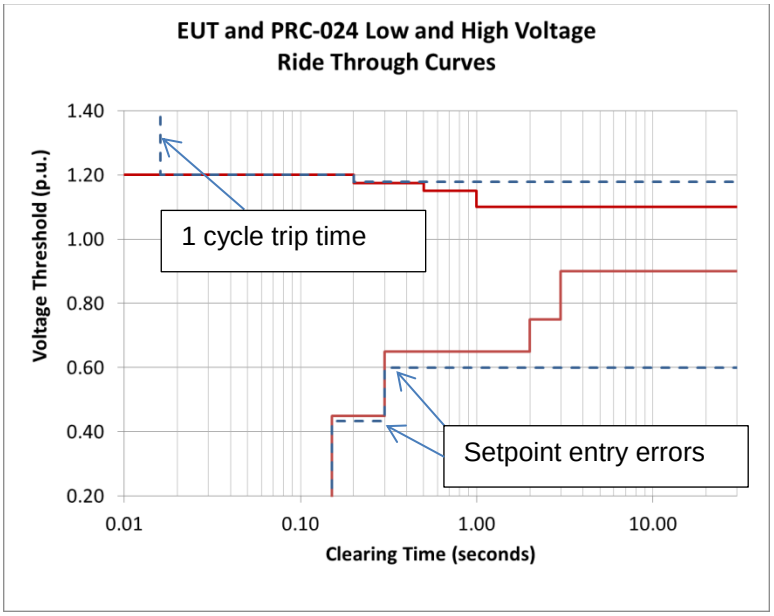


Figure 20: EUT VRT trip curves and PRC-024 limits.

5.2 Laboratory Setup

The 3 kW inverter EUT was connected to a single power supply (5 kW_{dc}) from a 20 kW PV simulator. A configuration of two strings of 20 75-W Si modules was selected. The temperature was adjusted in the PV simulator to provide 3000 W_p of DC power at the MPP.

The EUT was connected to a 180 kW grid simulator (240 V, 60 Hz nominal at the EUT). Voltage sags and surges were performed by the grid simulator, per the Sandia Test Protocols.

5.3 Test Procedure

The communications (interoperability) portion of the test was not performed. Only the Electrical Behavior Characterization steps were completed, as shown in Table 12. The steps taken for each of the tests in the Test Matrix in Table 13 were as follows:

1. The Data Acquisition System was setup to capture 6 kHz data with a 0.16 second pretrigger and a 7 second post trigger time. (Note: a longer post trigger may be necessary in the future.)
2. The PV simulator output was set to rated DC power by setting the PV simulator configuration, irradiance, and temperature.
3. The L/HVRT curves were entered into the EUT through the front panel of the inverter (as necessary).
4. The inverter was allowed to come up to a steady state power level with the grid voltage at the nominal level.
5. The grid simulator changed the voltage to the new value in Table 13 for 30 seconds.
6. If the EUT tripped, the data was saved. If the EUT did not trip, this was noted.
7. Steps 3-6 (above) were repeated for all the values in the test matrix until all tests were completed.

Table 12: L/HVRT Test Protocol Sequence.

	Step	Task	Function	Notes
Electrical Behavior	5	~~If Success response received,~~ verify command was successfully executed by running voltage tests as suggested in Table A9-3 with the grid simulator. ~~If the test causes the inverter to trip off, communications need to be re-established with the DS93 command.~~	**DM** – EUT output is recorded and logged	Monitor electrical output of EUT.
	6	Repeat test with varying parameters (Table A9-3). Each test should be repeated until behavior of the EUT is reasonably understood.		
Analysis	7	Characterize EUT's response.	**DS92; DM**	Determine if command was executed correctly.

5.4 Test Results

Example results for the L/HVRT tests are shown in Figures 21-23. The trip times are calculated by subtracting the voltage sag/surge start time from the inverter shut down time.

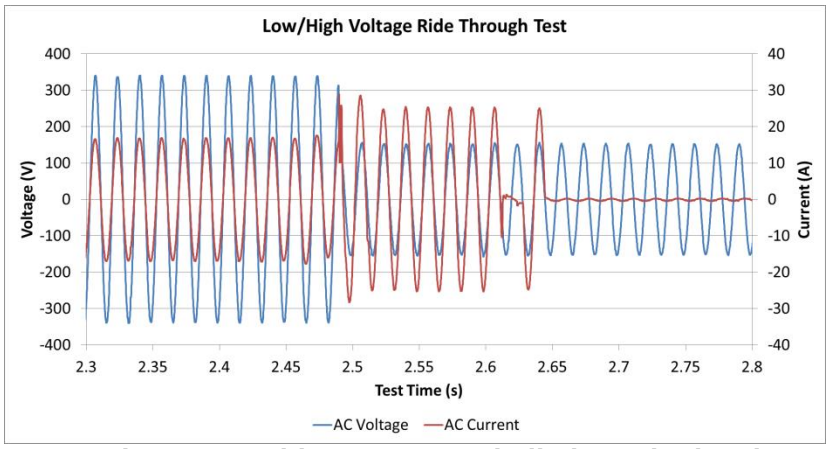


Figure 21: 0.45 p.u. voltage sag with IEEE 1547 trip limits. Trip time is 9 cycles (0.15 s).

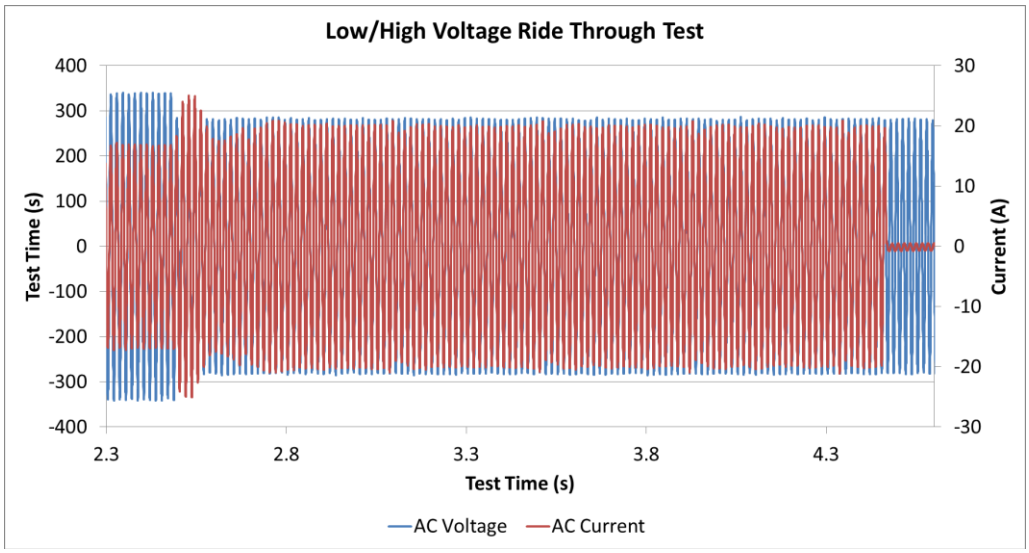


Figure 22: 0.83 p.u. voltage sag with IEEE 1547 trip limits. Trip time is 119 cycles (1.98 s).

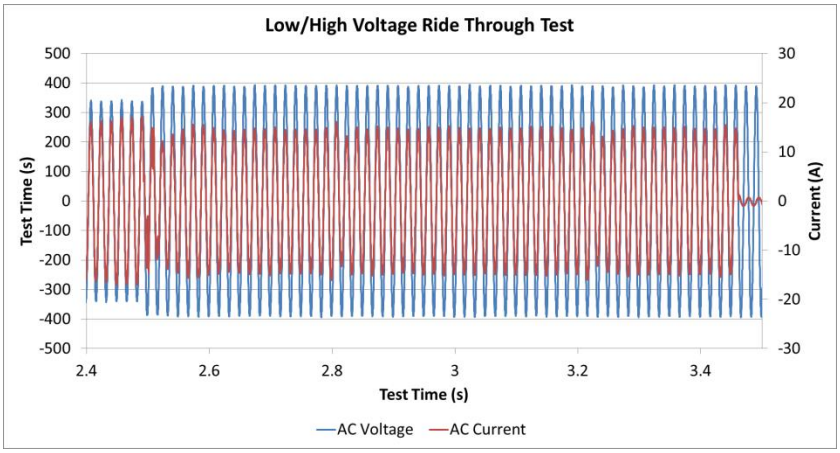


Figure 23: 1.15 p.u. voltage surge with IEEE 1547 trip limits. Trip time is 58 cycles (0.97 s).

The Test Matrix for L/HVRT with the expected results and EUT results is shown in Table 13. There were some tests that resulted in unexpected trip times, but overall the test procedure worked well. Picking a few voltage test points and running the voltage at that level until the inverter trips is a good method for characterizing the VRT functionality of the device.

Table 13: L/HVRT Test Matrix with Results. Red indicates unexpected results.

L/HVRT Curve	Test Number	Voltage Test Points	Expected Trip Time based on L/HVRT Curve	Expected Trip Time based on EUT settings	Trip Time
IEEE 1547	Test 1	0.45	0.16 s	0.15 s	0.15 s
	Test 2	0.83	2.00 s	1.97 s	1.97 s
	Test 3	0.95	No Trip	No Trip	> 30 s
	Test 4	1.05	No Trip	No Trip	> 30 s
	Test 5	1.15	1.00 s	0.97 s	0.97 s
	Test 6	1.25	0.16 s	0.15 s	0.15 s
Proposed IEEE 1547a "wide open limits"	Test 1	0.4	0.16 s	0.15 s	0.15 s
	Test 2	0.47	11.0 s	4.25 s	0.16 s
	Test 3	0.55	11.0 s	4.25 s	4.24 s
	Test 4	0.65	21.0 s	No Trip	4.27 s
	Test 5	0.8	21.0 s	No Trip	> 30 s
	Test 6	0.95	No Trip	No Trip	> 30 s
	Test 7	1.05	No Trip	No Trip	> 30 s
	Test 8	1.08	No Trip	No Trip	> 30 s
	Test 9	1.13	13.0 s	1.00 s	0.97 s
	Test 10	1.18	13.0 s	1.00 s	0.97 s
	Test 11	1.22	0.16 s	0.15 s	0.15 s
Standard PRC-024-1	Test 1	0.40	0.15 s	0.15 s	0.15 s
	Test 2	0.60	0.30 s	0.30 s	0.31 s
	Test 3	0.70	2.00 s	No Trip	0.32 s
	Test 4	0.80	3.00 s	No Trip	0.31 s
	Test 5	0.95	No Trip	No Trip	No Trip
	Test 6	1.05	No Trip	No Trip	No Trip
	Test 7	1.13	1.00 s	No Trip	0.21 s
	Test 8	1.16	0.50 s	No Trip	0.22 s
	Test 9	1.19	0.20 s	0.20 s	0.03 s

Once again, the Sandia Test Protocol does not have a pass/fail criterion for any of the tests, so there is no need to comment on performance.

5.5 Recommendations for the L/HVRT Test Protocol

There were a number of challenges in testing the L/HVRT capabilities using this EUT. There were only 2 points for the "must trip" curves so more complicated L/HVRT curves (e.g., PRC-024-1) were not able to be fully implemented. Further, there was no method of establishing "must remain connected" curves. Additionally, IEEE 1547a allows for a range of different setpoints, as shown in Table 14, so it was decided to only test the widest, 'open' trip limits. There was a mistake in the Test Matrix which referenced the default value in the 'Must Trip'

Upper Limit as opposed to the 'open' limit—this will be corrected in the next version of the L/HVRT protocol.

Table 14: 1547a interconnection system response to abnormal frequencies.

Default settings[a]		
Voltage range (% of base voltage[b])	**Clearing time (s)**	**Clearing time: adjustable up to and including (s)**
V < 45	0.16	0.16
45 < V < 60	1	11
60 < V < 88	2	21
110 < V < 120	1	13
V > 120	0.16	0.16
[a] Under mutual agreement between the EPS and DR operators, other static or dynamic voltage and clearing time trip settings shall be permitted [b] Base voltages are the nominal system voltages stated in ANSI C84.1-2006, Table 1.		

Some other comments and recommendations for the L/HVRT Protocol.

1. Voltage must trip curves are tested according to IEEE 1547.1 in UL 1741 in the U.S. with a different technique than used here. In 1547.1 there are two tests:
    a. A "magnitude" test in which there is a slow voltage ramp which determines the voltage of the inner limits.
    b. A "trip time" test in which a step function is used to test the response time of the EUT at different voltages.

    Only test (b) is performed in the Sandia Test Protocols, so it might be worth including a magnitude test to locate the innermost voltage which causes a trip.
2. IEEE 1547 also specifies that the EUT is tested at:
    a. Its minimum operating current
    b. Unity power factor at as close to 100% rated output current as possible.
    c. Minimum power factor (leading) at as close to 100% rated output current as possible.
    d. Minimum power factor (lagging) at as close to 100% rated output current as possible.

    The test protocols do not include (a), (c), or (d). These tests could be considered in future editions of the L/HVRT.
3. There is no discussion of how to handle single vs multiphase devices. For multiphase devices IEEE 1547.1 requires tests on each of the phases for voltage sags/surges. These tests are repeated 5 times. The Sandia Test Protocols need to include a discussion of multiphase devices.
4. IEEE 1547.1 requires testing EUTs with adjustable trip points at the midpoint and maximum overvoltage levels. This might be appropriate for tests of 1547a since there is a range of trip times for the different voltage ranges.
5. A 'Test 10' at 1.22 p.u. should be added to PRC-024-1 testing to ensure t_{OL}^{max} and V_{OL}^{max} are working correctly.
6. Only testing IEEE 1547, IEEE 1547a, and PRC-024-1 is both U.S.-centric and somewhat limited. These tests could be considered representative of EUT L/HVRT adjustments,

but it would be ideal to include more international testing and more *must remain connected* curves. Better yet, this test protocol should be revised significantly to make it more generic for any L/HVRT curves. For instance, creating instructions such as 'any steps in the voltage profile should be tested at 20% and 80%.' However, this may lead to excessive number of voltage test cases when there are many steps in the upper and lower trip curves.

Other comments about L/HVRT testing, results, and data collection.

1. The VRT tests were relatively quick once the grid simulator test profile was created and the trigger established. For this first run through of the L/HVRT tests, it took 2 hours, but that time is likely to become much smaller with experience.
2. Testing an EUT with "must stay connected" curves would help refine the test protocol.
3. 6 kHz sampling rate was sufficient for detecting the time when the voltage changed and when the EUT tripped off. Reducing this value is possible if there are hardware limitations.

6. CONCLUSIONS

The Sandia National Laboratories Inverter Interoperability Test Protocols are designed to be a pre-certification test procedure to be used by international laboratories, inverter manufacturers, utilities, and others stakeholders. Using the test protocols, these groups can work together to agree upon a set of consensus tests for advanced inverter and interoperability functions. Drafts of this document were circulated to a number of stakeholders in August 2013. Sandia National Laboratories, in conjunction with other stakeholders, are working to continuously improve the test protocols. In this report, four functions (INV3, VV11, FW21, and L/HVRT) were run through the electrical characterization portion of the Sandia Test Protocols in order to discover errors, discrepancies, or other areas of improvement. The improvements discovered through testing and documented here will be included in the next version of the Sandia National Laboratories Inverter Interoperability Test Protocols.

REFERENCES

[1] International Electrotechnical Commission (IEC) TR 61850-90-7 Edition 1.0, "Communication networks and systems for power utility automation – Part 90-7: Object models for power converters in distributed energy resources (DER) systems," Geneva, Switzerland, February 2013.

[2] J. Johnson, S. Gonzalez, M.E. Ralph, A. Ellis, and R. Broderick, "Test Protocols for Advanced Inverter Interoperability Functions – Main Document," Sandia Technical Report, SAND2013-9880, November 2013.

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