

# Power Cycle Testing of Power Switches: A Literature Survey

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**Abstract**— Reliability of power converters and lifetime prediction has been a major topic of research in the last few decades, especially for traction applications. The main failures in high power semiconductors are caused by thermo-mechanical fatigue. Power cycling and temperature cycling are the two most common thermal acceleration tests used in assessing reliability. The objective of this paper is to study the various power cycling tests found in the literature and to develop generalized steps in planning application specific power cycling tests. A comparison of different tests based on the failures, duration, test circuits, and monitored electrical parameters is presented.

**Index Terms**— Semiconductor reliability, failure mechanisms, power cycling, lifetime estimation, precursor indicators, physics of failure.

## I. INTRODUCTION

Reliability of power converters and lifetime prediction has been a major topic of research in the last few decades [1], especially for traction applications [3][4][5][6][7][8][9]. According to [1] and an industry based survey presented in [2], power semiconductor device failures are a major concern for reliability of the power converter. According to MILitary STanDard (MIL-STD 217), the Insulated Gate Bipolar Transistors (IGBTs) are the second most unreliable devices causing failure of the inverter, after capacitors [1]. The main failures in high power semiconductors are caused by thermo-mechanical fatigue [1-3], and thermal analysis of the inverter is essential for reliability testing in various applications such as adjustable speed drives, matrix converters, electric vehicle applications, etc. [1][3]-[9]. Power cycling and temperature cycling are the two most common thermal acceleration tests used in assessing reliability of semiconductors [10].

Power cycling tests are accelerated tests where the power to the devices is switched (on and off) so that the temperature in the device would vary (cycle). Power cycling tests include conduction and switching and are closer to actual operation of

the device. For this reason, power cycling tests are referred to as "Active" cycling tests while temperature cycling are referred to as "Passive" cycling tests. Both types of cycling methods suffer from extremely long test times since millions of power cycles are expected in many power applications. Highly accelerated test methods by increasing temperature variation are controversial due to the activation of different material related mechanisms [4]. Power cycling usually results in wire bond failure while thermal cycling causes solder cracks. According to [11][12][13], fast power cycling (time period in the order of tens of seconds) and higher temperature swing ( $\Delta T > 100K$ ) leads to wire-bond failure while slow power cycling (time period in the order of minutes) and lower temperature swing ( $\Delta T < 80K$ ) leads to solder fatigue related failures.

MIL-STD 217 and 750 do not have testing procedures for IGBTs and hence users are forced to follow a combination of bipolar and field-effect transistor guidelines [14][15]. Joint Electron Devices Engineering Council (JEDEC) standards, JESD22-105C and JESD22-A122 are specified for power cycling of semiconductors. However, they do not explain in detail the dependence of operating conditions, failure criteria/ indicators, etc. [10]. Hence there is a need to standardize procedures for power cycling with greater details.

The reasons for conducting power cycling tests is to study failure mechanisms, to detect weak links in the device packaging, test new packaging materials/new device designs, and estimate application-specific lifetime. LESIT (LeistungsElektronik Systemtechnik und InformationsTechnologie), a Swiss government funded research program, was the first to conduct power cycling tests and develop a semiconductor lifetime model based on temperature swing ( $\Delta T$ ) and medium temperature,  $T_m$ , of the device [4], followed by the RAPDSRA project [16]. This paper presents a general power cycling test design methodology based on a review of relevant literature. The objective of this paper is to study the various power cycling tests in the literature, in terms of circuit design, failure criteria, and failure analysis based on test results.

Fig. 1 illustrates the steps involved in the design of power cycling tests. The first step is to determine the test circuit to be used for power cycling based on the objective, expected failures, and application (lifetime model, mission profile test, etc.) of the tests. Once the test circuit is determined, the operating conditions of the test should be estimated based on the application requirement, and the limits on temperature, current, and voltage capabilities of the device under test. The

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Manuscript received March 10, 2014.

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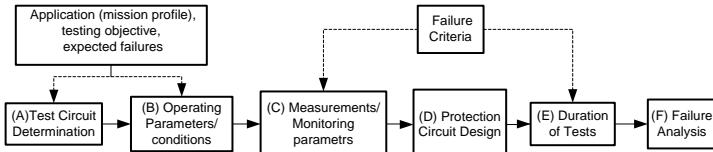


Fig. 1. Block diagram to show steps in planning power cycling tests.

next step is to determine the precursor parameters for data collection based on the failure criteria considered. The protection circuit is designed to prevent catastrophic failure of the device based on the failure criteria and the monitored parameters that indicate electrical degradation. The duration of the tests is determined by the failure criteria. Finally, after conducting the tests, the device degradation and/or failure is analyzed with the help of advanced imaging techniques such as X-ray diffraction, scanning electron microscopy, scanning acoustic microscopy, etc. [17]. Each of the steps is discussed in detail in section II.

## II. DESIGN OF EXPERIMENT: PLANNING POWER CYCLING TESTS

As already discussed, the important steps in planning power cycling tests are presented with a review of methods found in the literature. Circuit design, the precursor failure indicators and failure criteria, choice of operating conditions, duration of tests, and failure analysis will be discussed in this section.

### A. Circuit Design

Factors affecting the choice of the circuit are 1) application, 2) packaging materials, and 3) expected failures. The first step in planning power cycling tests is to determine the application of the power converter. The operating conditions (environmental, electrical, mechanical, etc.) have to be considered to be able to accelerate tests as near to operating conditions as possible.

Packaging of the semiconductors plays an important role in determining the types of failures to be expected. Press-pack semiconductors, used for very high power applications, do not have wire bonds and the failure mode would be caused commonly due to solder joints and pressure contacts. Press-pack and conventional package devices are compared in [15], [18], [19]. Pressure contact IGBTs are power cycled in [20]. In a press-pack, the usual failure mode is short circuit while in conventional modules, both open circuit and short circuit, are seen [15]. Reference [21] presents power cycling of transfer-molded direct bonded copper (DBC) in diodes and compares with conventional DBCs. Aluminum silicon carbide (AlSiC) and copper based baseplates are compared in [22]. Two different flip-chip ball grid array (BGA) packaged devices are tested in [23]. Reference [24] tests silicon carbide (SiC) MOSFETs, rated at 1200 V, and 13 A. Semiconductor device type (MOSFET, IGBT, diode etc.) also determines the common failures. For example, MOSFETs predominantly have oxide related failures while IGBTs can have latch-up based failures. Lead based and lead-free solders are compared in [25].

The main function of power cycling circuit is to have current conduction through the semiconductors such that the

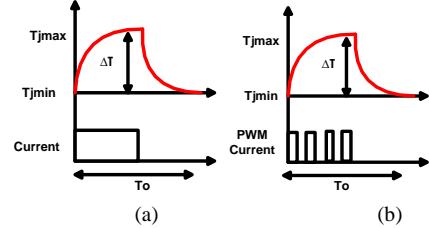


Fig. 2. (a) DC and (b) AC power cycling test concepts.

temperature increases to a maximum rated value, usually less than 125°C. Then the power is turned off until the temperature is decreased to a minimum value, greater than 25°C. The power cycling circuits are classified as AC and DC circuits based on the current used for testing. Fig. 2 demonstrates the waveforms of the current and temperature for DC and AC power cycling.

**DC circuit [10]:** A constant current for a continuous period of time is considered a DC circuit. The DC circuit is simple and easy for monitoring parameters.

**AC circuit [10]:** A PWM switching sequence for a time until the IGBT rises to a maximum temperature is applied and the device is turned off until it cools to a minimum temperature value. This circuit is usually preferred since it tests the device with the usual operating conditions.

The different circuits used in the literature are briefly described in the following sections.

#### 1) Pulse Current Source:

A specified load current  $I_{load}$  is periodically applied to the IGBT whose gate is permanently set to a constant voltage, as shown in Fig. 3(a). This is a commonly used DC power cycling test circuit. The gate voltage  $V_{ge}$  thereby must be set to a value above but closer to the gate-emitter threshold voltage  $V_{ge(th)}$  in order to assure high power losses in the device [4]. The lower and higher temperature limits,  $T_{jlow}$  and  $T_{jhigh}$ , are the parameters to be set initially in power cycle tests by means of adjusting  $I_{load}$ ,  $t_{on}$ ,  $t_{off}$  and the cooling system to appropriate values. In [4], a 300 A, 1200 V single device IGBT module was tested at gate voltages near operating condition,  $V_{ge} = 15$  V, current,  $I_{load}$  between 240 and 300 A,  $t_{on} = 0.6$  to 4.8 s,  $t_{off}$  between 0.4 and 5 s with water cooled heatsinks to maintain ambient temperatures of 60, 80, and 100°C, and a temperature swing ( $\Delta T$ ) in the junction of 30-80°C.

**Advantage:** This is one of the most popular testing circuits. Higher power losses in the device ensure faster changes in temperatures.

**Disadvantage:** The switching of a current source instead of the gate source might lead to a different failure mechanism from that during operation.

#### Switching Device Test Circuits:

The testing concept is similar to that shown in Fig. 3(a) but the device itself is switched instead of switching the current source. This ensures that switching losses are included in the testing. Avalanche mode testing is an example of switching device tests.

#### 2) Avalanche Test Circuit:

Avalanche mode testing [27] using an inductive load with a single device switching is shown in Fig. 3(b). This test circuit ensures that the losses in the diode are considered. In [27], a MOSFET, rated at 180 A, is tested at rated 20 V gate-source

voltage, and on resistance of  $4 \text{ m}\Omega$  is observed. The input DC voltage is 33 V. The indication of failure observed was 20% increase in thermal resistance.

**Advantage:** Single device is tested. The testing times and currents are reasonable.

**Disadvantage:** This circuit is not ideal for testing devices in a module with anti-parallel diodes. The parasitic inductance, shown in Fig. 3(b), can result in high  $di/dt$  and avalanche based diode failures.

#### AC power cycling test:

As already mentioned, the device is switched at a switching frequency on the order of a few kHz for a time until the temperature rises to maximum in AC power cycling tests.

#### 1) Inverters Back-to-Back [7]:

Two three phase 800 kW identical inverters are arranged in back to back form, with inductors joining the three phases for traction application, as shown in Fig. 4(a). With this arrangement, the system currents are made to circulate between the two inverters so that they each can operate at their full power of 800 kW. Only the losses (60 kW) are provided by the DC power supply. No failures were observed in the tests.

**Advantages:** This circuit is applicable to test semiconductors (devices with anti-parallel diodes) in three-phase inverter application. Minimal energy input is required. Only the losses in devices are provided by power supply.

**Disadvantage:** Three phase control is complicated compared to single phase control. Since the diodes are equally stressed, the causes of failure could be a combined effect. This circuit is best suited for application specific power cycling and not for individual device testing.

#### 2) Motor Drive Loaded Inverter [8], [9], [28]:

In references [8][9], constant current at motor rated value for 20 s and an overload motor current of 1.5 pu for 5 s were used for power cycling a motor drive, as shown in Fig. 4(b) to be able to accelerate the temperature variation and mean temperature within a short period of time. Failures were observed within 15 days. In reference [28] a “seeded” fault testing platform was used, where one of the devices in the 3-phase inverter motor drive system is replaced with an already degraded IGBT. The IGBTs are degraded for temporary latch-

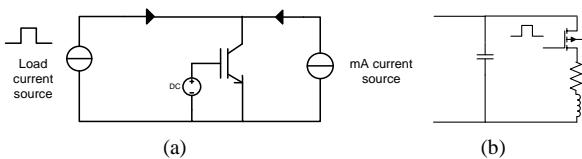


Fig. 3. (a) Typical power cycling test circuit without gate switching [4], (b) avalanche breakdown testing circuit.

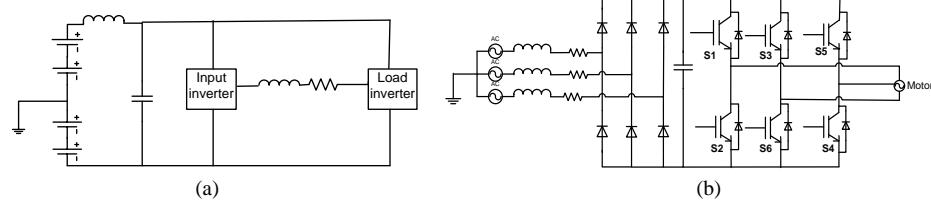


Fig. 4. Power cycling test circuits (a) three phase back-back inverters test circuit [7], (b) motor drive test circuit [8][9][28].

up after pulsing it to 125% of its rated junction temperature. **Advantages:** Failures are accelerated and occur in a low test duration time of 15 days.

**Disadvantage:** A detailed failure analysis was not conducted in [8][9]. Since motor windings are highly inductive, the failures can be a result of high  $di/dt$  in the diodes.

#### 3) Push-pull [6] [22][29]:

Two IGBT modules, rated at 1200 A and 3.2 kV were tested by Siemens in push-pull mode and the gate voltage was turned off after the collector current reached zero to avoid switching losses. The turn-off base plate temperature was maintained at 45°C. The temperature swing of the base plate was adjusted to  $\Delta T_c = 50 \text{ K}$ . For the temperature of the IGBT junction, this corresponds to a swing of  $\Delta T_j = 60 \text{ K}$  and a maximum average value of  $T_j = 106 \text{ }^\circ\text{C}$ . A current of about 0.5 per unit, (600 A) is necessary to reach this swing. The ON-time and OFF-time were 50 seconds. Voltages and currents such as  $V_{ce}$ ,  $I_c$ , as well as the base plate, cooler and water temperatures were recorded. Copper and AlSiC base plate based modules were tested and compared. The copper base plate based module reached a temperature rise of 20% from initial value and failed. The lamination between substrate and base plate was observed. No failures were observed for the AlSiC base plate module.

**Advantage:** Single device is tested. The testing times and currents are reasonable.

**Disadvantage:** This circuit setup is best suited to test single devices in DC-DC converters.

#### 4) Half-bridge Inverter with Inductive Load [19][24][29][30]:

The test is a destructive type of test, with inductive load and short circuit current through the device. The test consists of a single quadrant converter with two IGBT modules, a DC link capacitor and a load inductance with values typical for traction converter as shown in Fig. 5(b). In the first test the high side module is turned on and the current builds up in the load inductance. The current is then switched off and the high side module fails. After failure, the diode of the low side module carries the high current. The diode fails because of excessive  $di/dt$ . The modules are 1200 A, 2.5 kV devices with 24 IGBT chips and 8 diode chips each. The input voltage,  $V_{cc} = 1500 \text{ V}$ ,  $C = 6.4 \text{ mF}$  and total stored energy is 7.2 kJ. Both modules (low side and high side) showed similar damage. The top of the housing is broken; the gate unit is destroyed but no parts are ejected. The contact leads are bent [19]. Another variation of the test circuit where the parallel devices,  $T_1$  and  $T_2$ , and  $T_3$  and  $T_4$ , are controlled together, resulting in short circuit is considered as the worst-case fault in [30].

Fig. 5(c) shows the typical half bridge inverter with inductive load [43].

Advantage: Highly accelerated test.

Disadvantage: Destructive type of test.

### 5) Full-bridge Inverter with Inductive Load [15] [31] [32]:

The full bridge inverter with inductive load, shown in Fig. 5(a) has several advantages over other circuits for its simplicity, inclusion of switching losses and minimum input energy requirements. Inductive loads ensure the distribution of losses between diode and IGBT. Since the power is circulating between the phase legs, the input power required is minimal to supply for device losses only.

Advantage: Energy saving test circuit.

Disadvantage: With purely inductive load, the time for which current is distributed between the diode and IGBT is equal. Hence the diode losses are higher in this circuit than that with resistive load or motor drive load.

### 6) Low Frequency and High Frequency Topologies [33]:

For solder layer degradation type of failure, long periods of temperature cycles with timescale of minutes are used, while wire-bond stresses are observed for shorter periods of temperature cycles. 3300 V, 1200 A IGBT with  $V_{ce} = 3.8$  V and 4.6 kW power dissipation at full power is tested using three phase power stepped down. Low frequency transformer (topology 1), and high frequency topology (topology 2) are proposed. Low frequency topology, as shown in Fig. 6(a), consists of a 50 Hz, 12 pulse transformer, and rectifiers followed by a multiphase buck converter with input voltage of 20 V. Due to low voltage, MOSFETs were used. At full load, each of the phases carries 300 A. 100 V, 1220 A MOSFETs from IXYS and diodes rated at 45 V, 400 A are used for converter and rectifier. The high frequency topology, shown in Fig. 6(b) consists of three phase rectifier followed by an isolated full bridge converter with input voltage of 600 V. There are four secondary windings, i.e. each phase carries 300 A at full load. 1700 V, 400 A IGBTs are used for full-bridge; 800 V, 20 A diodes are used for the rectifier, and 400 A, 45 V

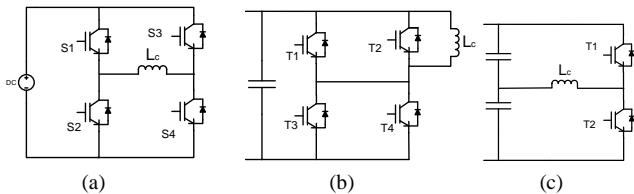


Fig. 5. (a) Single phase, full bridge with inductive load [31][15], (b) variation of half-bridge test circuit with inductive load, and (c) half-bridge test circuit with inductive load [29] [19] [30] for power cycling.

diodes are used for the secondary side of the converter.

High frequency topology is more compact than low frequency topology but the transformer design is complicated. The low frequency topology has the ability of the system to continue working if a single component fails, i.e., redundancy. However, the high frequency topology fails entirely if one of the components fails.

A current controller based on junction temperature control is implemented in both cases. To improve reliability, all components are derated by 50% to 65%. The MTBF calculated values are greater than 20 years. A prototype power cycling set up, based on boost/buck converter was developed. Advantage: High frequency and low frequency test circuits simplify the cost of set up with better control.

Disadvantage: No degradation and long-time testing results are presented.

### B. Choice of Operating Conditions

The second step in power cycling test design is to determine the operating conditions of the test circuits. The importance of the choice of the operating conditions is discussed below based on the operating conditions found in the literature.

**Temperature:** The choice of operating temperature plays a major role in the duration of power cycling tests. It is necessary to be able to have very high temperature swings in order to degrade and fail the device faster, and also operate within the ratings of the device. The influence of higher temperature swings is more significant than the maximum temperature [48]. The lower limit on temperature is usually chosen to be around 40°C to 50°C. The maximum temperature is set between 100 to 150°C [41].

**Current:** In most cases, the current is set to the rated value of the device. Sometimes, in order to accelerate the tests, the current is set to values greater than rated values [8][9]. However, since acceleration of parameters results in completely different failure mechanisms, it is not advisable to use values greater than rated.

**Voltage:** The same principle to use values less than rated applies to voltage condition too. Since most of the testing circuits use inductive loads, the voltage is usually low, as low as 1/10 of the rated value,

**Frequency:** The switching frequency plays an important role in determining the severity of the tests for AC circuit based tests. At high switching frequencies, the switching losses are high and result in high dissipation losses, thereby increasing the operating temperature. The tests have to be

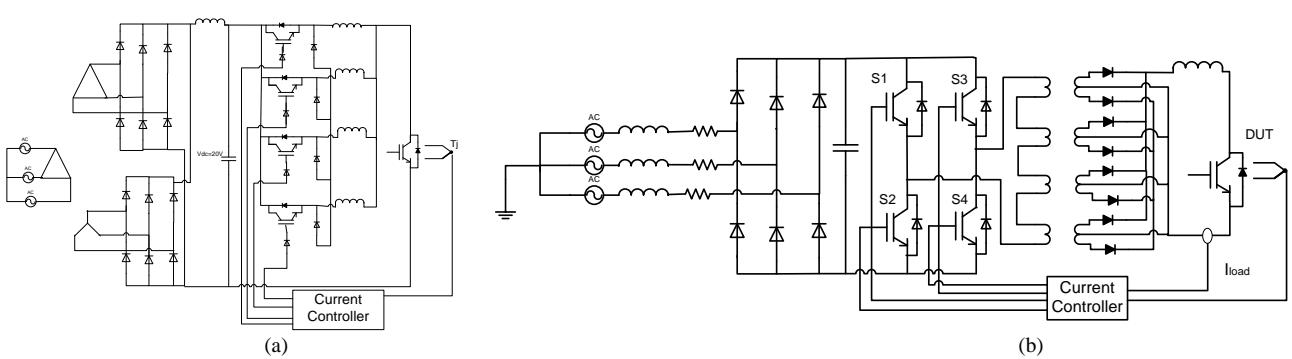


Fig. 6. (a) Low frequency and (b) high frequency circuit topologies for power cycling according to [33].

started at high switching frequencies of at least 1 kHz.

The frequency of the load or the output frequency also plays an important role in determining the time to failure [51]. For low frequency of the load current, the temperature swing is high as the time for the temperature to rise and fall is also high. Output frequencies as low as 16 mHz were observed in the literature.

### C. Precursor Parameter Monitoring for Failure Detection

Identifying the parameters/indicators of failures [34] to be monitored to first detect failures is an important aspect in design of power cycling experiments. This can be achieved with the knowledge of failure modes. Some of the common failure indicators are junction temperature, collector-emitter voltage,  $V_{ce}$ , gate threshold voltage, thermal impedance,  $Z_{th}$ , collector current,  $I_c$ , gate current  $I_g$ , drain-source resistance,  $R_{ds\_on}$ , turn-off time, voltage ringing [28], and breakdown voltage [14][35]. Reference [36] presents a detailed review of the popular precursor measurements, predominantly  $V_{ce}$  measurement. Reference [34] presents the failure modes in switched mode power supplies and their indicators. The choice of these parameters is based on their dependence on temperature. An indicator of solder cracks is thermal resistance,  $R_{thj}$ , while an indicator of wire-bond liftoff is collector-emitter voltage,  $V_{cesat}$ . In reference [37], a spread spectrum time domain reflectometry (SSTDR) is used to check for wire bond failures and are related to  $R_{ds}$  degradation.

Failure modes are interdependent and power cycling tests therefore require a careful failure analysis [38]. For example, a decrease in junction thermal resistance,  $R_{thj}$  results in increase in maximum temperature,  $T_{high}$  and this will escalate the thermal stress for the bond wires. On the other hand, bond wire lift-off leads to increased collector-emitter voltage  $V_{ce}$ , which together with the constant current causes increasing losses and raises the maximum junction temperature,  $T_{high}$ , resulting in more thermal stress in solder layers. Reference [39] describes the various failures and their indicators in MOSFETs, IGBTs and Schottky diodes. The time dependent dielectric breakdown is indicated by gate oxide leakage and gate threshold voltage. The latchup failures and hot carrier failures in IGBTs are indicated by a change in collector emitter voltage and junction temperature, respectively. A detailed survey on IGBT fault diagnostics, including gate faults, and short-circuit is presented in [40].

The prospect of monitoring precursor parameters is discussed in [31]. Table I lists the common failure indicators and the percentage drift above which failure is considered to occur [31]. The following section discusses important failure indicators.

**Temperature:** Since most of the failures are due to thermal impact, monitoring temperature would be a good indicator of failure. A failure is said to have happened when the temperature increases by at least 20% of its initial value for the same operating conditions. The failures that result from temperature increase are short circuit, hot carrier degradation, and thermal hotspot generation.

**Voltage:** The most common voltage measurements are collector-emitter voltage, gate threshold voltage, and breakdown voltage because they are dependent on temperature and also used as temperature sensing parameters.

The *collector-emitter saturation voltage* is commonly used as a temperature sensitive parameter (TSP) to obtain thermal impedance. In [3] an anomalous decrease in  $V_{cesat}$  is observed instead of the conventional increase in  $V_{cesat}$  observed in most papers. The anomaly can be attributed to activation of a solder fatigue in substrate leading to increased junction temperatures. Different deviation criteria such as, 5% [4][20], 15% [3] and 20% [48] change in  $V_{cesat}$  are considered for failure.  $V_{cesat}$  monitoring during the operation of semiconductors in an application is difficult and thus, monitoring is conducted off-line. In order to do so, the tests are either momentarily stopped or conducted during the cooling cycle [6][29][20], when the device is turned off. References [36][42][43] present new methods for measuring  $V_{cesat}$  online.

The *gate threshold voltage* is also a temperature sensitive parameter (TSP) and an indicator of gate oxide based failures. References [7][6][44] present data for gate threshold voltage degradation seen in IGBTs for operation at rated gate voltage. A 20% decrease in gate threshold voltage is considered as failure criteria.

*Breakdown voltage* is also a TSP and indicates passivation based substrate failures [45]. However, breakdown voltage as a failure indicator is not commonly found in literature. The possible reason is that the measurement of breakdown voltage during power cycling operation is difficult because it involves circuit change from the high current providing circuit, usually used in power cycling tests, to a high voltage providing circuit.

**Current:** Collector current, gate current, and leakage current are the usual indicators of failure. Current measurement, unlike voltage measurement  $V_{ce}$ , is not a conventional temperature sensitive parameter and hence is not commonly used. A 20% increase in the conducting current (*collector current*) is an indicator of thermal hotspot, and short circuit failures.

A 20% increase in the *gate saturation current* is an indicator of gate short circuit failure. Reference [46] presents the influence of gate current degradation during charging (turn-on) and presents a relevance-vector machine based prognostic method that utilizes Bayesian probability framework. However, the test results were “simulated” in [46] by lifting off bond-wires from the emitter on the chips for verifying the gate current degradation.

**Resistance:** The drain source resistance is predominantly used as a failure indicator [20][27][37], mostly in MOSFETs. The thermal impedance is also used as a failure indicator. resistance calculation is an indirect method because the voltage and current for on-state resistance, or power loss and temperature for thermal resistance, are required for its

TABLE I.

FAILURE CRITERIA EXPRESSED AS A PERCENTAGE INCREASE IN  
MONITORED DUT PARAMETERS [31].

Indicator	Symbol	% deviation for failure
Collector-emitter saturation voltage	$V_{ce(sat)}$	5%
Gate-emitter threshold voltage	$V_{GE(th)}$	20%
Collector current	$I_{on}$	20%
Junction temperature	$T_j$	20%
Gate saturation current	$I_{G(sat)}$	20%
Thermal impedance	$Z_{th}$	20%

calculation.

Turn-off time and Ringing: A. Ginart et al. proposed voltage ringing during switching as a diagnostic parameter in [47], while turn-off time is proposed as an indicator in [28]. These parameters have the advantage of easy online measurement but the time scale has to be very short on the order of nanoseconds, and hence require high band-width sensors. Periodic measurement, instead of continuous measurement, may be needed to reduce the measurement burden.

#### D. Protection Circuits

Protection circuits can be designed in order to prevent destruction of the equipment used in the test setup, and sometimes even devices under test. While protection circuits are not described in detail in power cycling tests in literature, the protection circuits are a requirement to ensure that the destructive damage is not carried to the testing, and measurement equipment.

#### E. Total Duration of Tests

The tests are required to run until failures are observed. The first estimate of the duration of tests is based on the application requirement in case of testing for lifetime estimation, and on previous tests for the conventional materials in case the tests are conducted to test new materials. However, some devices might not fail at all during testing. Hence a limit on the maximum test time, to give an estimate for planning the duration of the tests is essential. From literature, it has been observed that the power cycling tests last from 10 days to 12 months [41]. A million cycles or 6 months of test time can be considered as the maximum limit for duration of the experiments operating at near to maximum ratings. Devices that do not fail/ degrade after 6 months of high temperature power cycling testing are considered robust, and a more severe operating condition is required to accelerate failure. Most of the tests indicate linear or logarithmic relation between the lifetime of the tests and most operating parameters. Interestingly, in [49], the time to failure is estimated to be parabolic with respect to the output frequency of the testing circuit, and minimum lifetimes are found to be at 0.05 Hz. However, the test degradation is estimated based on the temperature data of the devices, curve fit to plastic strain and Coffin-Manson's lifetime model. The degradation was not accounted by physical degradations or precursor degradation.

#### F. Failure Analysis

Scanning acoustic microscope (SAM) is a non-destructive ultrasound based microscopy while electron microscopy (SEM) is based on electron scattering. SEM, SAM, and X-ray analysis are generally used for failure analysis [6][29][22][53]. Bond wire melting, bond wire lift-off, die-chip burn-out, and solder cracks are the common physical failures observed [44][17] in semiconductor packages. The failure factors and the type of failures are listed in Table II. Catastrophic damages to the devices with case blasting away were shown in [19]. Reference [39] presents the failures in SMPS in Avionics, tested at low voltage. Contact migration and thermal runaway type failures are observed in transistors, finally resulting in bond-wire failure. Electro-migration caused die damage was

TABLE II.

COMMON FAILURE MODES IN SEMICONDUCTORS [35][14] [44] [50].

Failure Factor	Failure Mode
Diffused Junction Substrate	Decreased breakdown voltage Short circuit Increased leakage current
Gate oxide film Field oxide film	Decreased breakdown voltage Short circuit Increased leakage current $h_{FE}$ and/or $V_{th}$ drift
Die bonding- Chip-frame connection	Open circuit Short circuit Unstable/intermittent operation Increased thermal resistance
Wire bonding- Wire bonding connection Wire lead	Open circuit Short circuit Increased resistance
Input/output pin- Static electricity Surge Over voltage Over current	Open circuit Short circuit Increased leakage current
Passivation -Surface protection film Interlayer dielectric film	Decreased breakdown voltage Short circuit Increased leakage current $h_{FE}$ and/or $V_{th}$ drift Noise deterioration

observed in diodes.

In the literature, there are two approaches to estimating lifetime models, the curve fit or statistical models and the physics of failure models [54]. Physics of failure methods require careful study of the degradation mechanism, resulting in thermo-mechanical fatigue. Some of the physics of failure mechanisms in wirebond [55], and solder [56]- [58], have been researched recently. After the failure mechanism is detected and analyzed, the physics of failure lifetime model is developed to relate the total duration of time or number of cycles and operation parameters. Development of physics of failure methods is a wide research topic by itself and is beyond the scope of this paper.

Table III compares the different power cycling tests in the literature and their results based on operating conditions, time to failure, type of failure and circuit. The choice of the comparison is mainly based on test circuit used and the type of failures observed, to encompass the power cycling test methodology and planning.

### III. CONCLUSIONS

A literature review of the state-of-art for power cycling tests of IGBT devices is presented. A design of experiment methodology is presented that includes determining circuit selection, parameters to be monitored, operating conditions, and duration of tests. While different circuits are used to power cycle semiconductor devices, inverter circuit with inductive load is popularly used due to its cost and energy saving capability for long-term tests. A 20% change in collector emitter voltage, on-state resistance, thermal resistance, gate voltage, and temperature are the commonly used parameter indicators for degradation and failures. The duration of power cycling tests depends on the application requirement and the testing objective. Failure mechanisms are analyzed using additional sophisticated. A comparison of the most popular test

TABLE III.

COMPARISON OF POWER CYCLING TESTS BASED ON OPERATING CONDITIONS, TIME TO FAILURE, AND CIRCUIT.

Reference/ method	Testing profile	Measure- ments	Cooling	Tempera- ture swing and $T_{max}$	Failures and indicators	Failure mecha- nism	Circuit		
Hamidi[52]	250 A for 0.9 s and off for 1.3 s	Junction temp., $V_{ce}$ , $I_c$	Water cooled	$\Delta T=60K$ $T_{max}=105-115$ °C	$V_{ce}$ increase at 400000 cycles	Wire bond lift-off	Pulse		
RCT[5]	500 A for 45 s and 2000A for 5 s	$V_{dc}$ , $I_{ac}$ , IGBT temp.	Air cooled	$\Delta T=7K$	No failures after 113522 cycles, 1491 hours		1 phase H bridge		
High temp Power cycling	200 A for 20 s, off for 40 s	Junction temp., $V_{ce}$ , $I_c$		$\Delta T=80K$ $T_{max}=150$ °C	$V_{ce}$ increase at 42800 and failure at 43,500 cycles	Gate leakage failure	3 phase inverter with current generator		
Acc.testing for traction [7]	Realtime current profile of traction used. 113 s period	Automatic temp. measurements,			No failures after 2200 hours		Two inverters joined by inductors, 800 kW power, 60 kW losses		
	Half sinusoidal current by rectifier bridge, different current profiles used	$V_{ce}$ and $T_j$		$\Delta T=100$ to 150K	Shown in table below		6 diodes tested		
High temp swing[21]			Results	$\Delta T_j$ (°C)	Heating time (s)	Cooling time (s)	Load current (A)	Failure cycles	
			Power cycling1	105	38	56	18	60k	
			Power cycling2	130	20	70	28	-	
			Power cycling3	155	28	85	32	-	
			Copper molded	110	21	84	28	3800	
Thermo- electric cooling[26]	50A in 12 s period, $T_j$ varying from 10 to 150 °C	Junction temp.	Thermo electric coolers	$\Delta T=140K$	1427 cycles, 37 hours	Wire bond liftoff		1 phase inverter	
Different temp. swing[20]	23 s heating and 5 s cooling cycle	$V_{ce}$ , $R_{th}$	Water cooled	$\Delta T=80K$ $\Delta T=110K$	85360 cycles at $\Delta T=80K$ 28900 cycles at 110K	Wire bond liftoff		6 pack IGBT module, 2 IGBTs in central H-bridge tested in series	
Destructive type tests[19]	Single pulse	$V_{ce}$	none	$T_j=25$ and 120 °C	1000 s	Lead bent		Half-bridge with inductive load	

circuits, failure mechanism, and time to failures is presented to give an insight of power cycling test design.

#### ACKNOWLEDGMENT

This work was funded by the Electric Drive Technologies Program of the U.S. Department of Energy. This work made use of Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and DOE under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

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