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Single Donor Doped and Undoped Accumulation Mode Metal Insulator Semiconductor Device Structures for Quantum Computing at SNL

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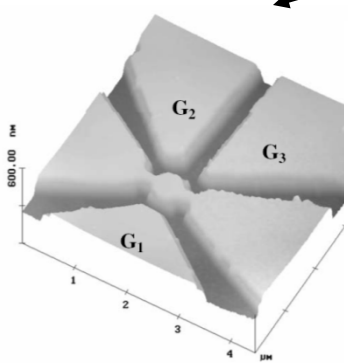
Outline

- Introduction
- MIS Structures to be pursued at SNL
- “Synergistic” QC Technology Development & CINT

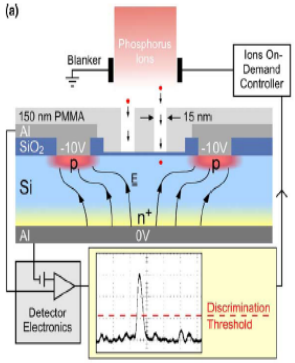
Introduction

Fabrication of Silicon Single Electron 2-level Systems

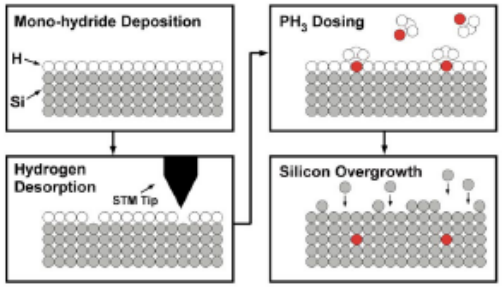
Single Electron and Single Spin Measurements



SiGe/sSi/SiGe QDs

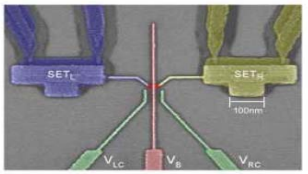


Top-Down Donor

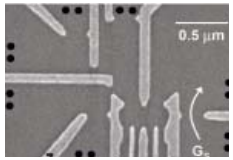


Bottom-up Donor

EDMR



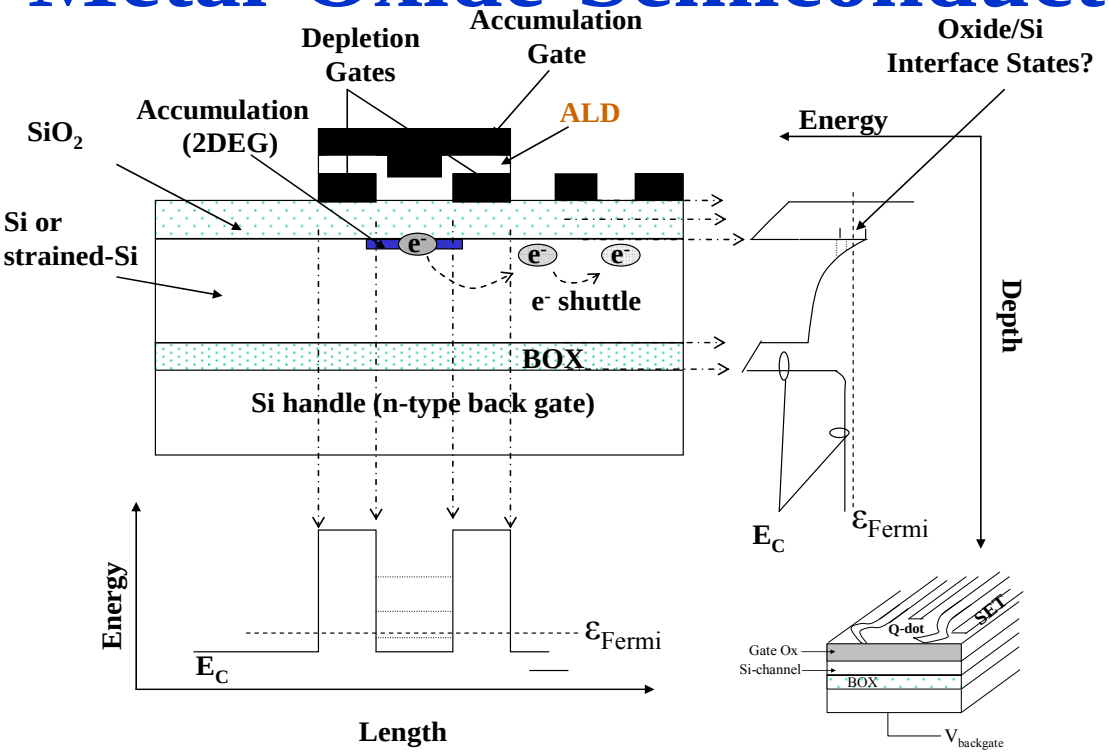
RF-SET

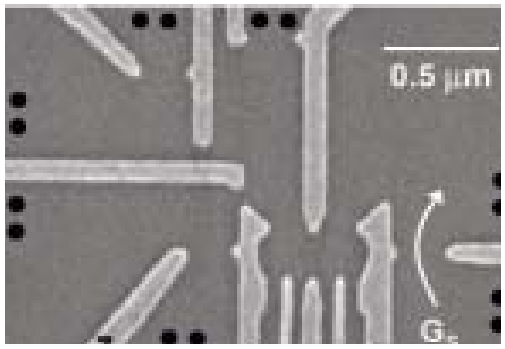


QPC

- **Several approaches to form single electron Si devices for qubits have shown great promise recently**
- **Sandia pursuing alternative Si quantum dot approach to complement community effort**
- **Approach: Accumulation mode metal-insulator-semiconductor based quantum dots (MIS-QD)**

Metal-Oxide-Semiconductor Structure





J. Petta, et al., Science v309 p2180

- Benefits of accumulation mode MIS-QD:
  - Standard CMOS and high purity (low dopant) material integration
  - Large valley splitting expected at Si/SiO_2 interface
  - Gates very close to 2DEG => small confining geometry
- Potential disadvantage:
  - Non-epitaxial oxide/Si interface

SNL staff

E. Nordberg

K. Eng

L. Tracy

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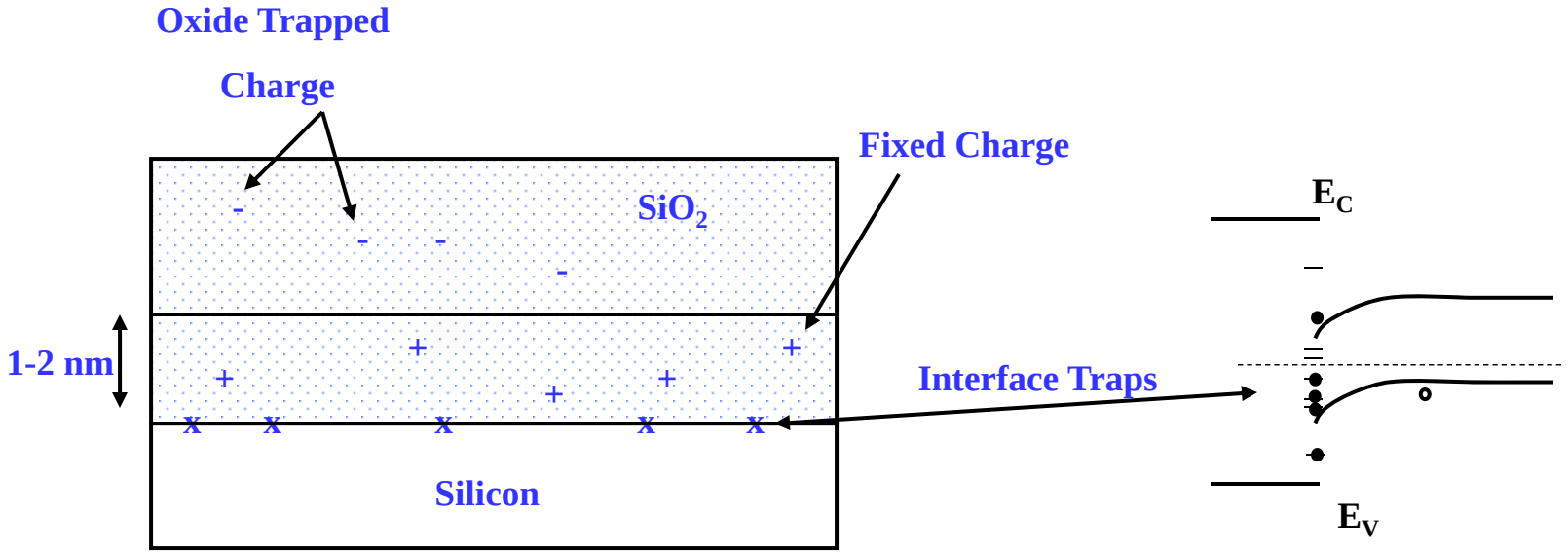
m6

Thermal Oxide Considerations



- High temperature thermal oxides are very good for MOSFETs but are they sufficient for Qubits?
- The perceived problems:
  - 1. $D_{it} \sim 10^9 – 10^{10}$ eV^{-1} cm^{-2} => uncontrolled trapping
  - 2. $Q_{ss}/q \sim 10^{10}$ -10^{12} cm^{-2} => remote scattering & surface accumulation
  - 3. Interface roughness => universal mobility curve

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m6 it - trivalent Si, extra O, impurities & fundamentally is related to the symmetry breaking at the surface

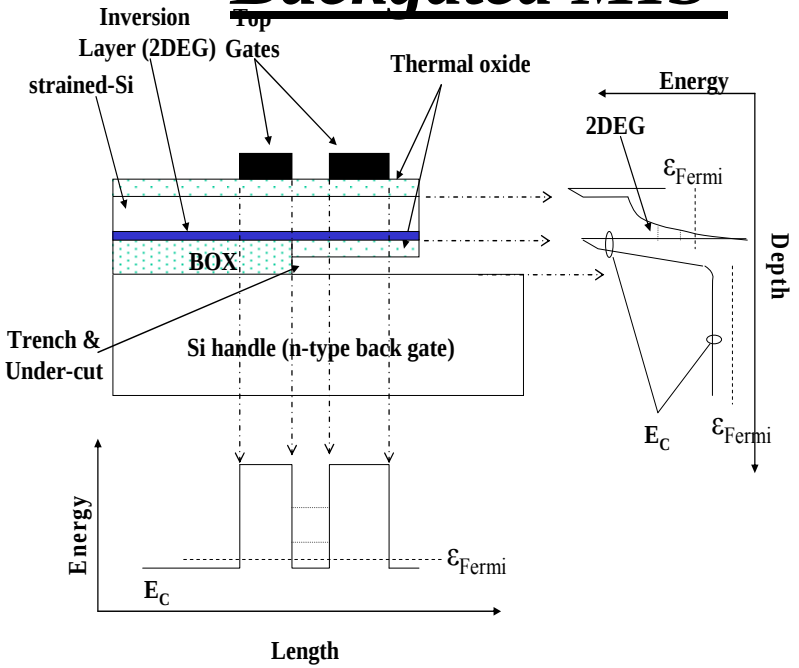
Fixed - near 1-2 nm of silicon - incomplete silicon-silicon

Trapped - from x-ray, UV, transport

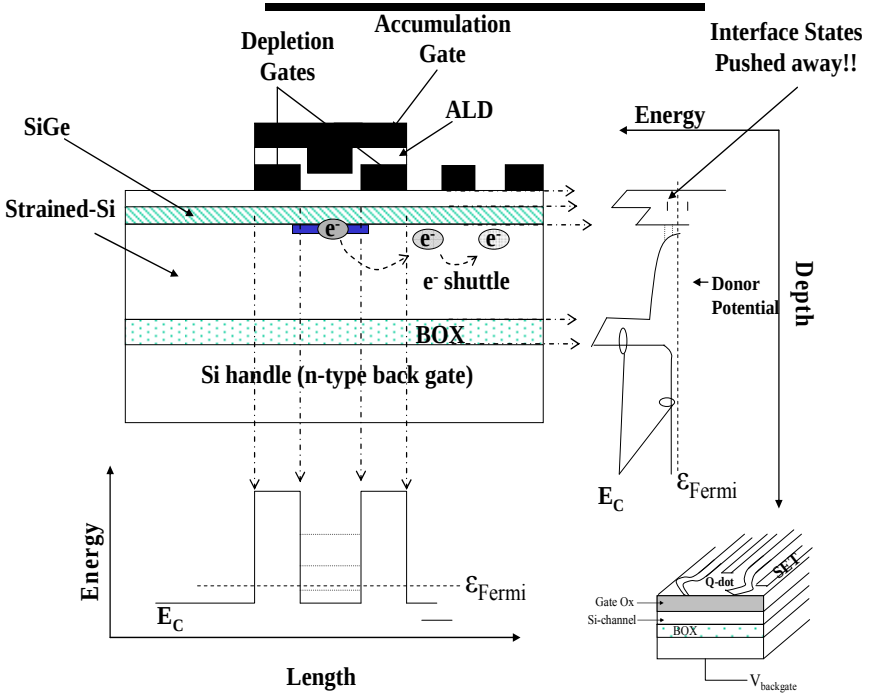
mscarro, 1/27/2007

Improved Interface Approaches

Backgated MIS



sSi-SiGe MIS



- Currently NOT clear that oxide interface is "death" for single qubit
  - Hirayama et al. => single electron & Pauli blockade
  - Yablonovitch => damage required to measure RTS
  - Angus et al. => "quiet" Si SETs
- Anticipated challenge (1):
  - Top gate poly-etch introduces defects => backgate
- Anticipated challenge (2):
  - Oxide just not good enough for N > 2 QDs => top-gate OR back-gate sSi/SiGe

SNL staff

K. Eng

L. Tracy

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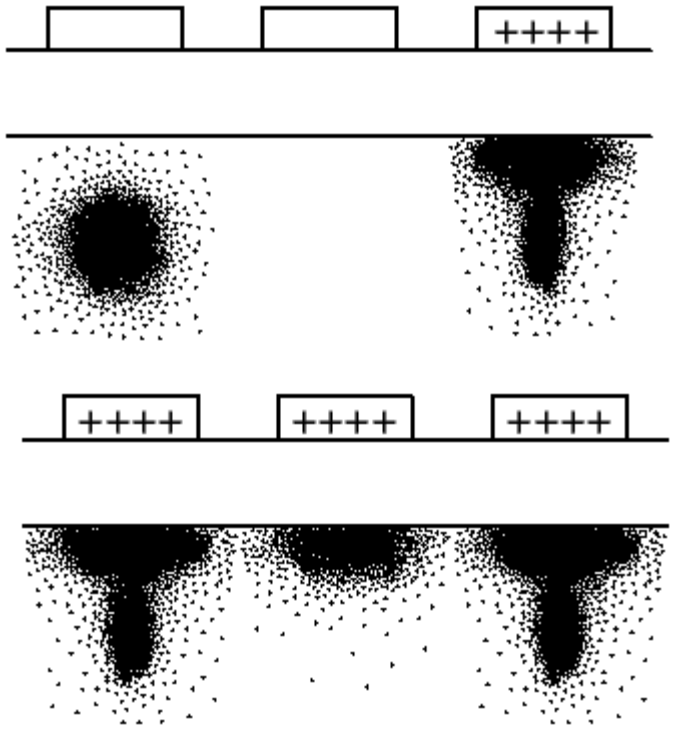
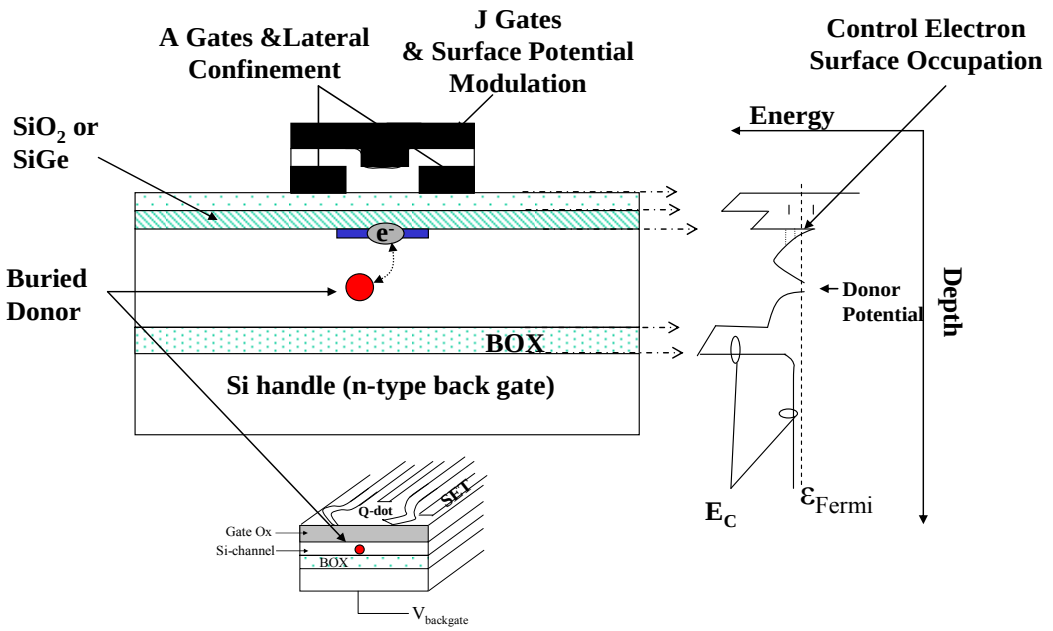
Single Donor Doped MIS-QDs

Kane, Fortsch. Phys. (2000)

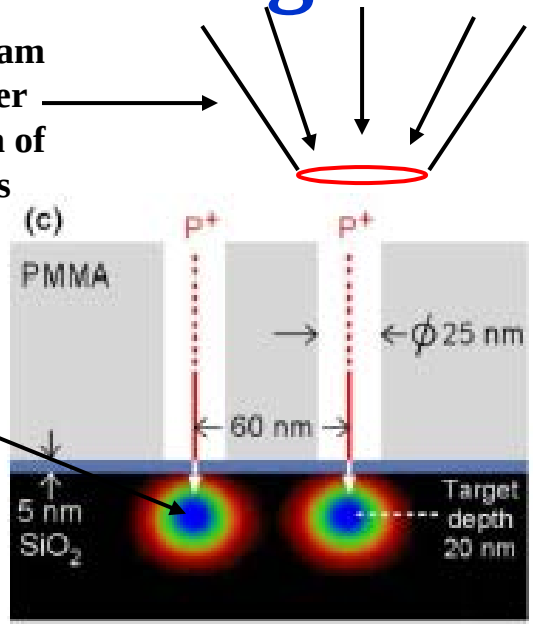




- **Kane based A-J-A scheme draws electron towards surface**
- **One challenge is an uncontrolled surface charge configuration (e.g., traps)**
- **SNL gate oxide integration w/CQCT process desired (poly-Si also …)**
- **Can MIS QD also be used to better understand and/or control donor?**
  - **e^- occupation in dot is gate tunable / donor provides exactly 1 e^-**
  - **Additional lateral confinement also provided by structure**

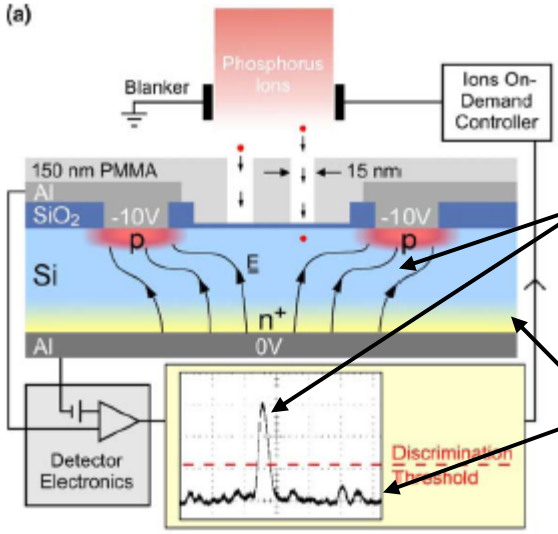
Single Donor Implantation

Focus of ion beam must be smaller than separation of quantum dots



Diameter is ion energy Dependent

Mitic et al., Micro. Elec. Eng. (2005)

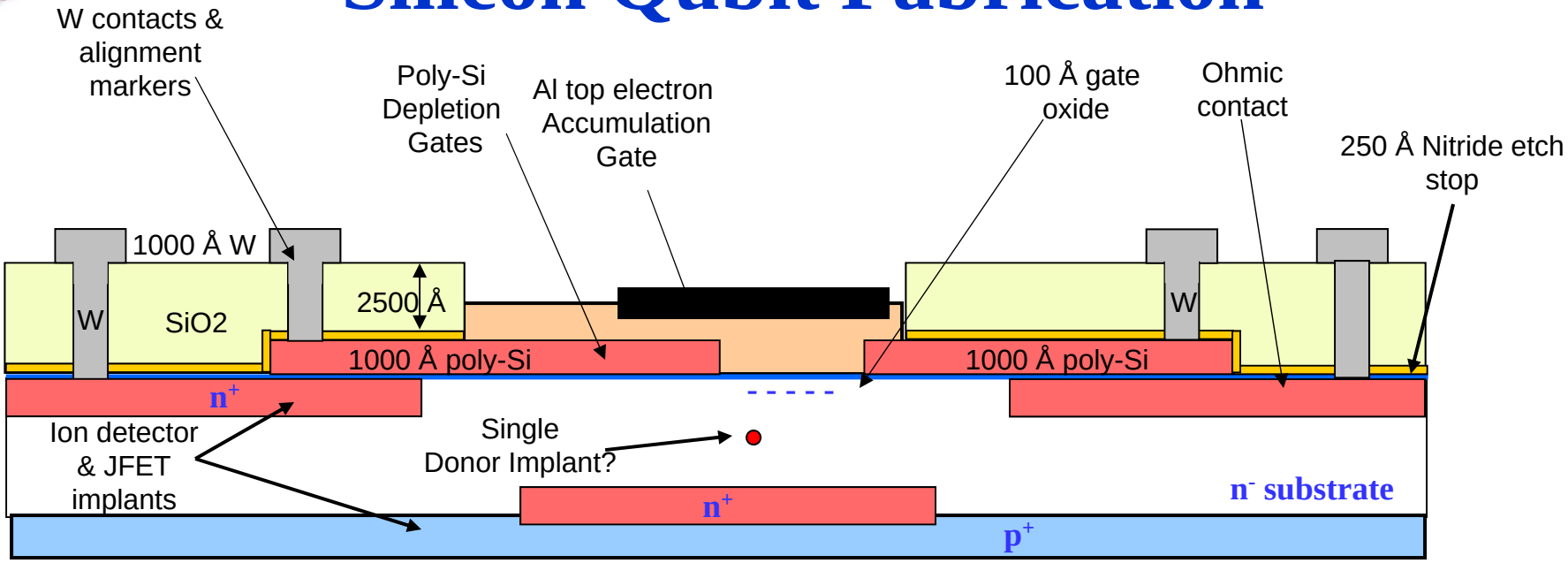


High field diode design produces avalanche gain using impact ionization

JFET or APD integration will reduce noise floor

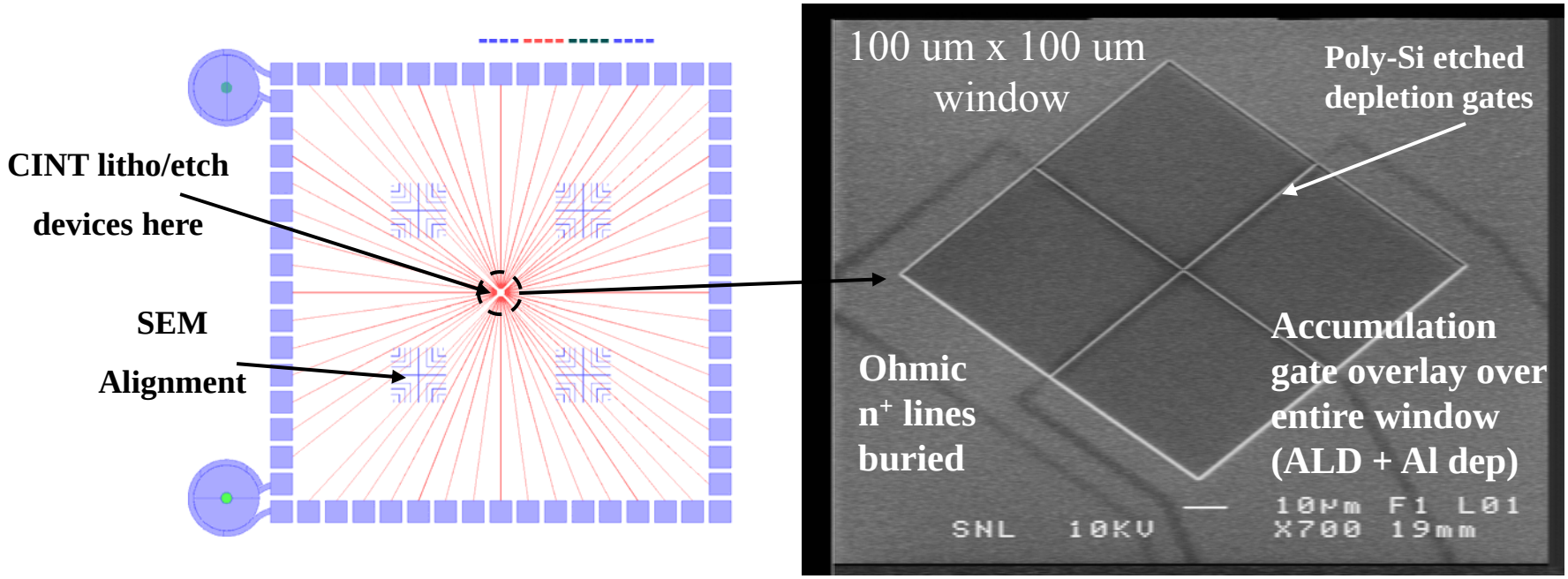
- CQCT has pioneered single ion implant using integrated p-i-n
- Focused ion beam desired to provide implant of individual QDs w/out multiple EBL
- APD or JFET integration will increase signal or decrease noise floor providing state-of-the-art control over straggle
- E. Bielejec and B. Doyle will be pursuing improved detection and sub-100 nm focus ion beam

Silicon Qubit Fabrication



- **Silicon "front-end" formed in MDL to leverage best silicon material processing**
- **CINT/Micro-fab "back-end" will be used for nanolithography, etching of depletion gates & deposition of accumulation gate**
- **Single donor integration is compatible with process**
- **Nanoschottky & RF-SET CQCT process may be developed either at SNL or CQCT ("Fed-Ex fab")**

“Back-end” Integration with CINT



- SNL “front-end” starts with a sheet of poly-Si in window
- Nanolithography combined with Si etch forms the poly-Si depletion gates (e.g., split gates)
- Atomic layer deposition combined with top metal completes device
- Ohmic contacts are made with buried n^+ layers under top gate
- Eric Nordberg will give more details in his talk

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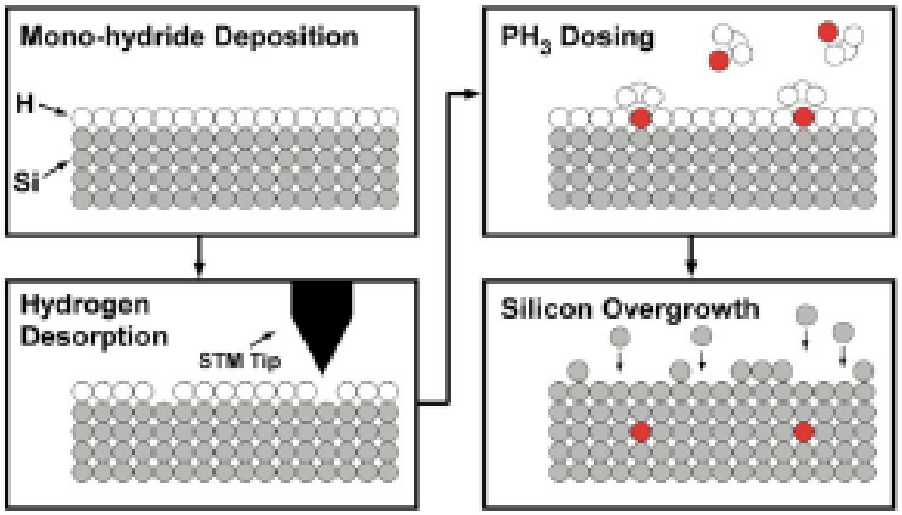
- “Synergistic” QC Technology Development & CINT

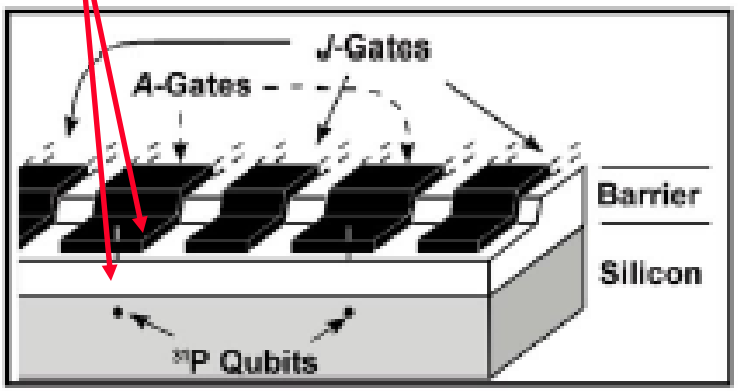
Other Application for ALD

1200ºC!



Low T

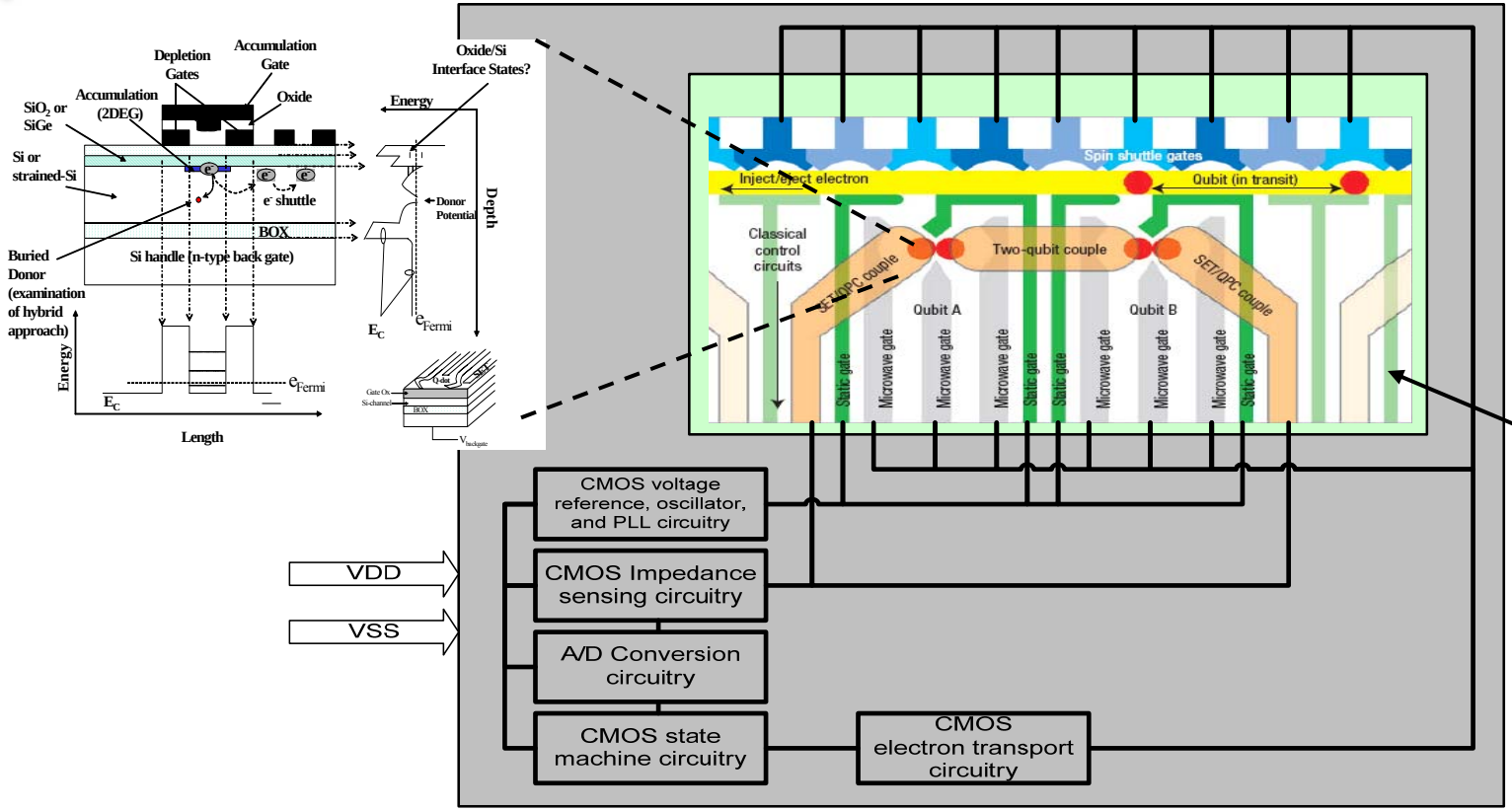
Ideal Insulator typically requires high T?!



•O'Brien et al., PRB (2001)

- Bottom-up approach has demonstrated atomic precision dopant placement
- STM lithography process presents unique challenges to integration with insulator/gate integration
- Primary challenge appears to be development of high quality low-temperature insulator on silicon
  - Donors will diffuse if standard thermal oxide is used
- ALD development by R. Grubbs will be examined

Long Term Goal



SNL Staff:
T. Gurrieri
J. Levy
C. Tigges
L. Pierson

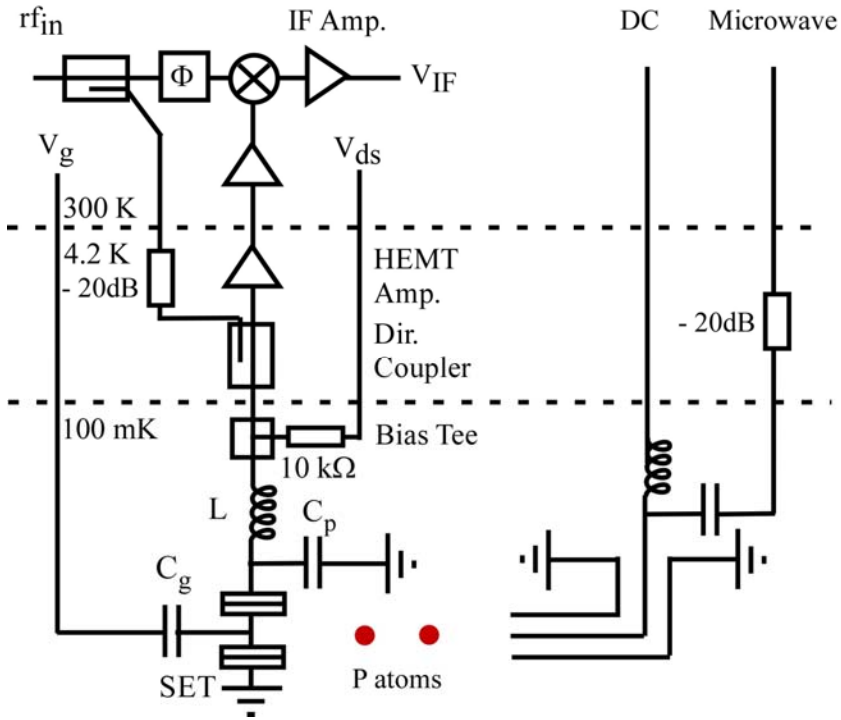
Taylor et al., …

- ***Primary goal:*** ***demonstrate silicon qubit for quantum circuitry***
- **Encouraging results suggest single Si qubit might come soon**
- **CMOS industry thinks in terms of doubling transistors every couple of years**
  => Is there a viable path for the single demonstrated physical Si qubit for useful quantum circuits with 2, then 4 then 8 physical qubits (i.e., first stage of logical qubit)?
- **What are the requirements for the classical circuit interface to control and read-out?**
- **SNL will leverage experience with integrated circuit design for complex systems**

Implementation of rf-SET

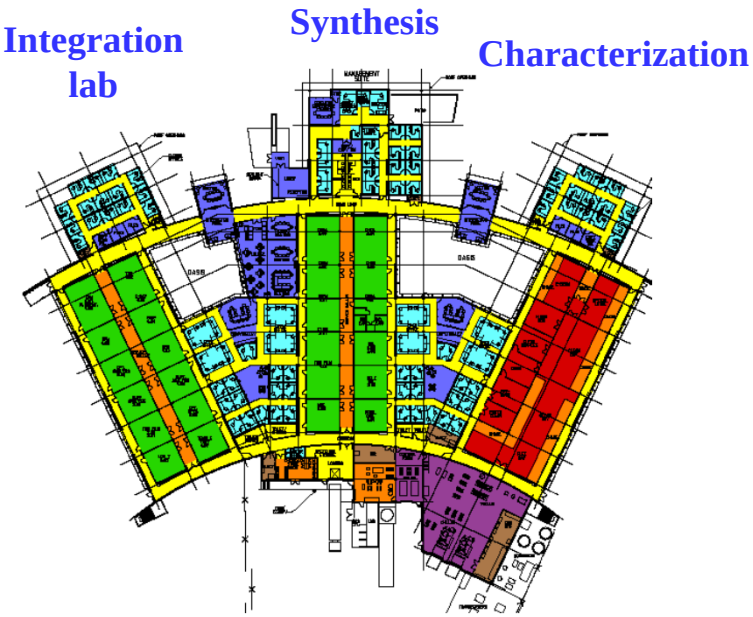
CQCT tank circuit for high speed readout in a dilution refrigerator

A. J. Ferguson



- **Fridge modifications**
  - **additional semi-ridgid coax**
  - **4K cold finger for preamp**
  - **rf board**
- **Equipment**
  - **sources, preamps, signal analysis, low T components**
- **Expertise**
  - **CQCT will provide current plans for rf SET infrastructure**

Measurement facility at CINT



- The Center for Integrated Nanotechnologies is a DOE user facility
- The low temperature capabilities are located at CINT
- Advantages – easy access for outside collaborators, extended working hours for FNs, on-site cleanroom, characterization tools and discovery platform development

Summary

- SNL initiating Si quantum dot project to complement and assist quantum computing community
- Si accumulation mode MIS-QD structure is platform that will be used to examine:
  - Oxide/Si interface concerns
  - Novel insulator integration approaches (e.g., SiGe & ALD)
  - Single donor qubit approaches
- Integrated circuit experience also leveraged to examine near term approaches to quantum circuit development
- CINT is one possible gateway to enable university collaboration between UW and CQCT