SAND2014-20657C

Reduced Complexity RHBD Logic Cells for 32-nm SOI ASICs

John Teifel, Jeff Black, Eric Edwards, Tom J. Mannos
Sandia National Laboratories
Albuquerque, NM 87185, U.S.A.
jteifel@sandia.gov

Abstract: *Reduced complexity 32-nm silicon-on-insulator (SOI) logic cell libraries and test chips have been developed for evaluation in harsh radiation environments. SOI-specific radiation hardened by design (RHBD) methods, including body contacts and stacked transistors, were leveraged for improved radiation hardness. The number of cells and their complexity was intentionally limited to lower development costs and simplify portability to other SOI technology nodes.*

Keywords: body contacts; radiation hardened by design; silicon-on-insulator; stacked transistors; 32-nm ASICs.

Introduction

In the nanometer-scale integrated circuit era, SOI fabrication processes have successfully competed against traditional bulk silicon processes for low power, high performance, and RF consumer applications. This has benefited military and space electronics suppliers with low-cost access to SOI technologies, which are inherently more tolerant to radiation effects than bulk technologies due to their transistor-level isolation, smaller sensitive volumes, and reduced junction areas. Nonetheless, commercial SOI devices still suffer from radiation effects and additional design techniques are required to use them in harsh radiation environments [1].

In this paper, we describe a family of reduced complexity RHBD logic cells for 32-nm ASICs. This work differs from previous efforts [2] in that the primary aim is to maximize radiation hardness; with speed, density, and power being secondary goals. In addition, the number of logic cells, listed in Table 1, and their complexity were minimized to reduce development costs and streamline portability to other SOI nodes. Similar reduced complexity logic cells have been used in rad-hard structured ASICs, with minimal performance impact to most applications [3].

Table 1: Reduced complexity RHBD logic cells.

Cell Name	Description
BUF	Medium-drive buffer for data signals.
CLKBUF	High-drive buffer for clock signals.
NAND2	Two-input NAND gate.
DFFR	Positive edge-triggered D flip-flop with asynchronous active-low reset.
TIE0	Ties signal to Vss.
TIE1	Ties signal to Vdd.

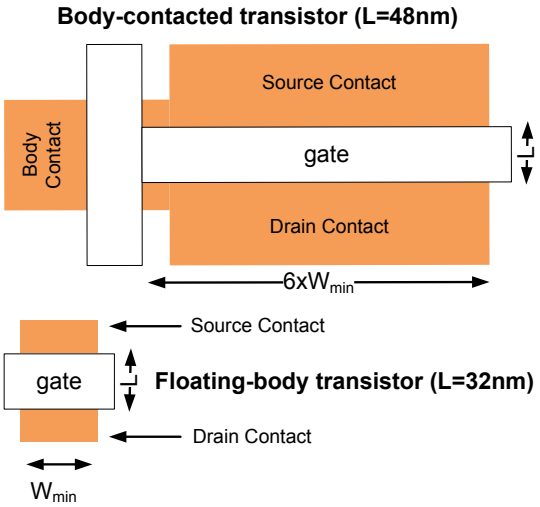

Figure 1: Notional layout geometries for 32-nm body-contacted and floating-body devices (not to scale).

Rad-Hard-by-Design Approach

Figure 1 shows 32-nm SOI transistor layout geometries for floating-body devices, normally used in digital logic cells, and body-contacted devices, typically used in analog/RF circuits [4]. The body-contacted devices, while six times larger than the floating body devices, have reduced parasitic bipolar amplification, which can improve hardness in dose rate, single event, and total dose radiation environments [1][5][6][7]. We designed reduced complexity logic cells with and without body contacts to compare their hardness levels.

While DICE (Dual Interlocked storage Cell) registers are often used to harden bulk silicon processes against single event upsets, SOI processes can leverage more efficient stacked transistor architectures to achieve a similar benefit [8][9][10]. Figure 2 shows a 32-nm stacked transistor DFFR register cell, where redundant series devices are used to mitigate upsets on any single transistor. We also used stacked devices in the combinational logic cells to decrease the generation rate of single event transients in the data path logic and clock networks.

Although recent work has investigated radiation effects in 32-nm devices and methods for mitigation [2][11][12][13], we believe the unique contributions of this paper include:

- 32-nm test chips for the direct comparison of body contacted transistors versus floating body transistors in RHBD logic cell designs.

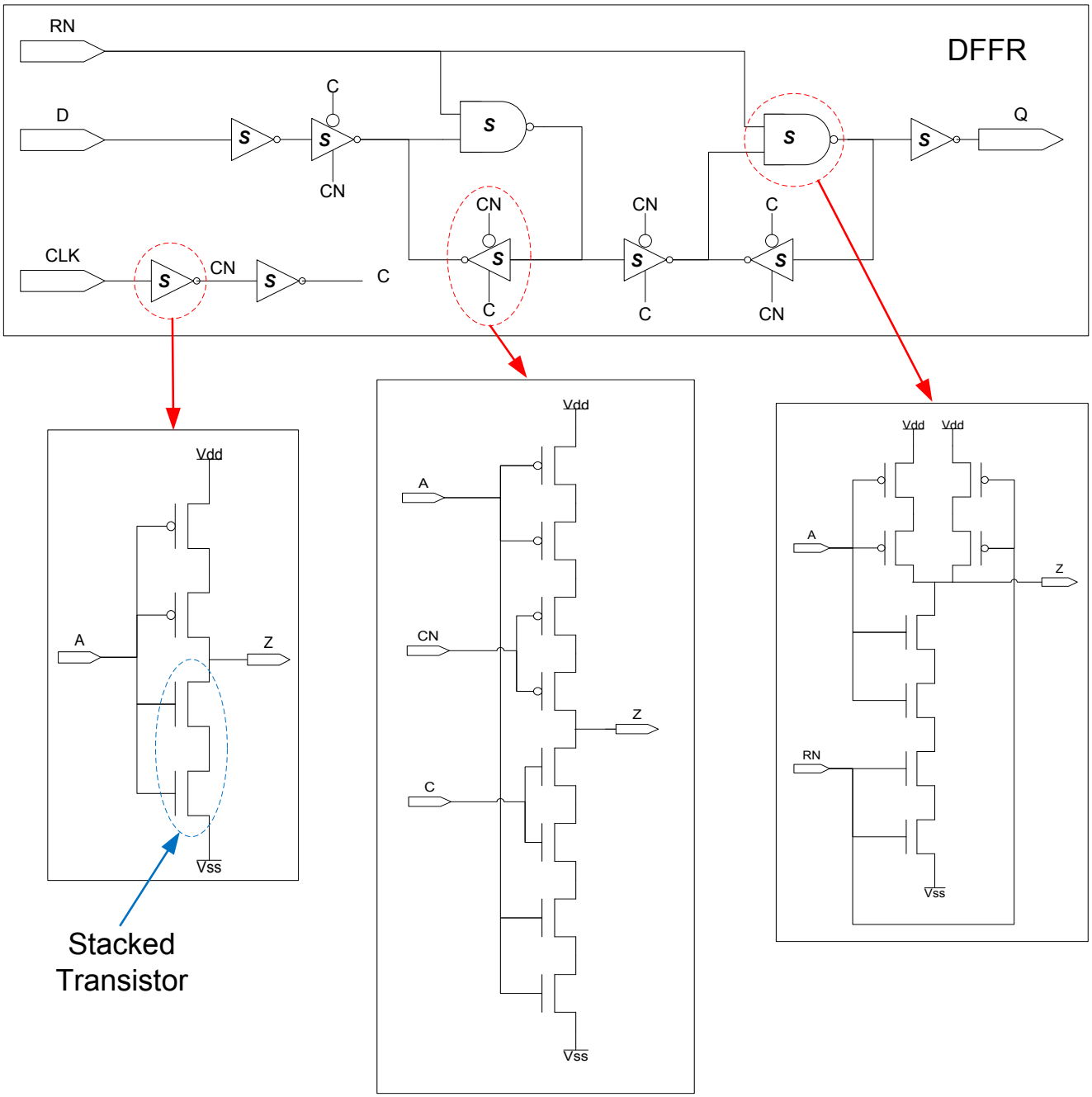

Figure 2: DFFR register circuit with stacked transistor devices (denoted with *S*) for single event effect mitigation.

- 32-nm test chips for the direct comparison of analog/RF transistors versus digital transistors in RHBD logic cell designs.
- 32-nm test chips for the direct comparison of fully stacked designs (flip-flops, combinational logic, and clock/reset trees) versus non-stacked designs.
- Logical effort analysis of stacked transistor logic cells.

Test Chips

Seven 32-nm reduced complexity logic cell libraries were created to evaluate the radiation performance of the RHBD techniques described in the previous section. Each cell library was implemented on a separate test chip, as summarized in Table 2. The first four test chips (ABNS, ABST, AFNS, AFST) used analog/RF transistors with their associated large transistor widths, and varied the body type (floating versus tied) and the stacking versus non-stacking configurations. These test chips allow direct comparisons of floating body versus body contacted devices, as well as stacked versus non-stacked devices. The fifth test chip (DFST) used digital transistors with the same width as the analog/RF chips and in a stacked configuration, which allows direct comparison between floating body analog/RF

Table 2: 32-nm RHBD test chip configurations.

Test Chip	Logic Cell Properties							
	Digital Transistors	Analog/RF Transistors	Body Contacted Transistors	Floating Body Transistors	Stacked Transistors	Large Width Transistors	Narrow Width Transistors	1-um Sensitive Node Spacing
ABNS		●	●			●		
ABST		●	●		●	●		
AFNS		●		●		●		
AFST		●		●	●	●		
DFST	●			●	●	●		
DFSS	●			●	●		●	
DFSX	●			●	●		●	●

transistors and floating body digital transistors of the same device width. The final two test chips (DFSS, DFSX) used digital transistors that were down-sized to have three times smaller widths than an analog/RF transistor. These enable performance comparisons with existing 32-nm RHBD cells that use the more area-optimal digital transistors [2][11][13].

The footprints and port locations of each cell layout, shown in Figure 3, were kept consistent across all of the logic cell libraries such that the same auto-place-and-route chip layout could be re-used across all seven test chips. While all of the test chips used I/O cells with non-stacked transistors, by relying on large I/O transistors to reduce single event transients, the test chips with body contacted logic cells also used body contacted transistors in their I/O cells to minimize SOI snapback effects. Additional miscellaneous cells, such as antenna and fill cells, were also created. All of the stacked circuit layouts used the 'end-to-

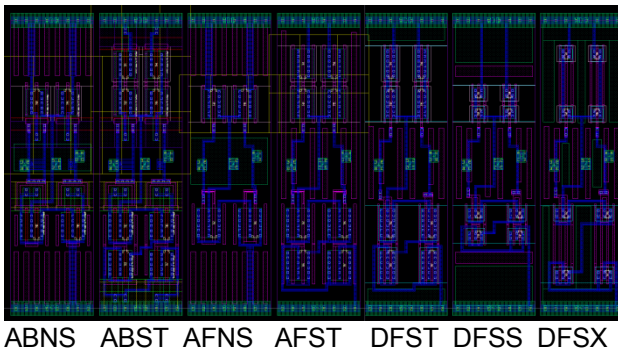

Figure 3: NAND2 cell layouts for each RHBD library.

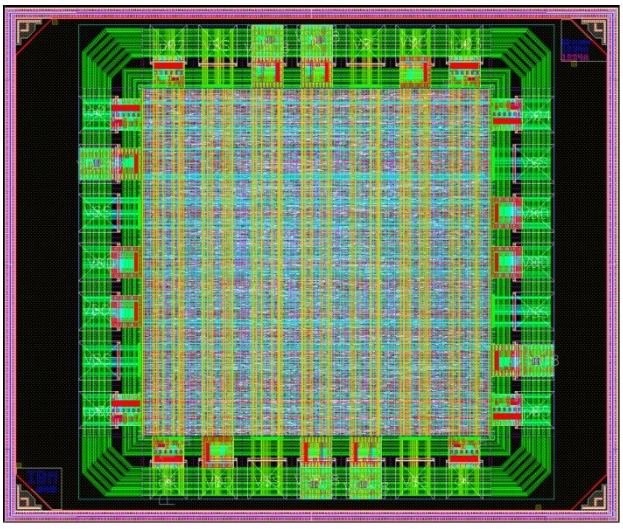
Figure 4: Test chip layout image (1.2mm x 1.0mm).

end' gate configuration presented in [11] for maximum robustness against angled particle strikes. In addition, one of the chips (DFSX) separated the sensitive transistors in the stacked cells by 1-um for added single event hardness.

Figure 4 shows the auto-place-and-route layout used for the seven 32-nm RHBD test chips. Each test chip implements an autonomous 3K logic BIST (Built-In-Self-Test) structure containing integrated state-of-health and error outputs that has been proven on earlier radiation test chips [3]. There are 28 peripheral wire-bond die pads, 8 for signal and 20 for power and ground. Separate test chips were required for each library so that the leakage current degradation and photocurrent generation in radiation environments can be correlated to the device configuration (i.e., transistor type, body type, etc.).

Stacked Circuit Performance Analysis

While standard spice circuit simulations were used to design and characterize the stacked library cells described in the previous section, it is worthwhile to analyze the circuit speeds of stacked designs with a more analytical model. 'Logical Effort' is one such model, which allows the performance of different logic families (e.g., static, domino, etc.) to be compared with each other, and also which can define how to select transistor widths for optimal circuit speed [14]. The gate delay in the logical effort model is defined by the following equation:

$$d = g \cdot h + p$$

where d is the delay normalized to a minimum sized inverter, g is the logical effort, h is the electrical effort, and p is the parasitic delay. The logical effort, g, is the input capacitance of the gate normalized to the input capacitance of an inverter sized to have equal drive strength. The electrical effort, h, represents the gates's fanout load, and is the output capacitance divided by the input capacitance. The parasitic delay, p, is the intrinsic delay of the gate when it does not drive a load.

Table 3: Logical effort model parameters for stacked and non-stacked logic cells.

	g (logical effort)	p (parasitic delay)
Inverter (non-stacked)	1	1
Inverter (stacked)	4	2
NAND2 (non-stacked)	1.5	2
NAND2 (stacked)	6	4
NUMX2 (non-stacked)	2	4
NMUX2 (stacked)	8	8

Table 3 lists the logical effort model parameters for stacked and non-stacked logic cells when assuming equal drive currents for the NMOS and PMOS transistors, which is a valid first-order approximation for the 32-nm transistors used in this paper. These model parameters show that the logical effort of a stacked cell is four times that of a standard non-stacked cell. Intuitively, this is a result of the 2x increase in input gate capacitance combined with the 2x decrease in drive strength due to the redundant series transistors in a stacked logic cell. This means that a stacked gate will be inherently four times weaker than a non-stacked gate when they are designed with equal sized transistors, and likewise that a stacked gate will be four times larger than a non-stacked gate when their transistors are sized to have equal drive currents.

When using the logical effort model, Figure 5 shows that the speed overhead of stacked logic cells is between 3x and 4x for typical logic loads. This closely agrees with 32-nm spice simulations of the library cells discussed in the previous section.

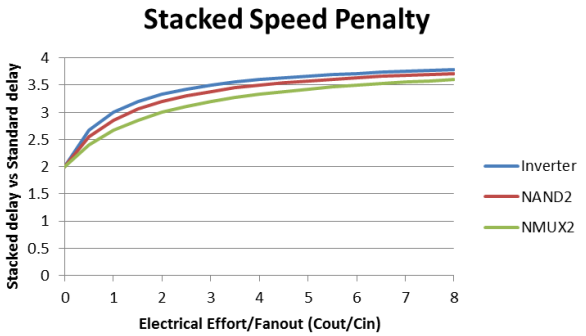

Figure 5: Logical effort performance analysis of stacked transistor cells, showing the speed overhead (ratio of stacked cell delay to non-stacked cell delay) versus electrical effort.

Summary

Seven 32-nm reduced complexity logic cell libraries and their associated test chips were developed to evaluate the radiation performance of SOI body contacted and stacked transistor cell designs. These chips will be fabricated at the IBM Trusted Foundry and undergo evaluation in relevant radiation environments.

Acknowledgements

Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

References

1. J. R. Schwank, et. al., Radiation Effects in SOI Technologies. IEEE Trans. Nuclear Science, vol. 50, no. 3, Jun 2003.
2. R. Brees, et. al., 32-nm RHBD. GOMAC, Mar 2014.
3. J. Teifel, et. al., ViArray Standard Platforms: Rad-Hard Structured ASICs for Digital and Mixed-Signal Applications. IEEE Aerospace Conference, Mar 2012.
4. S. Lee, et.al., Advanced modeling and optimization of high performance 32nm HKMG SOI CMOS for RF/analog SoC applications. VLSI Technology, 2012.
5. A. Madan, et. al., The Enhanced Role of Shallow-Trench Isolation in Ionizing Radiation Damage of 65 nm RF-CMOS on SOI. IEEE Trans. Nuclear Science, vol. 56, no. 6, Dec 2009.
6. K. A. Moen, et. al., Evaluating the Influence of Various Body-Contacting Schemes on Single Event Transients in 45-nm SOI CMOS. IEEE Trans. Nuclear Science, vol. 57, no. 6, Dec 2010.
7. R. Arora, et. al., Impact of Body Tie and Source/Drain Contact Spacing on the Hot Carrier Reliability of 45-nm RF-CMOS, IIRW Final Report, 2010.
8. K.K. Ma, Radiation-hardened transistor and integrated circuit, US Patent 7,298,010, 2007.
9. P. Oldiges, et. al., Stacked devices for SEU immune design. IEEE SOI Conference, 2010.
10. J. Warnock, et. al., POWER7 Local Clocking and Clocked Storage Elements. IEEE ISSCC, Feb 2010.
11. K.P. Rodbell, et. al., 32 and 45 nm Radiation-Hardened-by-Design (RHBD) SOI Latches, IEEE Trans. Nucl. Sci., vol 58, no. 6, 2011.
12. J.A. Maharrey, et. al., Effect of Device Variants in 32 nm and 45 nm SOI on SET Pulse Distributions, IEEE Trans. Nucl. Sci., vol 60, no. 6, 2013.
13. J.S. Kauppila, et. al., Utilizing Device Stacking for Area Efficient Hardened SOI Flip-Flop Designs, IRPS Proceedings, 2014.
14. I.E. Sutherland, et. al., Logical Effort: Designing Fast CMOS Circuits, Morgan Kaufmann Publishers Inc., 1999.