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Modeling Performance and Energy Consumption of Silicon Photonic Interconnection Networks via Analytical Cache Models

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I. Introduction

Increased parallelism and data intensity have added to the communication demands within high performance computing (HPC) systems. Silicon photonic (SiP) interconnects [1-2] have been shown capable of providing large bandwidth end-to-end connections over warehouse distances. These connections, eliminating the need for hop-by-hop electronic switching, significantly reduce the communication latency and energy consumption. Despite these advantages, SiP interconnects also have a set of peculiarities and special operation requirements. For example, resonance based devices such as microring resonators require wavelength tuning [3] and thermal stabilization [4] to reach desired operating wavelengths. These requirements, inducing potentially long circuit initialization delays, can easily negate the aforementioned latency improvement.

Therefore, a SiP interconnection network--with a circuit-switched nature--must therefore operate in such a way that a communication request can immediately find an established circuit (we call this a *circuit hit*); otherwise, the request sees a *circuit miss* and has to suffer from the setup penalty. In scenarios such as remote memory access (RMA) networks, the role of photonic circuits highly resembles that of cache lines in processor microarchitectures. The proposed technologies are may have broad impacts across the entire software/hardware stack of high-performance computing. Silicon photonics may demand new hardware support, new runtime systems to manage connections, or even new programming models to give application developers directly the ability to optimize circuit reuse. These design challenges must be first tackled with modeling and simulation.

Enabled by the integration capability of SiP technologies, a disruptive design choice for maximizing circuit hit rates is to allow each node to maintain (and update) a set of circuits towards a subset of frequently accessed destinations. Thanks to the temporal locality present in the communication pattern of many applications, this design permits to *reuse* an established circuit for a number of temporally near requests, thus effectively amortizing the circuit initialization overheads.

To idenfity the performance/cost trade-offs associated with this design, one must answer the following questions:

(1) How many circuits should be provisioned per node to achieve the best performance-energy balance?

(2) How to design the replacement policy for the case of circuit misses?

(3) Can on/off circuits save energy while retaining the same level of performance (e.g. hit rate)?

(4) Similar to cache prefetching, is it possible to replace or prefetch circuits in a predictive manner?

This work discusses methodologies for answering these questions. Our approach first profiles the temporal locality and circuit reuse behavior of an application, and reduces them to a simple model. Then, for efficient circuit replacement, we develop prediction approaches capable of predicting circuit reuses *at runtime*. The idea of using on/off links has been previously explored via the programming model. The approach given here fundamentally recasts the problem in terms of cache reuse policies in a runtime system [5].

For scalable evaluation of replacement policies, we propose coarse-grained discrete event simulations as well as use of *analytical cache models*, to which a reuse profile is input and the circuit missed is predicted. We also show approaches for optimizing the performance-energy consumption tradeoff. Although intended for silicon photonics, the cache models here are generally applicable to latency-hiding problems.

II. Modeling Circuit Reuse Behaviors of Applications

A. Reuse Distance Profiling

This work captures temporal reuse behavior of an application by profiling its *circuit reuse distance (CRD)*. CRD describes how frequent a circuit is used and can be either count-based or time-based. While the count-based metric can provide guidance for replacement policy designs, the time-based metric can indicate whether a circuit should be turned off to save energy or maintained to improve hit-rate performance. Profiling an application gives us a distribution of its CRDs and hence a better understanding of its temporal locality pattern.

Several reuse distance based models exist in cache performance modeling, which can estimate the missed rate given a cache size. Similarly, such models can be used to predict the circuit miss rate given the number of circuits provisioned per node and a specific circuit reuse profile. The estimated performance can be listed with the energy consumed by the provisioned circuits, and a desired balance can be found.

B. Prediction Model

Predicting reuse distance is also a key step for replacement policy design. A common practice is to select the CRD bucket with the highest frequency in the distribution. While such maximum likelihood based predictor (MLBP) works well for distributions that are concentrated, it performs poorly for those having two or more buckets with comparable frequencies. We propose a transition matrix based predictor (TMBP), which models the temporal aspect of a *CRD sequence* and predicts based on its temporal transition probabilities. A Markov chain is used to model the CRD sequence of a circuit (Fig. 1), where the states correspond to the CRD buckets and the transition matrix indicates the probability of the CRD transiting from one bucket to another. Each time a CRD sample is collected, the

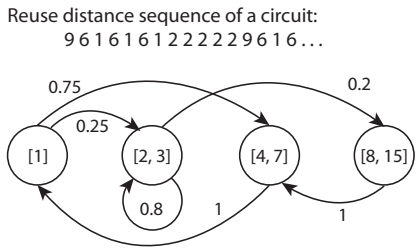

Fig. 1. Modeling transition behavior of a reuse distance sequence (top) using a Markov chain (bottom). Each state of the chain corresponds to a distance range in the distribution histogram.

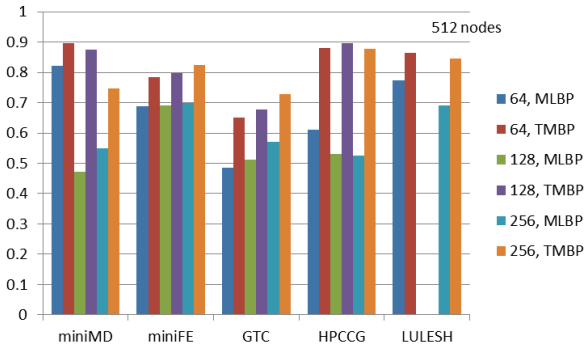

Fig. 2. Reuse distance prediction accuracy of Transition Matrix Based Preditor (TMBP) versus Maximum Likelihood Based Predictor (MLBP), across different benchmarks and numbers of nodes. TMBP (even bars) shows significantly higher prediction accuracy than MLBP (odd bars).

matrix element representing the transition from the last bucket to the current bucket increments by 1. Upon predicting the next CRD, TMBP finds the bucket to which the current CRD has the greatest transition probability. Our preliminary result shows that TMBP has much higher prediction accuracy than MLBP and better consistency as system scale grows (Fig. 2) [6-7].

III. Scalable Evaluation of Replacement Policies

Course-grained simulations using tools such as the SST macroscale simulator [8] to evaluate performance of circuit replacement policies within real application context, either through on-line simulation of application skeletons or post-mortem replay of MPI traces collected with the DUMPI tool. For modular simulation toolkits like SST, only straightforward changes to existing models are required. It can also leverage existing mini-apps, particularly the Mantevo suite [11].

While such representative benchmark-based evaluations can work as early-stage design hints, simulations can be expensive and evaluation for a broader application spectrum therefore clearly benefits from synthesizable and reliable models. Authors in [9] proposed an analytical model for predicting performance of cache replacement policies (i.e. missed rate) by inputting a simple *circular sequence profile* of the application. The model is based on a deduction that for an A-way associative LRU cache, the last access of a circular sequence with d distinct accesses will result in a cache miss if $d > A$, or a cache hit otherwise. It also abstracts each replacement policy by a *replacement probability function*, which specifies the probability of replacing a line at different LRU stack positions. It will be interesting to collect similar circular sequence profiles from applications' circuit uses, input them to the above analytical model, and see if modeling results match simulation results. Furthermore, synthesizability of this approach also enables investigation of behavior changes that can benefit more from circuit reuses, without the need for modifying application codes.

IV. Energy Consumption Tradeoff

Although roles of circuits and caches share many similarities, several notable differences persist. An obvious one is that maintaining a circuit explicitly costs time-proportional energy consumption (e.g. laser power). Although maintaining circuits as long as possible can help reduce miss rates, such reduction comes at a price of excessive energy consumption. Therefore, a mechanism is needed to proactively turn off unused circuits. One such method is to predict the time-based CRD of a circuit—if the CRD is greater than a threshold, the circuit will be turned off. However, 100% prediction accuracy is not possible, causing a performance-energy tradeoff that can be explored with modeling and simulation. Analytical cache models can include PTO operations into the model. One method is to attach a time-based CRD to each circular sequence, i.e. the time predicted to elapse between the first and last accesses. If the CRD exceeds a threshold, the circular sequence will directly contribute to a miss.

It should be noted that proposed approaches offers vast opportunities for application-circuit runtime co-design. The presence of temporal locality in applications can be potentially reinforced with awareness of underlying circuit reuse opportunities. Also, privileges can be given to programmers to guide PTOs for energy-efficient computing. One can exploit the simulation and modeling capabilities presented above to quickly iterate the co-design process.

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